# Carrier Phase Lock Loops Tested with Different Input Waves

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*Abstract*

**In this work, we will study the carrier phase Lock Loop (CPLL) when the input carrier changes its shape.**

**The CPLL has four prototypes which are the analog, the hybrid, the combinational and the sequential.**

**The input carrier can be a sinusoidal wave, a triangular wave or a rectangular wave.**

**The objective is to study the four synchronizer types and to observe their jitter behaviors as function of the input carrier SNR (Signal- Noise Ratio), when the carrier changes its shape between the three mentioned waves.**

***Key words:*** **Synchronism in Digital Communications**

## I. INTRODUCTION

The carrier Phase Lock Loop (PLL) is the conventional PLL device whose VCO (Voltage Controlled Oscillator) is able to follow the input carrier wave. Normally, the PLL input signal is a frequency modulated carrier and the PLL output signal is the demodulated base band signal. Other times the PLL output is the VCO frequency signal or clock which is a high quality version of the input signal.

We will develop four different Carrier Phase Lock Loop (CPLL) types which are the analog, the hybrid, the combinational and the sequential. [1, 2, 3, 4, 5, 6, 7, 8, 9].

Fig.1 shows the general configuration of the CPLL.

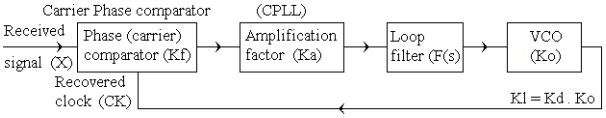


Fig.1 General aspect of the carrier Phase Lock Loop

Where, Kf is the phase comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop amplification gain parameter that acts on the root locus, controlling the loop desired characteristics.

Each one of the four synchronizers will be tested when the carrier input changes between sinusoidal wave, triangular wave and rectangular wave [10, 11, 12, 13, 14, 15].

Following, we will present the four CPLLs: analog, hybrid, combinational and sequential.

Next, we will show the three carrier waves: sinusoidal, triangular and rectangular..

After, we will present the design and the tests of the synchronizers in the presence of noise.

Then, we present the results with some comparisons.

Finally, we present the conclusions.

## II. FOUR TYPES OF CARRIER PHASE LOCK LOOP

We will present four types of phase Lock Loops namely, the analog, the hybrid, the combinational and the sequential. The difference between them is inside of the carrier phase comparator [1, 2].

### *A. Analog type*

In the analog type, the carrier phase comparator is based on an ideal multiplier, which is an analog component (Fig.2).

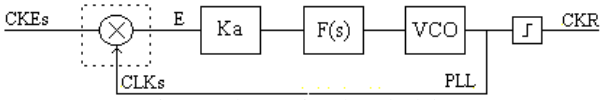


Fig.2 Analog carrier phase lock loop

The phase comparator inputs (main input and VCO output) are both analog.

### *B. Hybrid type*

In the hybrid type, the carrier phase comparator is based on a switch or real multiplier, which is an hybrid component (Fig.3).

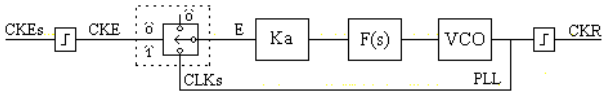


Fig.3 Hybrid carrier phase lock loop

The phase comparator main input is, now, digital but the input coming from the VCO output continues to be analog.

### *C. Combinational type*

In the combinational type, the carrier phase comparator is based on an exor gate, which is a combinational component (Fig.4).

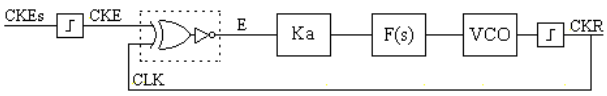


Fig.4 Combinational carrier phase lock loop

The phase comparator inputs (main input and VCO output) are both digital, but its output is only function of the main input (circuit without memory).

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*D. Sequentiall type*

In the sequential type, the carrier phase comparator is based on a flip flop, which is a sequential component (Fig.5).

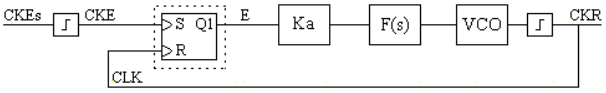


Fig.5 Sequential carrier phase lock loop

The phase comparator inputs (main input and VCO output) are both digital, but its output is simultaneously function of the main input and of the phase comparator state (circuit with memory).

## III. INPUT CARRIER CAN BE ONE OF THREE WAVES

We will study the behavior of the CPLL when the input carrier changes its form between the sinusoidal wave, triangular wave and rectangular wave [3, 4].

Fig.6 shows the input carrier changing its form but maintaining its signal power.

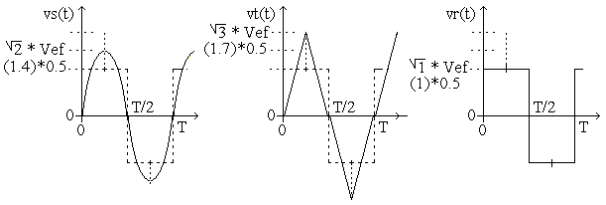


Fig.6 Three input waves: sinusoidal, triangular and rectangular

In the three waves, we wish the same signal to noise ratio SNR in order to have equal conditions.

Since the noise power Pn=No*Bn is equal in the three cases, then the signal power Ps=Aef$^2$ must also be equal in the three waves. Where, No is the noise spectral density, Bn is the extern bandwidth and Aef=Arms is the root mean squared signal amplitude.

So, in order to have the same signal power Ps= Arms$^2$ and consequently the same RMS amplitude for the three waves, the sinusoidal wave must have a peak amplitude Ap= √2*Aef, the triangular wave must have a peak amplitude Ap=√3*Aef and the rectangular wave must have a peak amplitude Ap=√1*Aef. In the last figure, we considered Aef=Arms=0.5V.

## IV. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [6].

*A. Design*

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = $A^2_{ef}$/(No.Bn). But, No can be related with the noise variance σn and inverse sampling Δτ=1/Samp, then No=2σn$^2$.Δτ, so SNR=$A^2_{ef}$/(2σn$^2$.Δτ.Bn) = 0.5$^2$/(2σn$^2$*10$^{-3}$*5)= 25/σn$^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is

*Bl=0.02=(Ka.Kf.Ko)/4* with (Km=1, A=1/2, B=1/2; Ko=2π)

*(Ka.Km.A.B.Ko)/4 = 0.02 -> Ka=0.08*2/π* (3)

For the hybrid synchronizers, the loop bandwidth is

*Bl=0.02=(Ka.Kf.Ko)/4* with (Km=1, A=1/2, B=0.45; Ko=2π)

*(Ka.Km.A.B.Ko)/4 = 0.02 -> Ka=0.08*2.2/π* (4)

For the combinational synchronizers, the loop bandwidth is

*Bl=0.02=(Ka.Kf.Ko)/4* with (Kf=1/π; Ko=2π)

*(Ka*1/π*2π)/4 = 0.02 -> Ka=0.04* (5)

For the sequential synchronizers, the loop bandwidth is

*Bl=0.02=(Ka.Kf.Ko)/4* with (Kf=1/2π; Ko=2π)

*(Ka*1/2π*2π)/4 =0.02 -> Ka=0.08* (6)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.

For analog PLL the jitter is

$\sigma\phi^2=Bl.No/Aef^2$=Bl.2.σn$^2$.Δτ=0.02*10$^{-3}$*2σn$^2$/0.5$^2$=16*10$^{-5}$.σn$^2$

For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

*B. Tests*

Fig.10 shows the setup that was used to test the various synchronizers.

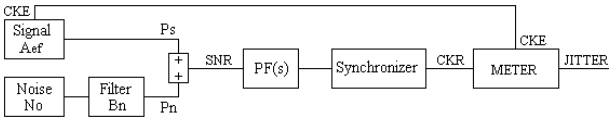


Fig.7 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

*C. Jitter measurer (Meter)*

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.11).

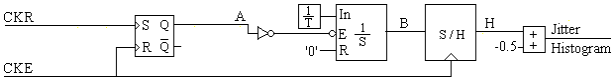


Fig.8 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

*D. Results*

We will present the output jitter UI-RMS (Unit Interval Root Mean Squared) as function of the input SNR (Signal to Noise Ratio) for the four carrier PLL considering three input waves, namely the sinusoidal, triangular and sequential.

These waves have the same SNR, we will see that the jitter diminishes almost exponentially when the SNR increases.

Fig.9 shows the UI jitter - SNR curves of the analog CPLL for the three input waves: sinusoidal (sin), triangular (tri) and rectangular (rec). This synchronizer hasn't input limiter what maintains the analog format to the input signal.

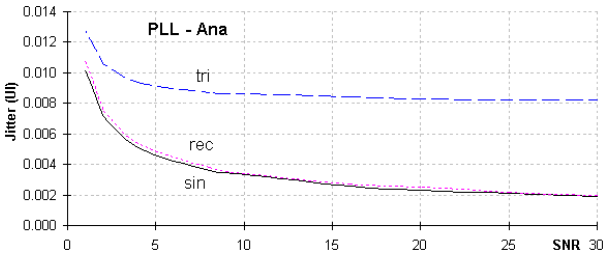


Fig.9 Jitter-SNR curves of the analog synchronizer for the three waves (sin, tri, rec)

We verify, that the jitter curves are similar for the sinusoidal and rectangular input waves and disadvantageous for the triangular wave.

Fig.10 shows the UI jitter - SNR curves of the hybrid CPLL, for the three input waves: sinusoidal (sin), triangular (tri) and rectangular (rec). This synchronizer has input limiter what gives digital format to the input signal.

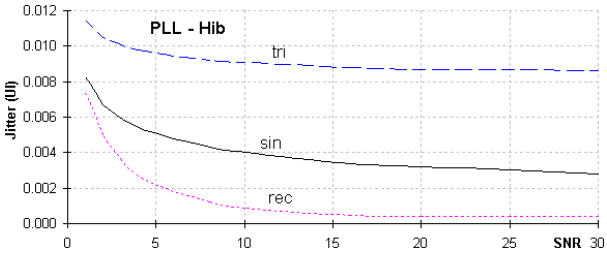


Fig. Jitter-SNR curves of the hybrid synchronizer for the three waves (sin, tri, rec)

We verify that the jitter curves, are different for the three waves. The jitter curves diminishes in the inverse direction of the transition slope increasing (tri. -> sin. -> rec.).

Fig.11 shows the UI jitter-SNR curves of the combinational CPLL, for the three input waves: sinusoidal (sin), triangular (tri) and rectangular (rec). This synchronizer has input limiter what gives digital format to the input signal.

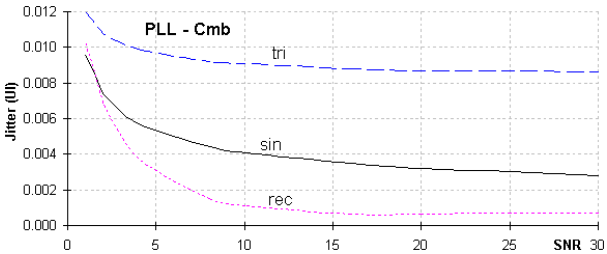


Fig.11 Jitter-SNR curves of the combinational synchronizer for the three waves (sin, tri, rec)

We verify that the jitter curves, are different for the three waves. The jitter curves diminishes in the inverse direction of the transition slope increasing (tri -> sin -> rec).

Fig.12 shows the UI jitter - SNR curves of the sequential CPLL, for the three input waves: sinusoidal (sin), triangular (tri) and rectangular (rec). This synchronizer has input limiter what gives digital format to the input signal.

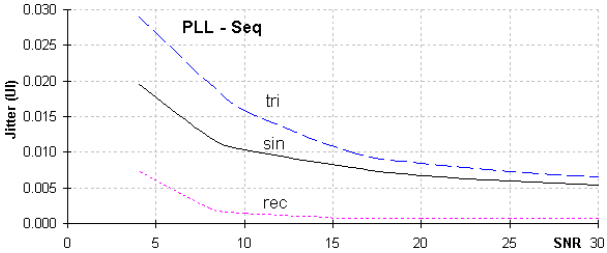


Fig.12 Jitter-SNR curves of the sequential synchronizer for the three waves (sin, tri, rec)

We verify that the jitter-SNR curves, are different for the three waves. The jitter curves diminishes in the inverse direction of the transition slope increasing (tri -> sin -> rec).

## V. CONCLUSIONS

We studied four synchronizer types namely the analog, the hybrid, the combinational and the sequential. Then, we observed their output jitter as function of the input SNR for three different input carrier waves, namely the sinusoidal, the triangular and the rectangular.

We noted that generically the output jitter UI diminishes almost exponentially when the input SNR increases.

For the synchronizer without input limiter (analog) the jitter curves are similar for the sinusoidal and rectangular input waves and disadvantageous for the triangular input wave. All the noise contributes to the jitter in the three waves, but the triangular wave introduces a static jitter that damages the jitter curve.

For the synchronizers with input limiter (hybrid, combinational and sequential) the jitter curves decreases when the input waves slope increases, what improves the noise immunity.

## VI. ACKNOWLEDGMENTS

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