
Universidade de Aveiro
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Departamento de Electrónica, Telecomunicações e Informática

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Amplificador CMOS de baixo ruído para imagiologia médica


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A low-noise CMOS amplifier for medical imaging

Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Electrónica e Telecomunicações, realizada sob a orientação científica do Doutor Luís Filipe Mesquita Nero Moreira Alves, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro, e do Doutor Ernesto Fernando Ventura Martins, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

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palavras-chave

Tomografia por emissão de positrões, tempo-de-voo, modo de corrente, amplificadores de baixo-ruído, foto-multiplicadores de silício, detectores de radiação, mamografia, electrónica analógica.

resumo

A presente dissertação aborda o projecto de um front-end analógico integrado para sincronização e amplificação de sinais produzidos por um foto-multiplicador de silício.

A solução proposta pretende possibilitar medidas de tempo com resoluções na ordem dos pico-segundos, para implementação em equipamentos compactos dedicados à Tomografia por Emissão de Positrões, com capacidade para medida do tempo de voo de fotões (TOF-PET).

O canal de front-end completo foi implementado em tecnologia CMOS 130nm, e compreende blocos de pré-amplificação, integração de carga, equilíbrio dinâmico do ponto de operação, bem como circuitos geradores de correntes de referência, para uma área total em silício de 500x90 µm.

A discussão de resultados é baseada em simulações pós-layout, e as linhas de investigação futuras são propostas.

keywords

Positron emission tomography, time-of-flight, current mode, low-noise amplifiers, silicon photomultipliers, radiation detectors, mammography, analogue front-end electronics.

abstract

An analogue CMOS front-end for triggering and amplification of signals produced by a silicon photomultiplier (SiPM) is proposed.
The solution intends to achieve picosecond resolution timing measurements for compact time-of-flight Positron Emission Tomography (TOF-PET) medical imaging equipments.
A 130nm technology was used to implement such front-end, and the design includes pre-amplification, shaping, baseline holder and biasing circuitry, for a total silicon area of 500x90 µm.
Post-layout simulation results are discussed, and ways to optimize the design are proposed.

Nomenclature

ADE	Analog Design Environment
APD	Avalanche Photo-Diode
ASIC	Application Specific Integrated Circuit
BW	Bandwidth
CERN	European Organization for Nuclear Research
CFD	Constant Fraction Discriminator
CG	Common Gate
CM	Current Mirror
CRT	Coincidence Resolving Time
CS	Common Source
CSA	Charge Sensitive Amplifier
CT	Computer Tomography
DH	Detector Head
DoI	Depth of Interaction
DRC	Design Rules Check
e-h	electron-hole
ENC	Equivalent Noise Charge
ESD	Electrostatic Discharge
FPGA	Field Programmable Gate Array

FWHM	Full Width at Half Maximum
IC	Integrated Circuit
LOR	Line of Response
LVS	Layout versus Schematic
LYSO:Ce	Cerium-doped Lutetium Yttrium Orthosilicate
MAPD	Micro-Pixel Avalanche Photodiode
MPW	Multi-Project Wafer
MRI	Magnetic Resonance Imaging
OA	Operational Amplifier
p.e.	photoelectron
PDE	Photon Detection Efficiency
PEM	Positron Emission Mammography
PMT	Photomultiplier Tube
RGC	Regulated Cascode
SACMOS	Self-Aligned Contact CMOS
SR	Slew Rate
TDC	Time to Digital Converter
TIA	Transimpedance Amplifier
ToT	Time-over-Threshold
UMC	United Microelectronics Corporation

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Chapter 1

Introduction

Early stage breast cancer detection is fundamental to reduce the mortality of the most frequent malign tumour among women, and substantially increase the rate of recovery. Conventional X-ray mammography has proven to be inefficient, either due to its low sensitivity (particularly in patients with dense breasts) or to its modest specificity, which leads to false positives and thus to unnecessary biopsies. In this regard, PET imaging is advantageous, as it increases both the detectability of small tumours and the specificity of the exam. However, while whole-body PET equipments are bulky, costly and more sensitive to background noise, dedicated scanners involve lower operational costs and have inherently higher event rate count. Yet with shorter exam times and smaller radiotracer dosages, a dedicated Positron Emission Mammography (PEM) unit achieves better spatial resolution than the whole-body counterpart.

In the framework of the Crystal Clear Collaboration at the European Organization for Nuclear Research (CERN) , the Portuguese PET Consortium develops, since 2002, dedicated PEM imaging technology applied for breast cancer detection. A first Positron Emission Mammograph (ClearPEM), with an unprecedented 1.4 mm spatial resolution and very high acquisition rate (up to 1 MHz, or $1Mevents/s$), is in clinical trials since 2008. A second prototype (ClearPEM-Sonic, shown in Figure 1.1) has been assembled at the time of the writing of this dissertation and will couple an ultrasound scanner to provide a multi-modal diagnosis. The current research activities will support the design of a new prototype capable of time-of-flight measurements, paving the way for unmet performances in this domain.

Figure 1.1: A dedicated PEM scanner, the second built by the Portuguese PET consortium, shall integrate PET and ultrasound imaging.

1.1 Positron Emission Tomography

PET is a nuclear medicine imaging technique capable of providing in vivo metabolic and functional information of the human body. It therefore contrasts with other imaging equipments, such as CT or MRI, which produce images of the anatomy and density of the tissues and organs. As far as cancer diagnosis is concerned, these techniques may not be sufficient. Since the neoplasms have atypical metabolic activity even before any visible morphological change occurs, the ability to perceive these changes is the key for early detection. In order to achieve such insight, PET builds up on the fact that every cell activity consumes energy and thus synthesizes glucose. As the patient is injected with a glucose molecule labeled with a radioactive tracer, the most energy consuming tissues will aggregate a higher concentration of the radioisotope. Knowing that cancer cells have higher metabolic activity due to the abnormal reproduction rate, their uptake will be excessive and hence the accumulation of the radiopharmaceutical in the tumor areas will be higher.

Several positron emission isotopes can be used for PET and thence the choice observes either a specific application domain (e.g. ^{82}Rb, common for the study of myocardial perfusion, and generally cardiac imaging) or the requirements in terms of ionization energy or half-life decay time (e.g. isotopes such as ^{11}C or ^{13}N are often chosen when the radiation exposure is a concern, since their decay is only of a few minutes). The Fluorodeoxyglucose ($^{18}F-FDG$) is a glucose analogue radiopharmaceutical commonly used for PET imaging. The molecule contains a Fluorine-18 isotope, which is produced in a cyclotron. Due to its unstable (over-energetic, with excess of protons) nucleus the ^{18}F atom will undergo a radioactive decay,

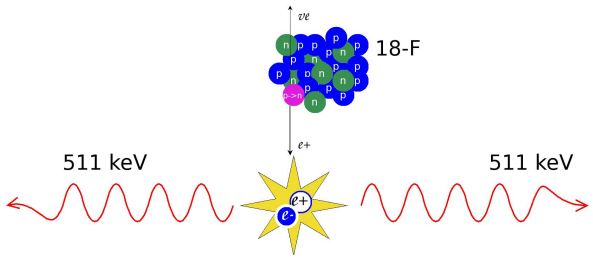


Figure 1.2: Positron-Electron annihilation following a β^+ decay, emitting two anti-parallel γ photons.

specifically a beta decay of type β^+. The β^+ decay is a radioactive conversion that creates a positron, which is the vis-à-vis of the electron (its "antiparticle"), having the same mass and a symmetric electric charge.[1] Flying away from the nucleus where it has been originated, the positron will collide with an electron within the neighborhood of the decay, resulting in the annihilation of both particles. The collision produces two gamma ray photons. Having said that the electron and positron have the same mass ($9.11 \times 10^{-31}\ Kg$), then each of the particles has an energy given by $E = mc^2 \approxeq 8.2 \times 10^{-14} Kg \cdot m^2 \cdot s^{-2} = 5.11 \times 10^5\ eV$. Since the process of annihilation must preserve the total net energy, each γ ray emitted is a 511 keV photon. Likewise, for the momentum to be conserved, the pair of γ photons is emitted in opposite directions. Figure 1.2 shows a graphical interpretation of the described interaction.

If the pair of photons is simultaneously detected (within a very short finite time interval), their back-to-back flight describes a line of response (LOR) that can be processed by an acquisition/trigger system, as demonstrated in Figure 1.3. These LOR correspond to the detection of events of interest, which need to be discerned from background noise, or random hits.

In order to achieve the discrimination of true hits, the data acquisition system relies on the fact that the photons reach the detector heads (DH) within a sub-nanosecond time frame difference (need for a good time resolution), and that the photons have a known energy (need for a good energy resolution).

The advent of faster electronics for PET detectors, along with the recent development of highly compact solid-state photodetectors, is scaling down the coincidence timing resolution of

[1]The positron (e^+) emission converts an excess proton (p) into a neutron (n) and produces also an electron neutrino (ν_e), from which the interaction can be described by: $p = n + e^+ + \nu_e$. A neutrino is an uncharged particle with negligible (but non-zero) mass that travels at the speed of light and with only a faint interaction with matter. Its inclusion here is justified by the laws of conservation of energy and momentum, since the kinetic energy with which the positron is emitted is not always the same.[DOE1993]

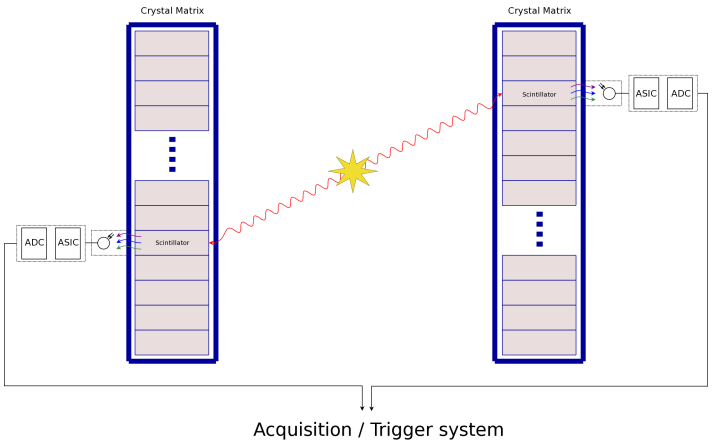


Figure 1.3: Event triggering with a dual-head PET detector: a pair of photons hit the detector within a coincidence time interval, generating a pulse signal that is processed by the front-end readout electronics.

the scanners to the deep nanosecond range, needed for time-of-flight (TOF) measurements. Knowing the difference of the time of arrival of the coincident photons, it is possible to restrict the position of the annihilation to a subsection of the LOR. Figure 1.4 illustrates such enhancement.

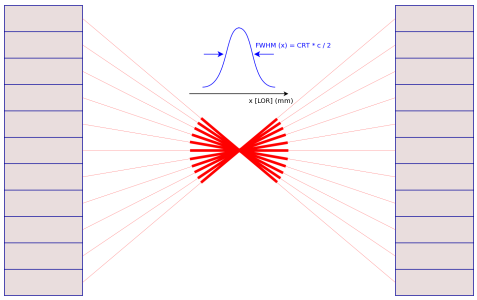


Figure 1.4: TOF principle in a double-readout PET detector; the arrival time difference of the pair of photons is used to calculate the position of the annihilation along the LOR, with a full width at half maximum (FWHM) spatial uncertainty that is a function of the timing resolution of the PET scanner.

The spatial positioning of the positron is, of course, affected by the timing resolution of the detector itself. Since the γ photons travel at a speed near the speed of light in the vacuum, the precision of the position along the line is given by (1.1) [Moses1999] :

$$\Delta x = \Delta t \frac{c}{2} \tag{1.1}$$

from which it can be predicted that a timing resolution of 200 ps will lead to a FWHM positional uncertainty of 30 mm along the line that connects the opposing detector pixels. The benefit achieved can serve the purpose of either reducing the scanning time or, equivalently,

the injected dose. Keeping those conditions, the TOF information can boost the image quality, since the signal-to-noise ratio and background (random events) rejection are greatly improved. However, the TOF capability requires the use of very high speed electronics, capable to extract temporal information with a resolution down to 25 ps.

1.2 Context and Motivation

The work herein reported is included within the Portuguese PET Consortium activities, specifically those concerning the design of integrated electronics for radiation detection. In the mid-term, the development of a new front-end multi-channel ASIC is envisaged. The new low-noise, low-power ASIC shall provide outstanding time resolution measurements for both medical imaging and particle physics.

Such performance, capable of time-of-flight (TOF) measurements, implies the use of fast electronics, very sensitive to the rising edge of a signal produced by the particle detector. The high gain of the newly introduced SiPMs makes them a much more attractive solution, when compared to the actual APD based systems. However, the high parasitic capacitance at the terminals of such device creates new problems in terms of noise and bandwidth of the front-end. Moreover, due to the large current signal at the input of the analogue channel and the high integration level of a succeeding multi-channel layout, new challenges will be posed in order to mitigate the voltage bouncing at the input nodes.

This work focuses the development of a new front-end amplifier, suitable to be used for timing and charge measurements of signals produced by SiPMs. Based on data provided by manufacturers, a simple electrical model for the SiPM will be used in analytical studies and simulations, where the optical input for the photodetector is produced by the scintillation of a L(Y)SO:Ce crystal hit by a γ ray. The pre-amplification, shaping, baseline holder and biasing building blocks must be implemented in a standard mixed-mode 130nm CMOS process technology from UMC .

1.3 Contents

The current chapter provided an overview of the fundamentals of PET imaging, as a general context for the work hereby reported. The subsequent sections of the manuscript are organized as follows.

Chapter 2 introduces the concepts of particle detection, as the common blocks of a radiation detector are depicted. The case study is the proven technology used in both the prototypes ClearPEM and ClearPEM-Sonic. The relevance of the low-noise requirements for the front-edge electronics is justified.

Chapter 3 covers the design of an analogue front-end amplifier for radiation readout. The architecture is described, and the building blocks are depicted down to the transistor level design. Where appropriated, schematic level simulation results are presented to validate the block design.

Chapter 4 depicts the layout implementation of a single-channel circuitry, verification process and simulations after parasitic extraction. The demonstration of functionality includes the analysis of the dynamic range of the front-end, and the circuit robustness to process variations.

The conclusions are drawn in Chapter 5, along with the briefing of the lessons learned and guidelines for future work.

Chapter 2

Radiation Detectors

This chapter introduces the constituent blocks of a front-end detector for PET medical imaging, and provides an insight on the signal characteristics at the input of the front-end electronics.

Generally, the outputs of a particle detector are both a shaped amplified waveform of the input pulse, and an accurate edge time stamp derived from a fast replica of the signal. The first will be used to extract the energy of the pulse, whereas the second provides the input for timing measurements. Alternatively, a single shaped amplified waveform can be used to extract both the energy and time information, using firmware and software level signal processing.

The front-edge chain includes a scintillator crystal that performs wavelength shifting of the incident photons, an optically coupled photodetector and the associated readout electronics. Figure 2.1 shows its conceptual representation.

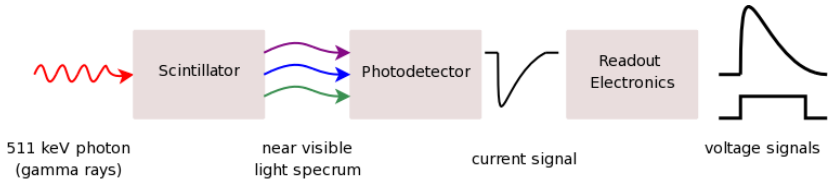


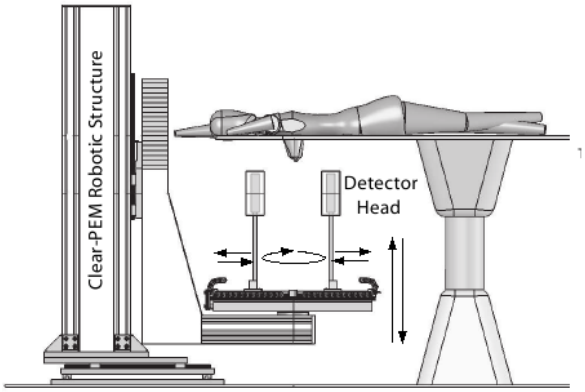
Figure 2.1: Block diagram of particle detectors

2.1 The ClearPEM front-edge

Although future developments will incur in deep architecture and design modifications, a good knowledge of a fully characterized prototype is in all aspects advantageous. Such understanding provides valuable hints on time resolution requirements, hence jitter and noise limitations of the front-end electronics. Moreover, the awareness of the colling system of a

compact detector head defines power dissipation constraints and therefore limits the available power budget for the front-end ASIC. Not least important is to perceive the boundaries of a data acquisition and trigger system for such an equipment, from which new methods for time and energy extraction can be proposed.

The ClearPEM is a dual-head planar detector, each head with approximately $16 \times 18\ cm^2$ of active detection area. Figure 2.2 represents the robotic structure of the scanner during a breast exam; neither the user workstations, the data processing and robot control frames are represented. The detector is based on fast LYSO:Ce crystals, optocoupled to avalanche



P. Rodrigues et al., "Clear-PEM system counting rates: a Monte Carlo study"
JINST 2 P01004, 2007

Figure 2.2: Representation of the structure of the ClearPEM detector; the angle of the dual-head structure can be bent by 90° to allow both breast and axilla region exams.

photodiodes (APD) and readout by dedicated full-custom ASICs. The whole scanner has 6144 $2 \times 2 \times 20\ mm^3$ LYSO:Ce crystals, grouped in 192 8×4 matrices. Each of these modules is glued to a 32-pixel APD in each side (to allow a double-readout scheme, as will be further explained). For a total of 384 multi-pixel APDs, 12288 electronic channels are fed into each one of the 64 ASICs. The 192:2 multiplexing ASICs perform readout, amplification, sampling (into analogue memories) of 192 channels, and outputs up to two simultaneous sampled pulses which voltage exceeds a defined threshold V_{th}, while a digital output maps each sample to the corresponding detector pixel.

Each analogue output sample pulse is digitized by a 10-bit ADC, serialized and transmitted off-detector via LVDS links. Choosing to have the digitized analogue samples driven off-chip does simplify the ASIC design, allowing the level of integration desired, as it endorses the time and energy extraction to the off-detector acquisition electronics. However, for that to be accomplished, an aggregate bandwidth of 144 $Gbit/s$ is required to drive the data out

of the DHs, though development guidelines on this subject have been already proposed in [Bugalho2009b]. The data is processed by 8 FPGAs, where energy and time information is extracted, and signaling of interesting events is generated. Thereafter, a trigger processor (also implemented in a FPGA) selects coincident events based in a programmable timing window and sends the respective data to a software based processing (acquisition PC) for further analysis. This post-processing includes depth of interaction (DoI) estimation, and event reconstruction corresponding to Compton events. The same processing layer must be able to recognize random (or uncorrelated) events and those which, having suffered scattering in the tissues, arrive to the detector with a leaned LOR.

As aforesaid, scintillation light is collected at both ends of the crystals by APDs, optically coupled to the crystals (double readout scheme). The system would otherwise assign all photon interactions with a crystal as a hit at the front face (or equivalently, at a fixed point along the axis), producing an arbitrary number of incorrect LOR, since such interactions can occur along all the crystal length. The erroneous lines would, after processing, result in the blurring of the reconstructed images (parallax) and/or decreased sensitivity due to the rejection of large angle LOR (in an attempt to mitigate the error). A double readout scheme, as illustrated on figure 2.3, uses a measure of the asymmetry of the signal energy read at the top and the bottom of the scintillator to calculate the longitudinal position at which the photon interaction took place. The parallax effect can thereby be reduced with

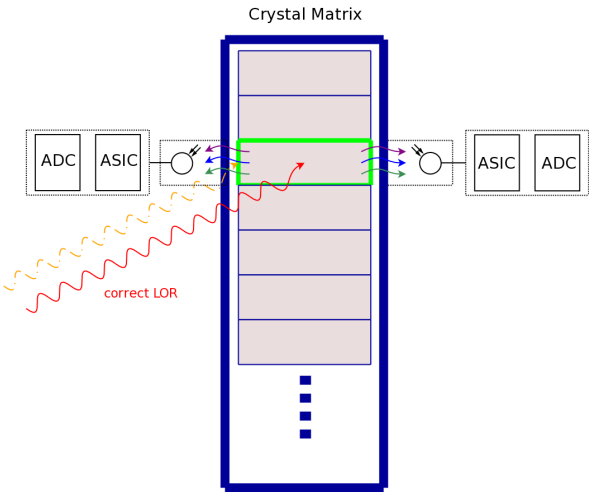


Figure 2.3: Double readout for DoI calculation: If double readout is not implemented, any photon hit on the crystal has to be assumed at a given position along the crystal axis (commonly, the crystal face).

the calculation of the DoI , leading to an increased sensitivity of the scanner.

However, lower energy photons do also arrive to the scanner heads. These low energy hits are originated due to Compton scattering of a photon in two or more crystals, leading to a dispersion of the total energy amongst those elements. The γ rays can arrive with an energy below 100 keV, and it is up to the software level to correlate the angles of incidence and energy deposition in each crystal. The scanner sensitivity relies on a proper handling of the lower energy scattered photons, as their wasting severely degrades sensitivity. In fact, the reconstruction of Compton events is vital to achieve a good performance in terms of sensitivity, since these can account for up to 30% of the events [Bugalho2009b]. In order to allow the detection of events with these low energies, the V_{th} of the comparator must be set low enough. However, a very low threshold voltage will increase the random event rate and, consequently, the ASIC dead time.

When a sufficient number of correct LOR is discerned, reconstruction algorithms are used to generate a multi-dimensional image, which identifies the regions with higher density of positron/electron annihilation. The resolution of such image is ultimately constrained by the surface area of the crystal, as it constitutes the minimum dimensions of the matrix[1]. From this postulate, one can foresee that fine-pixelized scanners are more likely to achieve better spatial resolution.

Effectively, other factors contribute to the degradation of this limit, such as the non-zero kinetic energy of the positron-electron system at rest, or the positron drift in the tissue before annihilation. While the first implies that the photon pair flight is not necessarily collinear, according to what has been predicted above $(180°)$[2], the second assumption indicates that the e^+/e^- collision may not always occur within the boundaries of the malign tissue (for a positron which decay occurred within the boundaries).

2.2 Front-edge improvement for TOF capability

The development of the front-end electronics for a TOF-capable detector takes into account the experimental characterization results of the ClearPEM, particularly in what concerns the on-detector electronics of the scanner. An adaptation of the developed technology for the use of new highly dense solid-state photodetectors is envisaged. With that in mind, new timing extraction strategies can be proposed in order to take full advantage of the char-

[1] That does not mean, however, that the resolution of the image is equal to the pixel size; the FWHM resolution is usually smaller than the pixel width

[2] The error introduced by the non-collinearity can reach 2mm for a 80cm ring detector [Rodrigues2007]

acteristics of the SiPMs.

2.2.1 Specifications for the readout electronics input signal

The SiPM is a recently introduced solid state photodetector, with a very high gain and sensitivity to single photon hits. Its fast rise time and good timing characteristics makes them suitable to extract the TOF information of two photons originated from the same positron decay on a PET detector. This section provides an overview of the SiPM device, from which a very simple electrical model can be further derived.

A SiPM is an array of solid-state photodiodes operating in Geiger mode, sharing the same substrate, and a network of quenching resistors [Pavlov2005]. The SiPMs are seen as an attractive solution for low energy photon detection in medical imaging, as they have important advantages with respect to the photomultiplier tube (PMT) or avalanche photodiode (APD). Besides having a very low form factor, the SiPM is immune to magnetic fields, as the course traveled by the charge carriers is short. The straightforward advantage of this characteristic is its suitability to be integrated in a multi-modal PET-MRI equipment. The work in [Hawkes2007] provides experimentally supported conclusions on the effect of static, gradient and RF magnetic fields over the performance of SiPMs. It uses significantly lower bias voltages ($25 - 50\ V$) than the other solutions and, nonetheless, achieves a high gain, similar to that of the PMTs. This high gain, typically of the order of 10^5, is much higher than that achievable (within the $100 - 500$ range) with APDs [Buzhan2001]. It is a robust and compact alternative, with excellent time resolution and quantum efficiency [Corsi2006], and also low sensitivity to temperature and bias variations [Buzhan2001].

On the event of an incident group of photons, the current pulses generated by each photodiode of the dense array sum up, since all cells are connected in parallel. Likewise, the integral of the current pulse is nearly proportional to the intensity of the incident light pulse of finite duration. This proportionality only applies if moderate light intensity is considered, since it does not account for the probability of multiple incidences within the microcell recovering time [Seifert2009]. When n microcells fire simultaneously, we have a total current $I_{ph}(n) = n \cdot i_{ph}$, where i_{ph} is the avalanche pulse current generated by a single microcell hit by an incoming photon [Badoni2007]. Electrical models for SiPMs were described by Corsi et al.[Corsi2006], Pavlov et al.[Pavlov2005] and Badoni et al.[Badoni2007]. Similarly, the authors have proposed experimental set-ups to extract the relevant electrical parameters. The use of an electrical model that is able to relate the device output response with the number

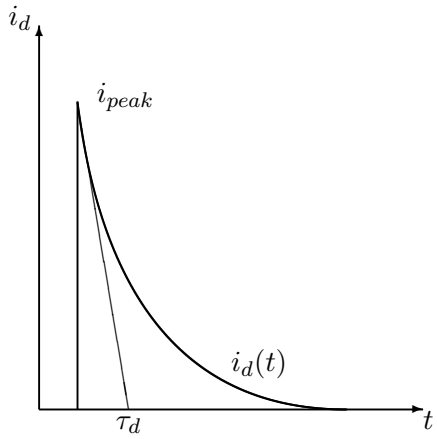


Figure 2.4: Waveform of the current pulse produced by the SiPM.

of fired cells, or that takes into account second order effects due to the stray inductances does in fact increase the accuracy of the simulations. However, as far as a validation of the front-end topology is concerned, and given that it must be flexible to a wide range of devices, a current mode stimulus with known damping factors is seen as an adequate model from an electronic circuit designer perception.

Figure 2.4 introduces the parameters of a general waveform representing current pulse at the input of the pre-amplifier. It can be approximated by the convolution of the bi-exponential function of the SiPM response to a Dirac pulse and the exponential decay characteristic of the scintillator.

The simplest equivalent circuit of an APD can be described as a current source with current i_{ph}, in parallel with a capacitance C_d [Albuquerque2006b]. It may be assumed that the SiPM can be represented in a similar way, but with a higher current i_{ph} in parallel with an also higher C_d. Typically, for a SiPM gain of $2.5 \cdot 10^5$ with a photon detection efficiency (PDE) of 25% (typically 75% for APDs), there is an increase of about 600 in the number of electrons generated, compared to an APD with gain 150. For a double readout configuration (511 keV photon, LYSO crystal), we may thus assume a peak current of 550 μA. Table 2.1 briefs the characteristics of the input charge and signal peak currents for each readout configuration. A 40 ns time constant is considered, such that $I_0 = Q/\tau$. The dynamic range of the input amplifier must hence comply with an input current reaching 1 mA peak, and as low as 50 μA.

The total parallel capacitance C_d accounts not only for the grid capacitance C_G (due to the grid parallel interconnection) but also the pixel capacitance $C_{pixel} = C_d + C_q$, a sum of the junction capacitance and the parasitic C_q, using the nomenclature in the models proposed

by [Corsi2006] and [Pavlov2005]. Therefore, C_d depends on the number of cells in the array, thus the active area, and may be in the range of $35 - 320\ pF$, respectively concerning 1 mm^2 and 9 mm^2 devices.

Double Readout Configuration	Photon energy	Input charge	Input peak current
Average charge (highest DoI)	511 keV	33.5 pC	840 uA
Average charge (center DoI)	511 keV	22.3 pC	550 uA
Average charge (lowest DoI)	511 keV	11.2 pC	280 uA
Maximum charge (extreme DoI)	511 keV	40.3 pC	1010 uA
Average charge (lowest DoI)	100 keV	2.2 pC	55 uA

Table 2.1: Estimations of amplifier input charge, for a L(Y)SO:Ce and SiPM typical characteristics.

2.2.2 Readout Electronics

The ClearPEM detector performs waveform sampling of a shaped and amplified pulse, i.e., it stores successive values of the pulse in a word of analogue memories. If the sampling period is short enough, then the off-chip processing scheme can reconstruct an accurate mathematical replica of the pulse, from which it will extract both time and energy information. However, given that the input signal from the SiPM has a very sharp rise, alternative signal processing techniques may result in significant improvements for the timing extraction. If the signal is directly fed to a discriminator (or comparator), then a logic pulse can be created whenever the pulse voltage exceeds a pre-defined threshold. Such logic pulse can be interpreted by a time to digital converter (TDC) and used to deliver time stamps defining the leading and trailing edges of the signal. This very fast readout electronics, capable to extract a sub-nanosecond time stamp, would provide the time-of-arrival of the leading photoelectrons without the need to process the calibrated function of a known pulse response (as in waveform sampling).

Whichever method is used for time and energy extraction, the system's time resolution is required to be maximized. The time response of the detector is, however, constrained by timing fluctuations which statistics can be drawn by a Gaussian distribution which FWHM is a quadratic sum of the individual contributions of each sub-system (light propagation on the crystal, photon transit time on the photodetector, or jitter due to electronic noise).

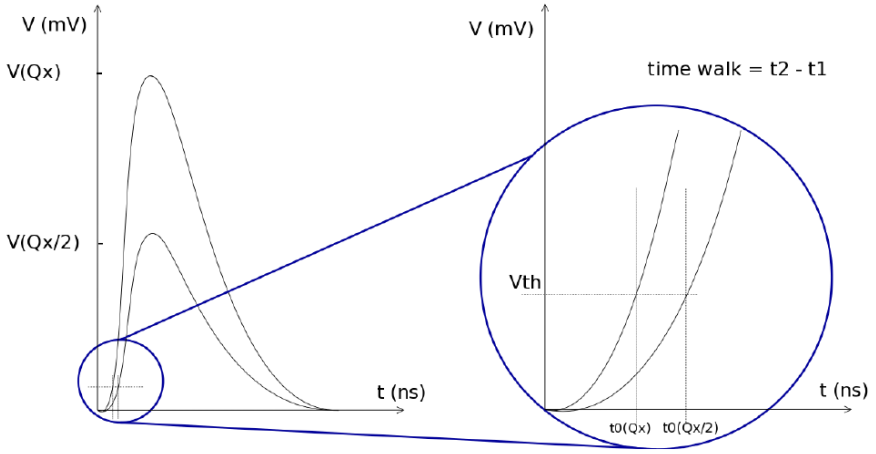


Figure 2.5: Time walk of the leading edge of the pulse.

Pulse height fluctuation

Ultimately, if the time stamp of the leading and falling edges of the input pulse are extracted with enough precision, then it will become possible to, after calibration, relate the time difference between the two samples and the pulse amplitude. A function of the time-over-threshold (ToT) information versus input charge would thus serve the purpose of extracting a measure of the pulse energy. As these measurements would greatly rely on the condition of having precise time information, the time resolution of the front-edge becomes of utmost importance. Nonetheless, even if a ToT vs. input charge relation is linear (studied further in the text), thorough calibration processes may be needed to compensate the time walk of the signal within its dynamic range. Figure 2.5 illustrates the time walk issue, which fundamentally consists on the variation of the crossing times with different pulse heights or, equivalently, input charge. Although the impact of the time walk can be lessened with the use of fast amplifiers, it still requires the implementation of correction measures. Waveform sampling architectures can use amplitude information as input to a constant fraction discriminator (CFD). That being the case, the threshold is set as a function of the pulse height, which results in a constant delay for the dynamic range of the input charge. If a ToT architecture is envisaged instead, there is no such input, hence time walk correction shall likely require off-detector look-up tables which, after calibration, will feed the trigger algorithm with a rectification factor.

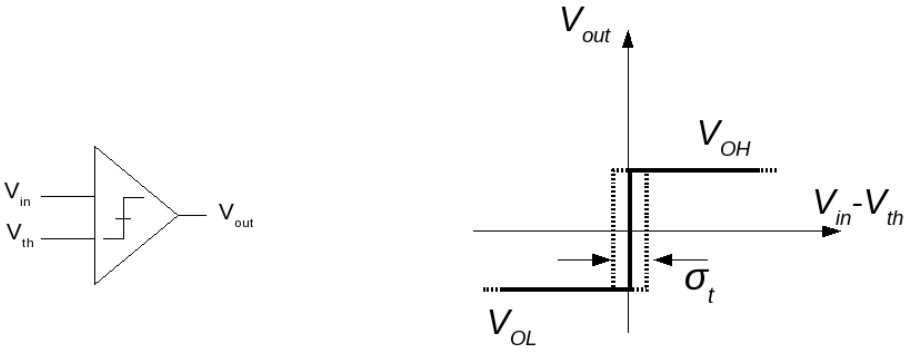


Figure 2.6: Jitter on the comparator output caused by fluctuations of the input signal

Electronic noise

Since the design effort of TOF-PET detectors lies on the possibility of having precise time stamps, this section focuses on the degradation of such measurement due to excessive electronic noise. A time stamp of the event will be obtained by feeding a discriminator with a very fast triggering pulse, produced by a high-bandwidth amplification stage. The output *rms* noise voltage of the signal output appears as an input to the discriminator, and will be translated as an uncertainty on its transition region, leading to jitter and thus deteriorating the timing measurement accuracy. Figure 2.6 represents this postulate when a comparator is used to generate the time stamp. For this discussion, it can be assumed that such comparator has infinite gain, and it is further assumed that the noise introduced by the comparator is negligible. If its output is clamped at V_{OH} and V_{OL}, then the transfer curve (shown on the right) is affected by the variation σ_t, which is a function of the voltage noise at the input V_{in}.

Being the transition region (of the comparator) centered at a given threshold V_{th}, then the slope of the signal $[\delta_v/\delta_t]_{v_{in}=V_{th}}$ must be maximized in order to mitigate the voltage fluctuations caused by the unwanted random electronic noise. That is to say, given the total *rms* noise voltage σ_v and the slope $[\delta_v/\delta_t]_{V_{in}=V_{thX}}$, then the contribution of the electronics noise (superimposed to V_{in}) to the degradation of the timing resolution is given by [Blum, Casey2003]:

$$\sigma_t\ (ps) = \frac{\sigma_v}{\left[\frac{\delta_v}{\delta_t}\right]_{v_{in}=V_{th}}} \left[\frac{mV}{mV \cdot ns^{-1}}\right] \tag{2.1}$$

Figure 2.7 shows a graphical insight of the problem. The effect of the electronics noise in the time resolution of a particle detection system can be isolated from the influence of the photon arrival time fluctuations, as it is considered that the contribution to the jitter due to the variance introduced by the SiPM itself and scintillation is statistically independent

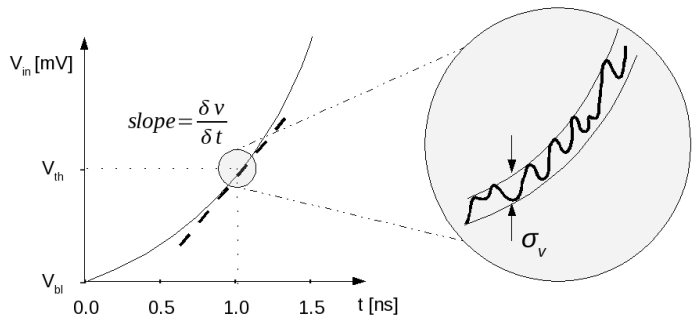


Figure 2.7: Detail of the input electronic noise at the threshold level, where the derivative of V_{in} is calculated.

from that of the electronics. This variance includes changes in the shape of the scintillation pulse [Maas2008], as well as the time drift inherent to the e-h pair generation in the SiPM. In fact, if the transit time of a single photon in the SiPM is reported to be around $100 - 200\ ps$ [Seifert2009b], one could predict that the coincidence resolving time (CRT)[3] would be constrained to this minimum. Fortunately for those who envisage the design of time-of-flight systems, that may not hold true.

Electron arrival time fluctuation

The current pulse produced by the SiPM is evidently of a finite slope, i.e., its rise time is not zero. As a result of the scintillation crystal decay time, the group of photons arrive to the photodiode matrix within a finite interval of time. Each incident photon creates an e-h pair, producing a finite amount of charge that sums up in time to that produced by the precedent photoelectron. Meaning, the contribution of each phototoelectron increases, arithmetically, the slope of the signal produced at the output of the SiPM [Blum]. Or even, that is equivalent to say that the slope of the SiPM current output due to the simultaneous arrival of n photons is n times steeper to that produced by a single photon. From this postulate, and according to Equation 2.1, it is foreseeable that a higher comparator threshold and thus higher signal slope would improve time measurements.

However, the time of arrival of these photons is weakly correlated to t_0. In addition, the statistical time distribution of the arriving photons (number of photoelectrons per time unit) is reflected as a fluctuation in the shape of the rising edge of the output signal. Needless

[3]defined in [IUPAC] as "The greatest time interval that can elapse between the occurrence of two or more consecutive signal pulses, in order that the measuring device processes them as a coincidence". For a PET detector, the two consecutive pulses refer to the signals produced at the extremities of the LOR.

is to say, it has been proven that an optimum threshold exists, and it corresponds to a number of 2-5 photoelectrons [Seifert2009b]. Therefore, a good time measurement implies a discriminator that is able to detect the arrival of these first photoelectrons, within the first nanosecond after the event.

It can be thus assumed that the trigger level V_{thX} can be optimized in order to minimize the effect of the noise produced by the amplification chain. That is to say, V_{thX} must be set high enough to avoid constant triggering due to the high dark current rate and to hold a large derivative, but low enough to avoid the pulse shape fluctuations due the photon arrival statistics.

In any case, it has been demonstrated that the low-noise is a key requirement for assertive time measurements. This work intends to lower the contribution of the electronic jitter to the degradation of the system's time resolution, which can be achieved with a low-noise oriented design.

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Chapter 3

Analogue Front-end Circuit Design

The front-end amplification channel herein reported is to be integrated in a new front-end ASIC suitable for data acquisition of radiation detectors with accurate timing. Such a chip will find application in TOF applications for medical imaging, and will be required to be a multi-channel, low-noise and low-power front-end integrated circuit for timing and charge measurement. This chapter introduces the proposed channel architecture and depicts the design iteration from a top to bottom perspective.

3.1 Channel architecture

The goal of the analogue front-end design reported in this work is to validate an architecture suitable to be used with waveform sampling, time-over-threshold or multi-threshold based signal processing schemes. Two outputs must hence be produced in order to accomplish the required flexibility: a fast current pulse, appropriate for timing measurements and the amplified voltage signal with an integration constant that maximizes signal-to-noise ratio, from which the charge of the input signal can be extracted. The current produced by the SiPM, hence the input charge for the readout electronics, is considerably large (cf. with Section 2.1) and thus there is not much amplification needed. However, since the channel design is expected to be back-compatible with other low-gain photodetectors [1], a two-stage solution is envisaged. Likewise, a first stage shall be used to buffer the signal pulse, shielding a second-stage charge sensitive amplifier from the high parasitic capacitance of the photodetector.

Figure 3.1 exemplifies the derivation of a discriminator signal *Vsync* out of the fast current pulse path. A fast trigger pulse is generated as an amplified (or unitary) replica of the input

[1] Zecotek MAPD-3N characterization was performed at TagusLIP [Ines2009] and shown to have typical gains 10x lower than those achieved with the SiPM specified in section 2.2.1.

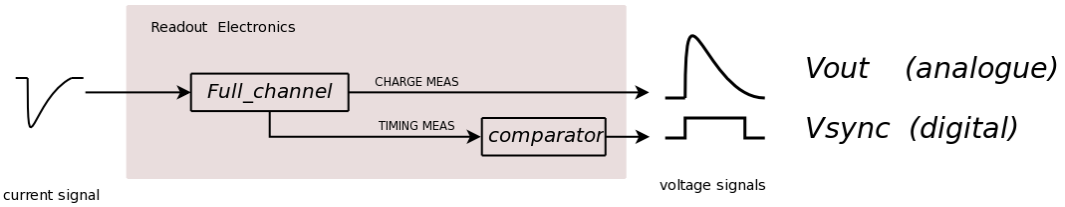

Figure 3.1: Readout electronics I/O topology: a fast and a shaped signals are used for timing and charge measurements, respectively.

current signal. The trigger output can be fed to a comparator, which threshold voltage shall be programmable, and used for ToT extraction.

An analogue shaped output, V_{out}, is directly produced by the $Full\_channel$ circuitry. The V_{out} output peak voltage must be proportional to the input current peak (labeled i_{peak} in Fig. 2.4). If a general transimpedance function with two poles is admitted, then the transfer function would be described by Equation 3.1:

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{R_{TIA}}{(1+s\tau_1)(1+s\tau_2)} \tag{3.1}$$

The specifications impose an output pulse maximum swing of $1.0V$ for an input pulse peak of $550\mu A$ (corresponding to the average charge measured with a centered DoI, for a 511 keV photon: refer to Table 2.1). The peaking time of the response to a Dirac delta (with a duration of 50 ps) is expected to be below 20 ns. These requirements define the transimpedance amplifier in terms of gain and pulse shaping constants.

The overall channel architecture is represented by the block diagram in Figure 3.2. The proposed circuit comprises two distinct signal paths for both timing and charge measurements, which common input is a buffered current-mode replica of the signal from the photomultiplier. For the charge measurement circuitry, the current is scaled down by a fixed factor of M, whereas for time extraction a multiplication ratio of $N = \{1, 2\}$ provides a fast replica of the input current signal. Feeding the shaper with higher currents would not only increase the overall power, unnecessarily, but also require a higher value of the feedback capacitance in order to keep the time constant of the integrator, as the transresistance, hence R_F, would be made smaller. A set of PMOS and NMOS current mirrors scales down the current buffer output current by a (fixed) factor of 32. This strategy, however, lowers the amplifier sensitivity G_0 at least by the same order. Being that a delta pulse of charge Q_δ produces a voltage output of amplitude ΔV_{out}, then an equivalent noise charge (ENC) can be defined as the delta charge $Q_{\delta ENC}$ at the input that produces an output ΔV_{outENC} which is equal to the total output

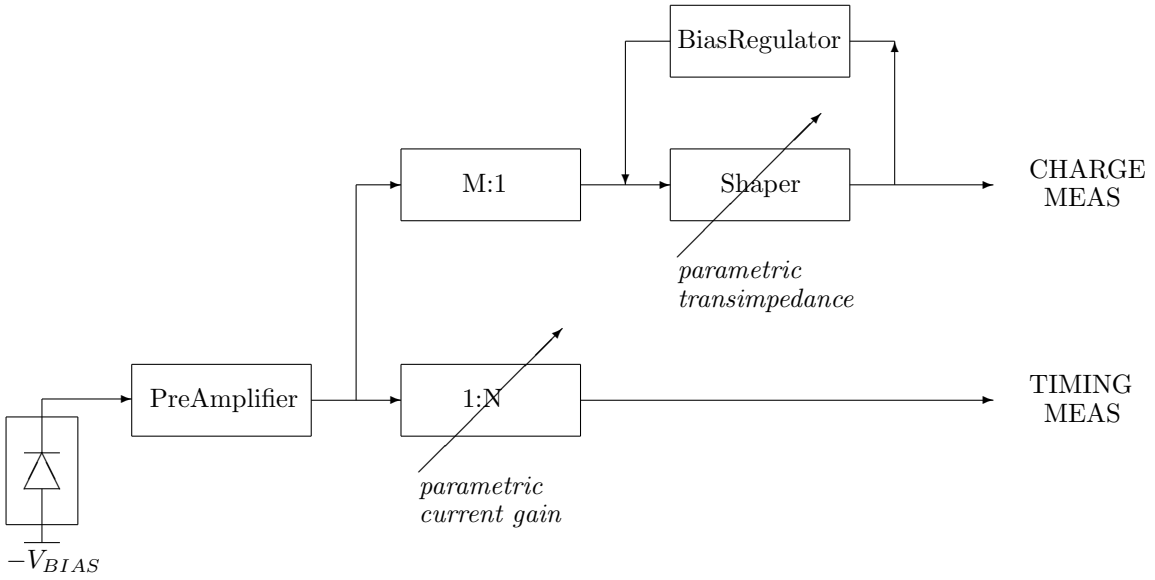

Figure 3.2: Block diagram representation of the front-end electronics.

rms noise voltage of the amplifier, $V_{no\ rms}$, or (with convenient units conversion)[2]:

$$ENC\ (e^-) = 6250 \cdot \frac{V_{no\ rms}\ (mV)}{G_0\ (mV/fC)} \tag{3.2}$$

One can thus anticipate an ENC that is, at least, k times superior to what is found in literature for low gain photodetector amplifiers. Hence, the ENC is not an even-handed benchmark of comparison, in the knowledge that the input referred noise will also be decreased by the same amount.

If lower gain photodetectors are to be used (as above mentioned in page 29), the scaling factor has to be lowered. Albeit the solution thought is quite simple, as it is based on the same principle used for the *Itrig boost* option, it has been decided not to implement it on the first test chip. Similar strategies to generate a fast trigger and an "energy branch" can be found in the literature, either in discrete implementations ([Seifert2009b]) or fully integrated solutions ([Corsi2009]).

The SiPM produces, typically [MPPC], a negative current signal, as suggested by the representation of the n-type cathode at the output port of the device. Thus, the input port of the current buffer collects electrons, which is to say, the input signal presented to the pre-amplifier is a negative current pulse. The need for a current buffer as first stage is due to the high value of the stray capacitance C_d at the terminals of the device. In fact, considering

[2] $1\ e^- = 1.6 \cdot 10^{-19}\ C$

a generic amplifier with an input impedance Z_{in}, the frequency response of the amplifier is affected by the pole with a time constant given by $\sigma_1 = Z_{in} \cdot C_d$. Considering the hind-end of the SiPM capacitance (more than 300 pF for a 9 mm^2 device) and an input impedance of 50 Ω (DC), then the amplifier would be plagued by a dominant pole around 15 ns (≈ 10 MHz). This value is of the same order of τ_1 and τ_2, defined by equation 3.1. Consequently, the shaping function would no longer be well defined, as the position of its poles should drift with the value of C_d. A buffer placed before the shaper serves the purpose of breaking the dependency of $V_{out}(s)/V_{in}(s)$ with the value of the photodetector's stray capacitance. The output of the current buffer feeds the shaping stage, which limited frequency response is used to optimize the signal-to-noise ratio for the energy measurement.

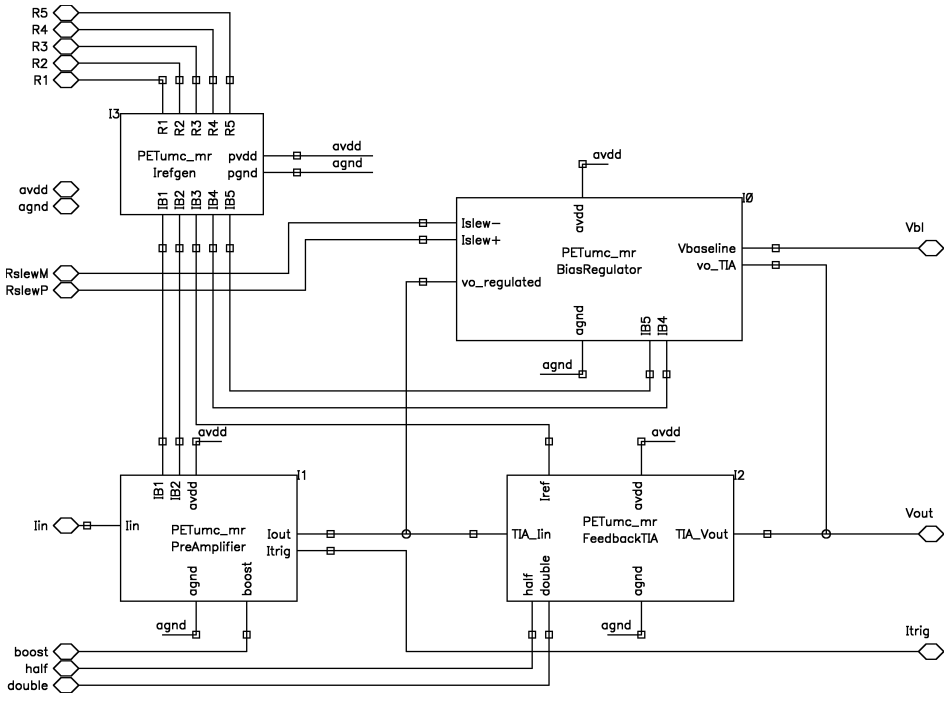

Figure 3.3: Schematic diagram of the top level *Full_channel*

Figure 3.3 gives an overview of the block level hierarchy of the above described architecture. The project can be intuitively subdivided into 4 blocks, hereinafter designated as *PreAmplifier*, *FeedbackTIA*, *BiasRegulator* and *Irefgen*. The top cell *Full_channel* is represented by figure 3.3. In the attempt to cross-relate this representation with the one of Figure 3.2, both the *BiasRegulator* and the shaper stage (*FeedbackTIA*) are easily matched. The *PreAmplifier*, however, includes both the pre-amplification stage (current buffer) and the current conveyors with unitary and parametric current gains. The proposed implementation for a single-channel prototype comprises also a current reference generator, *Irefgen*, which

is here considered as a sub-block of the *Full_channel*. If a multichannel test chip had been proposed, the reference generator circuit would be shared.

The signal *I/O* are labeled *Iin*, *Vout* and *Itrig*, which respectively carry the input current, a voltage output of a shaped signal (suitable for charge measurements) and a current output for timing measurements. Three logic control signals, *boost*, *half* and *double* are used to increase the output current on *Itrig*, halve and double the transimpedance gain of the shaper, respectively. *RslewM* and *RslewP* connect to an adjustable off-chip resistor used to change the non-linear buffer slew-rate, whereas *Vbl* sets the front-end output baseline voltage level. An additional set of five off-chip resistors, connected to *R[1..5]* allow trimming of the reference currents *IB[1..5]*. The analogue signal power planes *avdd/agnd* were, due to restrictions on the number of *I/Os*, shared with the *Irefgen* power planes *pvdd/pgnd*.

3.2 Pre-Amplifier

3.2.1 Low input impedance stage

It has been predicted that the excessive parasitic capacitance at the terminals of the SiPM can pose severe bandwidth constraints to the design of the front-end amplifier. That is easily confirmed by inspection of Figure 3.4, which shows the relevant capacitive elements of a general signal equivalent model of the photodetector and the input amplifier[3]. Although a

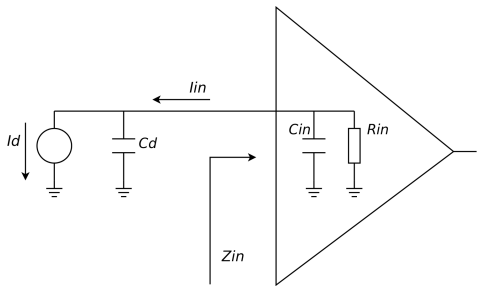

Figure 3.4: Front-end amplifier input impedance and internal poles: effect on amplifier bandwidth.

first order system is a simplistic approach of the input impedance of the amplifier, it serves the purpose to demonstrate the contribution of the SiPM capacitance to the input node related time constant. A fair design of the amplification chain will likely make this pole dominant. Defined by the input resistance of the amplifier and the node capacitance, $\tau_{in} = R_{in}(C_d+C_{in})$, then the amplifier input current is given by Equation 3.3:

$$I_{in}(s) = \frac{1}{1 + s\tau_{in}} I_d(s) \tag{3.3}$$

It is common sense that a transimpedance topology shall provide the most adequate gain-bandwidth product for the current signal amplification of a photodetector, as it can have considerably low input impedance values. Unfortunately, that can only be achieved at the cost of moderate closed-loop gains. Even with an optimized design, the condition of having an input impedance that is dependent of the transimpedance gain is inevitable. For the envisaged application, the use of a multi-channel chip implies that the gain of each amplifier is configurable, such that it compensates the intrinsic gain of the respective optical detection chain. In that scenario, the input impedance of each channel would change accordingly to the defined transimpedance gain. That is not an option if one intends to build an ASIC with 192 inputs, since both noise and inter-channel crosstalk effect would become unpredictable.

[3]Adapted from [Nero2008]

More than knowing that a lower input impedance shall fasten the circuit, one needs to assure that Z_{in} is low enough to allow high integration of amplifier channels. In fact, since the signal current pulse may exceed 0.5 mA, a 50 Ω resistance will cause a 25 mV bounce at the input node. With that in mind, the designer must aim to drop Z_{in} down to a maximum of 1-2 Ω, perhaps at the cost of having a reduced stability margin.

In brief, the above discussion summarizes the problem statement: not only a low input impedance must be achieved in order to reduce bandwidth constraints, but also the dependency of the TIA gain and the photodetector capacitance must be broken. The solution is the inclusion of a pre-amplification buffer, capable to convey a current from a low-Z input port into a high-Z output port. This problem is extensively depicted by [Nero2008], wherein appropriate design techniques are proposed for the implementation of such current matching devices.

A survey on the noise performance of common transimpedance topologies ([Rolo2010]) has revealed that the regulated common-gate[4] topology not only ensures a very low input resistance but also allows a good low-noise performance. The circuit, also referred to as regulated cascode, common-gate with gm-boosting or RGC, can be used as a current conveyor (rather than as transimpedance), as shown by Figure 3.5. An intuitive understanding on the

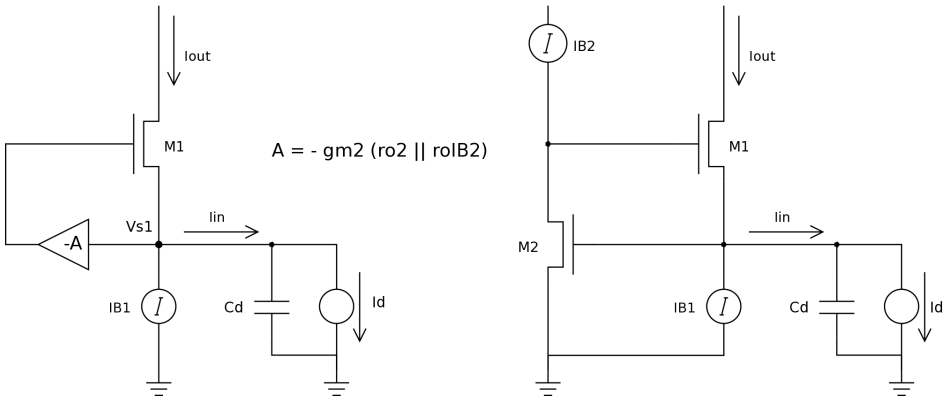

Figure 3.5: The RGC circuit diagram: regulation gain schematic (left) and its implementation with a common-source amplifier of gain $-A$ (right).

effect of the circuit input impedance may help to depict this circuit. Consider the equivalence stated by equation 3.4:

$$Z_{in} = \frac{\Delta V_{s1}}{\Delta I_{in}} \Leftrightarrow \Delta V_{s1} = Z_{in} \Delta I_{in} \tag{3.4}$$

[4]The gain boosting technique described was introduced by [Hosticka1979] and further studied in [Scakinger1990] with a 3 μm SACMOS (a proprietary technology from FASELEC AG, subsidiary of Philips Semiconductors) process.

In practical terms, that means the lower the input resistance, the lower will be the voltage bounce at the input node due to a pulse of the signal current. That is exactly what is envisaged, in order to reduce crosstalk effects on highly integrated multi-channel solutions. Furthermore, as a result of a smaller variation at the input node, the drain current I_{ds} of M1 remains steadier, yielding an output resistance that is increased by the same amount of the regulation gain, thus becoming $Z_{out} = Ag_{m1}r_{o1}$.[Razavi]

The small-signal equivalent of the regulated cascode is shown in Figure 3.6, where

$$Z_{in} = \frac{V_{s1}}{I_{in}} \tag{3.5}$$

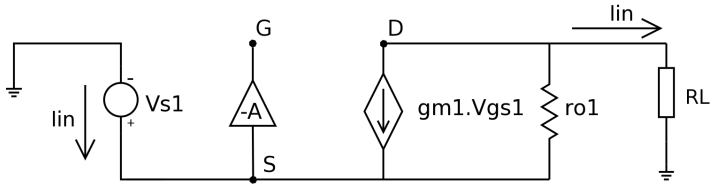

Figure 3.6: The RGC circuit small-signal equivalent: the load R_L has ideally a zero small signal impedance, corresponding to an ideal power source biasing the drain of the input transistor.

The Kirchhoff's current law can be derived from the small-signal model:

$$-I_{in} - g_{m1}V_{gs1} + \frac{V_{s1} - I_{in}R_L}{r_{o1}} = 0 \tag{3.6}$$

Having the gate-to-source voltage of M1 given by

$$V_{gs1} = -AV_{s1} - V_{s1} = -V_{s1}(1 + A) \tag{3.7}$$

Equation 3.6 can be re-written as:

$$-I_{in} + g_{m1}V_{s1}(A + 1) + \frac{V_{s1} - I_{in}R_L}{r_{o1}} = 0 \tag{3.8}$$

From 3.5,

$$-1 + Z_{in}\Big(g_{m1}(A + 1) + \frac{1}{r_{o1}}\Big) - \frac{R_L}{r_{o1}} = 0 \tag{3.9}$$

Considering a typical value for $r_{o1} = 20\ k\Omega$ ($g_{ds1} = 50\ \mu S$); if the drain of M1 is a diode-connected PMOS load with high transconductance, then the value of R_L is indeed very low and given by $R_L = \big(\frac{1}{g_m}\big)||r_o \approx \frac{1}{g_m}$ [Razavi]. In any standard deep submicron technology, a saturated wide PMOS ($W/L > 500$) will exhibit a resistance down to some hundred Ohm (assuming $R_L = 250\ \Omega$). The above premises imply that $\frac{R_L}{r_{o1}} << 1$.

Moreover, with a transconductance of 5 mS and a regulation gain of 80 ($A >> 1$), one can postulate $g_{m1}(A+1) >> \frac{1}{r_{o1}}$. Equation 3.9 can suitably be simplified to:

$$Z_{in} = \frac{1}{Ag_{m1}} \tag{3.10}$$

The RGC effectively enhances the transconductance of the input stage as its input resistance is diminished by a factor A, when compared to the common-gate (CG) topology. It is though worth mentioning that the later would already impose a small Z_{in}, since a current input into the source of an NMOS sees a resistance which is given by the inverse of its transconductance, $R_{in} = g_m^{-1}$. However, given that the input transistor of a CG circuit is the predominant source of noise, its g_m can only be increased with the penalty of increasing the transistor current noise.

If the regulation gain of the RGC is implemented with a common-source amplifier, the amount of feedback is given by the voltage gain A:

$$A = g_{m2}(r_{o_{M2}} || r_{o_{IB2}}) \tag{3.11}$$

That is equivalent to

$$A = g_{m2}\frac{1}{g_{ds_{M2}} + g_{ds_{IB2}}} \tag{3.12}$$

inasmuch ro_{M2} and ro_{IB2} are, respectively, the g_{ds}^{-1} of the common-source M2 and the PMOS current mirror IB2. In the RGC circuit, the newly introduced regulation transistor adds a new source of thermal noise. Its contribution becomes dominant to the total rms output noise voltage, which can be driven down with higher transconductance values of M2 [Medeiros2009].

The above estimate measures the resistive component of Z_{in} with a good level of agreement with experimental validation (refer to Section 3.2.2 for a concrete example). It is valid only at low frequencies though, since the regulation gain rolls-off for higher frequency. On account of the total parasitic capacitance at the input node, the frequency response of the regulation loop will show the effect of such capacitive load. More than a decrease of A at high frequencies, the stability of the feedback loop is also affected with C_{tot} (a sum of the total device capacitance and those of the local signal path parasitics). Predictably, higher values of C_{tot} increase the phase margin of the loop, since the dominant pole is pushed towards zero and hence the zero-gain crossover happens earlier in frequency. Therefrom, the bandwidth is cut back and a larger fraction of the high frequency spectra of the input current signal is rejected, enlarging the rise time of the buffered replica at the output.

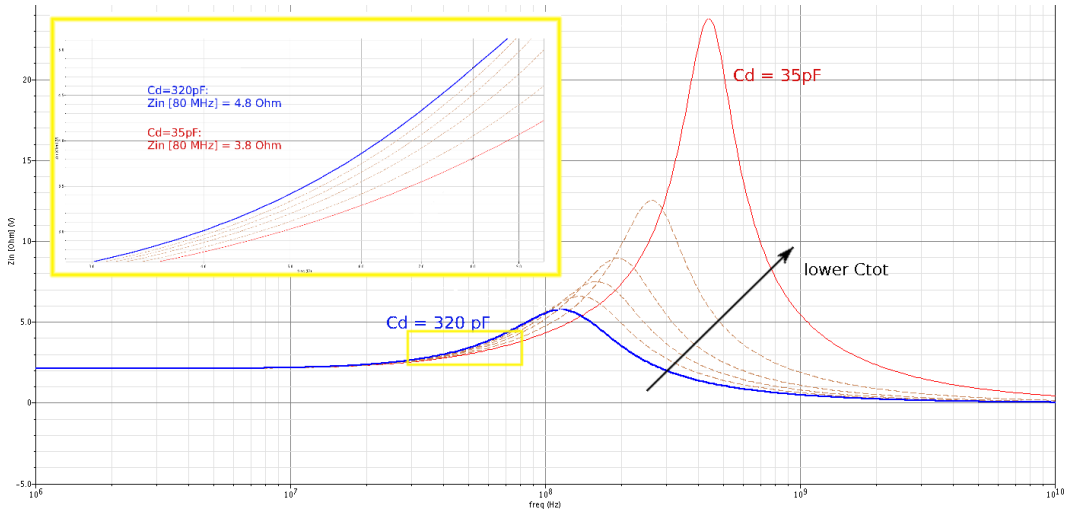

Figure 3.7: *PreAmplifier*: Input impedance frequency characteristic. The blue and red bold lines correspond to the curves of Z_{in} when the photodiode parasitic capacitance is, respectively, 320 pF and 35 pF. The highlighed fraction shows a sub-range of the frequency sweep (30-90) MHz, while the waveforms are plotted for the extended range 10 MHz up to 10 GHz.

The data plotted on Figure 3.7 supports the above axiom, proving that higher parasitic capacitances at the input node reduce the bandwidth of the regulation loop gain and hence the circuit input impedance grows earlier in frequency. The same data seems to suggest that Z_{in} rolls-off for higher frequencies. However, a closer look reveals the sense of the peaking observed, as it turns evident that the misleading effect is caused by the indirect measurement of Z_{in}. The impedance curves are generated by exciting the *PreAmplifier* input port with a 1A amplitude frequency-variable sinusoidal current and probing the voltage of the input node with respect to the ground plane (the practical visualization of equation 3.4). Indeed, the total capacitance of the input node appears as a current divider to the sinusoidal signal. That being said, the reactance of C_{tot} at higher frequencies will also drop, beyond a point where it is comparable to the resistive input impedance, and further to a degree where it behaves like a short-circuit for small-signal. This can be easily corroborated; being the capacitive reactance given by:

$$X_C = \frac{1}{2\pi f C} \tag{3.13}$$

Then, for $C_{tot} = 320\,pF$, $X_C[f = 120\,MHz] = 4.2\,\Omega$. From that frequency point onwards, this value will continue to decrease and the current is sunk by the ideally infinite admittance of C_{tot}.

There is, however, an important learning from the above conclusions. A large peak of Z_{in} (seen at high frequencies for low values of C_{tot}) may evidence an insufficient margin between

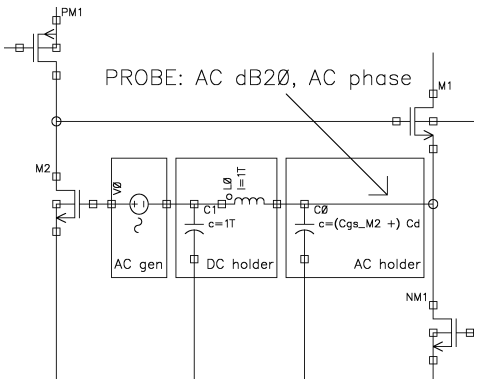

Figure 3.8: *PreAmplifier*: Testbench for regulation loop gain stability.

the gain and phase crossover points of the regulation loop. As such, the ratio (Zin[peak], Zin[DC]) is a first measure of stability of the regulation loop. Meaning, the higher harmonics of the input signal will cause voltage ringing, since they are affected by an higher input impedance. That is tolerable up to a certain extent, as long as the poles remain on the left half of the s-plane.[5] Figure 3.8 represents the schematic diagram used for a rough assessment of the loop stability. Once the loop is broken, a capacitor of value $Ctot$ is included to emulate the AC environment. Even with a very large regulation transistor, the device parasitic C_d shall be much larger that the total gate capacitance of M2, and thus the later can be neglected.

It is of utmost importance to be aware that the low input resistance of a circuit, which nonetheless expectably defines the dominant pole position in frequency, may not realise the fastest slope of the output signal. Not, at least, if that reduction is not paired with an increased bandwidth of the regulation loop. The work on [Nero2008] proves with transversal benchmarks that a current conveyor such as the RGC (or "super-transistor" [Nero2008, Scakinger1990]) may not hold the best compromise between input impedance reduction and bandwidth. Thus far, one can also admit that the bandwidth performance of a regulated cascode can be improved with traditional analogue techniques, namely the reduction of the open-loop gain A.

3.2.2 Transistor-level: *PreAmplifier*

The discussion on the transistor level implementation of such design is supported by Figure 3.9.

The optimization of the RGC circuit is not straightforward. Meaning, although small-

[5] Assumption based on experimental results from transient simulations.

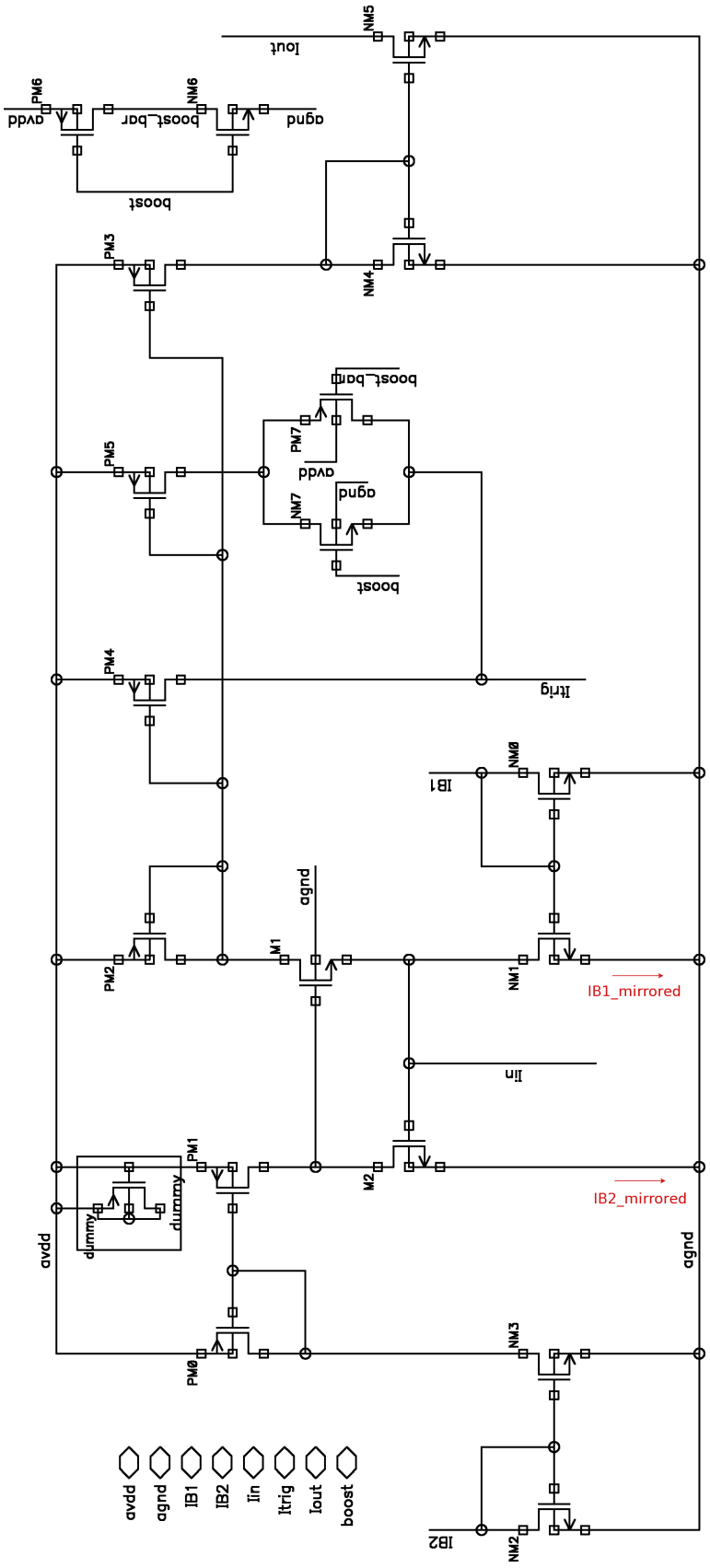

Figure 3.9: Schematic diagram of the *PreAmplifier* block

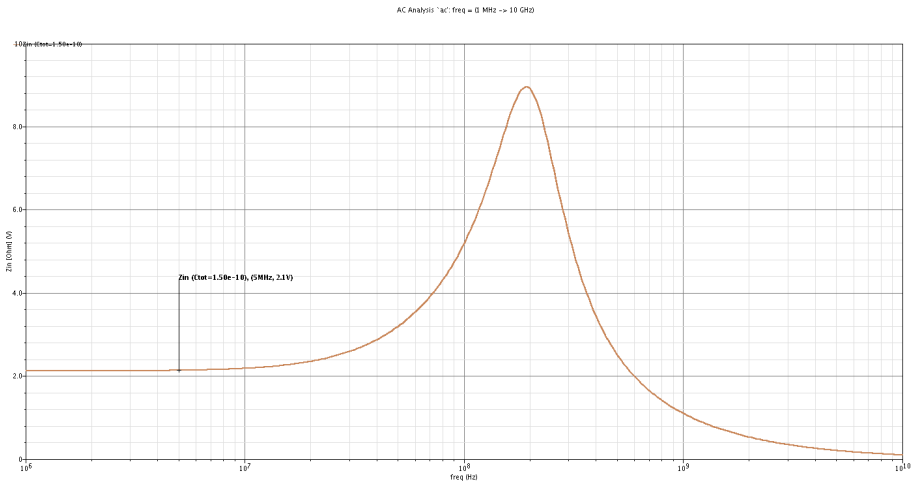

Figure 3.10: Input impedance characteristic for nominal operation: Z_{in} is the indirect measure of the AC response of the pre-amplifier, probed in voltage at the input node, when excited by a 1A amplitude frequency-variable sinusoidal current. For a device terminal capacitance of 150pF (depending on the active area, this value can reach 320 pF, being that the minimum is around 35 pF), the input impedance is kept purely resistive up to a frequency of 5 MHz: (Z_in[DC] = 2.1 Ω. The power dissipation required for biasing M1 and M2 is ≈ 5 mW.

signal analysis of the open loop amplifier may provide valuable hints, extensive simulations are required. Meaning that, since the bias current of both the input and the regulation transistors are of the same magnitude of the input signal itself, non-negligible voltage excursions of the internal node cause a drift on the operating region of M_2. Likewise, the local pole and zero positions in frequency change during the transient.

The current buffer was designed, departing from the considerations made by [Scakinger1990] and [Park2004], for what is expected to be the optimum compromise between input impedance, power consumption and and stability. The *PreAmplifier* input stage is biased by $IB1$ and $IB2$ (parametric), which define the transconductance of the input and regulation transistors ($M1$ and $M2$) of the regulated common-gate. Given by the inverse of the transconductance of the input transistor multiplied by a factor of A, the resistive value of the input impedance is thus tunable by adjusting the bias current of M1 and the regulation gain. Evidently, the operating point is changed whenever these bias are re-defined.

For the typical operating conditions, with $R1\_GND = R2\_GND = 10\ k\Omega$ (from which the bias currents on M1 and M2 are, respectively, 500 μA and 1000 μA), the DC value of Z_{in} was extracted from the operating point computed by simulation and compared with the simulated AC response of the input stage.

From the data in Figure 3.11 and Equation 3.11, $A = g_{m2}/(g_{dsM2}+g_{dsIB2}) = (14.2m)/(153\mu+$

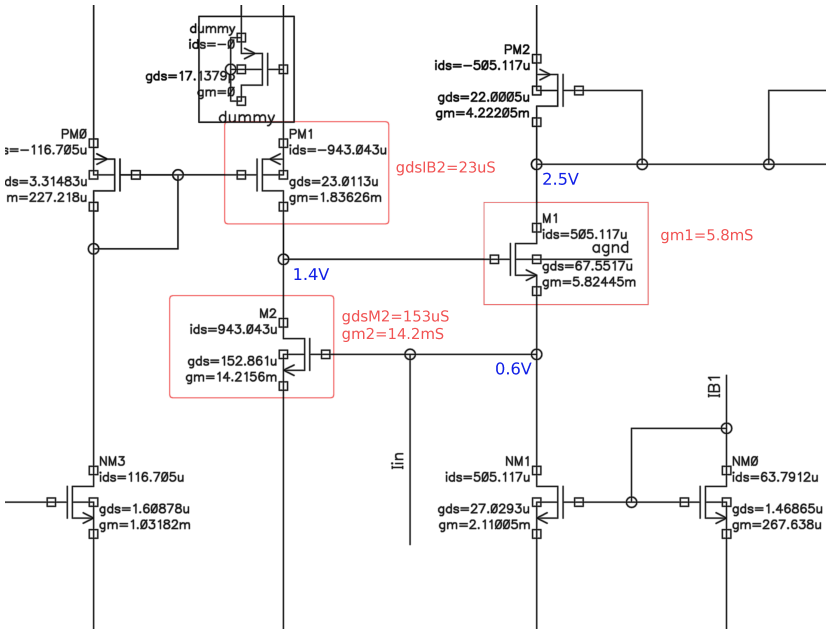

Figure 3.11: Operation point of the input stage (typical), from which the key parameter labels used for the calculus of Z_{in} are signaled

$23\mu) = 81$. With $g_{m1} = 5.8\ mS$, using Equation 3.10 results in:

$$Z_{in} = \frac{1}{Ag_{m1}} = \frac{1}{81 \cdot 5.8m} = 2.1\ \Omega \tag{3.14}$$

which is in good agreement with what was measured by simulation.

Figure 3.12 illustrates the current mode outputs of the buffer. The charge and timing measurement paths are fed by the $PreAmplifier$ current outputs $Iout$ and $Itrig$, respectively. As specified, the fast output rise time can be improved (12-15%) by doubling the multiplication factor or the current mirror. For that purpose, the *boost* signal is externally set to a logic "1", from which a complementary signaling is produced to control a CMOS transmission gate. The RGC current is scaled down by a factor of 32 and output for the charge measurement circuitry.

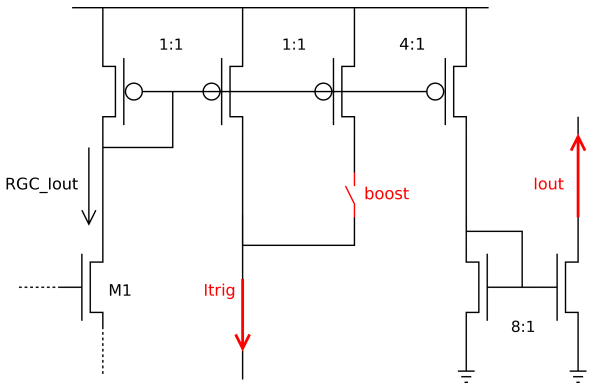

Figure 3.12: Operation point of the input stage (typical), from which the key parameter labels used for the calculus of Z_{in} are signaled

3.3 Shaper module

3.3.1 Feedback transimpedance amplifier

The charge measurement and signal shaping is performed by a transimpedance amplifier (TIA) with variable gain, which high-level representation is shown in Figure 3.13. As the input charge, replicated by the *PreAmplifier* circuit, is transferred to the capacitor C_F, a voltage across it is developed. Consequently, the output node suffers a potential increase that is proportional to the charge deposited in the capacitor and, hence, $V_{out} \propto Q_{in}$. In this context, the circuit is commonly designated as a charge sensitive amplifier (CSA), as it performs a charge-to-voltage conversion. The circuit integrates the input current, with a shaping constant τ_F given by $R_F C_F$. The output voltage signal is thus an amplified (and inverted, due to the OA topology) and shaped function of the input charge.

If the OA gain is very high, then the transimpedance gain approaches the value of the feedback resistor R_F. Since the shaped signal is intended to be routed directly outside the chip, a buffer (with high input impedance and low output impedance) needs to be included such that the OA experiences no significant gain loss (cf. with Figure 3.14).

Likewise, would the feedback resistor R_F load directly the high output impedance output of the OA, then an open-loop gain drop, more severe if the transimpedance gain was set lower (refer to Table 3.1), should be observable. Not only the buffer solves this issue, it also isolates the feedback capacitor from the parasitic capacitances of the output node. Specifically, if the circuit is to drive directly a signal off chip, the junction capacitance of the ESD protection diodes (that can be as high as 2pF) would largely degenerate the integration constant of the shaper.

Nominal values of the feedback resistance and capacitance components are 95 $k\Omega$ and

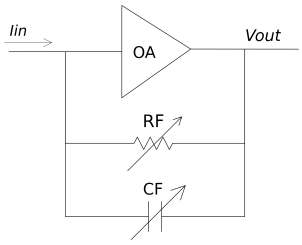

Figure 3.13: Generic transimpedance amplifier with variable gain.

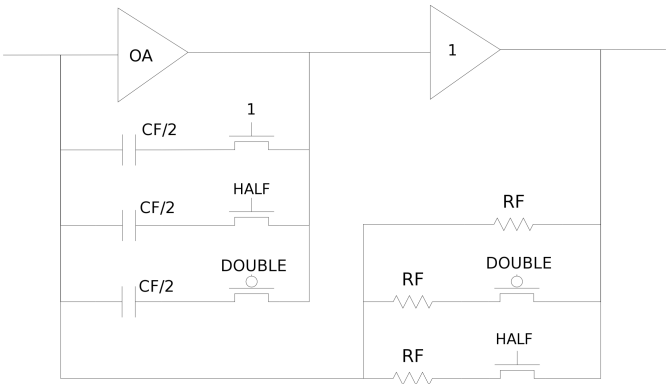

Figure 3.14: Implementation of the TIA variable gain, switching controlled by external signaling.

175 fF, yielding $\tau_F = 17\ ns$. The use of a smaller feedback capacitor could leave the transfer function more susceptible to process biasing. Meaning, if C_F was set lower than 100 fF, then its value would become of the same order of that of the parasitic capacitances (which can be estimated after layout netlist extraction). The value of the shaping constant is not arbitrary, but was specified to lay between 15 and 20 ns. Actually, it shall be made programmable for maximum flexibility, such that it can address application domains other than PET. Despite the value of τ_F is fixed, the transimpedance gain has to be programmable. A proof-of-concept was implemented, consisting of a two-bit gross gain control based on transmission gates with differential signaling. If such concept is validated by silicon results, a 5-bit word will be used to implement a coarse and fine tuning scheme for gain parametrization, suitable to address the expected distribution spread of the optical channel gain.

This spread in the channel gain is due to the SiPM gain variability, crystal pixels light yield or optical coupling. In order to account for these effects, parametric gain control must be a feature of a multi-channel solution. If SiPMs from different manufacturers are considered, or if different pixel sizes are two be used, the gross gain range would have to be necessarily wider that what was considered by the current design. The S10362-11 series [MPPC-11] have available $25 \times 25\ \mu m$, $50 \times 50\ \mu m$ (nominal) and $100 \times 100\ \mu m$ pixel size devices, with gains of 2.75×10^5, 7.5×10^5 and 2.4×10^6, respectively. Being G_{max} and G_{min} the limits of such interval, a gain range $G_{max}/G_{min} \cong 9$ would be required.

Table 3.1 shows the gross gain parametrization implemented, with $G_{max}/G_{min} = 4$.

3.3.2 Transistor level: *FeedbackTIA*

Figure 3.15 depicts the transistor level implementation of the TIA.

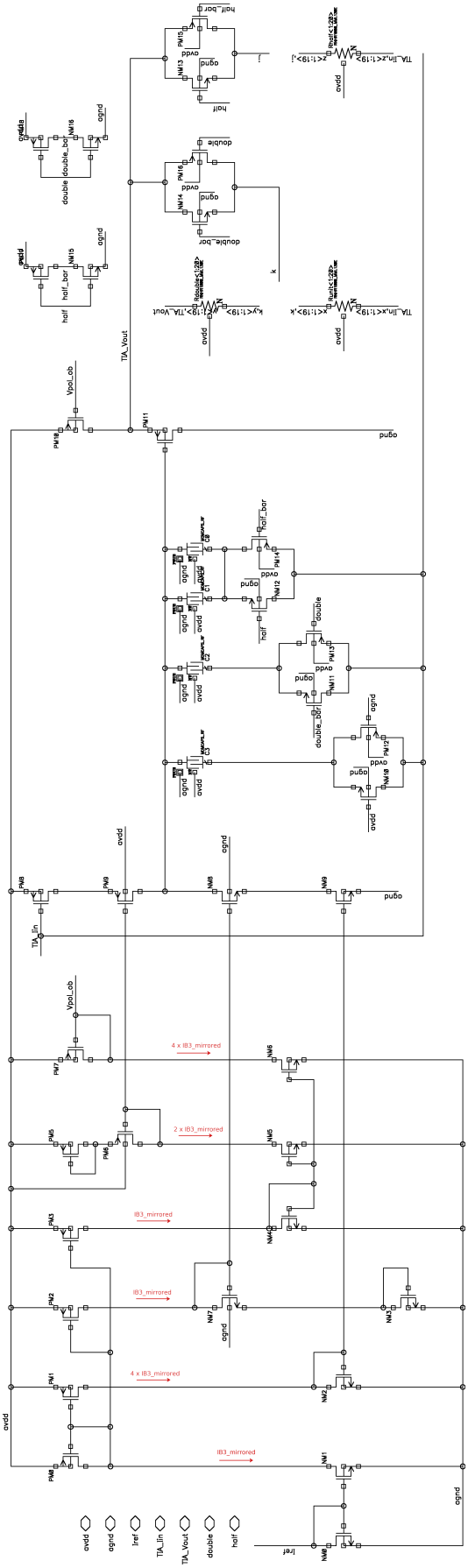

Figure 3.15: Schematic diagram of the *FeedbackTIA* block

DOUBLE	HALF	Total $C_{feedback}$	Total $R_{feedback}$	TI Gain	τ_F
0	0	C_F	R_F	$\approxeq 100k$	$R_F \cdot C_F$
0	1	$2C_F$	$R_F/2$	$\approxeq 50k$	$R_F \cdot C_F$
1	0	$C_F/2$	$2R_F$	$\approxeq 200k$	$R_F \cdot C_F$
1	1	$3C_F/2$	$2R_F/3$	$\approxeq 65k$	$R_F \cdot C_F$

Table 3.1: Parametric gain control set-up.

The OA is implemented with a cascode common-source PMOS input[6], loaded by a cascoded current-source (CS). The motivation is, obviously, to maximize the voltage gain while keeping enough voltage headroom at the output.

Given that the voltage gain for a CS stage ($A_v = -gm_{CS}R_D$) with a current-source load is $A_v = -gm_{CS}(r_{o_{CS}}||r_{o_L})$, the ways to maximize A_v are either the increase of the input transistor transconductance (PM8) or the load resistance. Every increase of g_m implies unavoidably the use of larger bias currents (more power) or wider transistors (increased parasitic node capacitances). Instead, it is desirable to put the effort on the increase of the output resistance. Although that can be achieved simply by increasing the length L of the transistor, the increase of the output resistance is only 50% when L is doubled, which is a modest result when compared to what can be obtained by cascoding devices. [Razavi]

A cascode transistor PM9 boosts the load resistance of the CS, $r_{o_{CS}}$, by a factor of $g_{m_{PM9}}r_{o_{PM9}}$ (neglecting the body effect of the PMOS devices). Similarly, a cascode NM8 increases the output resistance of the current-source mirrored by NM9. If we were to assume that the body effect of NM8 was also negligible, then the output resistance of NM9 would also raise by a factor of $g_{m_{NM8}}r_{o_{NM8}}$.[7]

The overall gain accomplished by the chosen topology is then given by Equation 3.15:

$$A_v = -gm_{CS}(r_{o_{CS}}||r_{o_L}) \approx -g_{m_{PM8}}\left[(g_{m_{PM9}}r_{o_{PM9}}r_{o_{PM8}})||(g_{m_{NM8}}r_{o_{NM8}}r_{o_{NM9}})\right] \qquad (3.15)$$

Using the values from Figure 3.16, retrieving $r_o = g_{ds}^{-1}$ an open-loop gain of ≈ 3600 can be estimated, when all transistors operate in the saturation region. The very high output impedance obtained by cascoding both the CS and the current-source not only permits high open-loop gains, but also isolates PM8 and NM9 from the voltage fluctuations on the output

[6]The use of PMOS type transistors reduces the flicker noise by a factor of 2 to 5 times, typically, when compared to an NMOS input.[Allen]

[7]That is a careless simplification though, since in this case the bulk and source of NM8 cannot be tied together. Nonetheless, the the twin-well analogue option does exists in the used technology, and the transistor could be laid in a separate well at the cost of a larger area consumption. If that is not the case, then the transconductance of the transistor is expected to be slightly higher, since the increase of V_{TH} due the the body effect will push the NMOS deeper in the saturation region.

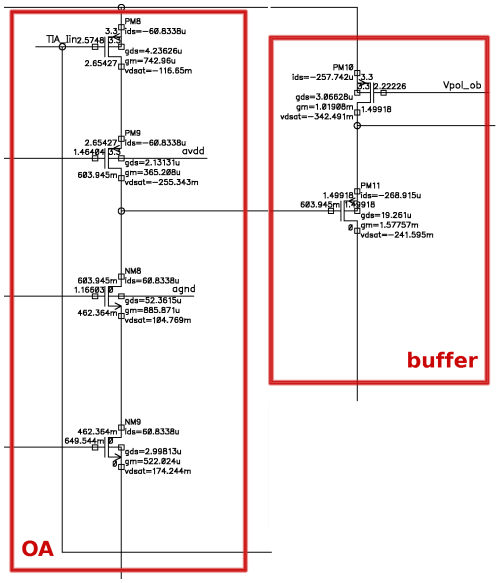

Figure 3.16: *FeedbackTIA*: DC node voltages and operation point, nominal transimpedance gain of $100k\Omega$, for the operational amplifier (left) and the voltage buffer (right).

node. With that, the input transistor is less prone to leave the saturation region, and the value of its transconductance is kept stable.

A common-drain stage is used as voltage buffer, and simultaneously eases the design effort to shift the DC level of the signal at the output of the *FeedbackTIA* block (typical values for V_{bl} lie around 1.5 V). The voltage signal at the output of the OA is replicated with unitary gain at the source of PM11, hence the configuration used for the output buffer is often called source-follower. PM10 is a current source, and operates in saturation. Since PM11 is built in a separate well, it will not suffer body effect. That being assumed, then the output impedance of the stage is approximately $Z_{out} = 1/g_{m_{PM11}}$ and the voltage gain is $A_v = 1$. If implemented with NMOS, or if the source and bulk of the PMOS were not tied, the V_{TH} dependence with the source voltage would cause undesired non-linearity. The only perceivable disadvantage is the lower mobility of P-type devices, which leads to a relatively higher output impedance.[Razavi]

In order to abide with the choice of a PMOS source follower as buffer, the DC level output of the OA (PM9/NM8 drains) must be kept very low (600 mV). In order to comply with the DC level required at the output (typical 1.5 V) and the voltage swing required (+1.0 V), the gate of PM11 is necessarily at a DC node voltage of $1.5 - V_{GS}(V)$.

3.4 Baseline holder circuit

The design of a 2-stage architecture requires both AC coupling (high-pass filtering) between stages and a baseline stabilization able to avoid the unwanted amplification of any offset voltage appearing at the output of the pre-amplifier. A simple strategy is to simply insert a blocking capacitor in the signal path which, if large enough, will not introduce significant changes to the transfer function. The drawback of using large capacitance values in multi-channel integrated circuits is the obvious prohibitive area overhead. Pulse amplitude measurements make therefore use of more efficient DC compensation schemes to avoid baseline shifts. The DC operation point at the input of the shaping stage is forced by a baseline stabilization block, commonly used in particle detectors due to its ability to correct baseline drifts with pulse rate [East1970, DeGeronimo2000].

Recall that the signal input vo_TIA and output $vo\_regulated$ of the block are, respectively, the shaped pulse voltage (channel output node) and the current injected at the input of the shaper. The external analogue signal $Vbaseline$ is sampled and compared to the output baseline voltage, producing a voltage difference which is fed to a transconductor. The current output of the transconductor is injected to the input of the transimpedance amplifier. This results in a virtual short-circuit between the inputs $Vbaseline$ and Vo_TIA, thus keeping the external output node DC value at a fixed programmable voltage level [Corsi2009b]. The transconductance function must reject variations caused by the fast signals at the output of the shaper, which is accomplished with a slew rate limited buffer. The block diagram of such low-pass transconductor is shown in Figure 3.17, where the non-inverting unitary gain buffer is implemented with a source-follower [Rivetti2007, Cobanoglu2007b].

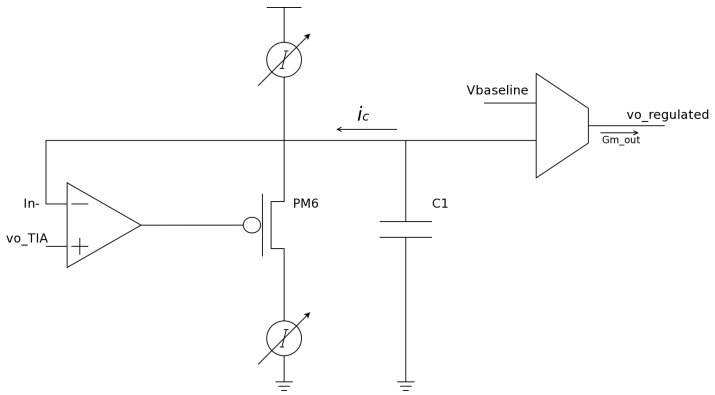

Figure 3.17: Block diagram of the *BiasRegulator*

3.4.1 Non-linear buffer

As above mentioned, the first stage is a non-linear voltage buffer with limited slew rate, which rejects the variations caused by fast signals to be processed by the feedback loop. With the exploration of this non-linearity, the gain of the series-series feedback loop can be dynamically reduced for fast and large signals [DeGeronimo2000]. That is to say, the transconductance gain of the *BiasRegulator* is attenuated for large input signals (voltage pulses at V_{out}, while slow movements of the baseline (imposed by trimming *Vbaseline*) are not affected by the buffer slew rate limitation. A clearer schematic of such circuit is shown in Figure 3.18. For simplicity, the dummy devices were removed in this representation. The input stage of the buffer is the PMOS differential pair PM0, PM1, with NMOS active loads (NM2, NM3). This topology converts a differential input ($IN+, IN-$) into a single-

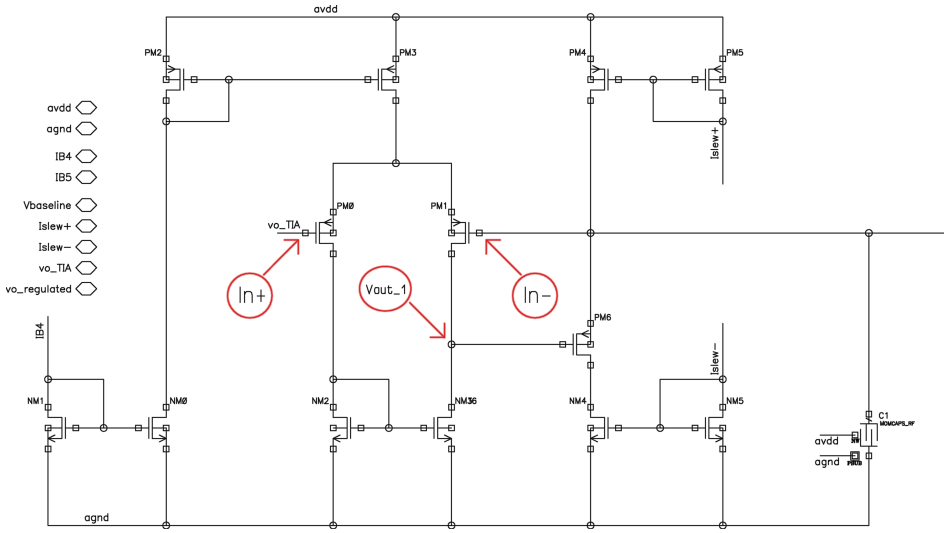

Figure 3.18: Non-linear buffer: Schematic diagram detail of the *BiasRegulator* block

ended output ($Vout\_1$). The output voltage signal (drain of PM1) is then driven into a low impedance node by the source follower stage implemented by PM6. Inherently, the voltage gain of this common-drain output stage is unitary and, since the source of PM6 is connected directly to $IN-$,a unity-gain feedback factor closes the loop of the buffer. The output of the voltage follower buffer is loaded by a capacitance C_1, which is driven by PM6. In the same way, C_1 defines the frequency response of the negative feedback loop, as it creates a pole around $C_1(r_{o_{PM6}}||r_{o_{PM4}}) \approx C_1 r_{o_{PM6}}$. The current that charges/discharges C_1 is imposed by I_{PM6}[8] which is, by its turn, limited by the current-starving transistors PM4 and NM4 [Cobanoglu2007]. The value of the imposed current, controlled by the means explained further

[8] the bulk currents are neglected.

in the text, defines the rate at which the output capacitance C_1 is driven. This rate, or the value of the partial derivative of the voltage in time, is commonly called slew rate (SR) . Neglecting the output resistance of the buffer, and given $i_{C_1}(t) = C_1 \frac{\partial V}{\partial t}$, then the slope of the output when a large signal is applied [Sedra&Smith] at $IN+$ can be approximated by (3.16):

$$SR = \frac{\partial V}{\partial t} = \frac{i_C}{C_1} = \frac{I_{PM6}}{C_1} \tag{3.16}$$

The slew limiting current I_{PM6} can be trimmed by an off-chip resistor, connected between $Islew+$ and $Islew-$. [9] Typical values of $I_{PM6} = 250\ nA$ and $C_1 = 1.4\ pF$ produce $SR = 180 \mu V s^{-1}$.

Higher values of $Rslew$, which define a lower current I_{PM6}, yield lower voltage bounces at the inverting terminal of the differential amplifier (waveform $IN-$ of Fig. 3.21). It is worth to note that, according to (3.16), to lower the value of C_1 (aiming the reduction of the area overhead) necessarily yields the same degrading effect of the filtering function.

If $Rslew$ is not set high enough, then the average current of the transconductor increases correspondingly (waveform Gm_out of Fig. 3.21 shows a larger area for $Rslew = 1\ k\Omega$) and the baseline is depleted. Figure 3.23 evidences this baseline drift of the amplifier for higher SR currents ($Rslew = 1\ k\Omega$) when the front-end is exposed to a 1 MHz event rate. With $Rslew = 1\ M\Omega$, the design copes with a 1 MHz event rate per channel, which complies with the high dead counts rate expected with SiPMs (low energy events due to the high dark current of those photodetectors)[10].

3.4.2 Transconductor

A simplified representation of this sub-block is in Fig 3.19, where the negative input of the differential pair $IN-$ is the output of the non-linear buffer [11], and $IN+$ is the reference baseline voltage. The difference between these two generates a proportional current through PM12, which is fed into the input of the shaper. For the nominal gain of the shaper (ref. table 3.1), figure 3.20 plots the output current of the the transconductor for a baseline voltage swept between 1.0 and 2.0 V. The waveforms on the right refer to transient analysis, whereas the left plot shows the linear variation of the current $Iout$ with Vbl. The large signal behavior can be described as follows. When a higher reference voltage Vbl is applied, the current on the NM10 branch increases and thus the voltage at the drain of NM11 goes up, which in

[9] An optimized solution is proposed in the discussions chapter (page 99).

[10] The typical event rate of high energy events, based on data collected with ClearPEM and ClearPEM-Sonic, is around 2.5 kHz per channel.

[11] also appears as $IN-$ in Figure 3.18, because of the series-shunt configuration with unity gain.

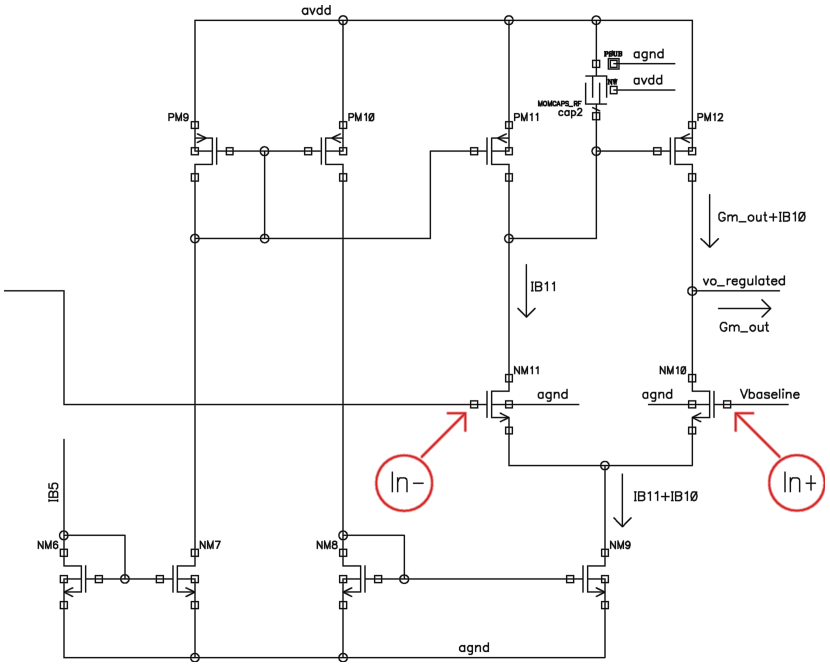

Figure 3.19: Transconductor sub-block: simplified schematic.

turn decreases the current through the output transistor PM12, as its V_{SG} becomes smaller. Figure 3.21 provides hints on the effect of an insufficient slew-rate limitation of the buffer. The solid red line represents the aforementioned unfiltered signal pulse at the output of the buffer $(IN-)$[12], for $Rslew = 1000\ \Omega$. Keeping Vbl constant, the differential pair produces a negative voltage signal at the gate of $PM12$. As a result, the current output suffers a sharp transitory increase, which will affect the DC baseline of the output.

Since PM12 operates as a current source, the noise introduced by the circuit can be minimized by the introduction of the filtering capacitor $cap2$ at the gate of the PMOS and by keeping a low transconductance of the common-source output transistor.[13] More importantly, $cap2$ introduces the dominant low-frequency pole of the transconductor, necessary for the stability of the loop, filtering the single-ended output (drain of NM11) of the differential amplifier. Using $cap2 = 1.4\ pF$, and having the drain-to-source output conductances of the saturated PM11 and NM11 given by g_{dsPM11} and g_{dsNM11}, then the time constant τ_0 is given by equation 3.17:

$$\tau_0 = cap2 \cdot \frac{1}{g_{dsPM11} + g_{dsNM11}} = 1.4p \cdot \frac{1}{420p + 185p} = 2.3\ ms \tag{3.17}$$

[12]The negative inputs **buffer**/$IN-$ and **transconductor**/$IN-$ are the same net.

[13]Note that, if the output of a single-stage amplifier is a current, than the total output rms noise current decreases with lower values of gm [Razavi]

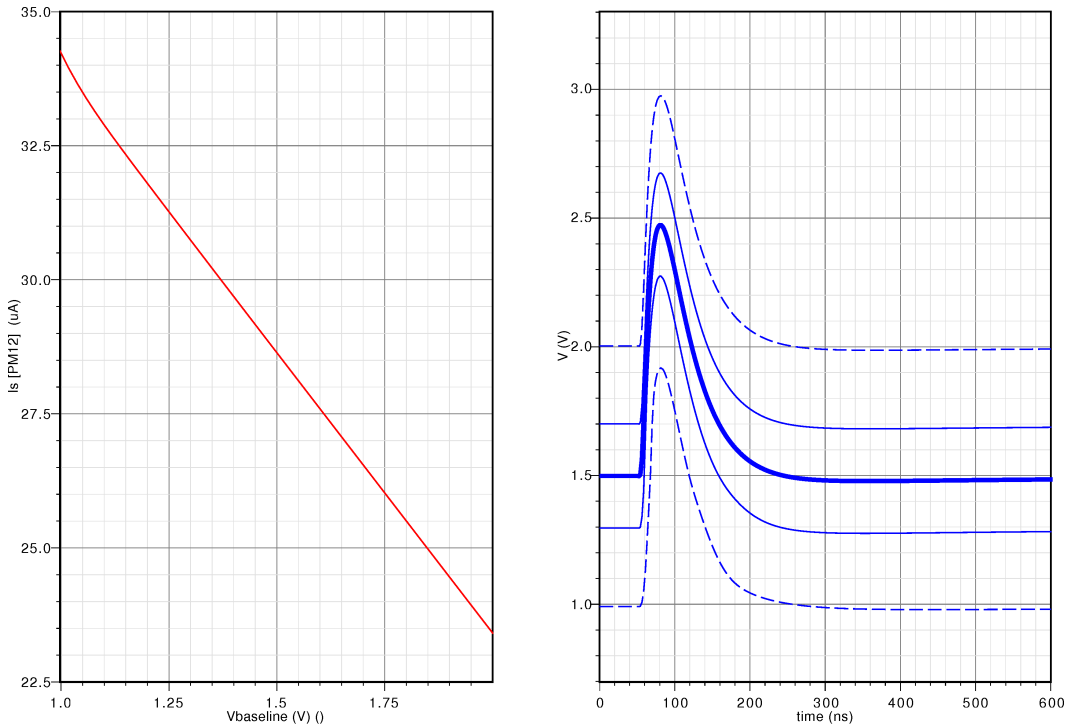

Figure 3.20: Transconductor function $I_{out} = f(Vbl)$: DC sweep (left), and the respective waveform of the shaped output (also the Vo_TIA input for the non-linear buffer).

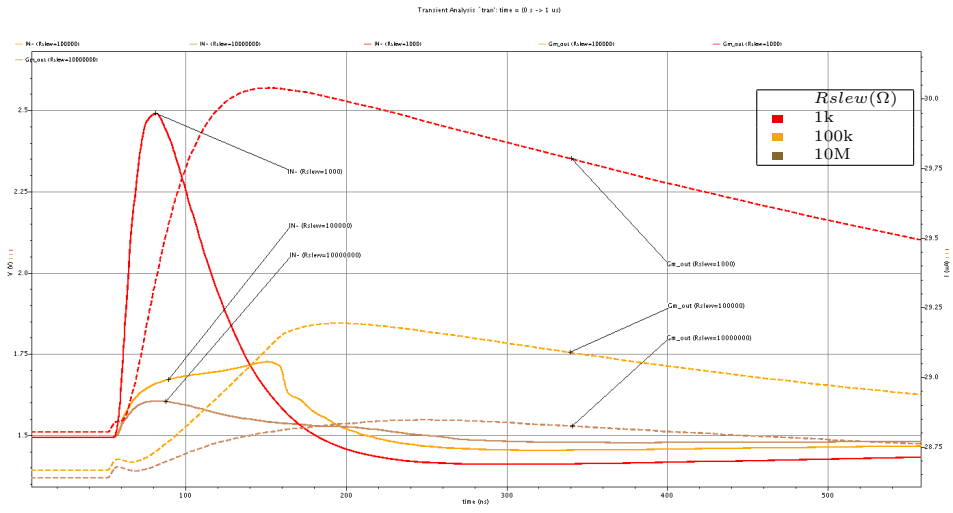

Figure 3.21: Low-pass transconductor I/O: Parametric slew rate, transient analysis, *Gm_out* (dotted lines) and *IN-* (solid lines) plotted.

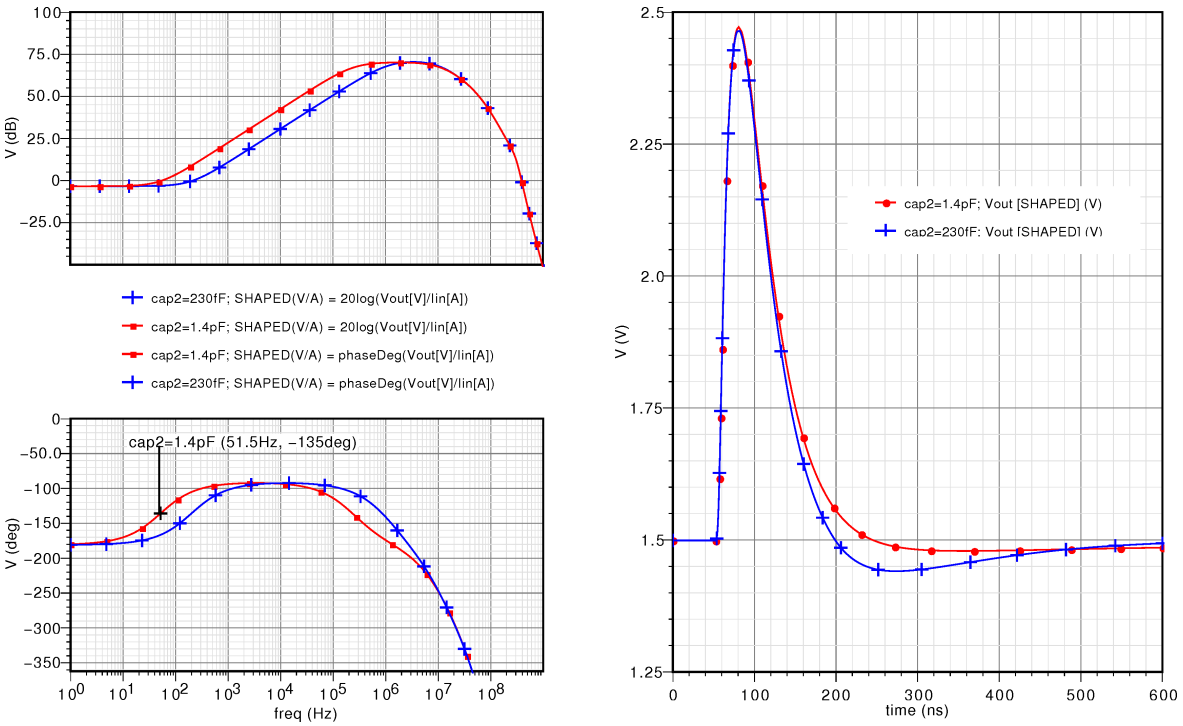

Figure 3.22: Transconductor low-pass filtering. Transient analysis ($C_d = 70\ pF$) (right plane) and frequency sweep on the left plane: $V_{out}(s)/I_{in}(s)$ dB20 (upper) and phase (bottom). Results for 1.4 pF and 230 fF.

This approximation results in a pole located in $p_0 = (2\pi\tau_0)^{-1} = 68\ Hz$. In fact, the total gate capacitance of the voltage-to-current conversion transistor ($C_{gg\ PM12} \approx 150\ fF$) was not taken into account in the above calculations (as it sums to $cap2$, $p_0 = 62\ Hz$). Since p_0 is a pole of the feedback transfer function, then it defines the low-frequency zero z_0 of the *FeedbackTIA+BiasRegulator* closed loop transfer function $T(s)$. Simulation results of $T(s)$, in figure 3.22 (left plane), show $z_0 = 52\ Hz$ (measured at -135 degrees, as the forward function is an inverting transimpedance amplifier.

The small-signal transfer function of the shaped signal path evidences the shaping component at high frequency, defined by the the shaper integration constant, and the high-pass behaviour of the *FeedbackTIA+BiasRegulator* closed loop where the position of the zero is imposed by the low-frequency pole τ_0 of the transconductor. Placing a pole of the *BiasRegulator* in such a low frequency guarantees that the forward *FeedbackTIA* transfer function (at the input signal spectrum of frequencies) is not affected, which is the envisaged characteristic of classical AC coupling, and the motivation to use large values of capacitance when such method is employed. The right plane shows a transient analysis of the shaped output.

When the dominant low-frequency pole of the transconductor is pulled up by decreasing

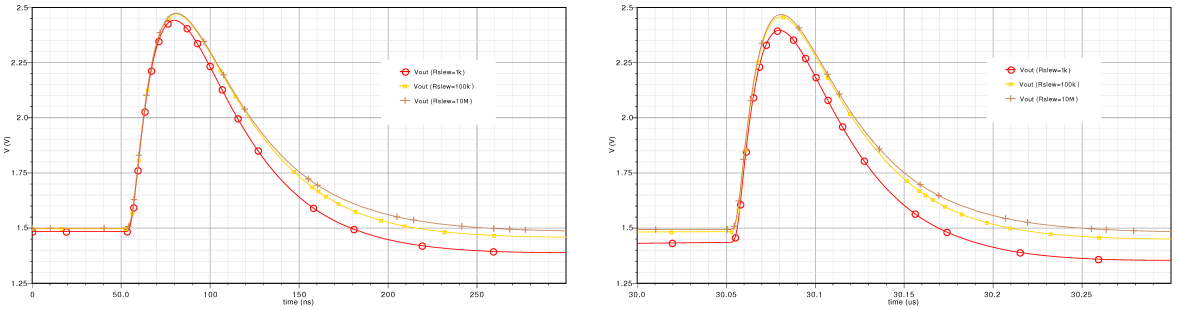

Figure 3.23: Shaper output $Vout$, also *BiasRegulator* input vo_TIA voltage waveform, transient analysis with parametric slew rate. The sub-plots are snapshots at $0 - 0.3\ \mu s$ (left) and $30.0 - 30.3\ \mu s$ (right), when the front-end amplifier is due to a process a 1 MHz event rate. The plot on the right evidences the degradation of the baseline voltage for $Rslew = 1\ k\Omega$.

the value of the filtering capacitance (made six times smaller), the displacement of z_0 pushes the unity gain frequency of the closed loop closer to the cut-off frequency (ω_F) of the low-pass transimpedance function. The transient waveform of the shaped output plotted in the right plane of figure 3.22 evidences the result of moving z_0 to $\approx 250\ Hz$.

In order to avoid that the closed loop fast signals become affected by $T(s)$, its unity gain frequency must be placed at least two decades below ω_F [Corsi2008].

3.4.3 Transistor level: *BiasRegulator*

Figure 3.24 shows the circuit design of the full non-linear low-pass transconductor block. The transistor level implementation the circuit is based, with corrections, on what was proposed by A. Rivetti in [Albuquerque2006]. Modifications were introduced to the prior design (CMOS 0.35 μm), in order to comply with the new technology node.
The dummy transistors, needed for matching purposes, are boxed and labeled.

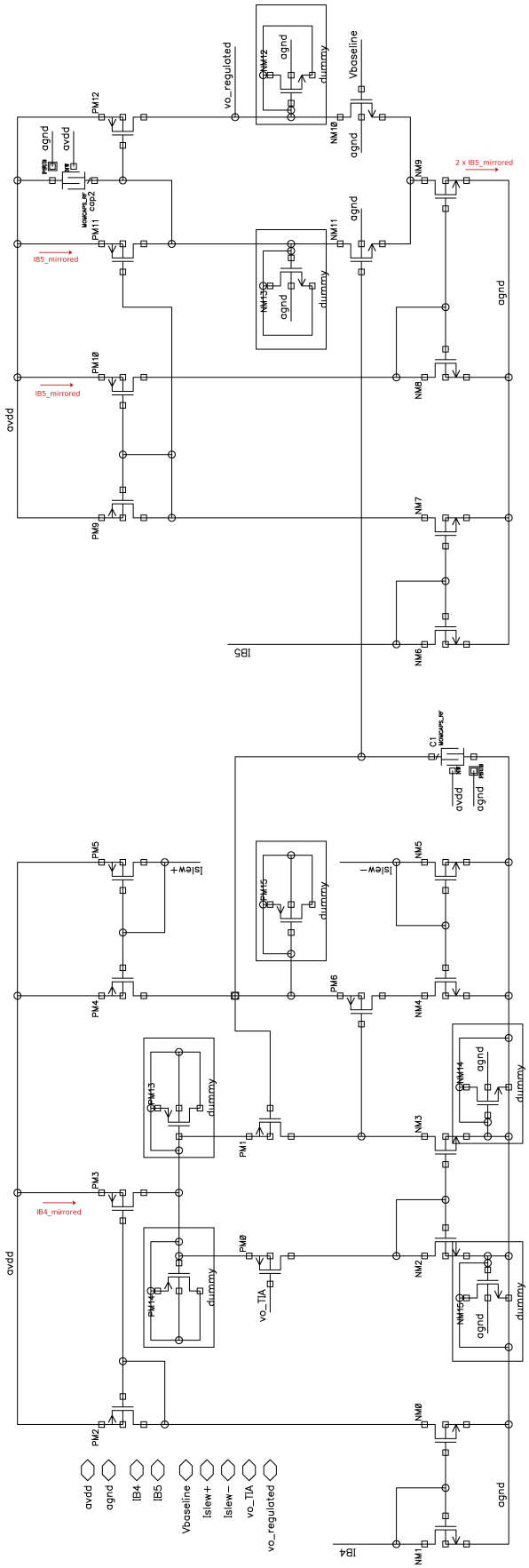

Figure 3.24: Schematic diagram of the *BiasRegulator* block

3.5 Biasing circuitry

3.5.1 Choice of the bandgap topology

As for any analogue design, a bandgap reference with good temperature, process and power-supply variations rejection ratio was studied for implementation. For the specific application of particle detectors, the dependence on temperature is less problematic, given the stringent requirements of such systems in terms of thermal stability. Temperature drifts can cause significant deterioration of the energy resolution [Bugalho2009], as the gain of solid-state photodiodes is temperature dependent. For the Hamamatsu S10-362-11 series, the nominal gain of a device ($M = 2.75 \times 10^5$) drops by a factor of $M = 5 \times 10^3$ for every increase of 1 °C [MPPC]. The amplifier is thus expected to be operating at a relatively constant ambient temperature (around 24 °C), and the fluctuations will only be due to self-heating. Considering that transistor-scale temperature peaks (e.g., caused by chip level power transistors) are negligible within the area of the analogue channel circuitry, it is also possible to neglect the temperature gradient between different voltage/current mirroring points. The effect of statistical process variation is lessened by an attentive layout, whereas corner drifts affect all reference generators in the same way.

The matching of references is also optimized by choosing a current reference, instead of a voltage reference. In this way, the effect of the interconnect resistance along the ground line (common to the mirroring points) is minimized [Razavi]. The "golden" reference is thus distributed in the current domain and mirrored locally in each sub-block. A good matching of bias currents is specially required for the *PreAmplifier* block, as the operation point of the regulated common-gate is greatly affected by opposite drifts of $IB1$ and $IB2$. The bandgap current reference must therefore meet a good power supply rejection ration, and be able to generate currents in the range of the hundreds of nanoampere.

The circuit shown by figure 3.25 [Vittoz1977] is a good choice for generating currents in in the micro-ampere range. Straightforward analysis to the schematic reveals that:

$$V_{GS0} = V_{GS1} + RsI_1 \tag{3.18}$$

considering that both NM0 and NM1 are saturated, where their drain current is defined by (3.19),

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{3.19}$$

then equation (3.20) can be derived:

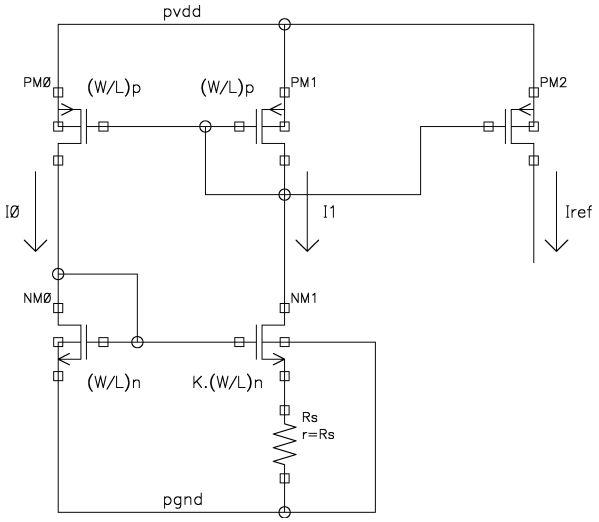

Figure 3.25: Micro-current generator with external biasing resistor.

$$V_{GS} = \sqrt{\frac{2I_D L}{\mu_n C_{ox} W}} + V_{TH} \tag{3.20}$$

and thus, from (3.18) and (3.20),

$$\sqrt{\frac{2I_0 L_0}{\mu_n C_{ox} W_0}} + V_{TH0} = \sqrt{\frac{2I_1 L_1}{\mu_n C_{ox} W_1}} + V_{TH1} + RsI_1 \tag{3.21}$$

If $(W/L)_1 = K(W/L)_0$, (3.21) can be simplified to:

$$\sqrt{\frac{2I_0 L_0}{\mu_n C_{ox} W_0}} + V_{TH0} = \sqrt{\frac{2I_1 L_0}{\mu_n C_{ox} W_0}} \frac{1}{\sqrt{K}} + V_{TH1} + RsI_1 \tag{3.22}$$

If the voltage drop across Rs is indeed very small (making $V_{S0} \approxeq V_{S1}$), the body effect can be neglected and thus $V_{TH0} = V_{TH1}$. Moreover, since the PMOS devices are matched, the current in the branch I_0 is mirrored to I_1. That being assumed, if I_{ref} is extracted with the current mirror PM1 - PM2 (of unitary current gain),

$$\sqrt{\frac{2I_{ref}}{\mu_n C_{ox} (W/L)_0}} - \sqrt{\frac{2I_{ref}}{\mu_n C_{ox} (W/L)_0}} \frac{1}{\sqrt{K}} = RsI_{ref} \tag{3.23}$$

simplifies to:

$$I_{ref}{}^2 = \frac{1}{Rs^2}\frac{2I_{ref}}{\mu_n C_{ox}(W/L)_0}\left(1-\frac{1}{\sqrt{K}}\right)^2 \tag{3.24}$$

which, solving in order to I_{ref}, yields:

$$I_{ref} = \frac{1}{Rs^2}\frac{2}{\mu_n C_{ox}(W/L)_0}\left(1-\frac{1}{\sqrt{K}}\right)^2 \tag{3.25}$$

The results in [Razavi] confirm this synthesis. A self-biased (or bootstrapped) supply independent current reference is therefore achieved, as equation 3.25 evidences that the reference is properly made independent of the supply voltage variations. Dependence on process corners or temperature is though kept.

The off-chip resistor Rs is a good option for a first test chip, as it allows to individually trim each biasing current. In addition, the start-up of the circuit is ensured with such option, since the parasitic capacitances of NM1 will induce bouncing on the internal nodes, hence causing a "false start-up". In fact, the simplification made to obtain equation 3.25 supposes a non-zero reference current on the loop, as both sides of the equation are divided by I_{ref}. Clearly, from Equation 3.24, the loop can be stuck with a zero current in both branches. If the degenerative source resistance is implemented on-chip, a start-up circuit must be added. [Razavi, Maloberti]

The apparent alternative for an on-chip resistor would be the non-salicide high resistive poly, which is made available by the technology with a nominal resistance of 984Ω/□.However, since low currents are required, either the silicon area required becomes prohibitive, or the design must comply with large drifts of the absolute value of Rs. The latter appears with the use of large L/W ratio, necessary to achieve a large resistance, with which the process variability can lead to a maximum of 30% shifts. A better approach is to substitute the resistance by an active load, which not only reduces silicon consumption but also reduces mismatch.

Nevertheless, the need for low currents (down to sub-microamp range) demands for small multiplication factors. Considering the approximation made by equation (3.25), one can

predict that the minimum value for K is always above the unity, as $K = 1$ would yield zero current. The author of [Maloberti] also refers to the condition $(W/L)_1 < (W/L)_2$, since having $(W/L)_1 = (W/L)_2$ would imply that the voltage drop across Rs was zero. Although, the derived expression supposes a negligible body effect, which may not be a reasonable expectation when very small currents are referenced (below $1\mu A$). Actually, a unitary multiplication factor can be used to generate sub-microampere range currents, though leaving the reference more prone to the variability of V_{th} caused by transistor mismatch. Recalling equation (3.22), one depicts that, for $K = 1$, the reference current is a factor of the difference between the threshold voltages of NM0 and NM1. The difficulty to arrive to the full analytical expression that unequivocally defines V_{th} may set a drawback to the attempt of defining $Iref$. The designer may although define a unitary multiplication factor and verify, by simulation, that the NMOS are kept in saturation or sub-threshold region. That was done to generate the reference $IB5$, where a current of 200 nA was needed (refer to section for details). By choosing $K = 1$ and $R5 = 15\ k\Omega$, $V_{th0} = 338.1\ mV$ and $V_{th1} = 335.8\ mV$ (after simulation, where $V_{th} = V_{gs} - V_{dsat}$ [14]).

From these premises, I_{ref} is given by (3.26)

$$I_{ref} = \frac{V_{th0} - V_{th1}}{Rs} = \frac{2.3 \times 10^{-3}}{15 \times 10^{3}} = 153\ nA \tag{3.26}$$

which is a fair approximation to the generated value of 203 nA.

The use of such a small voltage drop across an external resistor may leave the circuit more susceptible to line bounce with digital signaling or charge pulse (important in multi-channel configurations).

Figure 3.26 is useful for a first qualitative approach for such problem. The test set-up takes as example the aforementioned susceptible current generator. Although the same conclusions may be drawn for every generator, as the crosstalk effect is the same, the relative ripple that it causes is higher when the voltage drop across the off-chip resistor is lowered. Considering a maximum readout charge of 40 pC, corresponding to a current pulse with nearly 1 mA peak; if the preamplifier would have a 10 Ω input resistance, then a voltage bounce of 10 mV is produced at the signal input line (recall that the preamplifier collects electrons, thus a negative voltage pulse is expected). Supposing a very bad floor plan design

[14] V_{dsat} is the overdrive voltage; the UMC130 design kit models require an indirect calculation of the effective V_{th}, through the operation point parameter analysis.

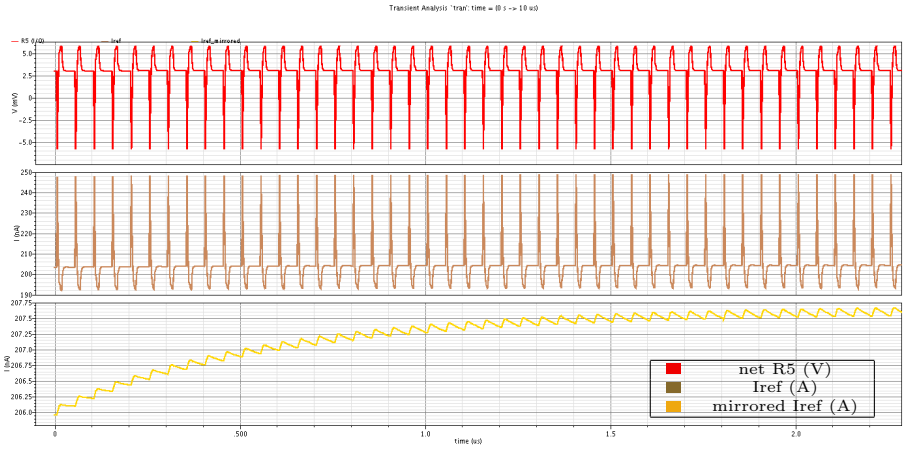

Figure 3.26: Crosstalk effect on current reference circuitry.

that could impose a 100 fF parasitic coupling between the signal input and the $netR5$ (source of NM1); then, I_{ref} would be affected by the change of Vth_{MN1}, due to the increased body effect. Despite that, the low pass filtering of the CM shall lead to a spurious current ripple at the mirroring point well below 0.5% (from the example, $\Delta I = 0.13\%$).

3.5.2 Transistor-level: *Irefgen*

The circuit herein described has been implemented for all the five trimmable bias currents. This is a costly solution, as it requires an additional pin for each reference. Obviously, if a multi-channel test chip is to be produced, the $Irefgen$ block needs not to be replicated. Figure 3.27 shows the schematic diagram and component parameters as implemented. The representation includes the important parameter labels obtained for the operation point at nominal conditions. Correspondingly, the off-chip resistor values set is found in Table 3.2, where the index of Rx indicates the bias current generated IBx. The entry "IBx_out" refers to the current output from the *Irefgen* block, while "IBx_mirrored" stands for the mirrored current in each circuit block. For convenience, Figures 3.9 (*PreAmplifier*), 3.24 (*BiasRegulator*) and 3.15 (*FeedbackTIA*) are labeled (in red) with the pertaining "IBx_mirrored". Where appropriate, the in-block biasing circuits also include the multiplication factors of "IBx_mirrored" for each extra current mirror branch.

For any current source, the noise can be reduced with lower transconductance (achieved both by diminishing I_{ref} and the aspect ratio W/L) of the output transistor and increased output impedance of the mirror [Nero2002]. That is proved by inspection of the total thermal noise generated by a MOSFET. Considering $\overline{I_n{}^2} = 4kT\gamma g_m$ as the current noise generated in

Off-chip resistor	Nominal (Ω)	IBx_out (A)	IBx_mirrored (A)	Parametric simulation
R1	10k	60μ	500μ	yes: "R1_GND"
R2	10k	15μ	$1m$	yes: "R2_GND"
R3	10k	15μ	15μ	no
R4	8k	20μ	40μ	no
R5	15k	$200n$	20μ	no

Table 3.2: Off-chip resistor values and the respective bias current generated.

the channel with a transconductance g_m, being γ a factor relative to technology ($\gamma = 5/2$ for a standard 0.25μm CMOS [Razavi]) and the drain-to-source voltage, then equation 3.27 can be derived for the total output thermal noise voltage generated by a MOSFET:

$$\overline{V_n}^2 = \overline{I_n}^2 {r_o}^2 = 4kT\gamma g_m {r_o}^2 \tag{3.27}$$

Current-mode circuits, and CMs in particular, do generate a significant noise that can ultimately jeopardize the performance of the circuit. Section 5.2 addresses this possibility, and discusses ways to improve the design in order to comply with the noisy blocks.

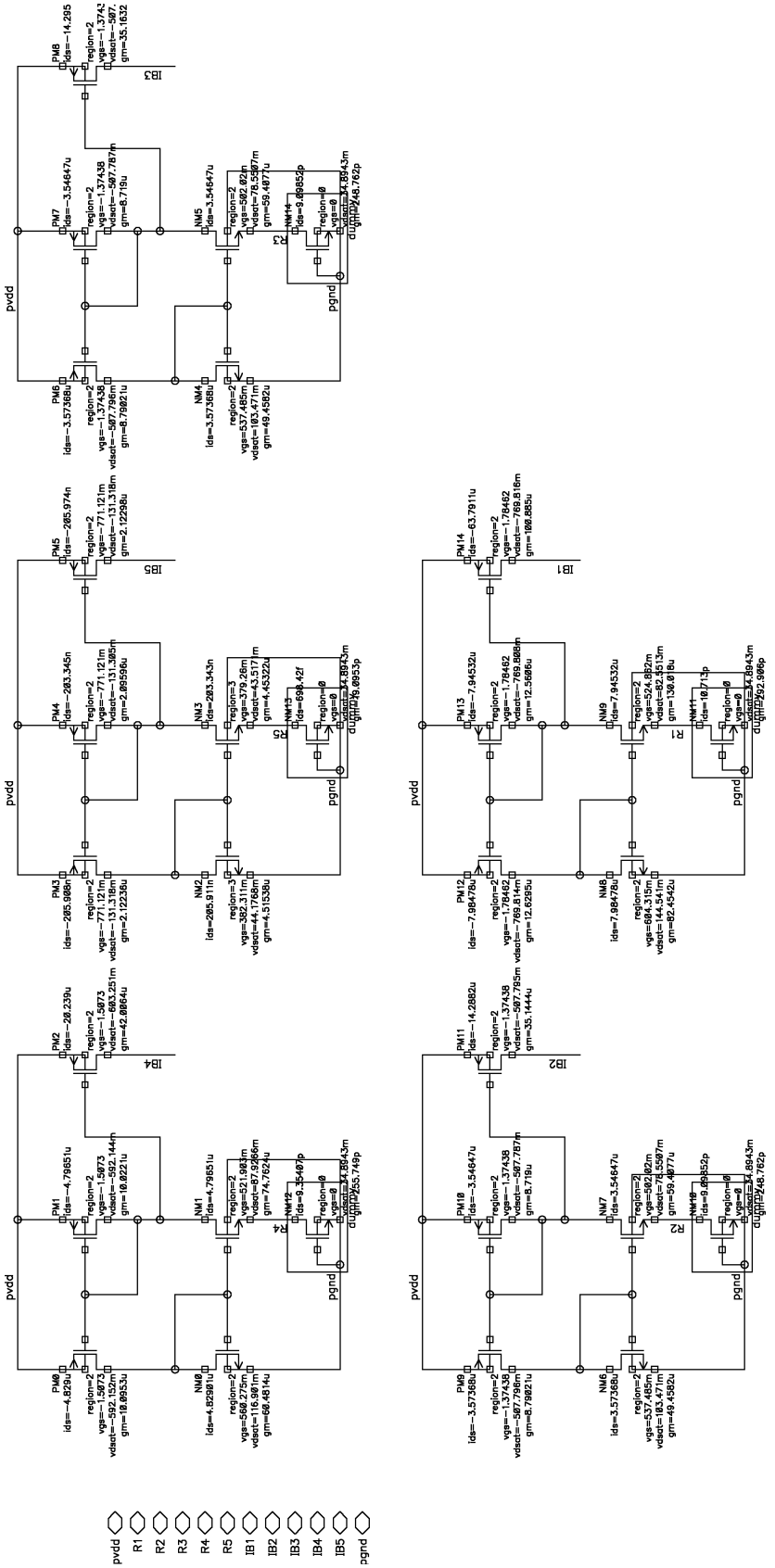

Figure 3.27: Schematic diagram of the *Irefgen* block

Chapter 4

Single-channel test chip

This chapter covers the layout design of a full-channel front-end, suitable to be included in a multi-circuit test chip for submission through a MPW program. Hence, it does not cover the full chip ($1.5 \times 1.5\ mm^2$) floorplanning or pad ring outline. The output of this work is thus a fully checked and post-layout validated *Full_channel* block, depicted in section 4.2, Figures 4.12 and 4.13. A briefing on some essential analogue design guidelines starts the chapter, and the physical layout of each block is unveiled. Section 4.3 thoroughly presents the simulation results obtained after parasitics extraction.

4.1 Design techniques

An important consideration in IC design for PET detectors and experimental physics is the total radiation dose expected for both applications. In HEP experiments, the front-edge electronics will be exposed, in a period of 10 years, to a total dose in the range $[10k..30M]\ rad$ [Anelli1999]. Contrarily, the ASIC of a PEM scanner shall expect a 0.5 $krad$ total dose in 10 years, considering an average of 100 exams per year [Rodrigues2007], and thus a standard deep submicron CMOS technology is appropriated. Advanced technology nodes are, in this regard, advantageous, as smaller gate oxide thickness improves radiation tolerance. The layout of the proposed front-end did not make use of radiation hardness design techniques, but efficient measures were taken in order to tackle transistor mismatch due to process gradients and variation.

The first observed rule to mitigate the undesired effect of process gradients is to dispose the transistors along with a well defined axis of symmetry. Common wafer lithography processing tilts the substrate (or the beam), usually by $7 - 9^\circ$ [Razavi], to prevent channeling of dopant ions. This channeling occurs when the wafer z-axis and the beam are perfectly aligned, and leads to a less predictable doping concentration. Although it mitigates this effect, the

tilting procedure creates shadowed areas that impact the matching of the transistors, due to asymmetries between sources and drains. Despite seemingly subtle, this effect may degrade performance or even lead to chip failure, thus it is highly advisable to keep all transistors disposed with the same orientation.

The interconnections observe some basic rules for coherence and physical robustness. The DC current paths are in accordance with the electromigration rules suggested by the foundry rule set [UMC130]. Given that the bias currents are programmable, the connections (metal width and number of vias per layer permutation) comply with the maximum current ratings. It is assumed that the die temperature is kept under 100 °C.

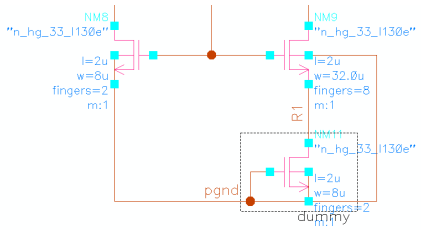

Figure 4.1: Dummy insertion: (schematic) detail of the *Irefgen* block

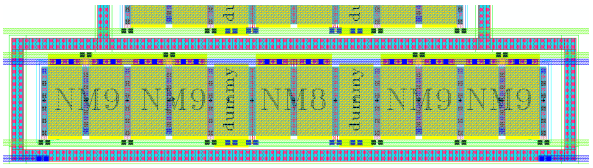

Figure 4.2: Dummy insertion: (layout) detail of the *Irefgen* block

The outer elements have a different boundary condition than those in the middle of the array, e.g. the mechanical stress of the adjacent structures. Above all, the inclusion of dummy gates prevents the over-etching of active elements, since the polysilicon etch is not uniform, and other defects caused by non-homogeneous diffusion. Though the effect is lightened if the number of transistor elements is high (see notes below on digitization), is is always advisable to keep the same conditions by inserting dummy elements at the head and tail. However, special care must be taken if the parasitic capacitance of such elements needs to be accounted. Validation simulations were run whenever the inclusion of dummy devices was not thought at the time of the schematic design (such as in the case illustrated by Fig. 4.1). The transistor

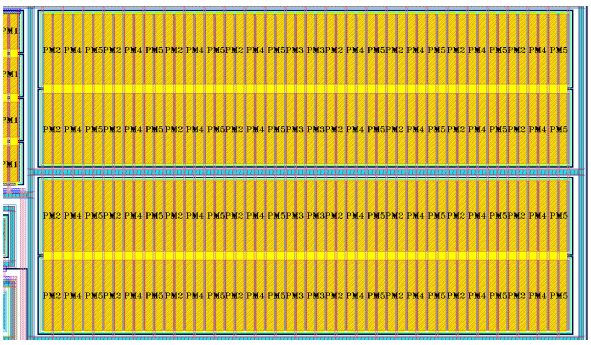

Figure 4.3: Inter-digitization: (layout) detail of the *Preamplifier* block

dimensions were defined such that the total number of fingers allow the inter-digitization of devices (Fig. 4.3). Inter-digitized structures reduce mismatch due to horizontal gradients. In the case that the inter-fingered transistors do not share a common node (source or drain), the insertion of dummy fingers in between is, albeit silicon costly, a valid solution. However, circuits that are more prone to fail due to process biases may need to be "shielded" against vertical or diagonal gradients.

With that in mind, appropriate common-centroid layout techniques were used in the design of the baseline holder differential pairs. Spatially dependent mismatches can be strongly mitigated with patterning the sections of sensitive devices into a symmetric disposition, such that the centroid of such devices is made coincident with its axis of symmetry. Figures 4.5 and 4.7 show different strategies for implementation.

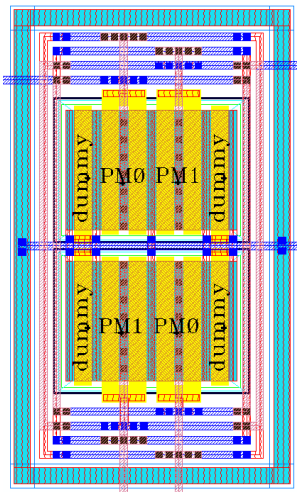

Figure 4.4: Common-centroid, option A: (layout) detail of the *BiasRegulator* block

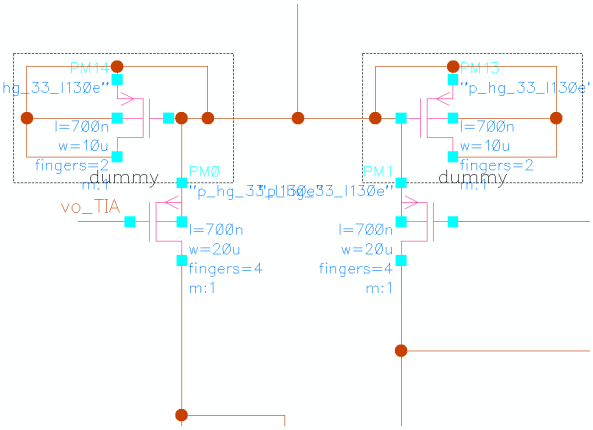

Figure 4.5: Common-centroid, option A: (schematic) detail of the *BiasRegulator* block

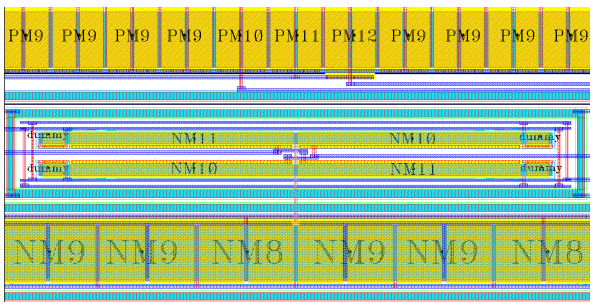

Figure 4.6: Common-centroid, option B: (layout) detail of the *BiasRegulator* block

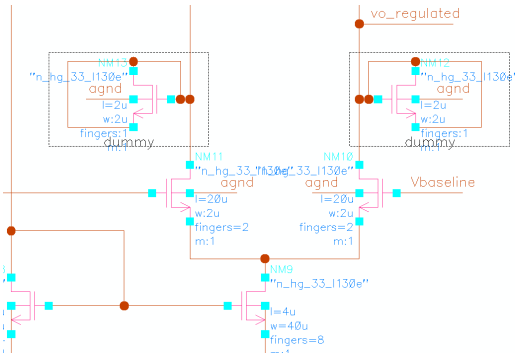

Figure 4.7: Common-centroid, option B: (schematic) detail of the *BiasRegulator* block

4.2 Full-channel front-end layout

The full-custom layout of the front-end was carried out with Cadence ®Virtuoso 5.10.41. All references to the layout area are approximated with the *ceil()* function to the micrometer. The color map is inverted, regarding the display resource layer of the technology.

Pre-amplification Stage Layout

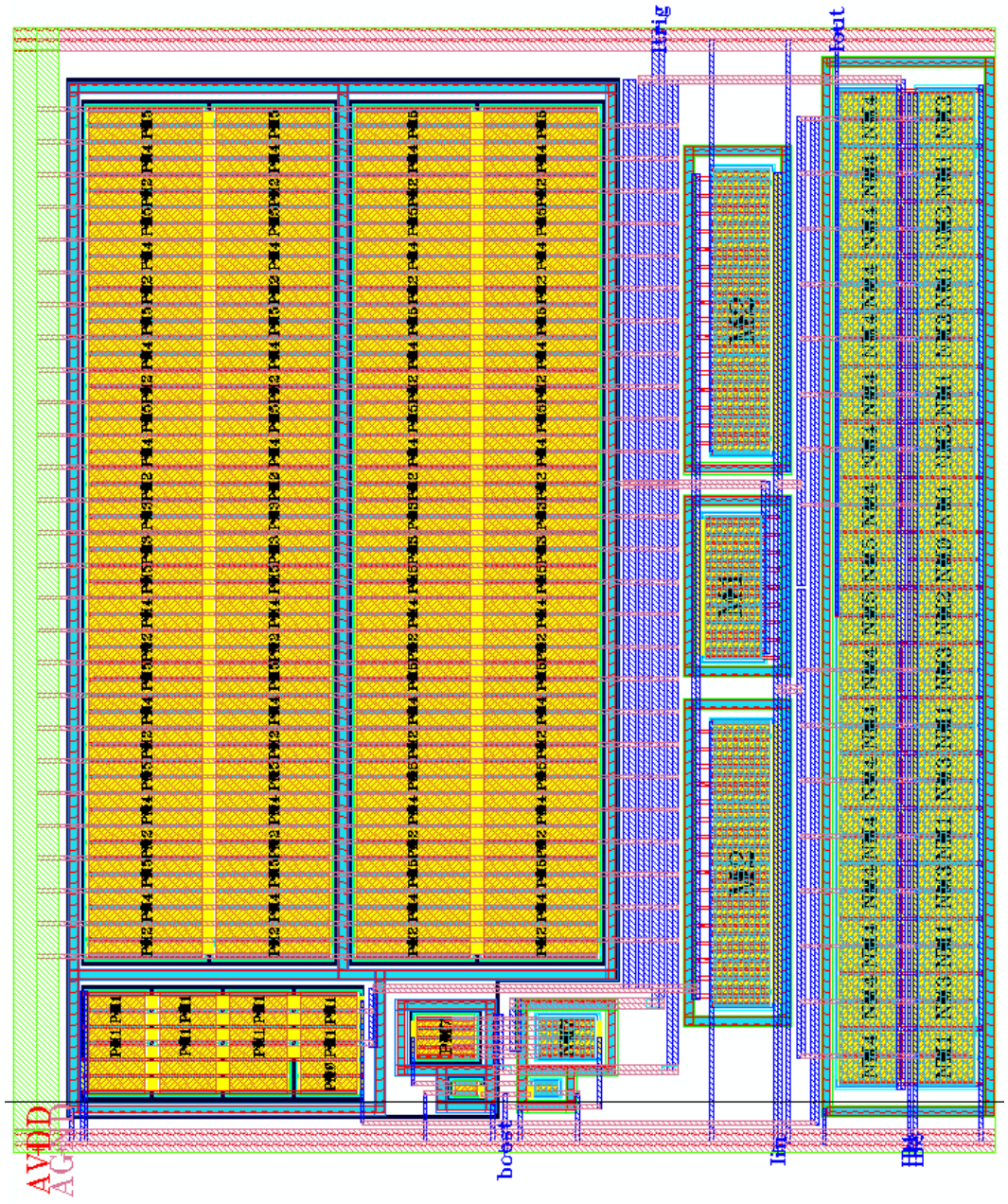

Figure 4.8: Layout ($100 \times 87 \mu m^2$) of the *PreAmplifier* block

Transimpedance Stage Layout

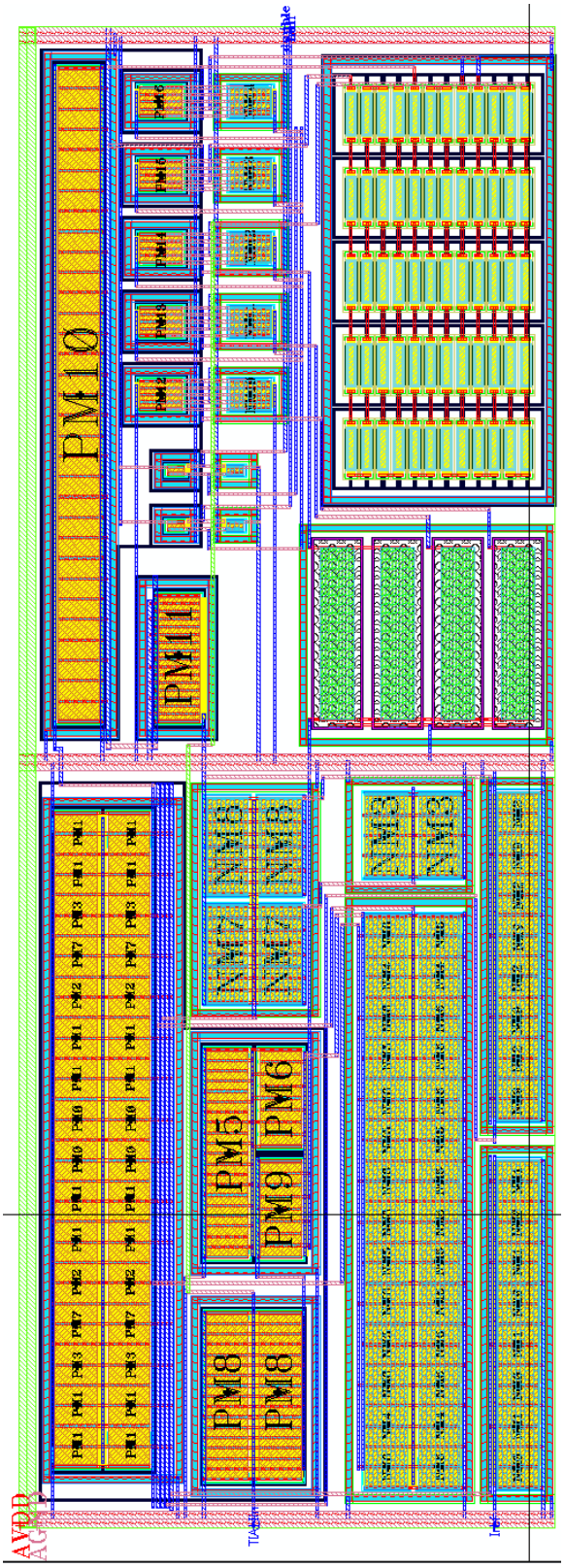

Figure 4.9: Layout ($180 \times 64 \mu m^2$) of the *FeedbackTIA* block

Baseline Holder Layout

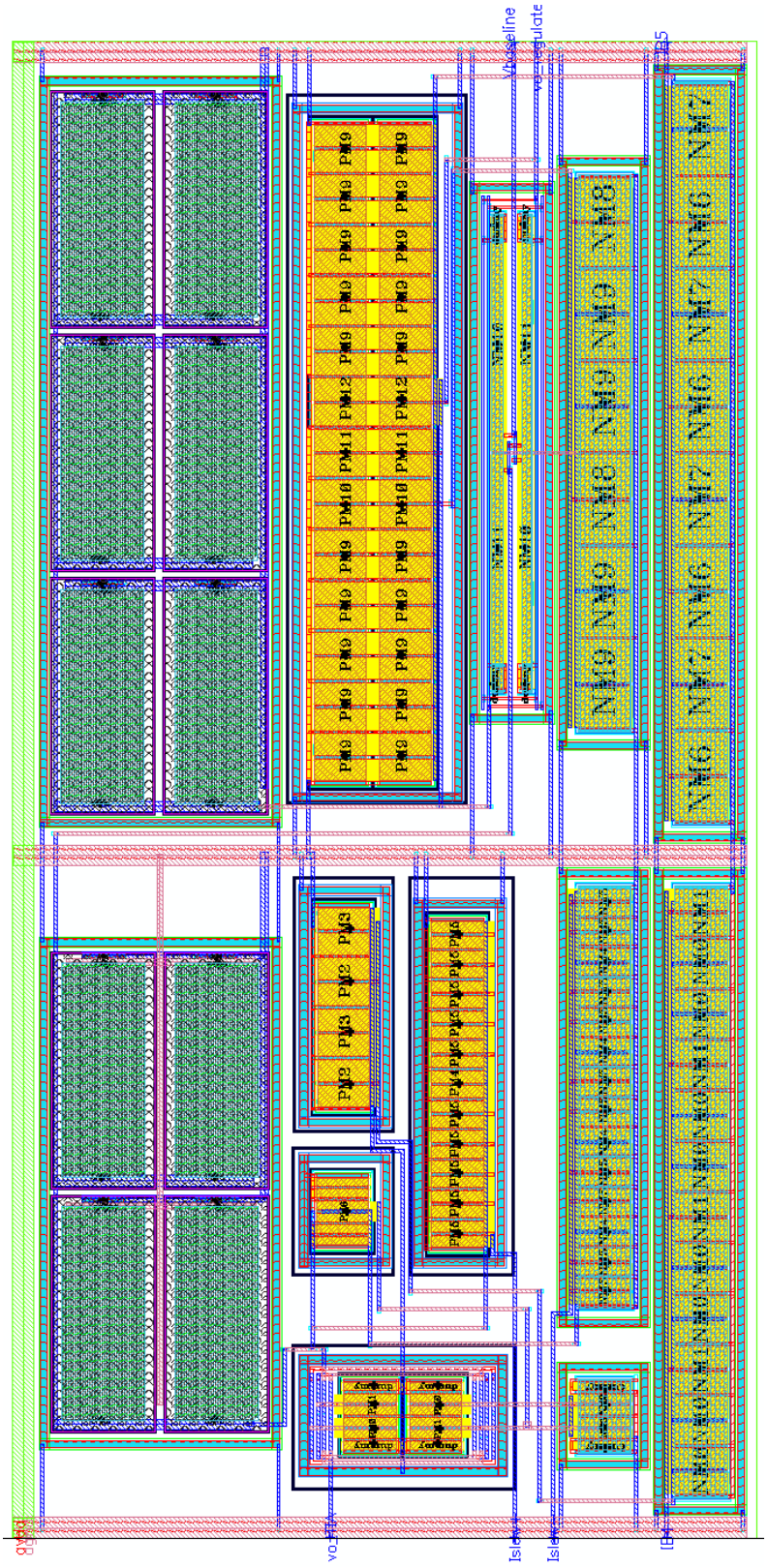

Figure 4.10: Layout ($144 \times 70 \mu m^2$) of the *BiasRegulator* block

Reference Generator Layout

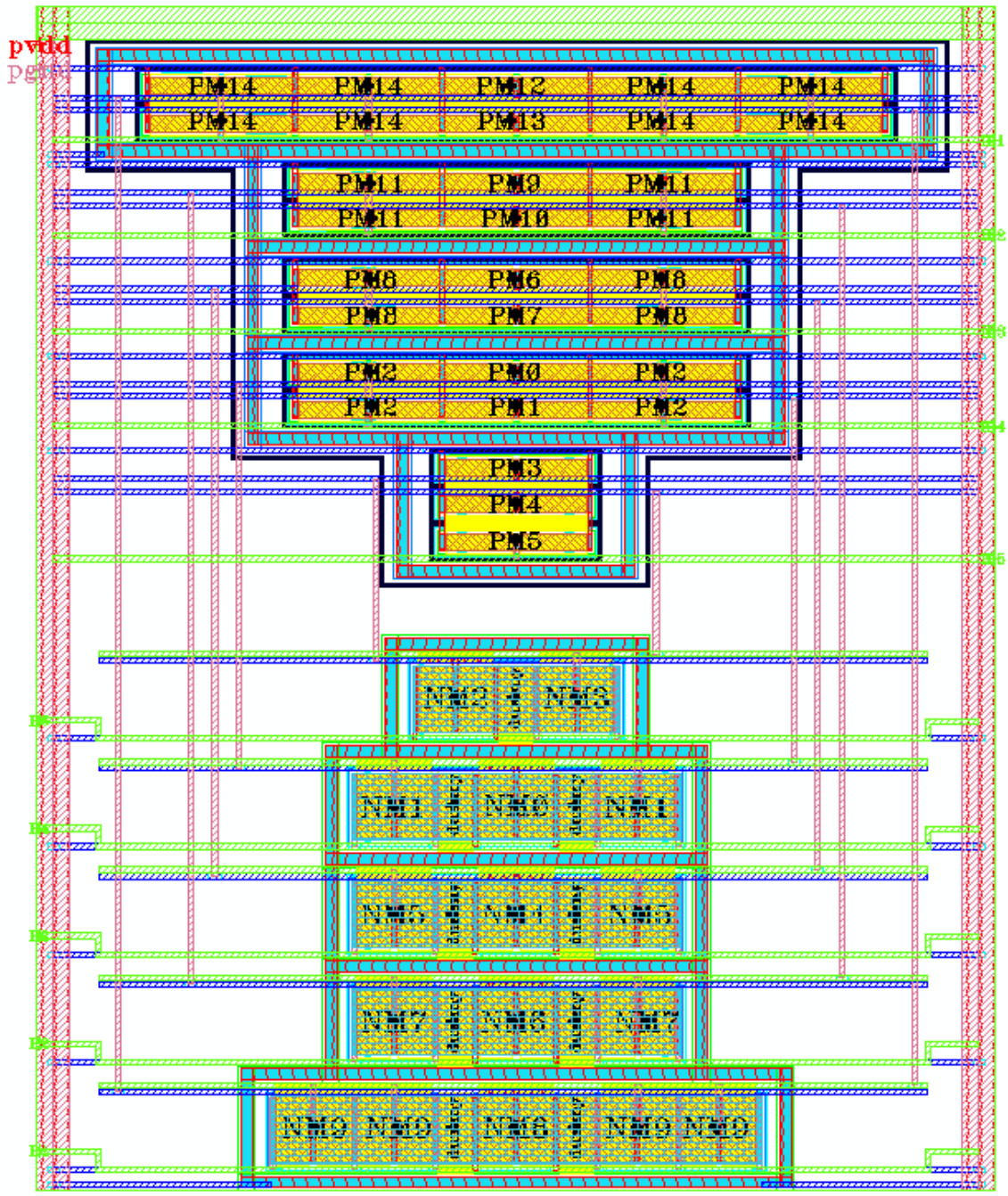

Figure 4.11: Layout ($58 \times 72 \mu m^2$) of the *Irefgen* block

Full Layout of the single-channel block

The full channel dimensions are $493 \times 87\ \mu m^2$. Figure 4.12 shows the top hierarchy of a single-channel design. Such disposition will allow to abut vertically the amplifiers in a multi-channel project. In such design, the removal of *Irefgen* block and the consequent routing of the current-mode references will be the major changes.

Four metal layers are used for (orthogonal only) routing being that, as a general rule, the pairs MET1/MET3 and MET2/MET4 were only (very few exceptions were made) vertically and horizontally disposed, respectively. This simple rule greatly enhances the layout legibility and eases its verification. Furthermore, the LVS procedure becomes less time consuming, as the number of incorrect nets due to faulty short-circuits is significantly reduced. In any case were the routing lines disposed above active devices. Moreover, a minimum of two contact per via was used, such that redundancy is guaranteed.

The top-hierarchy power routing is done horizontally on MET2/MET4 (*avdd/agnd*, in the order given). Likewise, the vertical routing for each circuit block is done on MET1/MET3 (*avdd/agnd*). Consequently, the closeness of the *avdd* power plane to the substrate increases the power supply decoupling capacitance, which is obviously a desired characteristic.

The fifth metal layer MET5 is used to build the 1 pF MOMCAPS capacitors of the *BiasRegulator*. These devices are also used in the *FeedbackTIA* block, but only with 4 metals.

Metal layers 6 to 8 are, therefore, left free for upper-level routing (where MET7 and MET8 are thick layers). In addition, no post-processing is required since the design makes no use of MIMCAPS option.

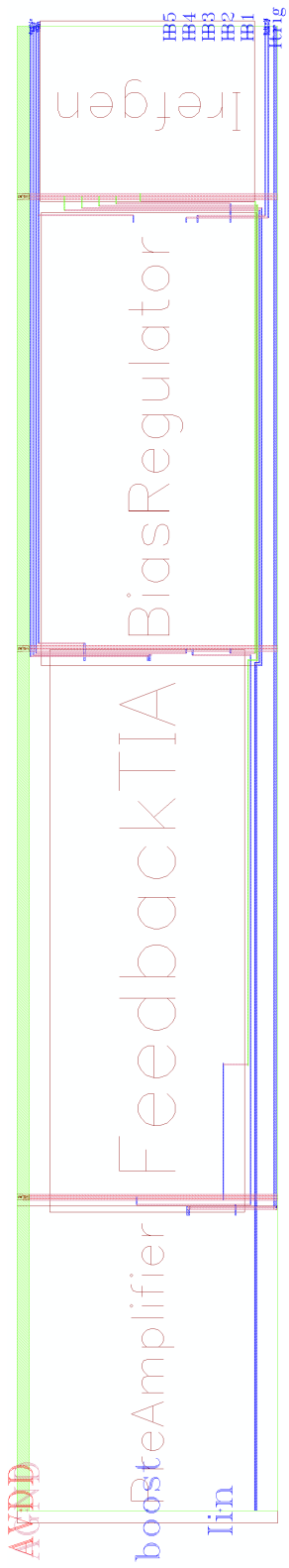

Figure 4.12: Layout top instance view of the *Full_channel* block (top hierarchy)

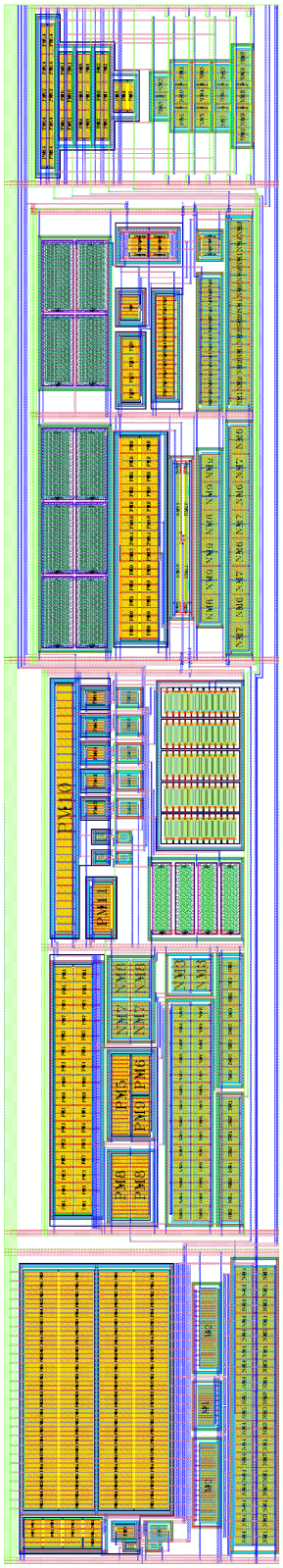

Figure 4.13: Layout ($493 \times 87 \mu m^2$) of the *Full_channel* block (top hierarchy)

4.3 Post-Layout validation

All the simulations (pre and post-layout) were run with Virtuoso® Spectre Simulator. While Virtuoso® Analog Design Environment (ADE) was used for the first schematic-level studies, dedicated OCEAN scripts were written for final data preparation, which can be found in Appendix (A.1). Besides transient and AC plots, the script writes an output file with the relevant simulation data and warning messages (a sample can also be found in Appendix A.1) and stores the operation point data in the design directory.

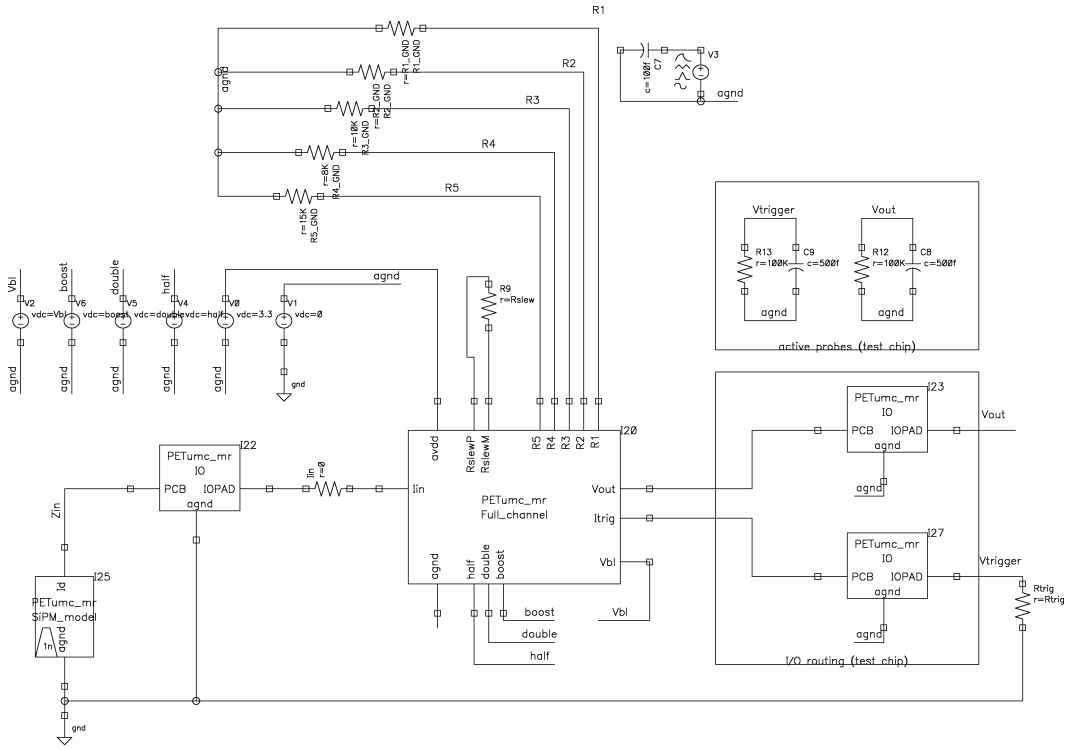

Figure 4.14: Testbench for results data preparation.

The validation testbench is shown in Figure 4.14. When mentioned, the results refer to simulations using a netlist that includes a model of the chip I/O parasitics, depicted by Figure 4.15. The parasitic elements associated with "Package" refer to a standard quad flat plastic packaging option, and includes inductive and resistive effects due to the routing redistribution layer and pin, as well as the capacitive coupling to substrate. The label "Bonding" applies to the RL parasitics of the gold wire bonding and the capacitance of the pad itself, which includes the ESD protection diode junction capacitance to the substrate. The model assumes that *agnd* is electrically anchored to the substrate. In order to decrease the transient simulation time, the inclusion of I/O parasitics was restricted to the signal path. To load the signal outputs with these parasitics is only meaningful for predicting the test chip characterization

results. Naturally, the performance of the amplifier can not be estimated with the RLC circuit loading the outputs, as they are not to be routed outside the chip in a mixed-signal design. Instead, they will be fed to a discriminator/TDC channel or into banks of analogue memories, dependent on the signal processing techniques used.

At this point, however, an internal voltage signal $Vtrigger[FAST]$ is extracted (and thus amplified) with a resistor $Rtrig = 2\ k\Omega$ loading the output current $Itrig$. From that fast voltage output, one can estimate the value of σ_t according to equation 2.1, measuring both the derivative of the signal in the first nanosecond and the total output rms noise voltage probed in $Vtrigger[FAST]$. Of course, this is a rough approximation and is not usable to generate absolute values for σ_t, since a pole τ_{trig} is introduced by $Rtrig$ and the total parasitic capacitance of the node. The current mirror PMOS devices of the *PreAmplifier* that generate the current output $Itrig$ are very wide and thus have a very large total gate capacitance. Supposing $C_{gs} = 2\ pF$ for those devices, then a pole around 40 MHz is created by the time constant $\tau_{trig} = 4\ ns$. Therefore, the information on $Vtrigger[FAST]$ is only useful to assess the sense of variation of σ_t for circuit optimization.

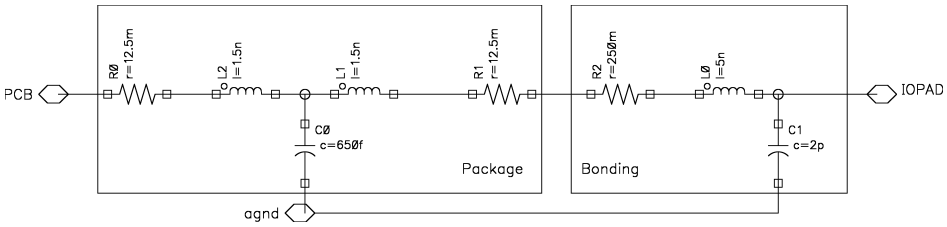

Figure 4.15: Chip I/O parasitics model

The DRC and LVS are performed with CALIBRE. The same tool is also used to extract parasitic elements. Its output is a set of 3 files:

- *cellname*.pex.netlist
- *cellname*.pex.netlist.pex
- *cellname*.pex.netlist.*CELLNAME*.pxi

In order to generate post-layout extraction results, a pre-generated netlist is used and each "schematic view" sub-circuit is substituted by the corresponding "extracted view" definition. The means to do that is to simply:

1. copy the above three files into the netlist directory; Then, for each block:
2. remove the netlist block of the sub-circuit;
3. include *cellname*.pex.netlist, which is done, intuitively enough, by typing (example for the *Irefgen* block): **include "Irefgen.pex.netlist"** directly in the netlist file.

Note that the CALIBRE tool does not follow the same order for the header I/O definition. Hence, for each block, the "*cellname*.pex.netlist" file may need to be corrected according to the header in the original netlist file. A malfunctioning circuit will serve as indicator that this procedure was not properly followed, since the simulator will assume a wrong I/O assignment.

For simplicity, since the simulator expects an input file named "∽/**netlist**", it is a good practice to have separate paths corresponding to "schematic view" and "extracted view". An example is shown below, taken directly from the OCEAN script used:
netlistfile=design("∽/Sim/Testbench_full_EXTRACTED/spectre/schematic/netlist/netlist")
netlistfile=design("∽/Sim/Testbench_full/spectre/schematic/netlist/netlist")

The respective header of each file can be modified to include the below information:
Layout extraction ?: // CALIBRE EXTRACTED NETLIST R+C+CC
Layout extraction ?: // SCHEMATIC NETLIST: NO PARASITICS

This information is written to the results file (see Appendix, section A.1 for details), thus keeping an easy track on which netlist generates which results.

4.3.1 Nominal Operation

The performance of the amplifier in terms of amplitude (hence charge) measurements takes into account the realistic input stimulus (including SiPM rise time and LYSO decay) that has been proposed. Such test assesses the shaping characteristics of the output signal and measures the ratio between the peak output voltage and the total *rms* output noise voltage on the same node. For the minimum input signal of interest, this ratio must be higher than 15-20. Alternatively, the energy information can be extracted by measuring the leading and ending trails of the shaped output, so that ToT window can be correlated with the pulse amplitude.

The timing measurements requirements include gain and noise specifications, from which the additional time jitter introduced by the circuit is calculated. Testing the amplifier to extract these parameters imply the use of a delta function as input. Otherwise, the test would be addressing not only the pulse shape and noise characteristics of the amplifier, but also the sum of jitter due to the SiPM, photoelectron statistics and the characteristics of the scintillation (rise and decay time). The contribution of the amplifier noise to the FWHM

time resolution is required to be below 25 ps.

The nominal terminal capacitance is set to $C_d[TYP] = 70\ pF$. This value reflects the choice of a photodetector chip with $1.4 \times 1.4\ mm^2$ active area, which characteristics could be extrapolated from the information provided by [MPPC-11] and [MPPC-33]. Such an option, which has not yet been made available by the manufacturer, would optimize the optical interface matching, considering the physical characteristics of the LYSO:Ce scintillation crystals used, which cross section is $2 \times 2\ mm^2$. The baseline of the output is set to $V_{bl} = 1.5\ V$, and table 3.2 indicates the nominal values for the off-chip resistors; $Rslew = 1\ M\Omega$. The input stimulus is an exponential pulse with damping factors $\tau_{rise} = 1\ ns, \tau_{fall} = 40\ ns$, with a peak current of I_{in} and loaded by a capacitor C_d.

These conditions provide a realistic model of the input signal, from which the circuit transfer function and output characteristics can be validated. Instead, when the simulation aims to have an insight of the electronics noise contribution for the time resolution, a Dirac pulse with a finite duration 50 ps is used as input. That condition is suitable to extract valid benchmarks that can be used as points of reference for comparison of the time resolution performance of the circuit.

Table 4.1 outlines the total rms output noise voltage probed at each output, as a function of the total input capacitance. For a RGC stage, its value is roughly proportional[1] to the

	$V_{no\ rms}\ (mV)$	
$C_{tot}\ (pF)$	*Vtrigger*	*Vshaped*
35	1.57	2.99
70	2.28	3.07
150	3.88	3.43
320	6.62	4.72

Table 4.1: Total rms output noise voltage vs. device capacitance. $V_{no\ rms}$, or σ_v, is the square root of the noise spectral density integral defined in the range $[10 - 10G]\ Hz$; results are from post-silicon netlists for nominal values of bias current IBx.

value of the device terminal capacitance, thus the value of $V_{no\ rms}$ probed at *Vtrigger* grows accordingly. From that illation, we can predict a severe degradation of the FWHM timing resolution (results will be shown further in the text, in Table 4.3) with high values of C_{tot}, for a fast trigger output. Contrariwise, and despite the contribution of additional noise

[1] It is not a linear function, since the transfer function of the input referred noise is the same as that of the signal and, hence, has the dominant pole dependent on the value of C_{tot}. The general closed form equation was derived in [Medeiros2009].

sources, the $V_{no\ rms}$ at the *Vshaped* node is kept within reasonable values for higher input capacitances, since the band-pass transfer function poles of the *FeedbackTIA+BiasRegulator* no longer include C_{tot}.

Figure 4.16 plots both fast and shaped outputs, revealing the delay introduced by the physical layout parasitic capacitances on the transient response. These simulation results do not include the I/O pad model, in the attempt to isolate the effect of the layout parasitic elements. The transient response for a discrete 5 pC charge pulse at the input defines the

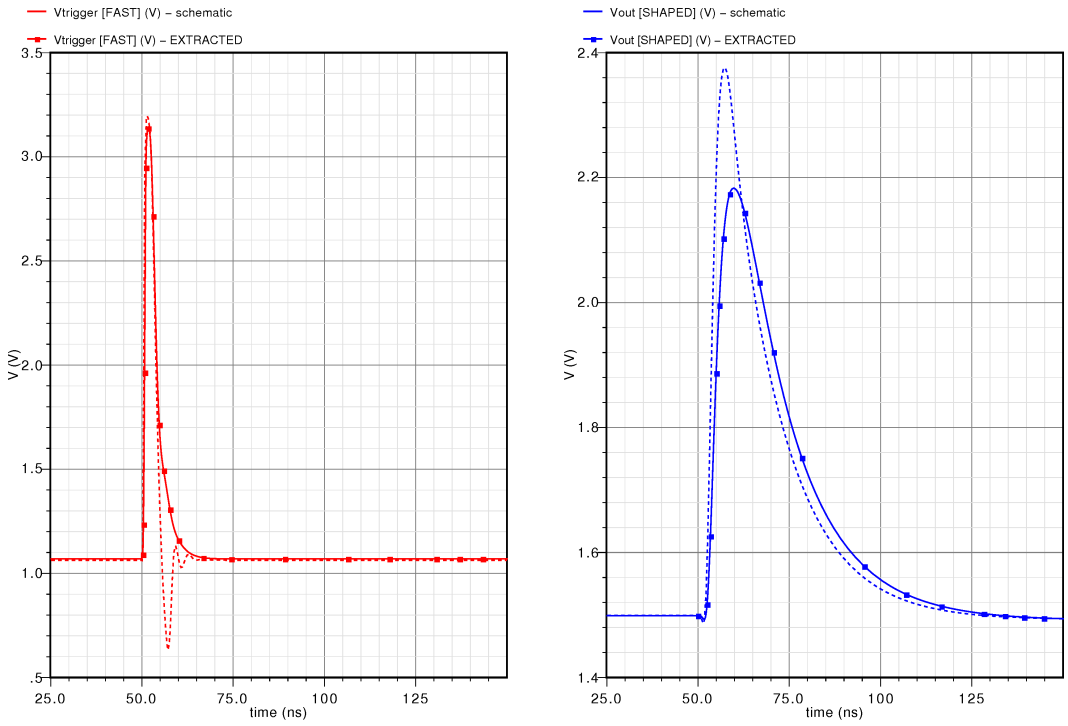

Figure 4.16: Transient waveforms of shaped (right) and trigger (left) signals for schematic level (dashed lines "schematic") and post-layout (solid lines "EXTRACTED") simulations Dirac pulse stimulus).

peaking time and gain of the signal paths. The results evidence a drop of nearly 20% on the gain of the shaper path (decreasing from 176 to 136 mV/fC). Moreover, the peaking time rises accordingly to table 4.2.

	Vtrigger		*Vshaped*	
Sim. environment	G_0 (mV/fC)	Peaking Time (ns)	G_0 (mV/fC)	Peaking Time (ns)
schematic	0.4	1.5	0.18	7.5
$post-layout$	0.4	1.8	0.14	10

Table 4.2: Gain and peaking time degradation after silicon layout, for a Dirac pulse input.

While the effect of the net parasitics results in an improved stability of the input stage

regulation loop, also implicit in the waveform of *Vtrigger*, the current-mode path of the fast signal makes it less susceptible to additional capacitive elements.

More worrying, the dramatic increase of the resistive input impedance shown by the data of figure 4.17 (*extracted*) suggests that the open-loop gain of the RGC feedback has been made smaller. The effect of AC peaking becomes more pronounced when the input path includes the RLC model of the package/bonding (label $IOPAD$), and the input impedance characteristic can thus be expected to be measured $[Z_{in\ DC}, Z_{in\ peak}] = [5.6,\ 16]\ \Omega$.

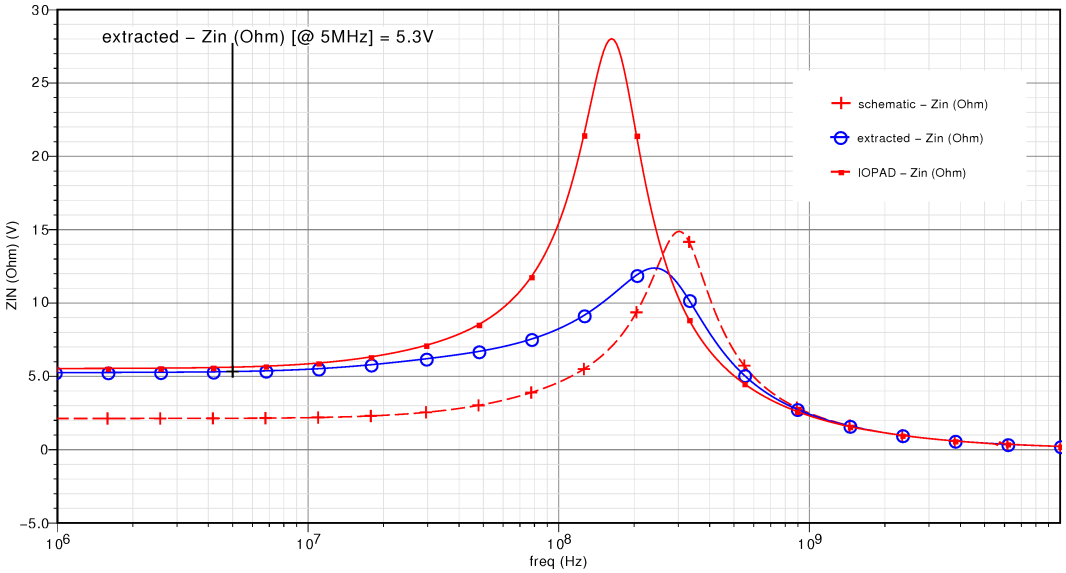

Figure 4.17: Input impedance characteristic for schematic level [*schematic*] and post-layout [*extracted*] (includes effect of I/O routing [$IOPAD$]) simulations.

Non-negligible resistive components on the signal input path have been identified, the dominant being depicted by figure 4.18. The resistivity of the metal path sums up to the DC input impedance predicted by equation 3.10, while the multi-fingering and multiple via (and multiple contacts) option of the subsequent route down to the source of the input transistor was seen as enough to prevent further increment of Z_{in}.

Figure 4.19 illustrates the effect of the chip I/O RLC filter (added only to the signal input and output ports). The non-idealities caused by the inclusion of the package/bonding model are not discussed in detail, but may provide hints for a straightforward analysis of unexpected results during the test chip. For that reason, this insight is only meaningful if a more realistic input signal model is used as stimulus.

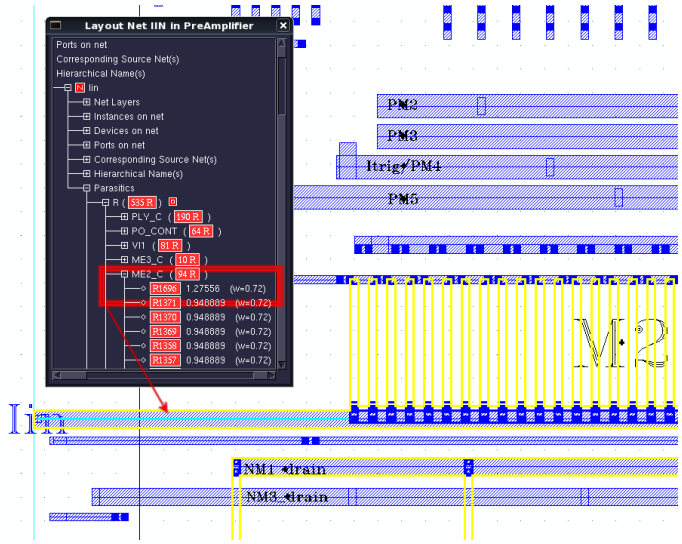

Figure 4.18: Signal Input path parasitic resistance: the routing of the input signal in MET2 affects the signal with $\approx 1.3\ \Omega$.

Timing measurement requirements

The gain and noise parameters are extracted by studying the amplifier response to a Dirac pulse stimulus. A practical approach is to use an *ipulse* with rise, hold and fall times of 50 ps. Actually, any pulse which width at half maximum height is much smaller than a tenth of the internal time constants of the circuit, can be considered to approach a delta function.

Still, the pulse must have a known charge, being that a the worst performance conditions of the circuit are due to feeble inputs. We consider a $1.4 \times 1.4\ mm^2$ active area device with a $50 \times 50\ \mu m$ pixel size, which accounts for an approximated 70 pF terminal capacitance. Bearing in mind that the weakest interaction is a minimum DoI (25%) of a 50 keV photon, then the input charge is 4.9 pC, which corresponds to a total of 42 photoelectrons hitting the SiPM. An *ipulse* with the aforementioned parameters has a current pulse height of I_D, and the total charge is the integral in time of the current: $Q = I_D(50p) + 2\frac{(I_D)(50p)}{2} = I_D(100p) = 5\ pC$, for $I_D = 50\ mA$. Affected by a parallel capacitance of $C_d = 70\ pF$, the filtered pulse keeps a 1 ns FWHM, which is still regarded as a delta pulse for this purpose. Evidently, even if C_d is increased, the pulse height lowers but the charge is the same. The above figure 4.16 plots the transient response of the amplifier to the input Dirac pulse.

If the time stamp is derived from $Vtrigger[FAST]$, then the jitter introduced by the amplifier is calculated as follows. From the amplitude of the output signal, the gain is evaluated:

$$G(mv/fC) = \frac{\Delta V_{trigger}}{Q_{in}} = \frac{2}{5}(V/pC) = 0.4(mV/fC) \tag{4.1}$$

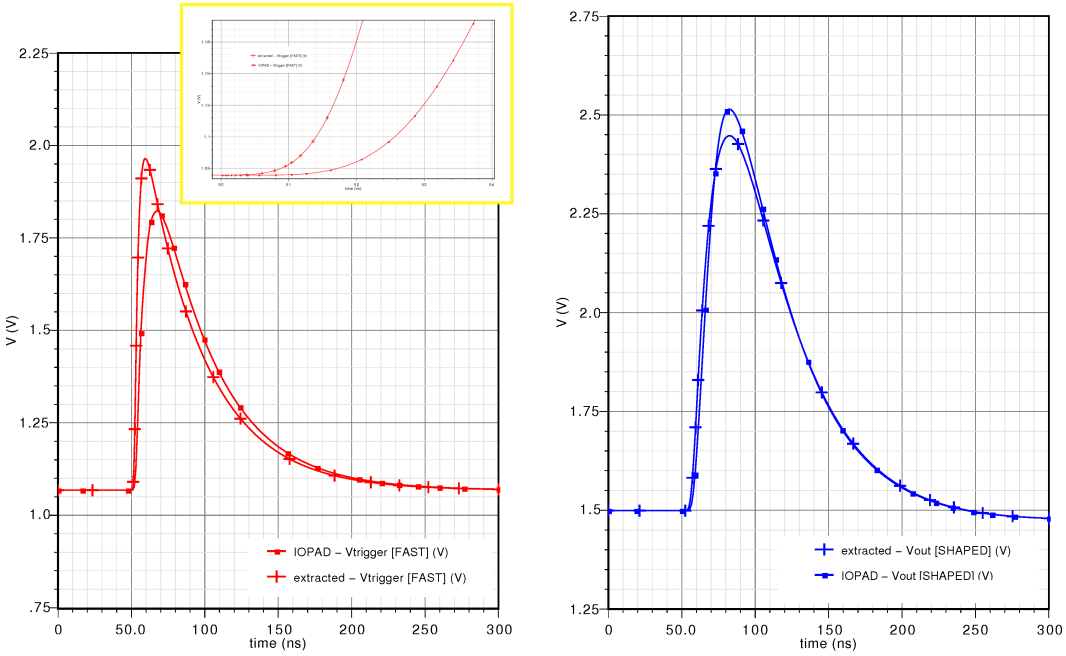

Figure 4.19: Transient waveforms of shaped (right) and trigger (left) signals for post-layout simulations with (label "- IOPAD") and without the effect of the chip I/O parasitics (SiPM+LYSO signal stimulus). Detail of the *Vtrigger* waveform reveals increased time walk and degraded slope with the RLC load.

From what has been discussed, (refer to page 27), we set the discriminator threshold at 2.5 photoelectrons, such that the comparator triggers after an input current pulse corresponding to to the arrival of the first 3 photoelectrons. However, since this threshold is to be programmable we may assume a minimum $N_{th} = 0.5$, which will enable the possibility to trigger on one single photoelectron.

Knowing that a 42 photoelectrons hit generates 5 pC of charge, then $N_{th} = 0.5$ implies a threshold charge of $Q_{th,min} = 60\ fC$. In the same way $Q_{th,typ} = 300\ fC$.

Figure 4.20 depicts in detail the first nanosecond after the event. It also includes the derivative waveform to which corresponds, for a given abscissa, the slope of the output signal, designated $\delta_{[th]}$.

Having the voltage gain of the path referred to the input charge given by Equation 4.1), we are able to describe the threshold charge in terms of a voltage swing ΔV. From there, each threshold voltage can be written as $V_{th} = V_{bl} + \Delta V$, where V_{bl} is the DC baseline of the output, where for *Vtrigger* it is measured $V_{bl} = 1.070\ V$ by simulation.

Having measured a total output noise voltage $\sigma_v = 2.28\ mV$ (printed in the output file,

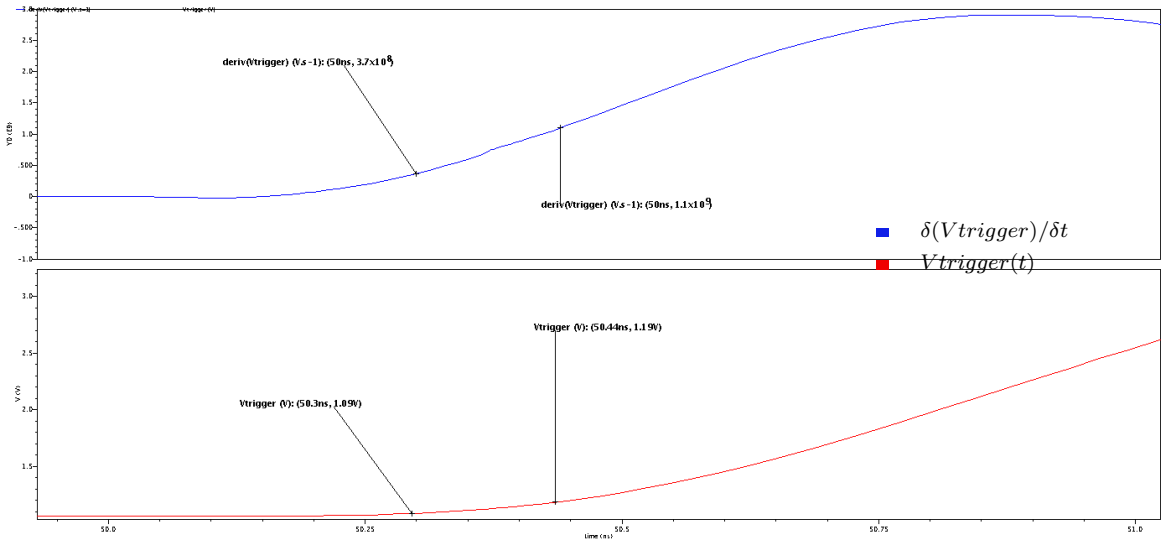

Figure 4.20: *Vtrigger [FAST]*: Detail of the transient response to a Delta pulse (below) and the derivative of the same signal (above). Note: Time of event (SiPM avalanche) is 50.0 ns.

Vnorms [Vtrigger] (V)), equation 2.1 can be re-written as:

$$\sigma_{tF} = 2.35\frac{\sigma_v}{\delta_{[th]}} \tag{4.2}$$

as to define the time resolution in terms of FWHM.

Table 4.3 summarizes the findings.

No. of photoelectrons	Q_{th} (fC)	ΔV (mV)	V_{th} (V)	$\delta_{[th]}$ (Vs^{-1})	σ_{tF} (ps)
0.5 (min)	60	24	1.09	3.7E8 (@50.3ns)	15
2.5 (typ)	300	120	1.19	1.1E9 (@50.4ns)	5

Table 4.3: FWHM time resolution for *Vtrigger [FAST]*, $C_d = 70pF$, $\sigma_v = 2.28mV$, $V_{bl_{FAST}} = 1.070\ V$

The demonstration for $Vout[SHAPED]$ is in Table 4.4, considering $\sigma_v = 3.07\ mV$ and a nominal gain of 0.15 mV/fC.

No. of photoelectrons	Q_{th} (fC)	ΔV (mV)	V_{th} (V)	$\delta_{[th]}$ (Vs^{-1})	σ_{tF} (ps)
0.5 (min)	60	9	1.51	3.1E7	234
2.5 (typ)	300	45	1.55	6.6E7	110

Table 4.4: FWHM time resolution for *Vout [SHAPED]*, $C_d = 70pF$, $\sigma_v = 3.07mV$, $V_{bl_{SHAPED}} = 1.499\ V$

These results prove, as expected, that a much better time resolution may be obtained with the fast current-mode output, rather than using the SNR optimized signal path.

Energy measurement requirements

Assuming that the pulse amplitude information is extracted from the measurement of the pulse width, the shaped voltage signal is fed into a comparator with programmable threshold voltage. Optionally, the inclusion of two comparators per output will allow individual thresholds for leading and trailing edges. A measure of the time window between the leading and falling edges of the signal is then used to extract the pulse amplitude and thus its energy. Figure 4.21 shows a function of the ToT versus the input charge, for a fixed threshold of 0.5 and 2.5 photoelectrons.

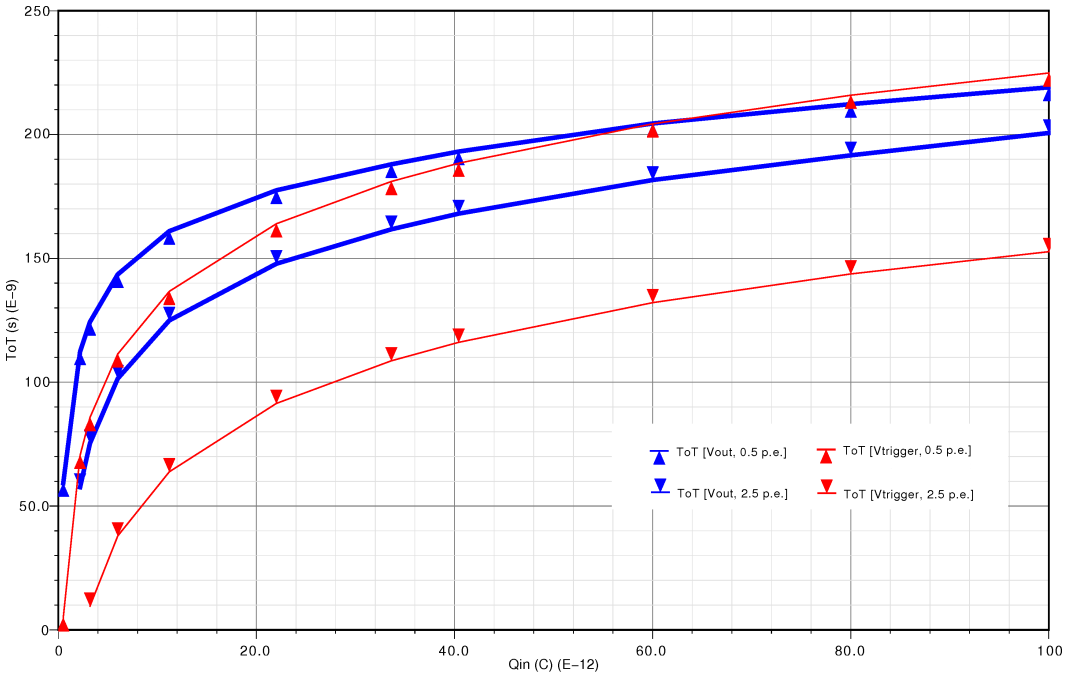

Figure 4.21: ToT: W(ns) vs. Qin(fC), measured on *Vout [SHAPED]* and *Vout [FAST]* for a threshold level of 0.5 and 2.5 photoelectrons.

Despite the V_{out} *vs.* Q_{in} function of the amplifier is only guaranteed to be linear for $Q_{in} = [2..40]\ pC$, the ToT technique allows the amplifier to become saturated, provided that the DC operating point of the input stage is not degraded. From the observed, the measured pulse width has a non-linear relation with the photon energy, i.e., $Q_{in} = f(W)$ is not a linear function. Both *Vout [SHAPED]* and *Vtrigger [FAST]* outputs show the same non-linear behaviour. The most evident solution to cope with this non-linearity is to build a look-up table in the firmware layer, written during calibration procedures.

4.3.2 Dynamic Range

This section assembles the results obtained with post-layout simulations, in what concerns the dynamic range of operation of the amplifier.

Programmable Variable Gain

The transimpedance gain has been made programmable, as specified. Figure 4.22 plots both the AC response of the shaping signal path (to a 1 A amplitude variable frequency superimposed to the signal current source at the preamplifier input) and the transient waveform when the input signal is a discrete delta pulse with $Q_{in} = 5\ pC$.

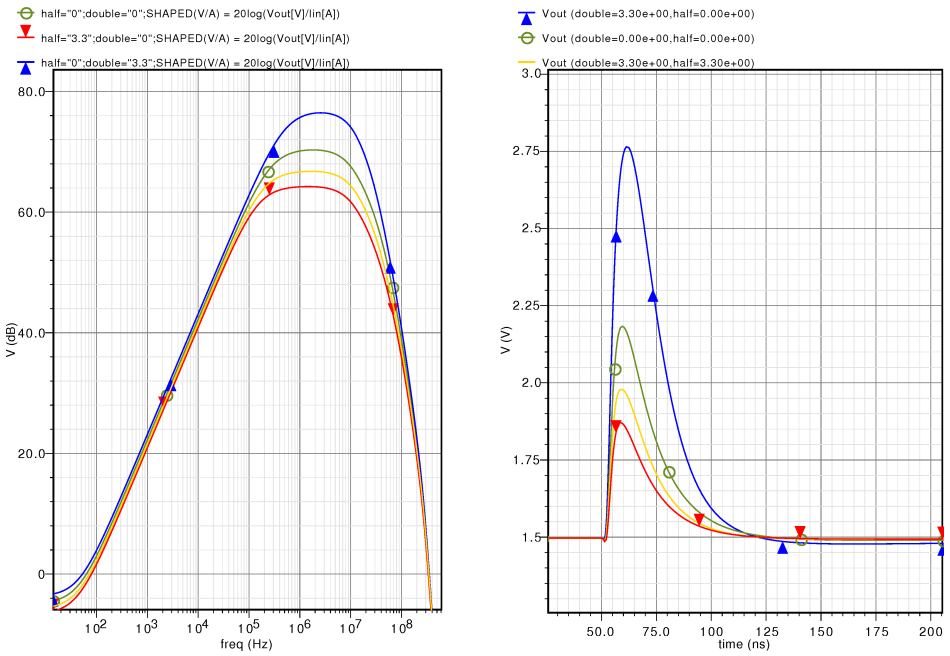

Figure 4.22: Transient (right) and AC response (left) waveforms of *Vout [SHAPED]*, for a coarse variable transimpedance gain defined by a 2-bit word

Table 4.5 summarizes the gain of the shaped signal path, in terms of mV/fC (according to equation 4.3:

$$G(mv/fC) = \frac{\Delta V_{out}}{Q_{in}} \tag{4.3}$$

The peaking time is seen to drift up to 20% from the nominal 10 ns. Following the transistor level implementation of the signal feedback path in Figure 3.15, one can now relate the effect with the the unsought load of switching circuitry. In fact, when each of the transmission gates is open, then the gate-to-source capacitance of both the P-type and N-type transistors sum-up to the capacitive load of the OA high-impedance output. Evidence can be shown for any of the table entries; for the worst case $[double, half] = [0, 1]$, all the

$C_{gs(sg)}$ of NM11(12), PM13(14) load the net with a parasitic capacitance that is of the same order of C_F (both P/N transistors have a 20/.4 ratio).

DOUBLE	HALF	G_0 (mV/fC)	Peaking Time (ns)
0	0	0.14	10.0
0	1	0.25	12.0
1	0	0.07	9.0
1	1	0.10	9.5

Table 4.5: Parametric gain measurements.

Total input pulse charge

From what has been predicted for the total pulse charge at the amplifier input (see Table 2.1), the transient response of the amplifier is plotted in figure 4.23 for a sweep of the input charge. The input signal is a realistic model for a LYSO+SiPM pulse, where a charge of 22 pC (average charge for the scintillation of a 511 keV photon, considering center DoI) corresponds to a 550 μA peak current of the exponential pulse.

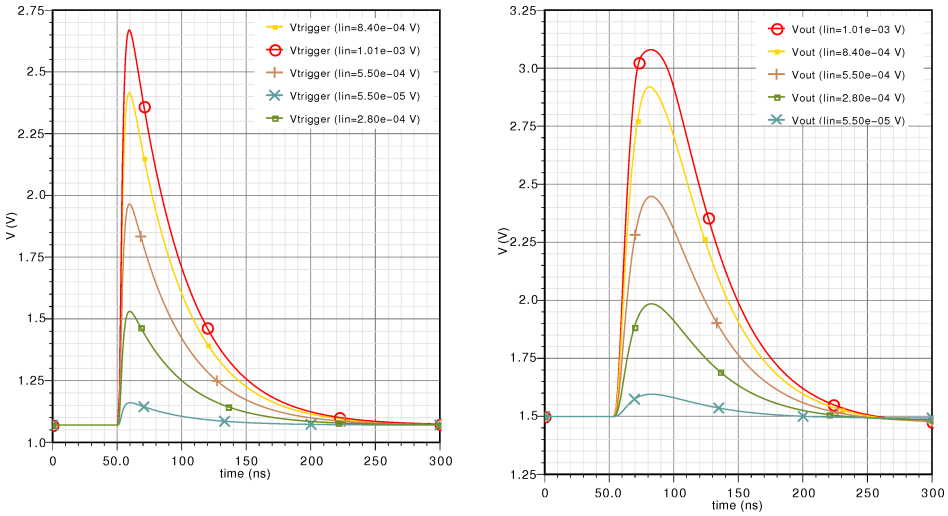

Figure 4.23: Transient waveforms of *Vtrigger [FAST]* (left) and *Vout [SHAPED]* (right), when the input charge is swept between 2.2 pC and 40.3 pC.

The input charge cross-check can be done by integrating the current pulse waveform in time, whence a plot of the output voltage swing versus the input charge can be plotted (Figure 4.24.

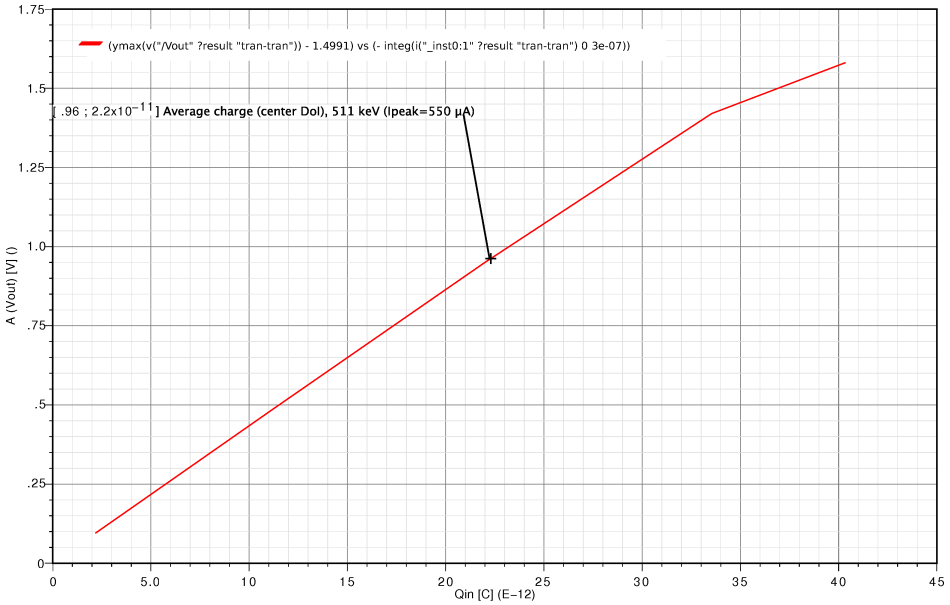

Figure 4.24: *Vout [SHAPED]* swing, labeled as $A(V_{out})$, plotted as a function of Q_{in}. The perceptible non-linearity for higher Q_{in} is seen also in figure 4.22, and is related to the fact that the transimpedance gain drops off when the output signal amplitude approaches the value of Vdd.

R1_GND (Ω)	$5k$	$10k$	$15k$
$I_{DS_{M1}}$ (A)	$1.5m$	$0.5m$	$0.3m$

R2_GND (Ω)	$5k$	$10k$	$15k$
$I_{DS_{M2}}$ (A)	$2.5m$	$0.9m$	$0.6m$

Table 4.6: Parametric IB1 and IB2: correspondence to Rx_GND.

Parametric operating point of the input stage

Figure 4.25 depicts the variation of the input impedance in frequency for both schematic and extracted views, when the biasing currents IB1 and IB2 are trimmed. Table A.1 (in Appendix) renders in numbers the relevant parameters that define the operating point of the input (M1) and regulation (M2) transistors. The correspondence between IBx and Rx_GND (swept to generate fig. 4.25) is summarized in Table 4.6.

From these results, we may expect to be able to reduce the input impedance down to 4.5 Ω, if IB1 is increased by 50% (IB1=1.5 mA).

4.3.3 Process variation robustness

The worst case files are extracted from an extensive database of chip characterization, and represent the spread window of process variation. Engineering lots (commonly denominated as Process Window Lots) of samples are produced by the foundry during the process

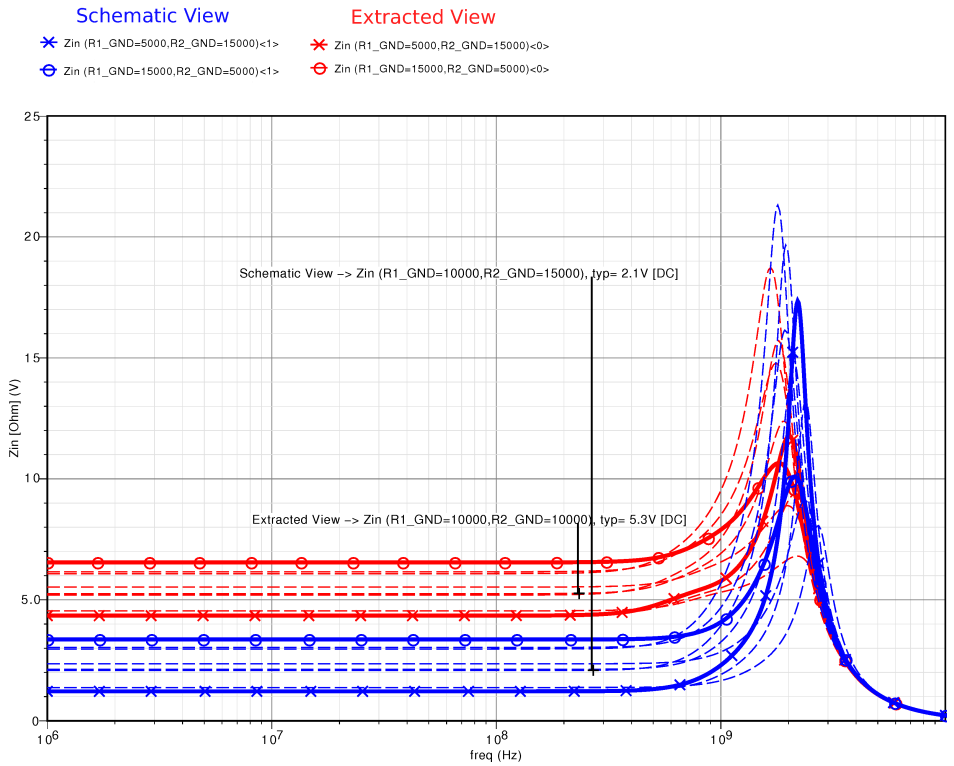

Figure 4.25: Parametrization on the input impedance through adjustment of the RGC operating point: expected by simulation with schematic environment, and results with post-layout netlists.

node ramp-up. Such lots are statistically meaningful and can be used both for back-end test development (product engineering) and to generate accurate device models.[2] For example, an MOS device with thinner gate oxide thickness t_{ox} will generally exhibit higher transconductance. The same is to say that, due to its higher C_{ox} (where $C_{ox} = \varepsilon_{ox}\varepsilon_0/t_{ox}$), the native V_{th} will be lower and hence the transistor lies in the "fast" corner [3]. Nonetheless, as the corners that they are, the probability that the processed wafer of a MPW run falls into one is considerably low, for a mature technology.

With corner models only, the simulator engine will build the circuit netlist considering that the parameters of all N-type/P-type transistors are drifted in the same direction, according to the general distribution explained in Table 4.7. Evidently, that may not hold true if the process gradient affects the block transistors differently. For instance, if a deviating doping profile or mask alignment has an x-axis dependent variation, then the transistors along such

[2]Of course that, as far as the qualification of new process nodes designs is concerned, process disturbance random generators are included into simulators to provide designers usable models, since in the first milestones there is not enough (or not at all) manufacturing data to create a statistically meaningful process window.

[3]It is intuitive to consider that if the transistors of a CMOS digital circuit have lower threshold, then the switching occurs sooner in time and thus the device operation is "faster". Or even, low-V_{th} NMOS induce smaller propagation delays t_{pHL} and, similarly, low-V_{th} P-type devices reduce the t_{pLH} of the logic gates.

sigla	Process corner model
tt	typical case model
ss	slow N and slow P model
$snfp$	slow N and fast P model
$fnsp$	fast N and slow P model
ff	fast N and fast P model

Table 4.7: Process Corner model nomenclature.

axis should be characterized with different geometry parameter lists, rather than being all described with a corner process model. This statistical distribution is described by Monte-Carlo models, in which the relevant parameters for each transistor of the netlist are randomly extracted from the foundry process characterization distributions. Of course, only a relatively high number of simulation iterations will add significance to the test.

However, when the analogue design effort thoughtfully includes mismatch mitigation techniques, the invocation of Monte-Carlo model parameters may over-estimate the circuit's performance degradation. That being said, and given that appropriate analogue design techniques have been employed on the design of the front-end amplifier, one can predict that the probability curve of the worst-case scenarios due to transistor mismatch is duly enclosed in that defined by the process corner models.

Still, Monte-Carlo analysis would be meaningful if a multichannel prototype was under study, as the drift of the biasing currents could cause non-negligible jitter between channels. That because, while the mismatch effects inside each sub-circuit are mitigated with appropriate design, the distribution of a shared bias current IBx within m stacked channels is susceptible to geometry variations between the m mirroring transistors. In that case, Monte-carlo model simulations with coincident events at the input of the multichannel block could be used to build a purposeful histogram of the time resolution with statistical process variations.

For a single-channel prototype, some of the relevant process envelope results are forwardly presented. Despite the fact that all capacitance, resistance and MOSFET corner iteration waveforms are superposed, the legends are created according to meaningful process bias. As an example, figure 4.26 demonstrates the decrease of Z_{in} with fast transistor models, up to a maximum of nearly 6 Ω.

While the fast output shows (in Figure 4.27) to have its baseline shifted down by less

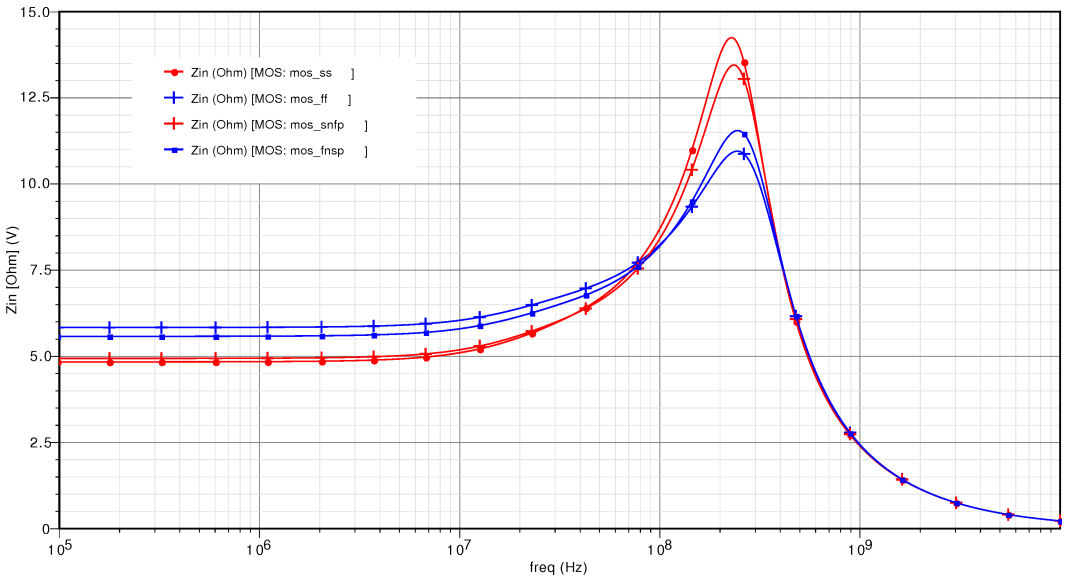

Figure 4.26: Frequency sweep of Z_{in}:Corner models simulation results

than $\approx 3.5\%$ if the die falls into a $fast$ NMOS corner, the (still, unlikely) deviation is enough to require a compensation scheme if this output feeds directly a current discriminator. In fact, if a voltage signal is directly extracted from the fast output signal, its baseline voltage is not regulated and, consequently, the variation due to process drifts does not allow the ToT measurement to be done directly on the trigger signal. The extraction of a time stamp would be as challenging, since the reference voltage of the timing comparator should need to be a function of the channel baseline. A similar scheme as what is used in the *BiasRegulator* may be adequate, where a limited slew-rate buffer would sample the *Vtrigger* output and feed it to the negative input of the timing comparator, while clipping the fast amplified signal. Besides, a channel-by-channel independent threshold adjustment could be used to compensate inter-channel gain variability. As in the case of the input impedance, there is also no observable drift caused by resistor of capacitor corners, unsurprising since neither Z_{in} nor $Vtrigger$ hinges on any process passive devices.

The shaped output, plotted in Figure 4.28, evidences that its transfer function is manifestly clung to the drift of the passive devices. That is not unexpected, in view of the fact that they define the integration constant of the shaper. One may verify, for example, that the peaking time is shorter when the capacitance corner shifts to min, or that the transimpedance is maximum for the resistance corner max. Nevertheless, these data may denote that the layout of the *FeedbackTIA* block could be ameliorated in order to better withstand the slide of R_F and C_F from their nominal values (e.g. increasing the L parameter of the resistors,

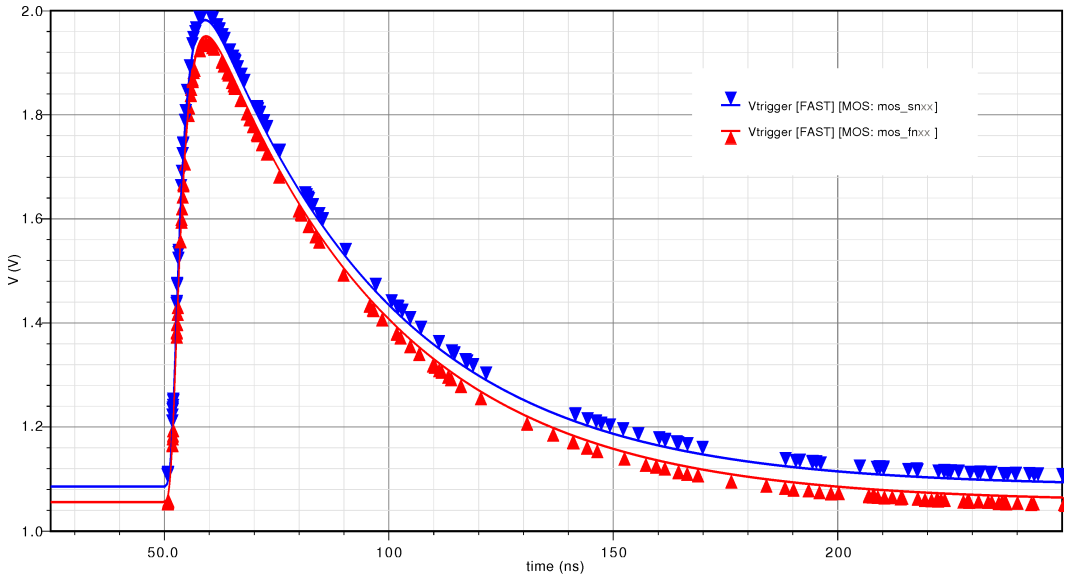

Figure 4.27: *Vtrigger*:Corner models simulation results

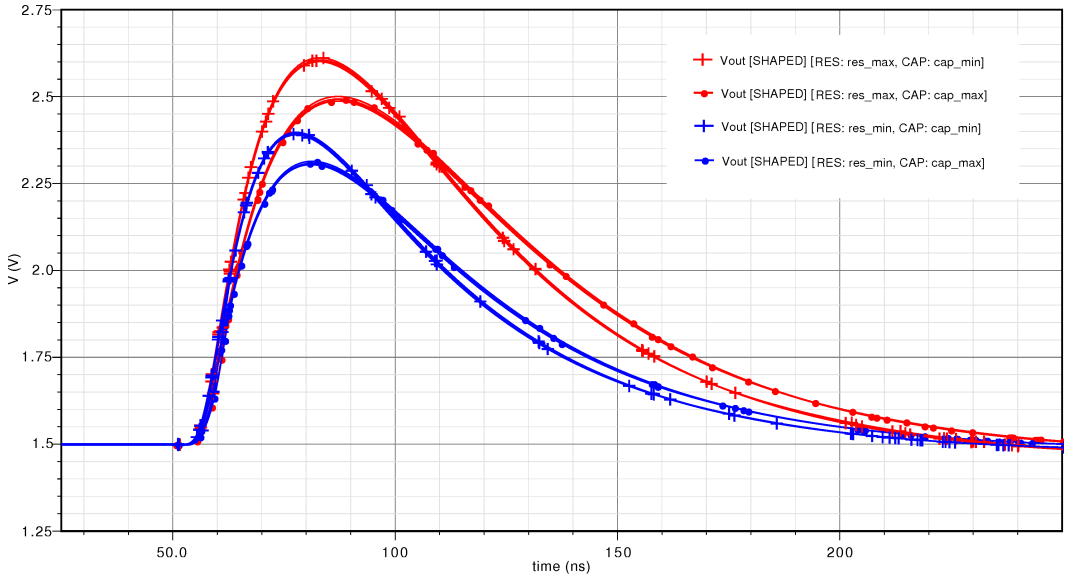

Figure 4.28: *Vout*:Corner models simulation results

from 1 to 2 μm).

It is important to reiterate that the process corner simulations do not create the most severe test conditions for a mixed-signal design. A thorough design for manufacturability assessment must employ the combination of a statistical and corner models for both active and passive devices.

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Chapter 5

Final Remarks

This chapter discusses issues that either were not solved or were not taken into account, and provides guidelines for future work, based on presupposed improvements or experiments that took place after the closed layout. A wrap-up of key figures and concluding remarks settles the accomplishments of the developed work.

5.1 Optimization of the input stage

The work in [Nero2008] suggests that a RGC-alike current conveyor topology has a modest bandwidth performance, though having the lowest input impedance of the studied circuits. The underlying trade-off between bandwidth and open-loop gain of amplifiers seems to be in agreement with that expectation. As aforementioned in Section 3.2.1, the optimization of the input stage can depart from this premise and attain a better compromise with lower open-loop regulation gain. Alternatively, the designer may try to reduce the phase shift due to the internal poles. In practical terms, pushing the phase crossover further in frequency (with a positive income on stability) means reducing the parasitic capacitances on the signal path. Specifically, the total gate capacitance of the regulation transistor[1] M2 and, with a less extent, the Miller capacitances due to the C_{gd} coupling of both the input transistor and the PMOS bias current mirror of M2. Of course that, if the dimensions of M2 are reduced, also does its transconductance and thus the regulation gain. Instead, the g_{ds} of the current mirror can be increased to reduce the value of the resistive coefficient of the internal pole that it produces. Then again, not only the reduction of r_o affects the gain A[2] but also it can change the operating point of the circuit (specifically, the input transistor gate node voltage).

[1] The largest component is obviously due to C_{gs}, but that appears in parallel with the photodiode total C_d

[2] It does affect the regulation gain, since $A = g_{m2}/(g_{dsM2} + g_{dsIB2})$, but to a less extent than the reduction of gm_2. Typically, $g_{dsM2} >> g_{dsIB2}$, ergo the reduction of r_{o2} does not cause, by itself, a dramatic reduction of A.

This optimization is inevitably a simulation-intensive work, but an efficient batch based on OCEAN scripts could be written to extract the relevant parameters and enable recursive simulation.

Complementary, a novel pre-amplifier topology could be studied to further improve the low input impedance and speed characteristics of the current buffer. Referred by [Nero2008], a positive feedback current-mode method may be simpler to implement and result in a better GBW. Input and output resistances of, respectively, 6 and 18M Ω were claimed in [Pennisi2002], evidencing the interest on the study of such methods.

5.2 Noise performance considerations of a current-mode architecture

It has been predicted (refer to page 61) that the additional noise that due to the use of a current-mode bandgap may set a drawback to the accomplishment of a good low-noise performance. While the design on the whole aims for the cutback of the total output noise voltage, the shaper block in particular has a transfer function that is intended to optimize the signal-to-noise ratio of the output V_{out}. This study was, however, part of a preliminary stage of the design using ideal current sources, whence the transimpedance amplifier poles and the baseline holder circuit were set to satisfy the filtering of the noise generated by the *PreAmplifier*.

Following the newly introduced noise contributors of the current reference generator, the overall noise performance has been degraded considerably. Figure 5.1 introduces this discussion, were noise and AC simulation results (post-layout netlist) are plotted for both fast (*Vtrigger*) and shaped (*Vout*) outputs. A first examination of the plotted data reveals that

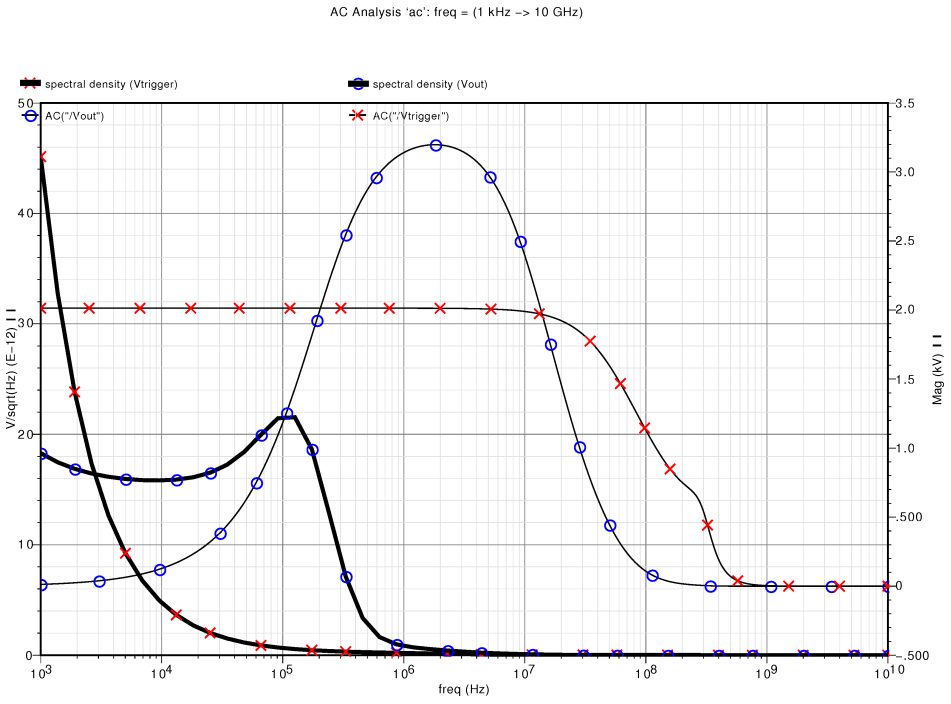

Figure 5.1: Noise spectral density (thick lines) and AC response (thin lines) probed at both voltage output nodes *Vtrigger* (red cross) and *Vout* (blue circle).

the fast path has a transimpedance gain of approximately 2000 (corresponding to $Rtrigger = 2\ k\Omega$), for a 60 MHz bandwidth (schematic level simulations indicated 65 MHz). The main contribution for the noise measured at *Vtrigger* is that due to the thermal noise of the input

stage regulation transistor M2, as expected.

The frequency response of the shaped signal path has the envisaged band-pass behaviour. While the high-frequency gain roll-off is defined by the shaping constant τ_F, given by $R_F C_F$, the low-frequency zero provided by the baseline holder circuitry. The low-frequency filtering is expected to dump the noise spectrum contributions, therefore increasing the signal-to-noise ratio at the output. For the frequencies of interest, the gain of the shaper block is 70.1 dB ($A_{simulation} \approx 3200$), which is in agreement with the 32:1 input current scale-down, followed by a transimpedance gain of 95 k ($A_{theoretical} \approx 2970$) [3].

Intriguingly, the noise spectral density function VN2() evidences a peak around 100 kHz, due to the high gain of the *FeedbackTIA+BiasRegulator* at these frequencies, that had not been predicted. The square of its integral ($V_{no\ rms}$) results in a total of 3.2 mV ($C_{tot} = 70\,pF$), which is even higher then what is measured at *Vtrigger* (2.7 mV). An analysis to the noise summary output reveils that the main noise contributors for the $V_{no\ rms}$ measured at the shaped output are the current reference NMOS of the $Irefgen$ block (/I20/I3/NM3(&2)), which generate the bias current IB5 of the *BiasRegulator* transconductor; the internal mirroring NMOS pair /I20/I0/NM8(&9) follows the list. The evident countermeasure to tackle this excess noise is to filter the noise of the reference generator (by the means explained further in section 5.2, such that the spectral density of thermal noise around the frequencies of interest would decrease. Figure 5.2 shows the change of the noise spectral density at the output node, when the transconductor reference IB5 is made an ideal current source. The bandpass behaviour of the low-pass transconductor is kept (plotted below, in dB, the two curves overlap), and the value of $V_{no\ rms}$ drops by almost 20%, $V_{no\ rms\ IDEAL\ IB5} = 2.7\ mV$ (compared to $V_{no\ rms\ IB5\ CM} = 3.2\ mV$). The noise summary reveals, as expected, that the internal mirroring NMOS pair /I20/I0/NM8(&9) are now the main contributors for the total noise at the output. In this regard, there are no evident options, since the transconductance of NM9 (current source of the transconductor differential pair) has already been made low ($\approx 1\ \mu S$).

Noise mitigation of current reference generators

The input referred output noise of a current source can be mitigated by filtering the noise voltage that drives the output transistor gate. At the cost of an overhead silicon area,

[3] The transistor level implementation of the 32:1 division results, in simulation environment with typical transistor models, in a measured 29:1 ratio of input:output currents - 2% deviation of the gain, for $A_{transistorlevel} \approx 3275$

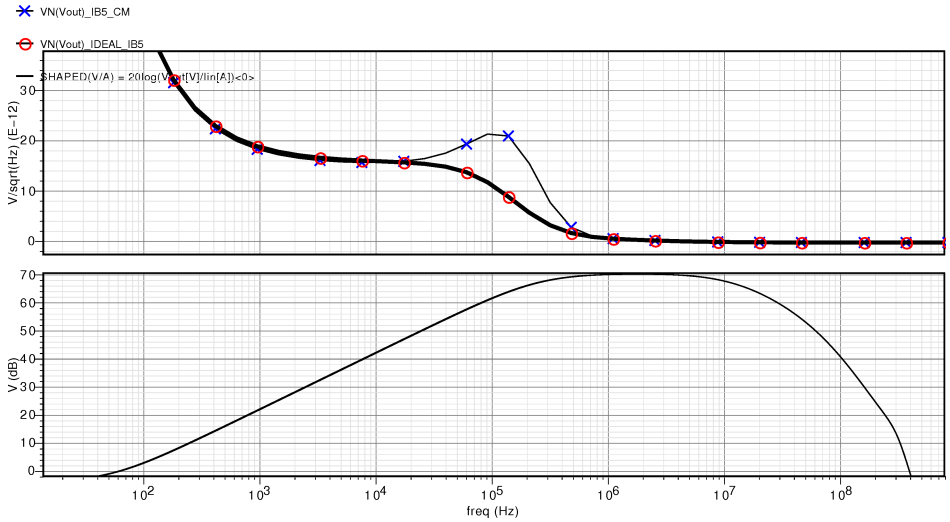

Figure 5.2: Noise spectral density (above) and AC response (below) probed at *Vout*, with IB5 generated by an ideal current source (red circle), or output of the *Irefgen* block (blue cross).

a filtering capacitor can be added to all the five current reference generators. Two noise suppression capacitors were added to IB1 and IB2, in agreement with what is shown in figure 5.3. The layout implementation is ready and LVS checked (Figure 5.4).

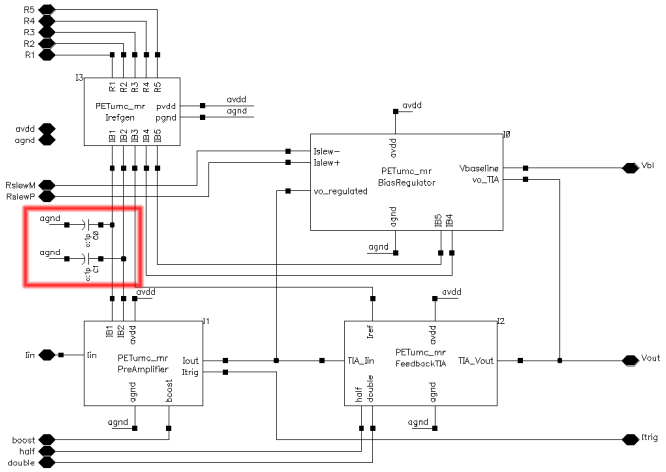

Figure 5.3: Schematics of the modified full channel to include two 1pF noise suppression capacitors in current references IB1 and IB2.

Following the inclusion of two 1 pF capacitors to reduce the thermal noise of the current references, a detailed analysis of the changes allowed to conclude that a reduction around 20% can be achieved. The below results refer to schematic-level simulations for nominal operating conditions, where a noise analysis swept the frequency range 10 Hz - 10 GHz.

Tables 5.1 and 5.2 compile the results from probing of the total output *rms* noise voltage

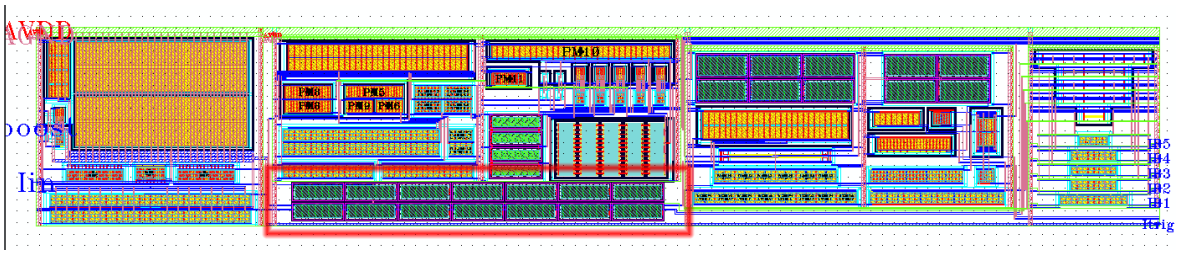

Figure 5.4: Layout of the full channel, including the noise capacitors.

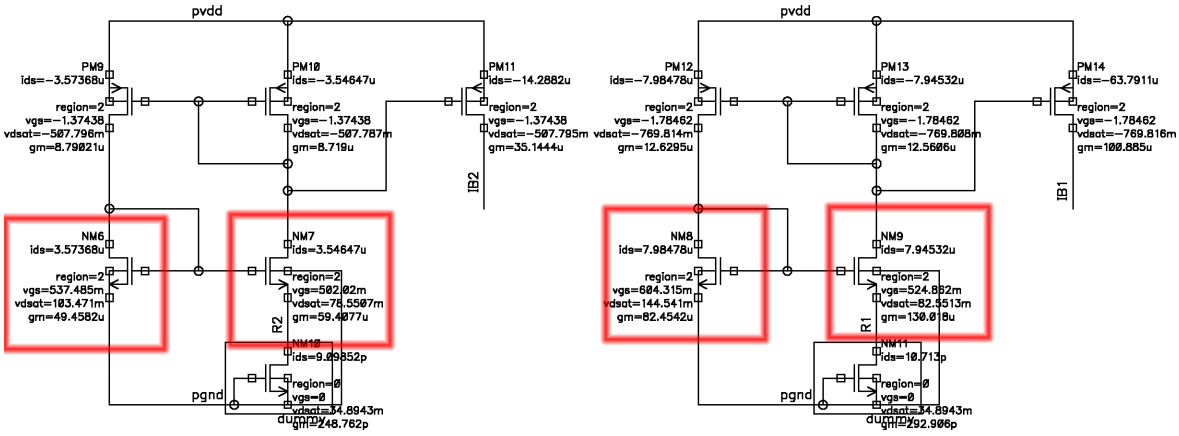

Figure 5.5: Detail of the *Irefgen* block, with the dominant noise source NMOS marked in red squares.

on *Vtrigger* and *Vshaped* outputs, with and without the filtering capacitors. The **device** (within hierarchy) and the **type** of noise source (*id*: thermal noise, *fn*: flicker noise, *fn*: resistor noise) is identified. The probing result is the total **rms** noise voltage source, integrated in the aforementioned frequency range, and the percentage (**% of Total**) of each contribution.

Tables 5.3 and 5.4 depict the variation of the contribution to the total output *rms* voltage noise, for each probing node, for the devices apiece. Since the variation is calculated by means of comparing the noise summaries without/with filtering capacitors, the entries "#N/A" indicate that the device is no longer a major 15 contributor. The thermal noise contribution of the saturated NMOS transistors corresponding to IB1 and IB2 on the micro-current reference generator appear as **bold** on Tables 5.3 and 5.4. The same transistors are marked in the *Irefgen* block with a red square. The ***bold italic*** device of Table 5.3 is the diode-connected NMOS that mirrors IB2 inside the *PreAmplifier* block. The "note" entry indicates the highest absolute reductions, above 500 μV.

Bottom line, the noise filtering capacitors dramatically reduce the thermal noise produced by the NMOS transistors of IB1 and IB2 micro-current reference generators. Preliminary results (schematic-level simulations) indicate that an average 20% reduction of the total output

Without filtering capacitor					
Vtrigger			*Vshaped*		
Device, type	rms (V)	% of Total	Device, type	rms (V)	% of Total
/I20/I1/M2 id	1.69E-003	18.60	/I20/I3/NM3 id	1.25E-003	9.37
/I20/I1/NM3 id	1.66E-003	17.93	/I20/I3/NM2 id	1.25E-003	9.27
/I20/I1/NM2 id	1.51E-003	14.87	/I20/I3/NM9 id	1.18E-003	8.24
/I20/I3/NM7 id	1.06E-003	7.32	/I20/I0/NM8 id	1.15E-003	7.95
/I20/I1/M2 fn	1.02E-003	6.73	/I20/I3/NM8 id	1.11E-003	7.40
/I20/I3/NM6 id	8.70E-004	4.93	/I20/I0/NM9 id	1.11E-003	7.40
/I20/I3/NM9 id	8.01E-004	4.17	/I20/I3/NM7 id	1.07E-003	6.84
/I20/I3/NM8 id	7.59E-004	3.75	/I20/I3/NM6 id	9.55E-004	5.44
/I20/I3/PM11 id	7.13E-004	3.31	/R1_GND rn	8.01E-004	3.83
/I20/I1/PM0 id	6.85E-004	3.06	/I20/I1/NM5 id	7.90E-004	3.73
/I20/I3/NM8 fn	6.75E-004	2.97	/I20/I0/PM11 id	6.75E-004	2.72
/I20/I1/PM1 id	5.48E-004	1.95	/I20/I1/NM2 id	6.17E-004	2.27
/R1_GND rn	5.29E-004	1.82	/I20/I3/NM8 fn	6.04E-004	2.18
/I20/I3/NM9 fn	3.92E-004	1.00	/I20/I3/NM5 id	5.33E-004	1.70
/I20/I3/PM13 id	3.34E-004	0.72	/I20/I3/PM13 id	4.97E-004	1.47
Vnorms [Vtrigger] (V) = 3.91938m			Vnorms [Vshaped] (V) = 4.09393m		

Table 5.1: Noise summary: without filtering capacitors.

With filtering capacitor					
Vtrigger			*Vshaped*		
Device, type	rms (V)	% of Total	Device, type	rms (V)	% of Total
/I20/I1/NM3 id	1.70E-003	28.15	/I20/I0/NM8 id	1.15E-003	12.73
/I20/I1/M2 id	1.69E-003	27.82	/I20/I0/NM9 id	1.11E-003	11.85
/I20/I1/M2 fn	1.01E-003	10.08	/I20/I3/NM3 id	1.08E-003	11.19
/I20/I1/NM2 id	7.33E-004	5.26	/I20/I3/NM2 id	1.08E-003	11.12
/I20/I1/PM0 id	7.00E-004	4.80	/I20/I1/NM5 id	7.90E-004	5.97
/I20/I3/NM8 fn	6.21E-004	3.77	/I20/I0/PM11 id	6.75E-004	4.35
/I20/I1/PM1 id	5.46E-004	2.92	/R1_GND rn	6.56E-004	4.11
/I20/I3/NM7 id	4.63E-004	2.10	/I20/I3/NM9 id	6.28E-004	3.77
/R1_GND rn	4.55E-004	2.03	/I20/I3/NM8 id	6.04E-004	3.49
/I20/I3/NM9 id	4.39E-004	1.89	/I20/I3/NM7 id	5.25E-004	2.63
/I20/I3/NM8 id	4.19E-004	1.72	/I20/I0/PM12 id	4.90E-004	2.29
/I20/I3/NM6 id	3.98E-004	1.55	/I20/I3/NM6 id	4.80E-004	2.20
/I20/I3/NM9 fn	3.59E-004	1.26	/I20/I3/NM8 fn	4.43E-004	1.87
/I20/I3/PM11 id	3.46E-004	1.17	/I20/I1/NM5 fn	4.34E-004	1.80
/R2_GND rn	3.00E-004	0.88	/I20/I0/PM10 id	4.10E-004	1.60
Vnorms [Vtrigger] (V) = 3.19468m			Vnorms [Vshaped] (V) = 3.23513m		

Table 5.2: Noise summary: with filtering capacitors.

Probing on *Vtrigger*			
Device, type	Reduction (%)	Absolute Reduction (mV)	obs
/I20/I1/NM3 id	-2%	-3.55E-005	
/I20/I1/M2 id	0%	5.28E-006	
/I20/I1/M2 fn	0%	2.54E-006	
/I20/I1/NM2 id	52%	7.79E-004	above 500uV
/I20/I1/PM0 id	-2%	-1.47E-005	
/I20/I3/NM8 fn	8%	5.48E-005	
/I20/I1/PM1 id	0%	1.71E-006	
/I20/I3/NM7 id	56%	5.97E-004	above 500uV
/R1_GND rn	14%	7.38E-005	
/I20/I3/NM9 id	45%	3.62E-004	
/I20/I3/NM8 id	45%	3.40E-004	
/I20/I3/NM6 id	54%	4.73E-004	
/I20/I3/NM9 fn	8%	3.32E-005	
/I20/I3/PM11 id	52%	3.67E-004	
/R2_GND rn	#N/A	#N/A	#N/A
Average reduction	24%		

Table 5.3: Noise summary for *Vtrigger*: changes per device

Probing on *Vshaped*			
Device, type	Reduction (%)	Absolute Reduction (mV)	obs
/I20/I0/NM8 id	0%	0.00E+000	
/I20/I0/NM9 id	0%	0.00E+000	
/I20/I3/NM3 id	14%	1.71E-004	
/I20/I3/NM2 id	13%	1.68E-004	
/I20/I1/NM5 id	0%	0.00E+000	
/I20/I0/PM11 id	0%	0.00E+000	
/R1_GND rn	18%	1.45E-004	
/I20/I3/NM9 id	47%	5.47E-004	above 500uV
/I20/I3/NM8 id	46%	5.10E-004	above 500uV
/I20/I3/NM7 id	51%	5.46E-004	above 500uV
/I20/I0/PM12 id	#N/A	#N/A	#N/A
/I20/I3/NM6 id	50%	4.76E-004	
/I20/I3/NM8 fn	27%	1.61E-004	
/I20/I1/NM5 fn	#N/A	#N/A	#N/A
/I20/I0/PM10 id	#N/A	#N/A	#N/A
Average reduction	22%		

Table 5.4: Noise summary for *Vshaped*: changes per device

rms noise voltage is attainable, measured in both time (*Vtrigger*) and charge (*Vshaped*) outputs.

5.3 Design revisions planning

Apart from the considerations that are expected to drive a major design revision, the following optimization steps are so far planned.

Multi-channel disposition

In the anticipated knowledge of the challenge to densely abut the blocks in a multi-channel design, due to the crosstalk effect caused by the large current pulse at the input, electrical characterization of a 4-channel arrangement is usefull. With that, the *Irefgen* is shared, and the trimming of references becomes transversal to all input channels.

Trimming of *Islew*

The design of the *BiasRegulator* shall be revised to substitute the symmetric PMOS/NMOS set-up of the non-linear buffer slew current, which currently requires two I/O pads. Concretely, *Islew* shall use an independent P-type/N-type current reference and internally mirror the reference for the NMOS or PMOS, respectively. (proposed in [Cobanoglu2007])

The subsequent need to redesign the *Irefgen* is implicit, if the option to individually trim the SR of the buffer is envisioned. The I/O expenditure is reduced to one pad, and the effort to implement this change is insignificant.

Input transistors voltage scale down

A future design will consider the use of lower V_{dd}, at least for the input stage transistors. The UMC130nm technology has, available for standard MPW (Multi-Project Wafer) runs, a low-V_{dd} "flavour" transistor option (1.2V). The signal dynamic range is kept unaffected when lower values of V_{dd} are used, as long as a current mode approach is used. A major power reduction is the obvious intent of this revision.

On-chip measurement of time stamps

Post-layout simulation results show that the amplifier performance far exceeds the original specifications in terms of timing resolution (Table 4.3). Such achievement is supported by the proposed dual-path configuration for timing and energy measurements, but that is nevertheless an optimistic assumption. The fast path signal is due to be fed to a finite BW

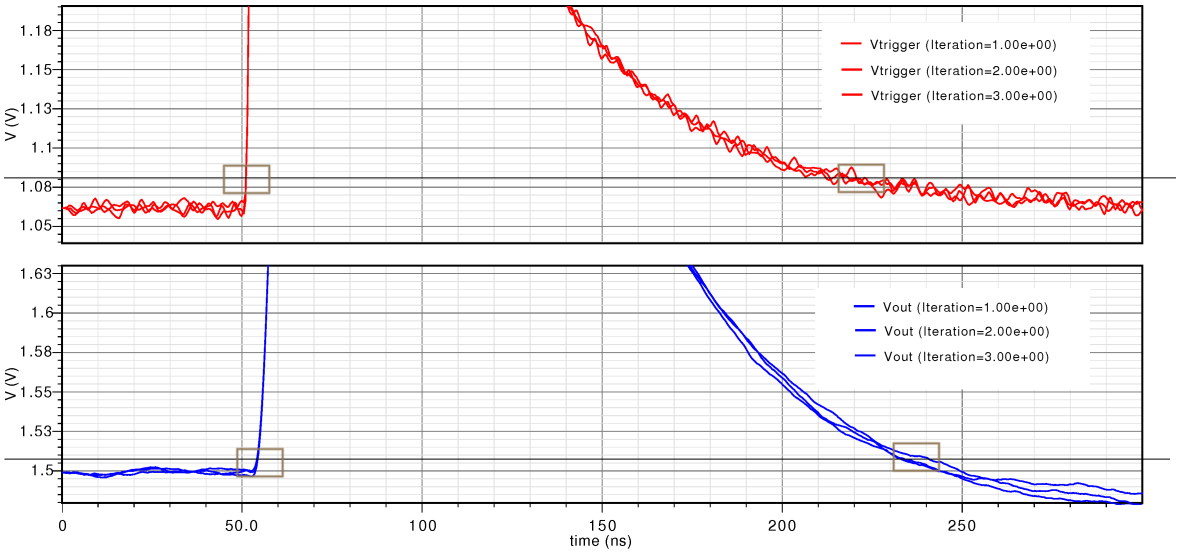

Figure 5.6: Transient noise (3 iterations) of trigger ($\sigma_v = 2.28\ mV$) and shaped ($\sigma_v = 3.07\ mV$) signals. Schematic view simulations, $C_d = 70pF$.

comparator which, more than slowing down the rise time of the trigger signal (because of the pole introduced by its input capacitance), is not noiseless and will thus have its own contribution to the total output jitter. Optionally, the inclusion of two comparators per output will allow individual thresholds setting for leading and trailing edges, if ToT measurements are envisaged. Figure 5.6 is helpfull to understand the implication of the output noise in the precision of energy measurements via with a ToT technique. The transient noise analysis waveforms evidence that the extraction of the falling edge time stamp (a 0.5 photoelectron threshold is exemplified) suffers from the much smaller slope of the signal, whence the jitter of the differential time interval will be higher. Regardless of the fact that the resolution of the time binning for energy measurement can be smaller, a simple solution consisting of a second comparator with higher threshold (programmable, typically 10 times higher) can remarkably improve the calculation of the pulse charge.

In order to account for these effects in a preliminary stage, the design of the amplifier must include CFD or comparator blocks, with variable threshold, from which a digital output can be used to conclude about jitter due to electronic noise, or the non-linearity arising from time walk.

5.4 Conclusions

Table 5.5 outlines the specifications of the CMOS analogue front-end herein reported. The benchmarks are put with reference to a nominal operation, and were obtained by simulation after extraction of silicon layout resistive and capacitive (both coupled and decoupled) parasitics. The electronic jitter is labelled ideal, as its measurement supposes a noiseless comparator with infinite input impedance and negligible capacitive loading. Validation of results included the use of package and wire bonding rough models.

Parameter	Value
Input impedance (DC)	5.3 Ω
Bandwidth (FAST)	60 MHz
Dynamic range (waveform sampling)	2 - 40 pC
Dynamic range (ToT)	0.5 - 100 pC
Power consumption	10 mW
Input polarity	negative
Peaking time (SHAPED)	10 ns
Peaking time (FAST)	1.8 ns
Noise (@70pF) (SHAPED)	3.1 mV
Noise (@70pF) (FAST)	2.3 mV
Sensitivity (Gain) (SHAPED)	0.15 mV/fC
Sensitivity (Gain) (FAST)	0.40 mV/fC
Electronic jitter (ideal) (FAST)	5.0 ps (@2.5 p.e.)
Electronic jitter (ideal) (SHAPED)	110 ps (@2.5 p.e.)

Table 5.5: Amplifier set of specifications.

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Appendix A

APPENDIX

A.1 OCEAN SCRIPTS

The script below was successfully validated, and provides monitoring of all the design variables, netlist and input stimulus changes. Along with the waveforms generated, an output file is written with information concerning the test conditions. Additionally, relevant simulation data is stored, whether direct measurements of results from calculation. The user is asked to define the both the input netlist and the path for the results output file. Furthermore, a parametric study of is possible for *IB1*, *IB2*, *Iin*, *Rslew*, *Vbl*, *Gain* and *Ctot*. It is worth mentioning the extra care that needs to be taken with some of the parametrization steps. Reference currents *IB1* and *IB2* can be trimmed by changing *R1_GND* and *R2_GND*, respectively. Since the first is used as reference for the current driver *Itrig*, and given that the characterization has used an ideal resistor *Rtrig* to measure a voltage signal, the DC baseline at this output node is $Vtrig = Rtrig \cdot Itrig$. Hence, increasing *IB1* woud not only increase the voltage gain but also rise the baseline, reducing the voltage headroom of the output signal. Accordingly, the transconductance of the output transistors drifts when *IB1* is made variable, and it is thus expectable to observe differences in the characterization of the signal path for timing measurements with variable *IB1*. Transient noise is also optional (default 3 runs). The AC analysis can also be turned off, for quick transient checks. The script also runs process corner models (no MC mismatch), whence automatically labelled waveforms are created for each (capacitance, resistance and MOSFET) corner iteration.

```
simulator( 'spectre )
clearAll()
;;newWindow()
netlistfile=design( "/home/mrolo/projects/PETumc/1v0/mrolo/Sim/Testbench_full/spectre/
schematic/netlist/netlist")
resultsDir( "/home/mrolo/projects/PETumc/1v0/mrolo/Sim/Testbench_full/spectre/schematic" )
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;ENVIRONMENT SET-UP;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;; USER ACTION: EXTRACTED/SCHEMATIC netlist directory (uncomment the line);;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;; USER ACTION: choose log file for simulation outputs:;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
netlistfile=design( "/home/mrolo/projects/PETumc/1v0/mrolo/Sim/Testbench_full_EXTRACTED/
spectre/schematic/netlist/netlist")
;netlistfile=design( "/home/mrolo/projects/PETumc/1v0/mrolo/Sim/Testbench_full/spectre/
;schematic/netlist/netlist")
;
resultsFile= "/home/mrolo/projects/PETumc/1v0/mrolo/Sim/Testbench_full/spectre/schematic/
ROLO_file"
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;VARIABLES SET-UP;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;; USER ACTION: define simulation variables ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
Rtrig = desVar(   "Rtrig" 2k    )
Ctot  = desVar(   "Ctot" 70p   )
Iin   = desVar(   "Iin" 550u    )
Cdirac= desVar(   "Cdirac" 0    )
Idirac= desVar(   "Idirac" 10m  )
R1_GND= desVar(   "R1_GND" 10k  )
R2_GND= desVar(   "R2_GND" 10k  )
Rslew = desVar(   "Rslew" 1000k )
Vbl   = desVar(   "Vbl" 1.5     )
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;RUN OPTIONS SET-UP;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;WARNING: may conflict with parametric runs!! ;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;; USER ACTION: enable/disable analysis ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
TRAN_NOISE=0
AC=1
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;PARAMETRIC RUN SET-UP;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;; USER ACTION: enable/disable and configure parametric runs ;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; PARAMETRIC ib1, ib2?  (type '0' to disable parametric run)
; (type '1' for parametric run with constant Rtrig)
; (type '2' for parametric run with constant Vtrigger
;baseline, dynamic Rtrig)
; PARAMETRIC Rslew  (type '3' for parametric RSLEW (parametric run of ib1,
;ib2 is disabled))
;
; PARAMETRIC Iin   (type '4' for parametric Iin (parametric run of Rslew,
;ib1, ib2 is disabled))
;
; PARAMETRIC Vbl   (type '5' for parametric Vbl (parametric run of Iin,
;Rslew, ib1, ib2 is disabled))
;
; PARAMETRIC Ctot   (type '6' for parametric Ctot (parametric run of Vbl,
;Iin, Rslew, ib1, ib2 is disabled))
; (type '9' for parametric Ctot for noise evaluation)
```

```
;
; PARAMETRIC Gain   (type '7' for parametric TIA gain (parametric run of
;Ctot, Vbl, Iin, Rslew, ib1, ib2 is disabled))
;
; type '8' for process corner sweep
;;;;;;;;;;;;;;;;;;;;;;
param=6;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
modelFile(
    '("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" "dio_t")
    '("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" "mos_tt")
    '("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" "bip_typ")
    '("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" "res_typ")
    '("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" "cap_typ")
    )
;; Idirac magnitude corresponds to Q = 2.Idirac.tn = 2.100m.1n, where tn=tr=tf=th
;;; Open results file (or create) in append mode:
pipe=outfile( resultsFile "a")
newline(pipe)
ocnPrint(?output pipe "\n***************************************************************")
ocnPrint(?output pipe "\n\t New set of data, generated " getCurrentTime())
ocnPrint(?output pipe "\n***************************************************************")
newline(pipe)
fprintf( pipe "\n\nDesign variables:")
newline(pipe)
fprintf(pipe "\n++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++\n")
newline(pipe)
fprintf(pipe "Nominal IB1, IB2  \n")
fprintf(pipe "R1_GND R2_GND \n")
foreach( var list(R1_GND R2_GND)
fprintf(pipe "%s\t" var)
)
newline(pipe)
fprintf(pipe "Rtrig Ctot Iin Cdirac Idirac \n")
foreach( var list(Rtrig Ctot Iin Cdirac Idirac)
fprintf(pipe "%s\t" var)
)
fprintf(pipe "\n\nInput stimulus detail (from spectre netlist):\n")
inpipe=infile(netlistfile)
gets(s inpipe) fprintf(pipe "Layout extraction ?: %s" s)
gets(s inpipe)
gets(s inpipe)
gets(s inpipe)
gets(s inpipe) fprintf(pipe "%s" s)
gets(s inpipe) fprintf(pipe "%s" s)
gets(s inpipe) fprintf(pipe "%s" s)
gets(s inpipe) fprintf(pipe "%s" s)
gets(s inpipe) fprintf(pipe "%s" s)
close(inpipe)
fprintf(pipe "\n+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++\n")
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; run only if parametric analysis is not enabled
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
unless( (param!=0)
fprintf( pipe "\n\n\n1. Device contribution for total output rms noise voltage
(for each node)\n\n")
;; noise analysis for Vtrigger, delete results, noise analysis for Vout:
analysis('noise ?start "10"  ?stop "10G"  ?p "/Vtrigger"
              ?n "/agnd" )
temp( 27 )
```

```
run()
VnormsTrigger=rmsNoise(10 10G)
fprintf( pipe "\n1.1. Noise summary for Vtrigger node\n\n")
noiseSummary('integrated ?output pipe ?noiseUnit "V" ?truncateData 15
?truncateType 'top ?from 10 ?to 10G ?deviceType 'all)
delete( 'analysis 'noise)
analysis('noise ?start "10"  ?stop "10G"  ?p "/Vout"
               ?n "/agnd" )
run()
VnormsOut=rmsNoise(10 10G)
newline(pipe)
fprintf( pipe "\n\n1.2. Noise summary for Vout node\n\n")
noiseSummary('integrated ?output pipe ?noiseUnit "V" ?truncateData 15
?truncateType 'top ?from 10 ?to 10G ?deviceType 'all)
)
unless( (AC!=1)
analysis('ac ?start "1"  ?stop "10G"  )
)
unless(       (TRAN_NOISE != 1 )
analysis('tran ?stop "300n"  ?errpreset "conservative"  ?tranNoise "Transient Noise"
               ?noiseseed "1"  ?noisefmax "1G"  ?noisescale "1"  ?noisefmin "1k"
               ?noisetmin "100p"  ?tranNoiseMultiRuns "Multiple Runs"  ?noiseruns "2"  )
)
unless( (param==9)
analysis('tran ?stop "300n"  ?errpreset "conservative"  )
analysis('dc ?saveOppoint t  )
save( 'i "/I20/I3/NM3/D" "/I20/I0/NM6/D" "/I20/I2/PM8/S" "/I20/I2/Runit<1>/MINUS"
"/Iout/PLUS" "/Rtrig/PLUS" "/Iin/PLUS" "/I20/I0/PM6/D" "/I20/I0/PM5/S" "/I20/I0/PM12/S"
 "/I20/I0/NM10/D")
save( 'v "/Vtrigger" )
save( 'v "/Vout" )
)
unless( (param!=3)
paramAnalysis("Rslew" ?values '(1k 100k 10M))
paramRun()
)
unless( (param!=4)
paramAnalysis("Iin" ?values '(50u 250u 500u 750u 1m))
; for ToT, uncomment below
; paramAnalysis("Iin" ?values '(12.5u 55u 80u 150u 280u 550u 840u 1010u 1500u 2000u 2500u))
paramRun()
)
unless( (param!=5)
paramAnalysis("Vbl" ?values '(1 1.3 1.5 1.7 2.0))
analysis('dc ?saveOppoint t  ?param "Vbl"  ?start "1.0"
               ?stop "2.0"  )
paramRun()
)
unless( (param!=6)
paramAnalysis("Ctot" ?values '(35p 70p 150p 320p))
paramRun()
)
unless( (param!=0)
run()
)
unless( (param!=7)
paramAnalysis("double" ?values '(0 3.3)
paramAnalysis("half"   ?values '(0 3.3)))
paramRun()
)
unless( (param!=8)
```

```
;only transient analysis
newWindow()
addTitle( "Process Corner sweep")
foreach(capvar '("cap_max" "cap_min")
foreach(resvar '("res_max" "res_min")

foreach(mosvar '("mos_ss" "mos_ff" "mos_snfp" "mos_fnsp")
modelFile(
    '("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" "dio_t")
    list("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" mosvar)
    list("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" resvar)
    '("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" "bip_typ")
    list("/home/mrolo/umc/Models/Spectre/L130E_MM_HS_MAIN_V161_SG.lib" capvar)
    )
analysis('ac ?start "10"  ?stop "10G" ?dec "100")
analysis('tran ?stop "300n"  ?errpreset "conservative"  )
analysis('dc ?saveOppoint t  )
run()

selectResult( 'tran )
plot(getData("/Vout") getData("/Vtrigger")
?expr list( strcat("Vout [SHAPED] [MOS: " mosvar ", RES: " resvar ", CAP: " capvar "]")
    strcat("Vtrigger [FAST] [MOS: " mosvar ", RES: " resvar ", CAP: " capvar "]")
   ))
selectResult( 'ac )
plot(getData("/Zin") ?expr list( strcat("Zin (Ohm) [MOS: " mosvar ", RES: " resvar ",
CAP: " capvar "]")))
)
)
)

)
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; parametric IB1 and IB2, no changes in Rtrig
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
unless(       (param != 1 )
paramAnalysis("R1_GND" ?values '(5000 15000 )
   paramAnalysis("R2_GND" ?values '(5000 15000 )
   )
   )
paramRun()
selectResults( 'ac )
plot(getData("/Zin"))
selectResults( 'tran )
plot(getData("/Vtrigger"))
)
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; parametric IB1, with Rtrig changed dynamically to keep the baseline
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
unless(       (param != 2 )
val_ctrl=0 ;print control variable
R2_GND = list(5000 15000)
foreach( val2 R2_GND
desVar( "R2_GND" val2 )
R1_GND = list( 5000 15000 )
foreach( val1 R1_GND
desVar( "R1_GND" val1 )
Rtrig= expt(val1 1.48)*2.5m
desVar( "Rtrig" Rtrig)
a=resultsDir( sprintf( nil "/home/mrolo/projects/PETumc/1v0/
mrolo/Sim/Testbench_full/spectre/schematic/
```

```
demo/R1_GND=%d_R2_GND=%d" val1 val2) )
printf( "%L", a )
run()
;; noise analysis for Vtrigger, delete results, noise
analysis for Vout:
analysis('noise ?start "10"  ?stop "10G"  ?p "/Vtrigger"
                ?n "/agnd" )
temp( 27 )
run()
VnormsTrigger=rmsNoise(10 10G)
;;;;;;;;;;;;;;;; uncomment below for extended log
;fprintf( pipe "\n1.1.1 Noise summary for Vtrigger node ,
R1_GND = %d, R2_GND = %d\n\n" val1 val2)
;noiseSummary('integrated ?output pipe ?noiseUnit "V" ?truncateData 15
;?truncateType 'top ?from 10 ?to 10G ?deviceType 'all)
delete( 'analysis 'noise)
analysis('noise ?start "10"  ?stop "10G"  ?p "/Vout"
                ?n "/agnd" )
run()
VnormsOut=rmsNoise(10 10G)
;;;;;;;;;;;;;;;; uncomment below for extended log
;fprintf( pipe "\n\n1.2.1 Noise summary for Vout node ,
R1_GND = %d, R2_GND = %d\n\n" val1 val2)
;noiseSummary('integrated ?output pipe ?noiseUnit "V" ?truncateData 15
;?truncateType 'top ?from 10 ?to 10G ?deviceType 'all)
)
)
foreach( val1 R1_GND
openResults( sprintf( nil "/home/mrolo/projects/PETumc/1v0/
mrolo/Sim/Testbench_full/
spectre/schematic/demo/R1_GND=%d_R2_GND=%d" val1 val2) )
if(( val_ctrl==0) fprintf( pipe "\n\n\n Rtrig [R1_GND= %d] (Ohm) =
%4.0f \n\n\n" val1 Rtrig))
)
foreach( val1 R1_GND
   openResults( sprintf( nil "/home/mrolo/projects/PETumc/1v0/mrolo/Sim/
Testbench_full/spectre/schematic/demo/R1_GND=%d_R2_GND=%d" val1 val2) )
   selectResults( 'ac )
plot(getData("/Zin") ?expr list( strcat( "Zin (Ohm):
R1_GND= " sprintf(nil "%d" val1) ", R2_GND= " sprintf(nil "%d" val2) )))
   selectResults( 'tran )
plot(getData("/Vtrigger") ?expr list( strcat( "Vtrigger (V):
R1_GND= " sprintf(nil "%d" val1) ", R2_GND= " sprintf(nil "%d" val2))))
deriv=deriv(v("/Vtrigger" ?result "tran-tran"))
fprintf( pipe " \n \t Vnorms [Vout] (mV) [R1_GND= %d; R2_GND= %d] =
     %g \n" val1 val2 VnormsOut)
fprintf( pipe " \n \t Vnorms [Vtrigger] (mV) [R1_GND= %d; R2_GND= %d] =
 %g \n" val1 val2 VnormsTrigger)
)
)
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; Bias regulator internal - uncomment to plot results
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;newWindow()
;;selectResult( 'tran )
;;plot(getData("/I20/I0/PM12/S") getData("/I20/I0/PM5/S") getData("/I20/I0/net0151")
;;getData("/net32") getData("/I20/I0/net057") getData("/I20/I0/PM6/D")
;;?expr list("GM_output" "Islew" "IN-" "IN+" "Vout_1" "Ic(=ID_PM6)"))
;;addTitle( "Bias Regulator internal: current and voltage outputs from NL Buffer,
;;output of differential pair")
;;unless( (param!=5)
```

```
;; selectResult( 'tran)
;; newWindow()
;; plot(getData("/I20/I0/PM12/S") getData("/I20/I0/NM10/D") ?expr list("Gm_Iout" "Ibias_IN+"))
;; selectResult( 'dc )
;; plot(getData("/I20/I0/PM12/S") getData("/I20/I0/NM10/D") ?expr list("Gm_Iout" "Ibias_IN+"))
;; )
;;newWindow()
;;selectResult( 'tran)
;;plot(getData("/I20/I2/net221") getData("/I20/I2/PM8/S") getData("/I20/I2/Runit<1>/MINUS")
;;getData("/I20/net25") ?expr list("Vx_TIA" "I_TIA" "I_RF" "DC2.5"))

;;newWindow()
;;selectResult( 'tran)
;;plot(getData("/I20/I0/NM6/D") getData("/I20/I3/NM3/D") getData("/R5"))
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
newWindow()
selectResult( 'tran )
plot(getData("/Vtrigger") ?expr list("Vtrigger (V)"))
deriv=deriv(v("/Vtrigger" ?result "tran-tran"))
plot( deriv ?expr '( "deriv(Vtrigger) (V.s-1)" ) )
addTitle( "FAST output (voltage waveform and absolute value of slope)")
newWindow()
selectResult( 'tran )
plot(getData("/Vout") getData("/Vtrigger") getData("/Iin/PLUS")
?expr list("Vout [SHAPED] (V)" "Vtrigger [FAST] (V)" "Iin [e- collected at
the amplifier input] (A)"))
addTitle("Transient input current and output voltages")
;;print to screen
printf(" \n \n \n \n \t Vnorms [Vout] =     %f" VnormsOut)
printf(" \n \n \t Vnorms [Vtrigger] = %f \n \n \n \n" VnormsTrigger)
;;print to output file "*ROLO_file"
ocnPrint(?output pipe "PLEASE NOTE: THE BELOW ANALYSIS (2 and 4) IS ONLY MEANINGFUL FOR
SIPM_DIRAC INPUT STIMULUS")
ocnPrint(?output pipe "2. Measure of the slope of Vtrigger within the 1st nanosecond:" )
ocnPrint(?output pipe deriv(v("/Vtrigger" ?result "tran-tran"))
?from 50.5n ?to 51n ?step 0.25n )
newline(pipe)
ocnPrint(?output pipe "3. Integrated noise 10-10G Hz: (for nominal values of IB1, IB2)" )
ocnPrint(?output pipe "   Vnorms [Vout] (V) = " VnormsOut ?precision 3)
ocnPrint(?output pipe "   Vnorms [Vtrigger] (V) = " VnormsTrigger ?precision 3)
newline(pipe)
ocnPrint(?output pipe "4. With DELTA being the electronics noise contribution to the time
resolution error, where \n\n   DELTA (s) =   Vnorms/slope: \n\n   For the fast output
Vtrigger, with the slope measured at 51.0 ns, this contribution is: \n")
slope=value(deriv(v("/Vtrigger" ?result "tran-tran")) 51n   )
deltaTrigger=VnormsTrigger/slope
ocnPrint(?output pipe "   DELTA (s) = " deltaTrigger ?precision 3)
unless( (AC!=1)
newWindow()
v\ \/Vtrigger\;\ ac\ dB20\(V\) = db(v("/Vtrigger" ?result "ac")) plot( v\ \/Vtrigger\;
\ ac\ dB20\(V\) ?expr '( "FAST(V/A) = 20log(Vtrigger[V]/Iin[A])" ) )
v\ \/Vout\;\ ac\ dB20\(V\) = db(v("/Vout" ?result "ac")) plot( v\ \/Vout\;
\ ac\ dB20\(V\) ?expr '( "SHAPED(V/A) = 20log(Vout[V]/Iin[A])" ) )
addTitle( "Frequency response of the transimpedance functions FAST and SHAPED [db20],
Input impedance")
addSubwindow()
selectResult( 'ac )
plot(getData("/Zin") ?expr list("Zin (Ohm)"))
ocnPrint(?output pipe "5. BW measurement for Vtrigger TF:")
BW=bandwidth( v( "/Vtrigger" ) 3 "low")
ocnPrint(?output pipe " BW [FAST] (Hz) = " BW ?precision 3)
```

```
ocnPrint(?output pipe "6. Zin @10kHz (real):")
ZIN=real(value(v("/Zin") 10000))
ocnPrint(?output pipe " |ZIN| (Ohm) = " ZIN ?precision 3)
close(pipe)
)
unless( (AC!=0)
ocnPrint(?output pipe "5. BW measurement for Vtrigger TF: ERROR! AC analysis results
not available!")
ocnPrint(?output pipe " BW [FAST] (Hz) =  ERROR! AC analysis results not available!")
ocnPrint(?output pipe "6. Zin @10kHz (real):  ERROR! AC analysis results not available!")
ocnPrint(?output pipe " |ZIN| (Ohm) =   ERROR! AC analysis results not available!" )
close(pipe)
)
;;ToT 2.5 p.e.
plot((cross(v("/Vout" ?result "tran-tran") 1.55 1 "falling" nil nil) -
cross(v("/Vout" ?result "tran-tran") 1.55 1 "rising" nil nil)))
plot((cross(v("/Vtrigger" ?result "tran-tran") 1.19 1 "falling" nil nil) -
cross(v("/Vtrigger" ?result "tran-tran") 1.19 1 "rising" nil nil)))
;;ToT 0.5p.e.
plot((cross(v("/Vout" ?result "tran-tran") 1.51 1 "falling" nil nil) -
cross(v("/Vout" ?result "tran-tran") 1.51 1 "rising" nil nil)))
plot((cross(v("/Vtrigger" ?result "tran-tran") 1.09 1 "falling" nil nil) -
cross(v("/Vtrigger" ?result "tran-tran") 1.09 1 "rising" nil nil)))
```

Below, an sample version of the text output generated. Where necessary, extra lines were removed and the text was formatted in order to comply with the line width of the present document.

```
*********************************************************************************
 New set of data, generated  Oct  1 12:12:28 2010
*********************************************************************************
Design variables:
+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Nominal IB1, IB2
R1_GND R2_GND
10000 10000
Rtrig Ctot Iin Idirac
2000 7e-11 0.00055 0.05

Input stimulus detail (from spectre netlist):
Layout extraction ?: // CALIBRE EXTRACTED NETLIST R+C+CC without IOPAD
// Library name: PETumc_mr
// Cell name: SiPM_Dirac
// View name: schematic
subckt SiPM_model Id agnd
    I0 (agnd Id) isource mag=1 type=pulse val0=0.0 val1=-Idirac delay=50n \

+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

1. Device contribution for total output rms noise voltage (for each node)

1.1. Noise summary for Vtrigger node

Device            Param    Noise Contribution    % Of Total

I20.I1.MNM2       id       0.000669674           8.66
I20.I1.MNM2\@2    id       0.000668847           8.63
I20.I3.MNM8\@2    fn       0.00044017            3.74
I20.I3.MNM8       fn       0.000440169           3.74
/R1_GND           rn       0.000439787           3.73
I20.I3.MNM8       id       0.00028598            1.58
I20.I3.MNM8\@2    id       0.00028598            1.58
I20.I1.MPM0       id       0.000270452           1.41
I20.I1.MPM0\@2    id       0.000270403           1.41
/R2_GND           rn       0.000259992           1.30
I20.I3.MNM6       id       0.000236659           1.08
I20.I3.MNM6\@2    id       0.000236658           1.08
I20.I1.MNM3       id       0.0002337             1.05
I20.I1.MNM3\@2    id       0.000233185           1.05
I20.I1.MNM3\@3    id       0.000232698           1.05

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.00227614
No input referred noise available
The above noise summary info is for noise-noise data

1.2. Noise summary for Vout node

Device            Param    Noise Contribution    % Of Total

I20.I3.MNM3       id       0.000744547           5.88
I20.I3.MNM3\@2    id       0.000744545           5.88
I20.I3.MNM2       id       0.00074176            5.84
```

```
I20.I3.MNM2\@2    id       0.000741758          5.84
/R1_GND           rn       0.000620881          4.09
I20.I0.MNM8       id       0.000550183          3.21
I20.I0.MNM8\@2    id       0.000550183          3.21
I20.I0.MNM8\@3    id       0.000550183          3.21
I20.I0.MNM8\@4    id       0.000550182          3.21
I20.I3.MNM8       id       0.000404509          1.74
I20.I3.MNM8\@2    id       0.000404509          1.74
I20.I0.MNM9\@5    id       0.000379917          1.53
I20.I0.MNM9\@8    id       0.000379917          1.53
I20.I0.MNM9\@6    id       0.000379917          1.53
I20.I0.MNM9\@7    id       0.000379917          1.53

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.00306942
No input referred noise available
The above noise summary info is for noise-noise data

PLEASE NOTE: THE BELOW ANALYSIS IS ONLY MEANINGFUL FOR SIPM_DIRAC INPUT STIMULUS

2. Measure of the slope of Vtrigger within the 1st nanosecond:

time (s)          deriv(v("/Vtrigger" ?resultsDir "/home/mrolo/projects/
PETumc/1v0/mrolo/Sim/Testbench_full_EXTRACTED/spectre/schematic" ?result "tran"))

   50.5n              1.45719G
   50.75n             2.7255G
   51n                2.80757G

3. Integrated noise 10-10G Hz: (for nominal values of IB1, IB2)

   Vnorms [Vout] (V) =  3.07m

   Vnorms [Vtrigger] (V) =  2.28m

PLEASE NOTE: the below analysis regarding the metric 'DELTA' is
only meaningful for SiPM_dirac input stimulus

4. With DELTA being the electronics noise contribution to the time
resolution error, where

   DELTA (s) =   Vnorms/slope:

   For the fast output Vtrigger, with the slope measured at 51.0 ns,
   this contribution is:

   DELTA (s) =  811f

5. BW measurement for Vtrigger TF:

 BW [FAST] (Hz) =  60.5M

6. Zin @10kHz (real):

 |ZIN| (Ohm) =  5.26
```

A.2 Extracted Netlist

The below netlist is used for parametric studies after parasitic extraction. Optionally, the effect of the I/O pad model can be suppressed in order to increase the simulation speed. The schematic netlist was first extracted from the schematic view using the ADE (Virtuoso ®Analog Design Environment L). After the post-layout netlists are created, their inclusion is done as indicated below. *SiPM_Dirac* and *SiPM_Model* are used as inputs for a Dirac delta pulse or a more realistic LYSO+SiPM signal.

```
// CALIBRE EXTRACTED NETLIST R+C+CC without IOPAD (change according to selection)

// End of subcircuit definition.

// Library name: PETumc_mr
// Cell name: SiPM_Dirac
// View name: schematic
subckt SiPM_model Id agnd
    I0 (agnd Id) isource mag=1 type=pulse val0=0.0 val1=-Idirac delay=50n \
rise=50p fall=50p width=50p
    C0 (Id agnd) capacitor c=Ctot
ends SiPM_model
// End of subcircuit

// Library name: PETumc_mr
// Cell name: SiPM_model
// View name: schematic
//subckt SiPM_model Id agnd
//   C0 (Id agnd) capacitor c=Ctot
//    I1 (agnd Id) isource mag=1 type=exp val0=0.0 val1=-Iin td1=50n tau1=1n \
//        td2=51n tau2=40n
//ends SiPM_model

// Library name: PETumc_mr
// Cell name: IO
// View name: schematic
subckt IO IOPAD PCB agnd
    C0 (net8 agnd) capacitor c=650f
    C1 (IOPAD agnd) capacitor c=2p
    L2 (net18 net8) inductor l=1.5n
    L1 (net8 net10) inductor l=1.5n
    L0 (net16 IOPAD) inductor l=5n
    R1 (net10 net14) resistor r=12.5m
    R2 (net14 net16) resistor r=250m
    R0 (PCB net18) resistor r=12.5m
ends IO
// End of subcircuit definition.

// Library name: PETumc_mr
// Cell name: Irefgen
// View name: schematic
//subckt Irefgen IB1 IB2 IB3 IB4 IB5 R1 R2 R3 R4 R5 pgnd pvdd
include "Irefgen.pex.netlist"

// Library name: PETumc_mr
// Cell name: FeedbackTIA
// View name: schematic
```

```
//subckt FeedbackTIA Iref TIA_Iin TIA_Vout agnd avdd double half
// End of subcircuit definition.
include "FeedbackTIA.pex.netlist"

// Library name: PETumc_mr
// Cell name: PreAmplifier
// View name: schematic
// End of subcircuit definition.
include "PreAmplifier.pex.netlist"

// Library name: PETumc_mr
// Cell name: BiasRegulator
// View name: schematic
//subckt BiasRegulator IB4 IB5 Islew\+ Islew\- Vbaseline agnd avdd vo_TIA \
//        vo_regulated
// End of subcircuit definition.
include "BiasRegulator.pex.netlist"

// Library name: PETumc_mr
// Cell name: Full_channel
// View name: schematic
subckt Full_channel _net0 Itrig R1 R2 R3 R4 R5 RslewM RslewP _net1 Vout \
        agnd avdd boost double half
    C1 (net055 avdd) capacitor c=0
    C0 (net057 avdd) capacitor c=0
    I3 (net057 net055 net053 net091 net049 R1 R2 R3 R4 R5 agnd avdd) \
        Irefgen
    I2 (net053 net25 Vout agnd avdd double half) FeedbackTIA
    I1 (net057 net055 _net0 net25 Itrig agnd avdd boost) PreAmplifier
    I0 (net091 net049 RslewP RslewM _net1 agnd avdd Vout net25) \
        BiasRegulator
ends Full_channel
// End of subcircuit definition.
// without IOPAD
// Library name: PETumc_mr_sim
// Cell name: Testbench_full
// View name: schematic
//V3 (net036 agnd) vsource type=pulse delay=5n edgetype=linear val0=0 \
// val1=-20mV period=50n rise=2n fall=10n width=2n fundname="100M"
//I0 (Zin 0) SiPM_model
//C7 (net036 agnd) capacitor c=100f
//C0 (Vout 0) capacitor c=0
//I20 (net086 Vtrigger R1 R2 R3 R4 R5 net35 net34 net31 net32 agnd net33 \
// Vboost Vdouble Vhalf) Full_channel
////I20 (net086 Vtrigger R1 R2 R3 R4 R5 net35 net34 net31 net32 agnd net33 \
//// agnd agnd agnd) Full_channel
//_inst0 (Zin net086) resistor r=0
//Iout (net32 Vout) resistor r=0
//_inst1 (Vtrigger agnd) resistor r=Rtrig
//R3_GND (R3 agnd) resistor r=10K
//R4_GND (R4 agnd) resistor r=8K
//R5_GND (R5 agnd) resistor r=15K
//R9 (net34 net35) resistor r=Rslew
//_inst2 (R1 agnd) resistor r=R1_GND
//_inst3 (R2 agnd) resistor r=R2_GND
//V2 (net31 agnd) vsource dc=Vbl type=dc
//V1 (agnd 0) vsource dc=0 type=dc
//V0 (net33 agnd) vsource dc=3.3 type=dc
////ROLO: added VDC sources for gain trimming and boost: (3 lines)
//V99 (Vdouble agnd) vsource dc=double type=dc
//V98 (Vhalf agnd) vsource dc=half type=dc
```

```
//V97 (Vboost agnd) vsource dc=boost type=dc

// with IOPAD
// Library name: PETumc_mr_sim
// Cell name: Testbench_full
// View name: schematic
I24 (VtriggerA Vtrigger 0) IO
I23 (Vout net062 0) IO
I22 (net034 Zin 0) IO
V3 (net036 agnd) vsource type=pulse delay=5n edgetype=linear val0=0 \
val1=-20mV period=50n rise=2n fall=10n width=2n fundname="100M"
I0 (Zin 0) SiPM_model
C0 (Vout 0) capacitor c=0
C7 (net036 agnd) capacitor c=100f
I20 (net086 VtriggerA R1 R2 R3 R4 R5 net35 net34 net31 net32 agnd net33 \
agnd agnd agnd) Full_channel
_inst0 (net034 net086) resistor r=0
Iout (net32 net062) resistor r=0
_inst1 (Vtrigger agnd) resistor r=Rtrig
R3_GND (R3 agnd) resistor r=10K
R4_GND (R4 agnd) resistor r=8K
R5_GND (R5 agnd) resistor r=15K
R9 (net34 net35) resistor r=Rslew
_inst2 (R1 agnd) resistor r=R1_GND
_inst3 (R2 agnd) resistor r=R2_GND
V2 (net31 agnd) vsource dc=Vbl type=dc
V1 (agnd 0) vsource dc=0 type=dc
V0 (net33 agnd) vsource dc=3.3 type=dc
//ROLO: added VDC sources for gain trimming and boost: (3 lines)
V99 (Vdouble agnd) vsource dc=double type=dc
V98 (Vhalf agnd) vsource dc=half type=dc
V97 (Vboost agnd) vsource dc=boost type=dc
```

A.3 Pre-Amplifier Biasing Control

The operation point of the *PreAmplifier* can be trimmed by adjustment of the currents IB1 and IB2. Although the aim is to affect, respectively, the transconductance of the input (M1) and regulation (M2) transistors, and hence to specifically control the input referred noise and input impedance, the operation point of the input stage is dependent of such parameters. Table A.1 summarizes the relevant operating point parameters (extracted by simulation after layout parasitic extraction) of the input (M1) and regulation (M2) transistors, and defines the correspondance between IBx and Rx_GND.

[Regulation transistor] /I20/I1/M2			
$R2\_GND(\Omega)$	$5K$	$10K$	$15K$
$R1\_GND(\Omega)$		$5K$	
ids	2.45611m	940.11u	571.425u
vgs	660.187m	586.014m	555.51m
vds	1.60077	1.50658	1.46717
vdsat	163.316m	112.868m	95.0906m
gm	26.1242m	14.1941m	9.77015m
gds	284.623u	149.123u	102.132u
$R1\_GND(\Omega)$		$10K$	
ids	2.46476m	943.043u	573.179u
vgs	661.917m	587.545m	556.992m
vds	1.47421	1.38194	1.34386
vdsat	163.869m	113.235m	95.3881m
gm	26.1393m	14.2156m	9.78988m
gds	293.246u	152.861u	104.537u
$R1\_GND(\Omega)$		$15K$	
ids	2.46762m	944.037u	573.781u
vgs	662.518m	588.085m	557.519m
vds	1.43059	1.3384	1.30039
vdsat	164.064m	113.367m	95.496m
gm	26.1423m	14.2221m	9.79628m
gds	296.692u	154.37u	105.515u

[Input transistor] /I20/I1/M1			
$R2\_GND(\Omega)$	$5K$	$10K$	$15K$
$R1\_GND(\Omega)$		$5K$	
ids	1.51943m	1.49809m	1.48408m
vgs	940.585m	920.569m	911.655m
vds	1.64832	1.72542	1.75786
vdsat	242.813m	240.713m	239.482m
gm	9.8798m	9.84378m	9.81495m
gds	134.929u	129.788u	127.531u
$R1\_GND(\Omega)$		$10K$	
ids	506.863u	505.117u	504.233u
vgs	812.298m	794.398m	786.873m
vds	1.82067	1.89545	1.92621
vdsat	152.725m	152.16m	151.908m
gm	5.82989m	5.82445m	5.82103m
gds	69.2023u	67.5517u	66.882u
$R1\_GND(\Omega)$		$15K$	
ids	289.758u	288.965u	288.585u
vgs	768.068m	750.316m	742.87m
vds	1.87905	1.95374	1.98443
vdsat	122.771m	122.367m	122.192m
gm	4.10682m	4.10148m	4.09869m
gds	47.4225u	46.382u	45.961u

Table A.1: DC Operating point of the RGC stage: parametric IB1 and IB2.