Universidade de Aveiro
2023

Inês Alexandra
Ventura Pinto

Funções Analógicas Configuráveis

Configurable Analog Functions

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"*Being brave means knowing that when you fail, you do not fail forever*"

— Elizabeth Grant

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações, realizada sob a orientação científica do Doutor Telmo Reis Cunha, Professor associado do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro.

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Palavras Chave

Funções analógicas, Processamento analógico de sinal, Pré-distorção, Amplificadores de potência, Funções reconfiguráveis.

Resumo

Nas últimas décadas, as implementações digitais têm dominado amplamente a área de telecomunicações, especialmente no que diz respeito ao processamento de sinal. No entanto, a tendência atual para aumentar substancialmente a largura de banda dos sinais envolvidos e reduzir consideravelmente a potência dissipada pelos dispositivos, salienta as limitações da tecnologia digital para uma gama considerável de aplicações. Assim, recentemente, surgiu a necessidade de implementar funções de forma analógica, uma vez que estas não requerem um processo de amostragem dos sinais e são potencialmente capazes de operar com menor consumo de energia e maior largura de banda. Esta dissertação apresenta uma visão detalhada do funcionamento de células de processamento analógico. São explicados os vários elementos que formam o circuito e o seu impacto no desempenho global. De seguida, aplica-se um sinal de entrada a ambas as células e analisa-se tanto o sinal de saída como a configurabilidade da célula, determinada por vários pontos de tensão configuráveis no próprio circuito. Finalmente, é dada atenção às características da largura de banda das células, uma métrica crucial para avaliar o seu desempenho.

Keywords

Analog functions, Analog signal processing, Predistortion, Power amplifiers, Reconfigurable functions.

Abstract

In the past few decades, digital implementations have exerted significant influence in the field of telecommunications, especially when it comes to signal processing. However, the current drive to increase very significantly the bandwidth of the signals involved, and to considerably reduce the power dissipated by the devices, highlights the limitations of digital technology for a considerable range of applications. Thus, recently the need has arisen to implement functions in analog form, since they do not require a sampling process of the signals, and are potentially able to perform with lower power consumption and higher bandwidth. This dissertation presents a detailed overview of the operation of analog processing cells. The various elements that form the circuit and their impact on overall performance are explained. Then, an input signal is applied to both cells and both the output signal and the configurability of the cell, determined by various configurable voltage points in the circuit itself, are analysed. Finally, attention is paid to the bandwidth characteristics of the cells, a crucial metric for evaluating their performance.

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Glossary

PA	Power Amplifier
DAC	Digital-To-Analog Converter
ADC	Analog-To-Digital Converter
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
BJT	Bipolar Junction Transistor
IC	Integrated Circuit
ANN	Artificial Neural Networks
PCB	Printed Circuit Board
DC	Direct Current
PAPR	peak to average power ratio
DPD	Digital Predistortion
APD	Analog Predistortion
RF	Radio Frequency
OpAmp	Operational Amplifier
ReLU	rectified linear unit
USB	Universal Serial Bus
SoC	system-on-chip

CHAPTER 1

Introduction

In today's digitally-driven society, we find ourselves in need of a relentless demand for faster and more efficient internet connectivity, fueled by the increase in vast quantities of information being globally broadcasted. Whether it is a 4K video streaming the latest news in crystal clear resolution, or a soccer game being live-streamed in real time to audiences around the world, the requirements for data transmission are in a constant state of evolution and expansion.

1.1 Motivation And Context

In this fast-paced environment, the number of bits being transmitted is exponentially increasing, resulting in a corresponding rise in the bandwidth needed to effectively carry these data. As the bandwidth of these signals escalates, so does the sampling frequency of digital processing, as well as the clock frequency of these processors, which further amplifies their power consumption.

Having this in mind, this dissertation endeavors to illuminate the development of configurable analog circuits that strike a balance between low power consumption and considerable bandwidth. Over the years, several research groups have been exploring analog processing techniques, particularly for Power Amplifier (PA) predistortion applications. However, these typically involve manipulating electronic circuits to emulate predefined mathematical functions, such as polynomials - an approach rooted to the preservation of the demonstrated mathematical properties of these functions.

This dissertation, however, treads a different path. It harnesses the inherent behavior of simple electronic components as the foundational building blocks for more sophisticated transfer functions. This innovative approach not only curtails circuit complexity but also extends its applicability across a wide range of scenarios. Moreover, the simplicity of these circuits paves the way for achieving high operational bandwidth, a key factor to meet the

increasing demands for rapid and efficient data transmission.

This dissertation begins with a concise review of the current state-of-the-art, underlining the crucial role of linearization for achieving optimal spectral efficiency. A variety of techniques for power amplifier linearization will be discussed, including feedforward linearization, feedback linearization, digital predistortion, and analog predistortion. Furthermore, the work dives into the use of neural networks in the context of non-linear modulation, highlighting the crucial role played by the activation functions of individual neurons in the overall accuracy of these networks. Subsequently, the philosophy underlying the configurable analog circuit will be explained, through the dissection of the circuit into blocks, to better understand it.

It is important to mention that in the scope of a research grant, my classmate Vitória Cruz along with Professor Telmo Cunha had started the developement on an earlier prototype of an analog circuit that was intended to be configured through control voltages set by Digital-To-Analog Converters (DACs).

1.2 Objectives

The objective of this work was the design, implementation, and testing of an analog configurable circuit capable of producing a wide range of input-output static transfer functions. This circuit serves as an analog signal processing unit and finds its primary application in the linearization of power amplifiers as a baseband predistorter.

Building upon prior developments of an earlier prototype, the goal of this work was to create a robust analog circuit that offers a high level of configurability while maintaining a wide operating bandwidth and low power consumption.

In addition, one of the specific objectives was to enable the circuit's output to be altered based on configurable voltages applied to the circuit. These voltages are controlled by a microcontroller operating with latch-enabled DACs.

1.3 Document Structure

This report is divided into five chapters:

Chapter 1 This dissertation begins with a brief introduction about the role of digital processing in the current era and the emerging need for analog processing due to the information surge. It also outlines the general objectives of this work.

Chapter 2 The second chapter presents a concise review of the current state-of-the-art, underlining the crucial role of linearization for achieving optimal spectral efficiency.

Chapter 3 The devised analog circuit is dissected in detail, dividing it into sections to help convey the philosophy behind it.

Chapter 4 In Chapter 4, the output of the Prototype of a Multi-cell Analog Processing Unit and the frequency response are analyzed.

Chapter 5 In the final chapter, conclusions are drawn about the entire work and some suggestions for future work are made.

CHAPTER 2

The Role of Analog Processing in Power Amplifier Linearization

Innovation has fundamentally reshaped our approach to telecommunications. Currently, advancements in digital communication technologies enable the transmission of substantial amounts of information at high data rates. This shift is especially prevalent in the wireless communications industry, where the primary objective is the efficient dissemination of vast data to a broad user base. Technological advancements in data transmission are rapidly evolving to accommodate the mounting demands for information exchange. However, as the available frequency for data transmission is finite, digital modulation methods are growing increasingly intricate to optimise the capacity of information conveyed within these constraints. This surge in information flow has spurred an unparalleled requirement for PA of high linearity. This level of linearity is vital to ensure a spectrally efficient conveyance of information, making it a critical factor in our data-driven society[1]. Spectrally efficient signals are signals that contain a lot of information in a limited frequency space. These are particularly susceptible to the generation of out-of-band spurious emissions, also referred to as "spectral regrowth"[2]. The ratio of peak to average power ratio (PAPR) can be very high (10 dB or greater) [3], which means that the linearity of the amplifier is a major concern. To maintain signal quality, the output power of the amplifier can be reduced in exchange for better linearity, however, PAs operate with the highest efficiency when they are close to their maximum power.

When PAs operate at high power levels, they can experience non-linear distortion which degrades the quality of the signal. To avoid this, linearization techniques are used to reduce the distortion caused by non-linearities, which leads to better efficiency and signal quality. By using linearization techniques, PAs can operate more efficiently. Therefore, linearization is an important technique to improve the performance of PAs in wireless communication systems [3][4]. There are various methods to achieve PA linearization, such as feed-forward linearization, feedback linearization, digital predistortion, analog predistortion.

Feed-forward Linearization was invented by Howard Black at Bell Telephone Laboratories.

He was working at Bell Telephone Laboratories at the time and was trying to reduce distortion in multiplexed telephone systems, in which voice-modulated carriers are transmitted on a single telephone cable. Due to the requirement of several amplifiers for long distances, the distortion from each amplifier adds up making this a huge problem for signal quality [5].

The concept, as depicted in Figure 2.1, involves comparing a scaled version of the PA output with the input signal, resulting in an error signal that theoretically consists solely of the PAs nonlinear distortion components. This error signal is then amplified using an auxiliary (highly linear) PA and subtracted from the main PAs output to eliminate the PAs nonlinear distortion while preserving the desired linear signal. Consequently, the feed-forward arrangement generates a linear replica of the input signal [6][3].

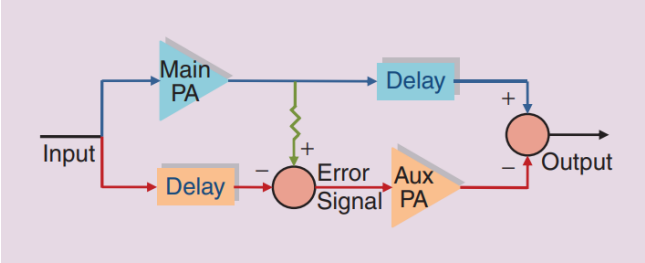


Figure 2.1: Feed-forward linearizer technique (retrieved from [6]).

Theoretically, the operation of feed-forward linearization should counteract nonlinearity and distortion. However, the process is complex and involves stringent requirements. It demands a pair of amplifiers that not only need to be perfectly matched but also must exhibit very linear behavior to prevent introducing distortion autonomously. It is critical to maintain stability in the components' values, especially when the circuit is comparing two nearly identical signals. Furthermore, feed-forward lacks an inherent self-regulating feature present in feedback systems. It cannot compensate for shifts in component values caused by external factors like temperature changes, aging, or supply voltage fluctuations. As a result, the effectiveness of conventional feed-forward systems tends to diminish rapidly under changing environmental conditions [7]. Moreover, the linearization process is complicated, because the system's efficiency faces limitations due to the involvement of amplifiers, mixers, attenuators, and phase-shifters, leading to potential power losses. Thus, despite its apparently simple nature, feed-forward implementation presents significant challenges due to its high component tolerance requirements and the complexity of maintaining system stability [8].

In 1927, Harold Stephen Black introduced the pioneering concept of feedback linearization, revolutionising the field of amplifiers. Figure 2.2 shows a simplified feedback diagram, this technique uses feedback to compare an attenuated version of the amplifier's output with the input signal. This process generates an error signal that is reinjected into the amplifier's input, effectively modifying its characteristics, including the gain. Black's vision of negative feedback amplification, in which the feedback was 180° out of phase, significantly reduced distortion, despite initially facing scepticism and patent rejection. The technique routes the system's output back to its input, neutralising non-linearities and guiding the system to mimic linear

behaviour. By applying advanced methods of linear system analysis and control to inherently non-linear systems, feedback linearization aims to improve system performance [3][6].

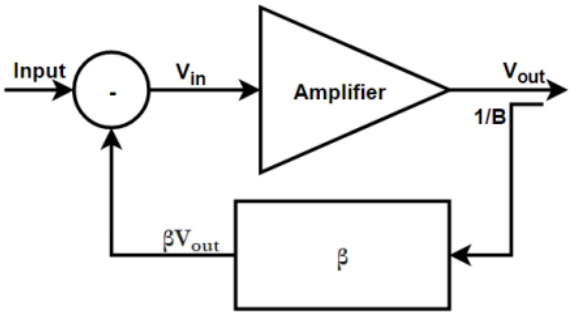


Figure 2.2: Simplified feedback linearizer technique (retrieved from [9]).

Power amplifier design is a prominent application of feedback linearization. This technique is used to boost the amplifier's linearity. Nevertheless, it does have its limitations. One of which arises in the form of instability concerns. The introduction of feedback linearization into a system can trigger unexpected dynamics. Oscillations or, as Black originally referred to as, "squealing", might emerge. These oscillations present a challenge to the system's operation, and if not adequately handled, could potentially lead to total system failure [3] [10]. Another constraint is the reduced efficacy of feedback linearization in systems operating at high frequencies or featuring wide bandwidths. With the increase in frequency, the phase shift within the feedback loop may become substantial. This shift could induce instability or decrease linearity. Moreover, maintaining uniform performance across extensive bandwidths proves to be a challenging task [11].

After discussing the feed-forward and feedback methods, it is crucial to examine another powerful approach to linearization: Predistortion. Predistortion serves as a fundamentally straightforward form of linearization for a power amplifier. It essentially entails the formation of a distortion characteristic that exactly counterbalances the distortion characteristic of the power amplifier itself. By doing so, it is possible to cancel out distortion and the output is ideally an amplified signal without distortion.

Most predistortion linearizes are implemented digitally [3], offering re-configurability capabilities and improved performance making it a practical solution for enhancing transmission quality and efficiency [12][13]. Digital Predistortion (DPD) is a technique that aims to linearize the overall system by compensating for the nonlinear effects of the PA. This is achieved by identifying an equivalent baseband model of the PA, which is ideally the exact inverse of the PAs equivalent baseband model. The identification process involves comparing a digitized part of the output signal to the reference input signal, and the extracted model is then used in real-time baseband processing of the input signal. By pre-compensating for the nonlinear effects of the PA, DPD can effectively linearize the system [12]. There are several methods to implement digital predistortion, one of which involves representing the amplifier as a polynomial function where each parameter can be adjusted in order to correct the non-linearities. The more terms there are, the greater the linearity of the system. However, this method presents a

problem: the complexity associated with the high number of parameters in the polynomial [14]. There are several problems associated with these implementations, and it is important to keep in mind that implementing DPD can be challenging due to the increasing need for wider bandwidth, which requires higher sampling rates and more complex software, even with its capacity to offer precise counteracting attributes, the application of this approach is restricted by the bandwidth of the DAC/Analog-To-Digital Converter (ADC) converters and also by the computational speed of the digital processor [13].

Furthermore, it is important to note that despite DPD being a highly effective and widely used linearization technique, we have reached a point where the contribution of baseband digital predistortion to the total power consumption of the system cannot be ignored, mainly in small cells [15]. Consequently, there is a need to implement new techniques that consume less power but still maintain good linearization capabilities [16]. An alternative that meets this requirement is Analog Predistortion (APD), which is particularly advantageous for large bandwidth applications due to its notable benefits such as cost-effectiveness, smaller footprint, and high bandwidth operation [13][3].

For instance, in applications like repeater systems, the unique characteristic of APD proves beneficial - it does not require baseband information. Repeater systems receive, amplify, and retransmit incoming Radio Frequency (RF) signals, making them a perfect fit for APD. These systems often employ high-power amplifiers to facilitate strong signal propagation. The ability of APD to directly process and correct frequency-modulated signals, without needing the original unmodulated signals, considerably simplifies the process and boosts the overall efficiency of the repeater systems[13].

It is evident that just like all the previously mentioned techniques, this one also has drawbacks, one of them being analog nonlinearities, particularly the limits between the smallest and largest signal the system can accurately process. To address this problem, one method that appears most suitable, due to the trade-off between performance and complexity, is the envelope memory polynomial [16]. This approach employs two techniques: i) Envelope Tracking, in which the amplifier's power supply is continually adjusted to track the input signal, and ii) the application of polynomials for the equation-based characterization of the amplifier. The use of Envelope Tracking can introduce memory into the system.This occurs because the non-linear behaviour of a PA is not solely due to the current amplitude value, but also to past amplitude values. The consideration of these memory effects in linearization began in the 1980s. These effects could be disregarded for applications with a narrower bandwidth, but as the bandwidth increased, memory effects started to be taken into account [3] [17].

Over the years, neural networks have emerged as an increasingly popular and effective methodology for modeling nonlinear systems [18]. Drawing inspiration from our brain, neural networks operate on a sophisticated network of nonlinear neurons that are adept at interpreting data and processing information. These networks are honed through the application of various learning algorithms such as backpropagation, feed-forward, and error calculation. A neural network is composed of numerous cells/nodes/neurons and layers, with each cell processing signals and feeding the output to the input of another neuron. These signals are associated

with a specific weight that designates its relative significance. Subsequently, the signals are processed through an activation function within the neuron to determine the output [19] [20]. There exists a range of activation functions, each with its own adequacy to the specific behaviors of the systems being modeled. They have the ability to approximate and process any given input function. Key examples include the sigmoid, hyperbolic tangent (tanh), and rectified linear unit (ReLU). These functions bring in the necessary non-linearity enabling neural networks to handle complex information. Without such activation functions, the output would merely be a linear transformation of the input. Each activation function places constraints on the output of each neuron. For example, the tanh function yields outputs between (-1,1), while the sigmoid function restricts outputs between (0,1). There are various ways to implement this network, one of which is using electronic components.

Finally, it is crucial to provide a practical example showcasing the application of the APD technique. What makes this approach particularly appealing is its remarkable practicality, as it facilitates seamless integration with a PA. The SC1887 it is a system-on-chip (SoC) solution, that plays a pivotal role in linearizing the final stages of power amplification within the transmitter chain. The SC1887 effectively implements the distortion correction function and applies it to the transmitted signal using solely analog signal processing circuits within the RF domain. This capability enables the chip to function efficiently across a broad frequency spectrum while maintaining low power consumption. In particular, the SC1887 has an input signal bandwidth of up to 10 MHz.

In this study, [21], the application of the SC1887 linearizer produced substantial benefits, including a reduction in amplifier distortion, enhanced power efficiency, and an increase in output power.

CHAPTER 3

Analog Processing Circuit

In the previous chapters, we explored the landscape of signal processing, noting the dominance of digital techniques and the emerging need for higher bandwidth and lower power consumption solutions. This led us to analog processing, a promising alternative that operates on continuous signals without the need for sampling. As we delve into Chapter 3, we will focus on the unique attributes of analog processing, particularly its ability to leverage the inherent behavior of electronic components. This approach offers the potential for reduced complexity and enhanced bandwidth. We will dissect the structure of the innovative circuit developed for this purpose, examining its neuron-like cells and base function parameters. Our journey will headlining the advantages of this novel approach, particularly its suitability for high bandwidth operation. Later on this chapter, we will contrast this approach with traditional analog processing techniques, highlighting the significant differences that make our method a groundbreaking contribution to the field.

An essential characteristic that sets analog processing apart from its digital counterpart is its continuous operation in time, free from the constraints of signal sampling. This continuous processing is a cornerstone of analog systems, allowing signals to flow and be manipulated in an uninterrupted stream. This feature is particularly crucial for high bandwidth operation. In digital systems, the bandwidth is often limited by the sampling rate according to the Nyquist-Shannon sampling theorem.

However, in analog processing, the bandwidth is primarily dependent on the electronic components and the implementation of the circuit, rather than any imposed sampling rate. This means that with careful design and selection of components, an analog system can achieve significantly higher bandwidths. The absence of sampling and the continuous nature of signal processing in analog systems can lead to more efficient utilization of bandwidth, opening the door to faster data transmission rates and more efficient communication systems. This makes analog processing a compelling choice for applications where high bandwidth and efficient operation are predominant.

To counterbalance the common approach of forcing electronic circuits to adhere to certain

mathematical models (such as polynomials) [2], it was necessary to find a basic non-linear function derived from the natural behavior of an electronic component to serve as the transfer function for the circuit.

Therefore, the current of a MOSFET, controlled by V_{GS}, was analyzed when the drain was loaded by a Bipolar Junction Transistor (BJT) current mirror, whose behavior, observed in the laboratory, is shown in3.1.

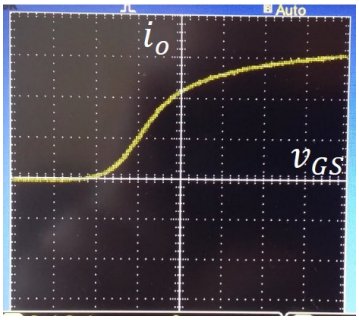


Figure 3.1: Drain current as a function of V_{GS} for a MOSFET

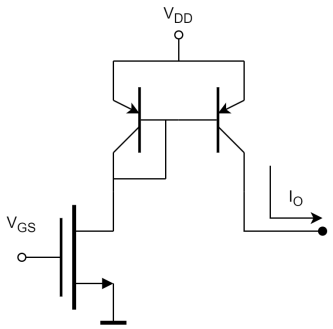


Figure 3.2: Schematic of the circuit: drain current as a function of V_{GS} for a MOSFET

In Figure 3.1, the current, which is controlled by the voltage V_{GS}, is depicted. Meanwhile, Figure 3.2 illustrates the schematic diagram of the circuit containing the MOSFET and the current mirror composed of BJTs.

Since the aim is to observe the current as a function of the V_{GS} voltage, it is crucial that this current varies solely due to changes in the gate voltage, as the source voltage is connected to the ground. In a MOSFET, the drain current I_D, although controlled by V_{GS}, can also be altered by variations in V_{DS}. The relationship between these variables is described by the characteristic functions of the MOSFET in three different operating regions: the cut-off region, the linear region, and the saturation region.

In the cut-off region, where $V_{GS} < V_{th}$, where V_{th} represents the threshold voltage, no current flows in the drain, ($I_D = 0$ A). When $V_{GS} > V_{th}$ and $V_{DS} < V_{GS}$ - V_{th}, the current I_D is given by (3.1) in this condition, the MOSFET operates in the linear region.

$$I_D \approx Kn'(\frac{W}{L})[(V_{GS} - Vth)V_{DS} - \frac{1}{2} * V_{DS}^2] \tag{3.1}$$

When $V_{GS} > V_{th}$ and $V_{DS} > V_{GS}$ - V_{th}, the MOSFET operates in the saturation zone and I_D is given by (3.2).

$$I_D \approx \frac{1}{2} * Kn'(\frac{W}{L}) * (V_{GS} - Vth)^2[1 + \lambda * V_{DS}] \tag{3.2}$$

Hence, it is possible to note that the current can be altered by the V_{DS} voltage in the linear region, where I_D increases linearly with V_{DS}, and in the saturation region, where the factor of multiplication (1+lambda*VDS) representes the channel modulation effect of the FET. In this circuit, the chosen MOSFET is the NEXPERIA NX7002AKW 115, which has a V_{th} ranging from 1.1V to 2.1V, with a typical value of 1.6V.

To ensure that the V_{DS} voltage did not alter the output function in the MOSFET, a current mirror made with BJT was used as the active load of the MOSFET, thus setting a fixed voltage at the drain [22].

It is crucial to note that the majority of contemporary Integrated Circuits (ICs) are designed to process voltage signals. This is largely due to the dominance of semiconductor technology that relies on MOSFETs, which are more suited to processing and amplifying voltage signals. However, within ICs, the voltage swing is constrained by the supply voltages provided to the IC. This implies that the range of values that the input or output voltage of an IC can assume is limited by the maximum and minimum values of the ICs supply voltages. To mitigate this effect, the processing of electrical currents is suitable for this case, given that the circuit will have multiple cells and adding or subtracting currents is trivial. Nonetheless, a voltage conversion may be required at the end of the circuit, or at certain internal points of the circuit.

These characteristics bear a resemblance to those of a sigmoid function in Artificial Neural Networks (ANN), as depicted in Figure 3.3.

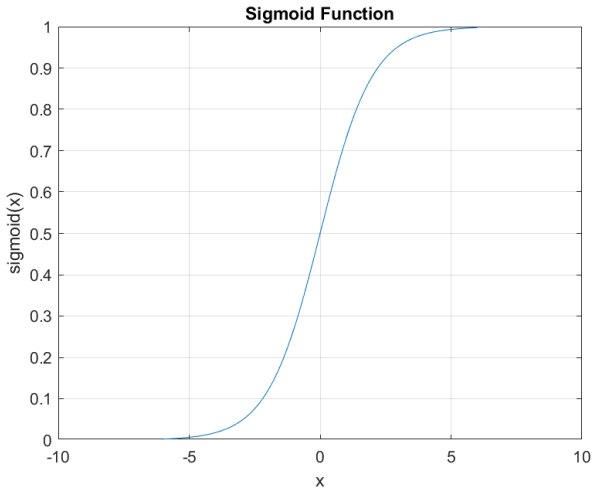


Figure 3.3: Sigmoid function

Therefore, capitalizing on the resemblance to the sigmoid function in ANN, it became clear that the same concept used in neural networks, where each neuron has an activation function for analog processing, could be replicated. Consequently, each cell represents a neuron in a

neural network, where the activation function is as follows:

$$I_o(V_i) = m * f(\alpha * V_i + \beta) + b \tag{3.3}$$

In this transfer function (3.3), the nonlinear function f(.) is the $I_o(V_{GS})$ characteristic of a selected MOSFET, and m, b, α, and β are the configurable parameters. By adjusting each of these parameters, it is possible to introduce various characteristics to the input-output characteristics of this basic cell circuit. The parameter α is responsible for introducing gain to the input signal, β introduces an offset to the signal, parameter m adds an output scaling factor, and b causes an offset to the output signal.

The initial concept for the circuit involved the use of two Operational Amplifiers (OpAmps) to configure the adjustable parameters (by means of a set of trimmers), as depicted in Figure 3.4. The output offset, not represented explicitly in this figure, is implemented through one of the parallel lines at the circuit output, which would contribute with a constant current to that node.

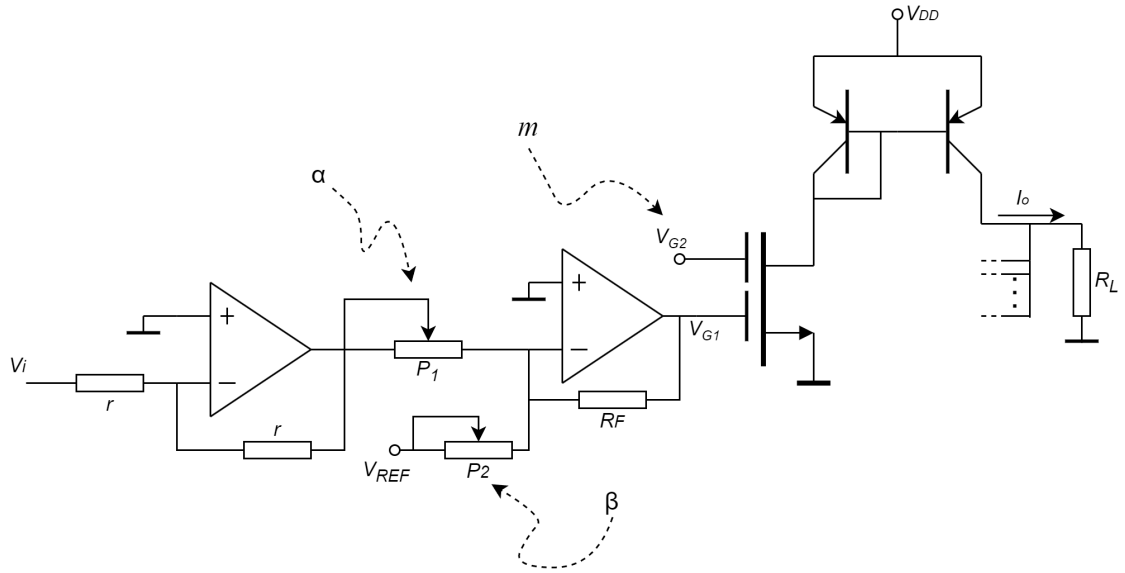


Figure 3.4: Fundamental concept diagram

The circuit shown in Figure 3.4 was implemented in stage prior to this work, and in order to evaluate the ability to construct different functions, a model of the $I_O(V_{GS})$ characteristic was extrated and then tested against measurements with various configuration parameters (m, α, β) being depicted some of the results in Figure 3.5.

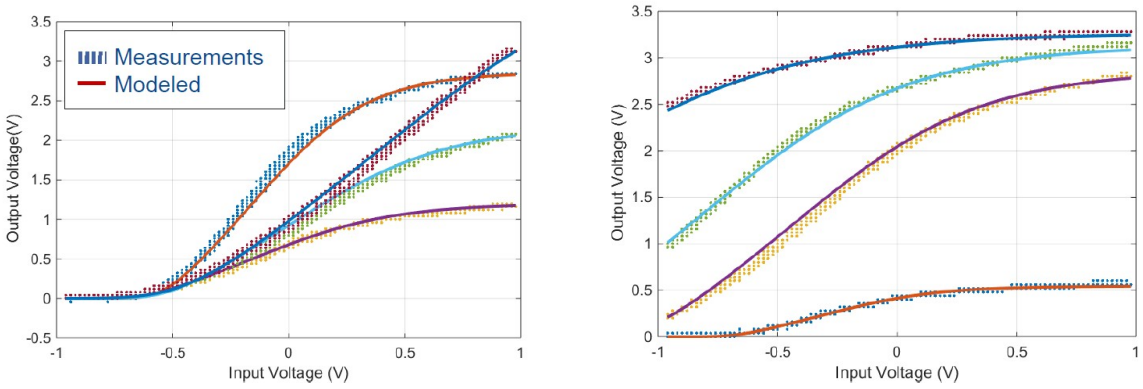


Figure 3.5: First essays

The previous prototype circuit has some aspects that need to be revised for a more practical implementation. The use of OpAmps for the configuration parameters makes the unit cell circuit overly complex and limits its operational bandwidth. The configurability of the unit cell should not be achieved through potentiometers, but should instead be implemented by reference voltages, which could be defined by a low grade microprocessor (while the potentiometers imply manual intervention). For instance, these could be set by latched serial DACs, whose values are specified by a low-grade microprocessor. Therefore, after the promising low-bandwidth results of the first prototype, a second circuit was considered for implementing the unit cell of the analog processing unit.

Consequently, for the unit cell, the op-amps were removed and replaced with two current sources, each controlled by a MOSFET, two OpAmps were kept in the inverter configuration with gain -1 in each cell before two MOSFETs because negative voltages were needed to control the current in the current mirrors where the voltages V_{G1} and V_{G2} are applied. A differential pair was also added. The voltages V_{G_1},V_{G_2},V_{G_3},and V_{G_4} are controlled by two dual DACs, as shown in the improved schematic of Figure 3.6.

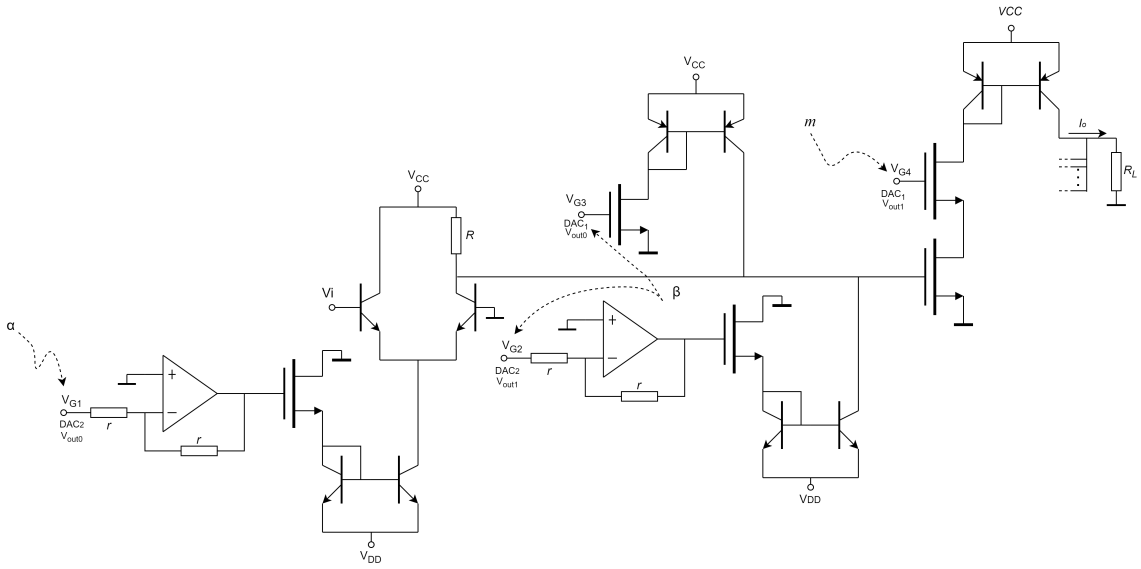


Figure 3.6: Improved circuit diagram for the push unit cell

The aim is to have one type of cell that increases the current in the load resistor and another that decreases it. To achieve this, two cells were created: the push cell of Figure3.6 and the pull cell shown if Figure 3.7, which is equal to that of the push cell except that it includes, at the output, an additional current mirror which inverts the current direction, driving it out of the load (i.e., pulling it out of the load).

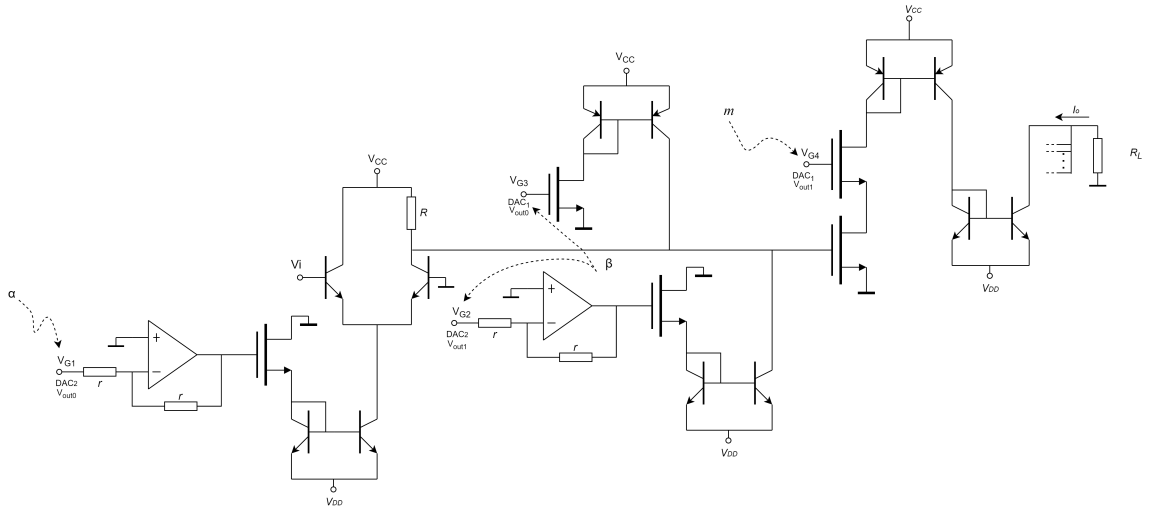


Figure 3.7: Improved Circuit Diagram for the Pull Unit Cell

This circuit is divided into blocks, each one responsible for a respective parameter of the transfer function represented in equation (3.3).

The differential pair, controlled by the current source of Figure 3.8, is primarily responsible for the gain of the input signal and corresponds to the α parameter. This current source is controlled by the V_{GS} voltage of the MOSFET of Figure 3.8.

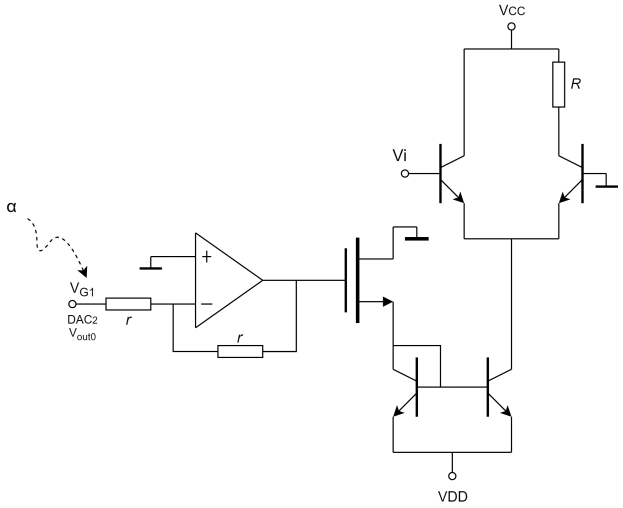
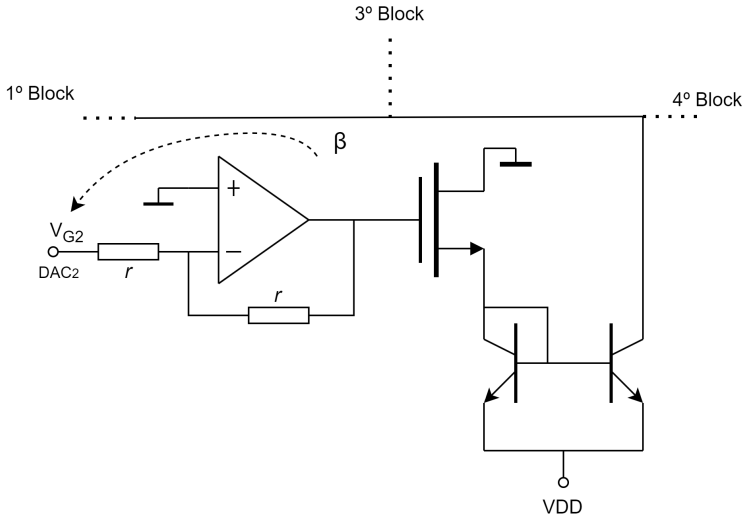


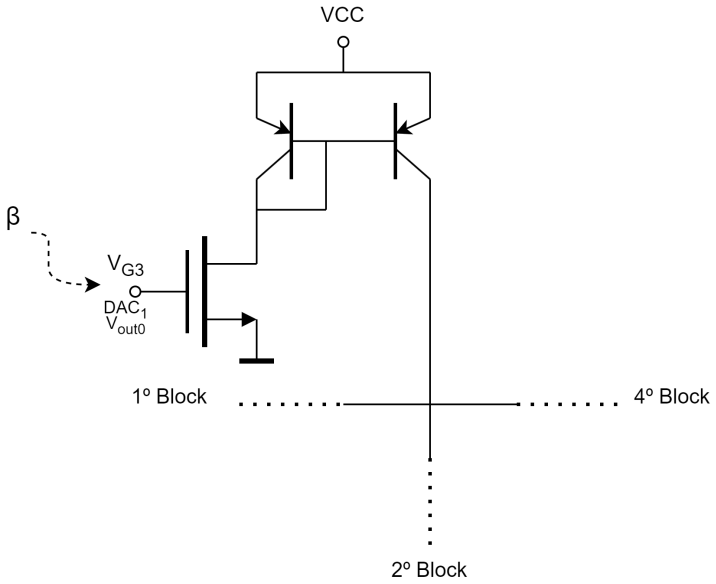
Figure 3.8: Diagram of the 1st block

As there are two circuits responsible for causing an offset in the input signal by varying the β parameter, as shown in Figure 3.6, they have been divided into two separate blocks

for easier individual analysis. The sub-circuit in the 2nd block, as depicted in Figure 3.9a, can increase the DC current flowing through resistor R of the differencial pair of the first block. Conversely, the 3rd block, 3.9b, can decrease that current. This offset caused by the two blocks corresponds to a shift along the x-axis of the input-output transfer characteristic.



(a) Increasing the dc current flowing through R while changing β



(b) Decreasing the dc current flowing through R while changing β

Figure 3.9: 2nd and 3rd Blocks responsible for the β parameter in the transfer function

The 4th block, shown in Figures 3.10 and 3.11, serves as the output stage of the unit cell. The input signal is in series with this block, and the output scaling is controlled by the 'm' parameter in the transfer function equation (3.3). This parameter can be adjusted by the voltage at the upper MOSFET's gate, V_{G4}, which alters the current flowing through the load resistor R_L.

The b parameter,3.3, responsible for the output offset and, consequently, the shift along

the y-axis, is determined by the addiction or subtraction of the output currents.

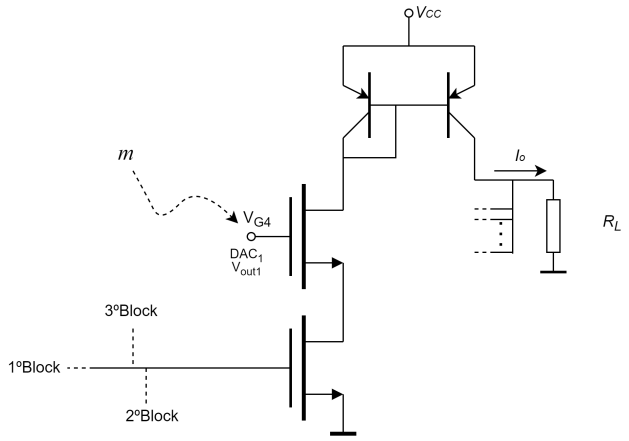


Figure 3.10: Diagram of the 4th block push cell

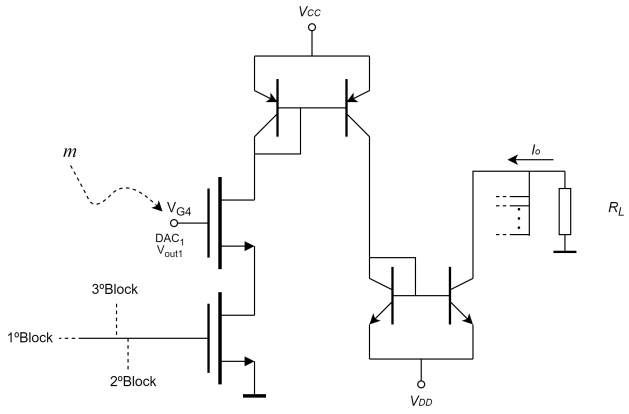


Figure 3.11: Diagram of the 4th block pull cell

3.1 Study and Analysis of the Unit Cell Prototype

The conceptual circuit design presented above had been developed before the beginning of this dissertation work. The latter, being described hereafter, consisted on the practical implementation, evolution and testing of a new prototype considering several unit cells operating in parallel.

In order to follow a sequential work ethic, the circuit was divided into three blocks and then separated into printed circuit boards for the different sub-circuits.

From the previous state of the circuit to the first block, some changes were made due to a problem with the previously sized current mirror branches. The current in the two branches was not equal, and this problem complicated the control of the current in the differential pair. Despite obtaining quite consistent current values in the input branch, the output branch did not follow the same pattern.

This problem could be due to numerous reasons, but the main ones could be the fact that even if the transistors are of the same type and from the same manufacturer, small variations in the manufacturing process can result in slight differences in the characteristics of each

transistor, leading to differences in current. Another very important factor is temperature, as it can also affect the behavior of transistors. If one of the transistors heats up more than the other, the behaviour of the transistors will not be the same and the fact that the current mirror is implemented with discrete components prevents them from maintaining balanced operating conditions, such as temperature, which would be much better controlled in an IC implementation. To solve this problem, a Wilson current mirror with a fourth transistor was introduced as well as two resistors in each branch to simultaneously try to produce a better balance between both branches of the current mirror and limit the current in those branches.

Incorporating an additional fourth transistor to the Wilson current mirror, as shown in Figure 3.12, achieves an equilibrium between the collector voltages of Q_{37} and Q_{38}, this is due to the fact that from the base of Q_{34} to the collector of Q_{38} there is a voltage drop equal to $V_{BE_{34}}$. Adding transistor Q_{33} therefore ensures that the collector of Q_{37} has a voltage drop equal to $V_{BE_{33}}$. As the base of transistor Q_{33} is connected to the base of transistor Q_{34}, they have the same voltage.

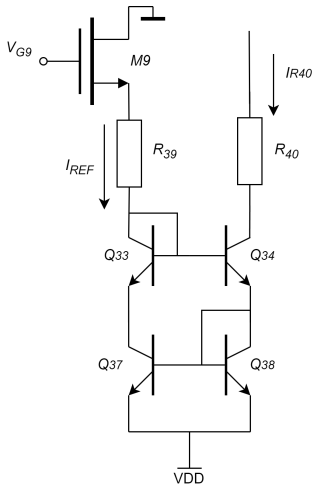


Figure 3.12: Diagram Current Mirror

This adjustment has three primary consequences: Firstly, it addresses the discrepancy between the behaviors of transistors Q_{37} and Q_{38}, which arises from the Early effect in Q_{37}. This discrepancy is a primary factor affecting the precision of the three-transistor Wilson current mirror [23, p. 274].

Secondly, at higher current levels, the current gain, also known as beta, of transistors reduces, causing a divergence from the standard collector current equation. The extent of this divergence depends on the collector voltage. By equalizing the collector voltages of Q_{37} and Q_{38}, the circuit ensures that the performance degradation in both the input and output branches is balanced at higher currents. This strategic alignment significantly extends the circuit's linear operational range.

Lastly, by aligning the collector voltages, the power dissipation in Q_{37} and Q_{38} is equalized. This power balance works to mitigate the discrepancies arising from temperature-induced effects on the base-emitter voltage V_{BE}.

Therefore, all the previously presented current mirrors have been replaced by the one depicted in Figure 3.12.

Another problem that came up is related to the NPN transistor BFP520 that was initially used. It had an unusually low collector-emitter breakdown voltage of just 3 V. This breakdown voltage is the point at which the transistor can be damaged. Since the power supplies are set at +/- 6 V, it is clear that the two transistors from the differential pair, in normal operation, consistently run with a collector-emitter voltage V_{CE} significantly above 3 V. Additionally, the transistor in the output branch from the current source applied to the differential pair, also experiences high voltage. As a result, when the circuit is powered up, these three transistors heat up quickly and are very likely to get permanently damaged within a few seconds.

As a result, this problem had to be solved and these transistors were replaced to ensure the circuit operates smoothly and safely, so the BFP520 was replaced by the MCH4015 transitor. The collector-emitter breakdown voltage of this transistor is 12 V, which is considerably higher than the previous value and provides a much more suitable voltage for the circuit to operate effectively.

In the selection of the MCH4015 transistor and other components, it was taken into consideration their behavior at high frequencies. This is because theoretically predicting or calculating the high cutoff frequency of the circuit is challenging, given the unpredictability of the discrete differential pair's behavior. Consequently, components with a high transition frequency were chosen to maximise bandwidth.

Regarding the differential pair (as depicted in Figure 3.8), ideally, it would be asymmetrical to improve bandwidth. This is because introducing a resistor in the input branch of the differential pair impacts bandwidth due to the Miller effect over the base-collector parasitic capacitance. However, controlling a differential pair with discrete components is not a straightforward task. Therefore, the analysis of the high cutoff frequency was deferred to the practical part of this dissertation. Based on the practical measurements conducted on a breadboard, the decision was made to add a resistor to the input branch of the differential pair. This step was taken to maintain both branches symmetric and improve the overall behavior of the differential pair.

For these reasons, in addition to the previously mentioned changes, resistors were added to both branches of the current sources. This served multiple purposes: to limit the current and prevent it from exceeding the maximum 100 mA rating of the MCH4015-TL-H transistors, to facilitate current measurements within each block, and to gain greater control over the signal swing achievable in each branch. In essence, it allows for the current to be restricted in different blocks by adjusting the currents.

After taking into account all these changes to the circuit and making several adjustments to both resistances and bias currents, the final versions of the push unit cell and pull unit cell are presented in Figures, 3.13 and 3.14, respectively.

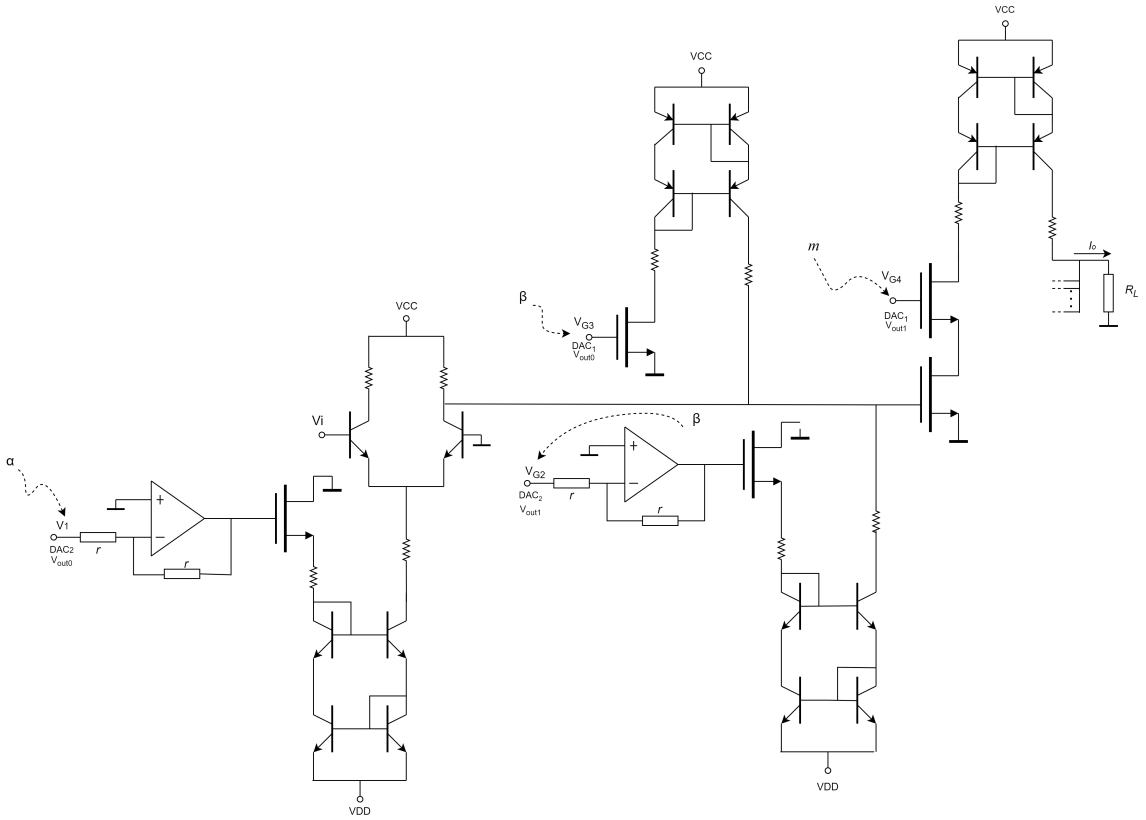


Figure 3.13: Final Version of the Push Unit Cell Diagram

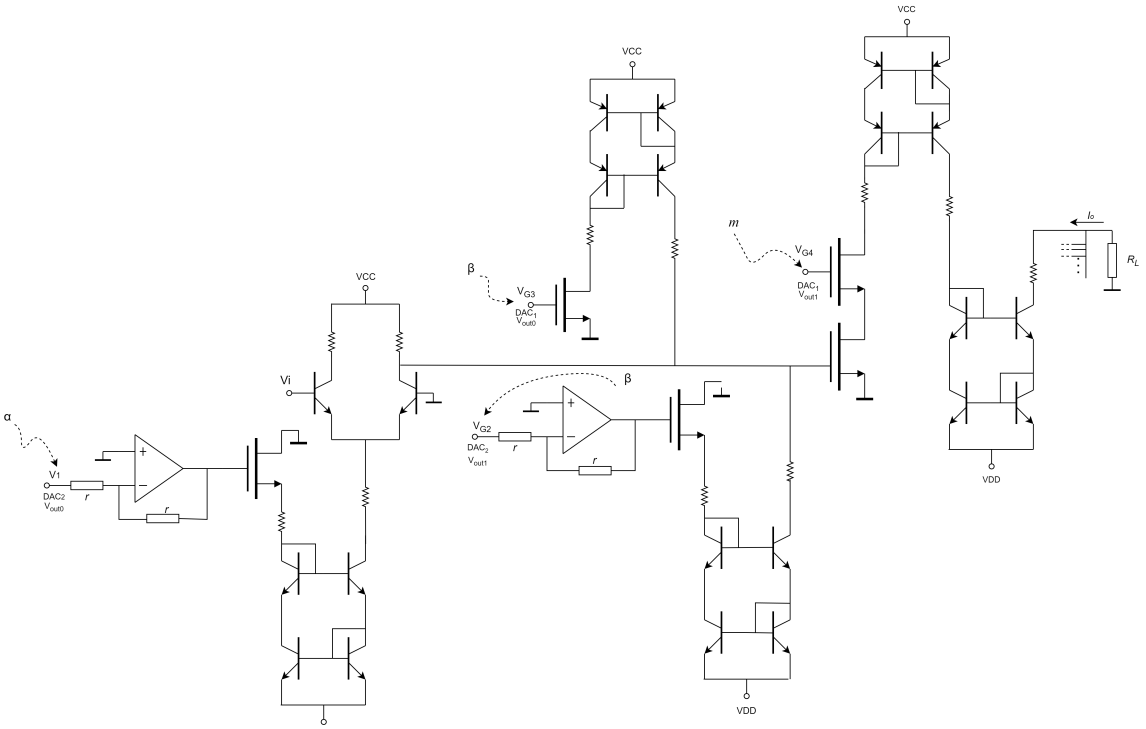


Figure 3.14: Final Version of the Pull Unit Cell Diagram

3.1.1 Bias Analysis of the Unit Cell

To assess the circuit's bias, various prototypes of each unit cell block were constructed and evaluated on a PCB. Throughout this analysis, the output on the Q_{31} collector of the differential pair and the output of the unit cell were measured by varying different voltage points. To facilitate tracking the circuit analysis, Figure 3.15 illustrates the current diagram of each current source branch in the 1st, 2nd, and 3rd blocks, as well as the current flowing through transistor Q_{31} and resistor R_{32}.

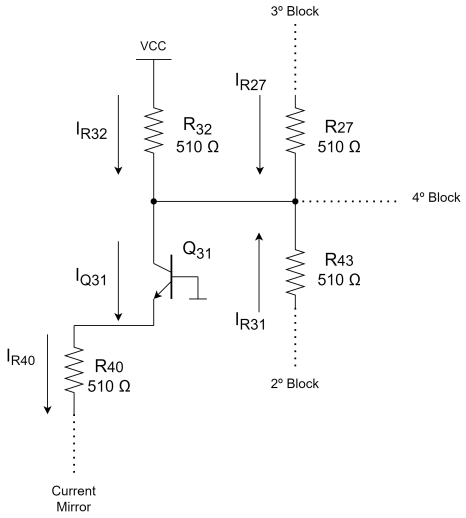


Figure 3.15: Current Diagram at the Output Node of the Differential Pair

3.1.1.1 1st block bias

The first block, shown in the Figure 3.16 consists of the current mirror and the differential pair. At this stage of the project, the main objective was the biasing of the circuit.

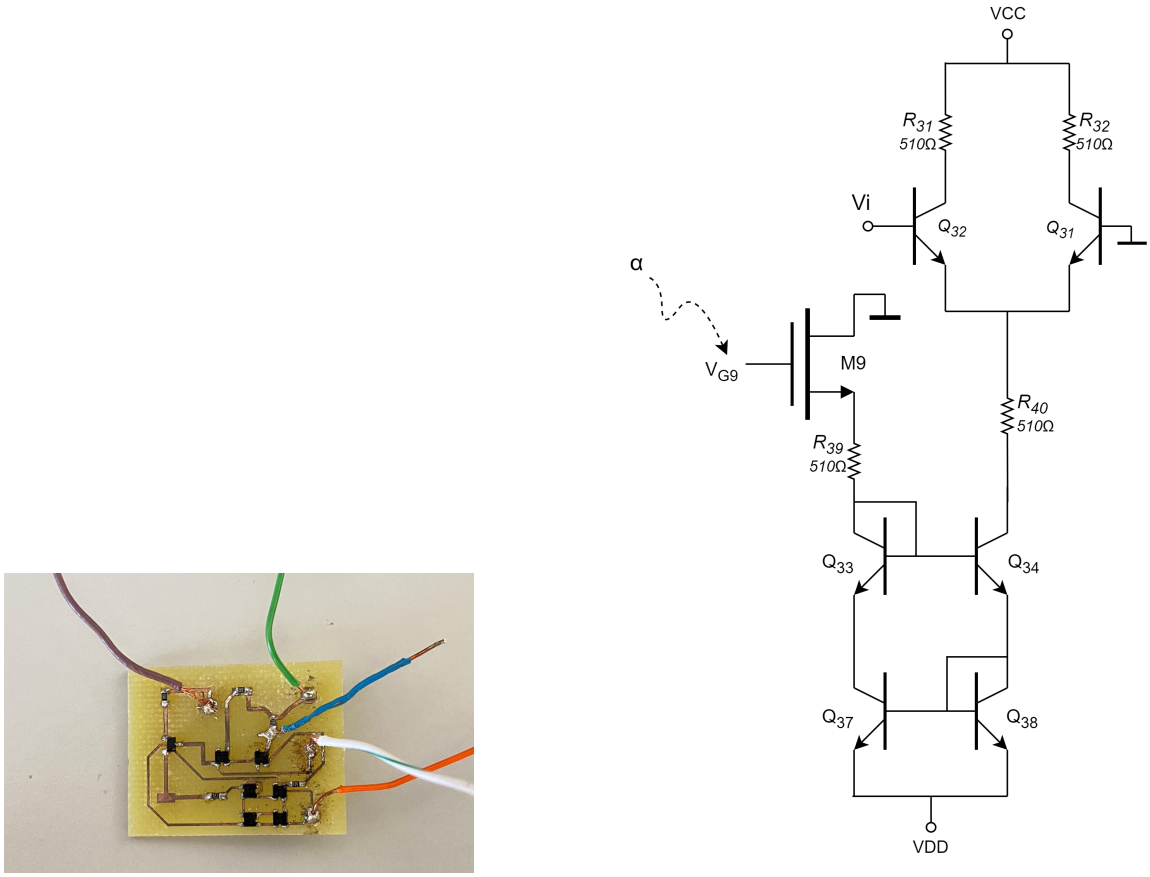


Figure 3.16: PCB and diagram of the 1st block

To observe the behavior of how the gate voltage of M9 affects the output voltage of the differential pair, a voltage was applied to the gate of the M9 MOSFET that ranged from -5.0 V to 0.0 V and the output of the differential pair was measured.

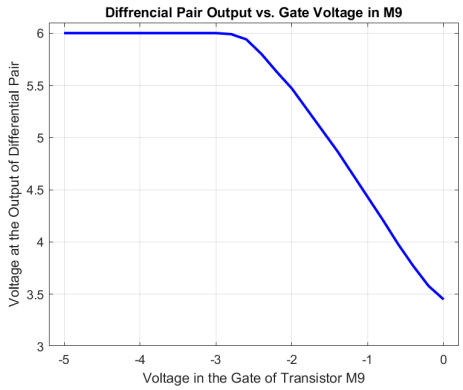
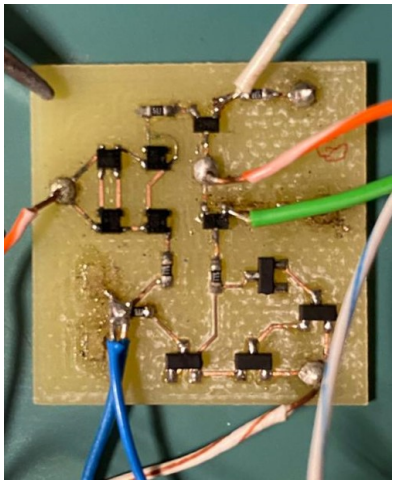


Figure 3.17: Differential pair output voltage vs. Gate voltage of M9 transistor

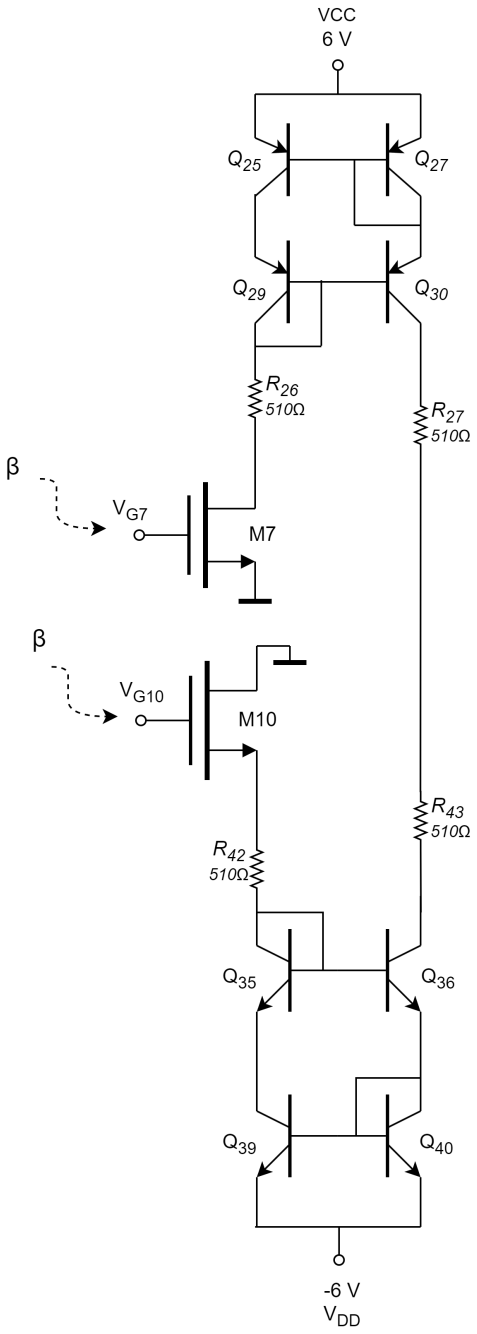
In the Figure 3.17, as the V_{GS_9} voltage increases and surpasses the V_{th}, which for the NEXPERIA NX7002AKW 115 is 1.6 V, the MOSFET begins to conduct and follows the equation (3.1). Following this principle, it was observed that the MOSFET begins to conduct when the output voltage of the differential pair is no longer 6.0 V, which occurs when the

gate voltage of the MOSFET is -3.2 V. From the moment the voltage continues to increase, the current in the current mirror also increases. As a consequence, since the current flowing in the branches of the differential pair is half the current of the current mirror, the current also increases, and the voltage drop across the collector resistor R_{32} of the differential pair also increases. From the voltage range of -3.8 V to 0.0 V, the behavior of the differential pair is quite linear, with a signal swing that goes from 6.0 V to 3.45 V.

3.1.1.2 2nd and 3rd block bias



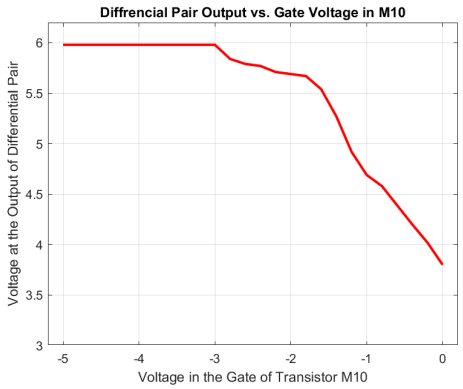
(a) Prototype PCB of the 2nd and 3rd block



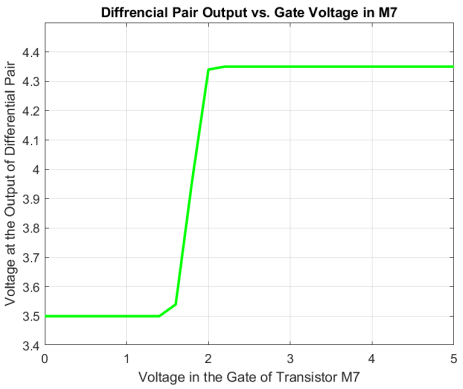
(b) Schematics of the 2nd and 3rd block

Figure 3.18: PCB and Schematic of the 2nd and 3rd blocks

The 2nd Block shown in Figure 3.18b, which is responsible for increasing the current in the collector resistor, I_{R32}, by changing the voltage at the M10 MOSFET and consequently, increasing the current in the current mirror, in Figure 3.12, was tested by applying a voltage of -3.40 V to the gate of M9. As a result, the output of the differential pair with 3rd block cut off is at 5.98 V. In the graph of Figure 3.19a, it is evident that the gradual increase of the voltage at the gate of MOSFET M10 results in an increase in current, which, in turn, leads to an increase in the voltage drop across resistor R_{32}. Notably, the voltage at the collector of the NPN transistor Q_{31} varies from 5.98 V to 3.80 V.



(a) Voltage at the collector Q_{31} as a function of the gate voltage of M10



(b) Voltage at the collector Q_{31} as a function of the gate voltage of M7

Figure 3.19: PCB and Schematic of the 2nd and 3rd blocks

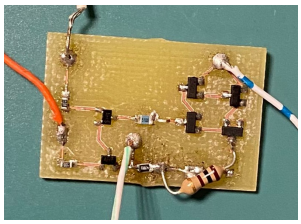
The third block, depicted in Figure 3.18b, responsible for reducing the current in the collector resistor R_{32}, was tested with an assumed differential pair output voltage of 3.5 V. In this scenario, as the current decreases, the voltage drop also decreases, leading to an increase in the gate voltage of the Q_{31} colletor, as shown in the Figure 3.19b.

As evident from the graph, as the gate voltage of the M6 MOSFET increases, the current conduction also rises in the branches of the current mirror, resulting in a decrease in the voltage drop across the collector resistor. Since the collector current of Q_{31} remains constant (given that the gate voltage of the M9 MOSFET remains unchanged), the current from the differential pair's current source remains stable. Therefore, if the current increases in resistor R_{27}, the current that flows in R_{32} must decrease, subsequently reducing the voltage drop across this resistance.

3.1.1.3 4th block push and pull cells bias

The voltage at the collector of transistor Q_{32} is connected to the gate of MOSFET M8 as can be seen in the Figure 3.20, which in turn controls the amount of current flowing in the 4th block of both the push cell and the pull cell. A higher voltage results in a greater V_{GS}, leading to increased current flow in the MOSFET M8. The M6 MOSFET represents the m parameter and controls the output scalling. It is important to note that as these blocks produce the signal output, it was necessary to introduce a load resistor for measurements. Taking into account the circuit's applications, a 50 Ω load resistor, $R_L = 50\,\Omega$, was chosen, as

the devices to be connected to this circuit have a low input impedance. Since the circuit has a current output, the current flowing in the output branches is adjustable and varies according to the value of R_{24}. In this case, in order to increase the limit of current in both branches of the output current source a resistor of 100 Ω was chosen.



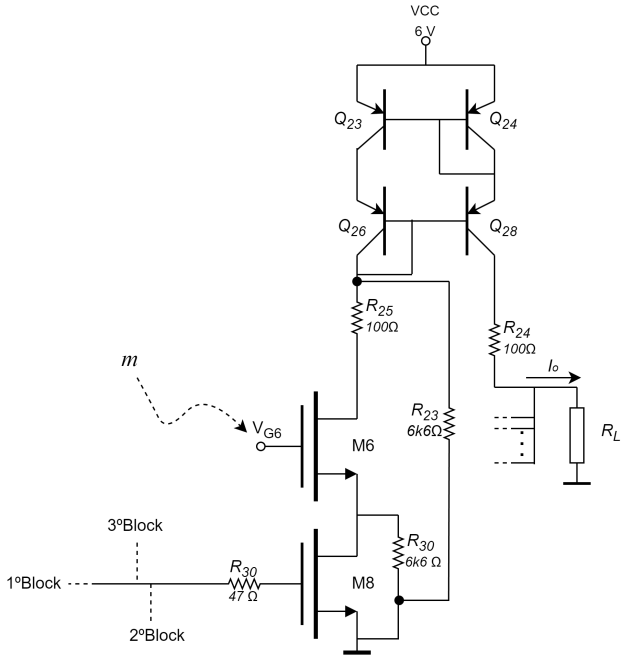
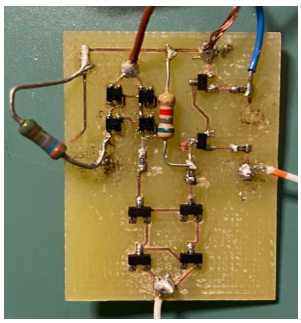


Figure 3.20: PCB and diagram of the 4th Block push cell



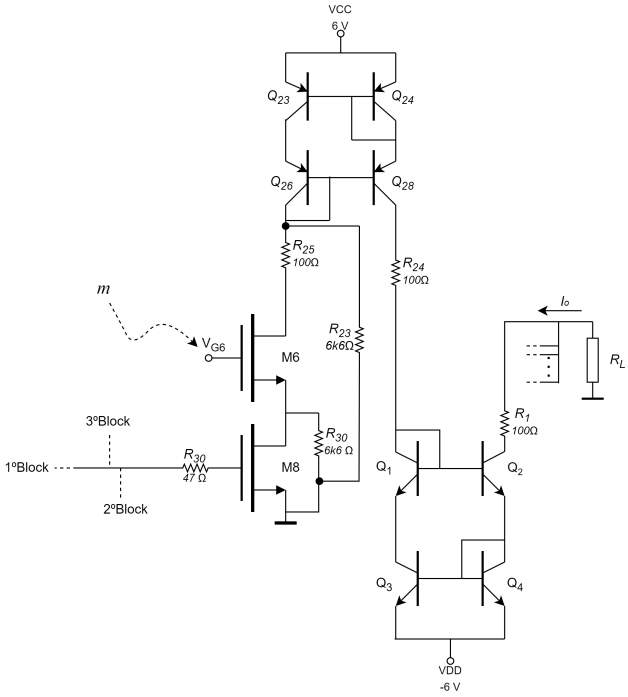


Figure 3.21: PCB and Schematic of the 4th Block Pull Cell

Initially, resistors with values of 510 Ω were placed in the branches of the push cell's current

mirror. This was done to ensure that all blocks were biased in the same way. However, this approach would not represent a typical application scenario, as the resistor in the output branch, R_{24}, would be in series with the load resistor, as illustrated in Figures 3.20 and 3.21, resulting in a total resistance of 560 Ω. The ideal situation would be to have no resistance in the branch, only the load resistor, allowing the current to increase with the conduction of the MOSFET, reducing resistor R_{25} to avoid limiting this current. However, this approach presents two problems. First, very high output current is not desirable, as the cell operates in current, and one of the goals is to keep power consumption low. Additionally, at higher currents, the circuit's behavior deviates from the expected, introducing noise and negatively affecting the performance of the cell, especially the last cell, as its current depends on the conduction of MOSFET M8, which, in turn, is controlled by the input signal amplified by the differential pair.

Therefore, it was necessary to reduce resistors R_{24} and R_{25} in a controlled manner, achieving a balance between signal swing, current, noise, and performance. A value of 100 Ω was chosen for this purpose.

In addition to all the considerations mentioned above, it is important to explain the reason for including resistors R_{23} and R_{30} in the circuit, see Figures 3.20 and 3.21. During some tests on the circuit, the presence of noise was observed when M8 was cut-off, but M6 was not. As a solution to this problem, the resistors were incorporated in order to establish a current path towards ground, in the case where one of the MOSFETs is not conducting and the other is, thus mitigating the noise identified.

To evaluate the behavior of the 4th block of the pull cell, a test was conducted with the gate voltage of the M8 MOSFET set to 3.14V, ensuring that the M8 MOSFET conducts current, given that its source voltage is fixed and connected to the ground and V_{GS} needs to be greater than V_{th}.

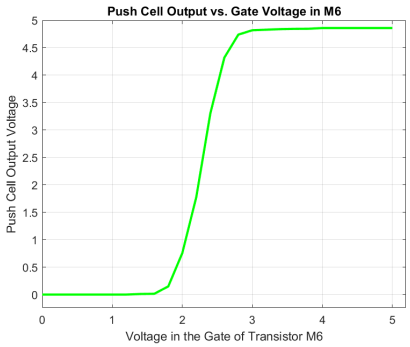


Figure 3.22: Push Unit Cell Output vs Gate voltage in M6

The Figure 3.22 illustrates the output voltage of the cell as the gate voltage of the M6 MOSFET gradually increases. Initially, when the M6 MOSFET is not conducting, the output voltage remains at 0V because the load resistor, which is in series with resistor R_{24}, is connected to ground. As the gate voltage increases, the MOSFET starts to conduct, allowing current to flow through the load resistor and raising the output voltage. The voltage increases

from 0V to 4.86 V.

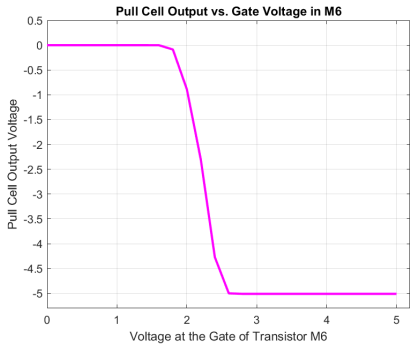


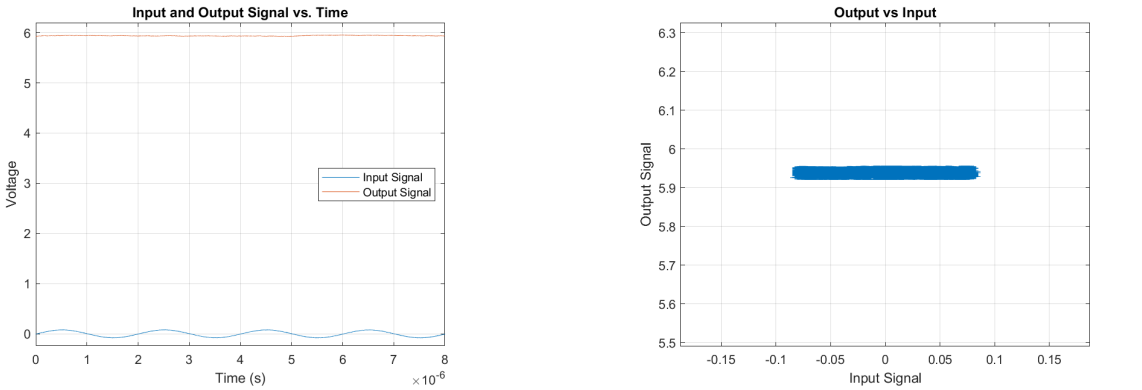
Figure 3.23: Pull Unit Cell Output vs Gate voltage in M6

Unlike what happens in the push cell, the pull cell (see Figure 3.23) is capable of pulling current from the load resistor. Since these cells are interconnected, all linked at a node, this cell can effectively subtract current from the load. The output swing of the cell ranges from 0 V to -5.01 V.

3.1.2 Study of the prototype's response with low frequency input signal

After evaluating the circuit's Direct Current (DC) bias conditions, the next step involves the application of an input signal to the circuit. This allows us to initially explore and assess the unit cell's response in the time domain. Subsequently,it was examined its output behavior concerning input variation when subjected to a low-frequency signal. This approach will be followed by a high-frequency analysis to assess the circuit's bandwidth.

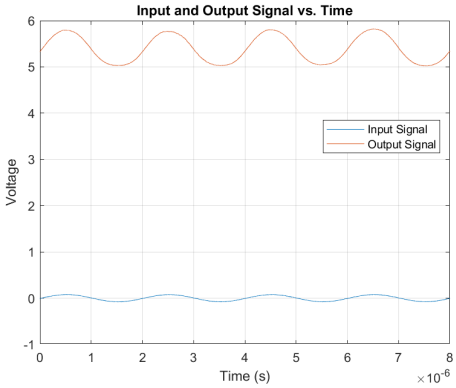
3.1.2.1 1st block analysis



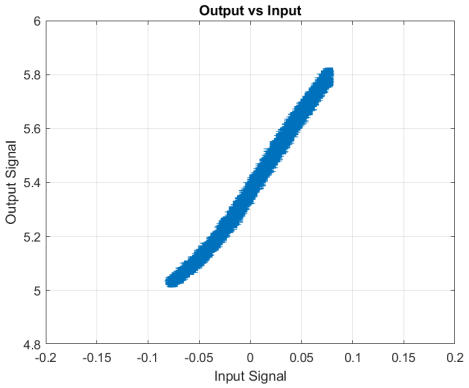
(a) Output signal at collector Q_{31} in the time domain

(b) Output signal at collector Q_{31} as a function of the input signal

Figure 3.24: Analysis of the signal from the 1st Block with V_{G_9}=-3.0 V



(a) Output signal at collector Q_{31} in the time domain

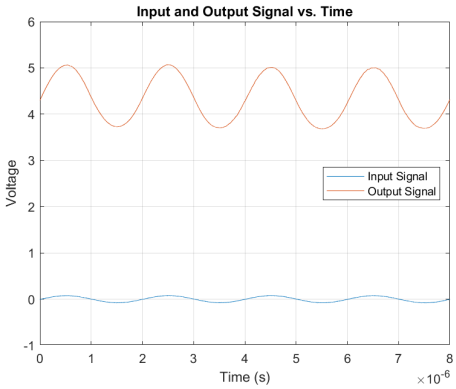


(b) Output signal at collector Q_{31} as a function of the input signal

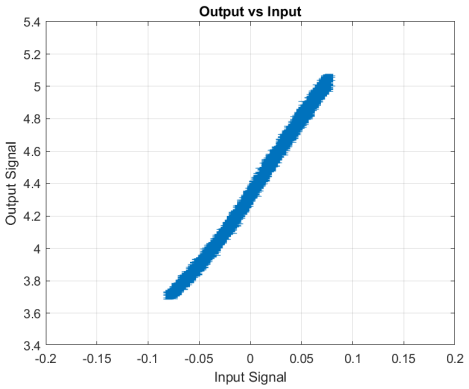
Figure 3.25: Analysis of the signal from the 1st Block with V_{G_9}=-2.0 V

Initially, the transistor M9 was in the cut-off region because $V_{GS_9} < V_{th}$, and the output remained at the value of $V_{CC} = 6.0$ V. Consequently, both in the time domain, see Figure 3.24a and in the XY Figure 3.24b, the output did not vary with the input.

Afterwards, a voltage of -2.0 V was applied at the gate og the M9 MOSFET, causing the transistor to begin conducting as $V_{GS_9} > V_{th}$. At this point, the output signal exhibited a excursion of 5.83 V down to 5.01 V, as can be seen in Figure 3.25a.

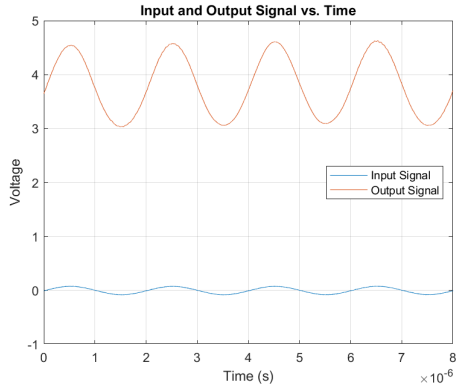


(a) Output signal at collector Q_{31} in the time domain

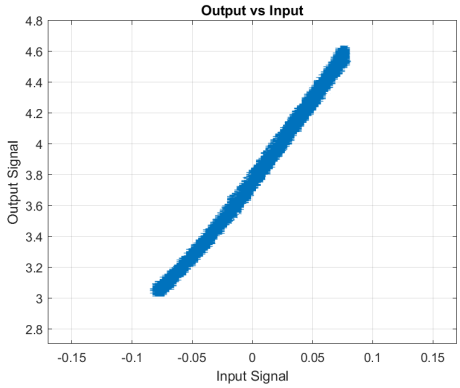


(b) Output signal at collector Q_{31} as a function of the input signal

Figure 3.26: Analysis of the signal from the 1st Block with V_{G_9}=-1.0 V



(a) Output signal at collector Q_{31} in the time domain



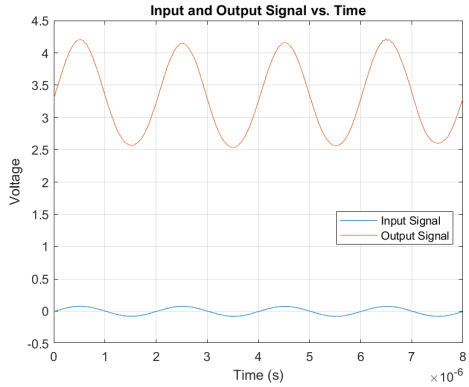
(b) Output signal at collector Q_{31} as a function of the input signal

Figure 3.27: Analysis of the signal from the 1st Block with V_{G_9}=-0.5 V

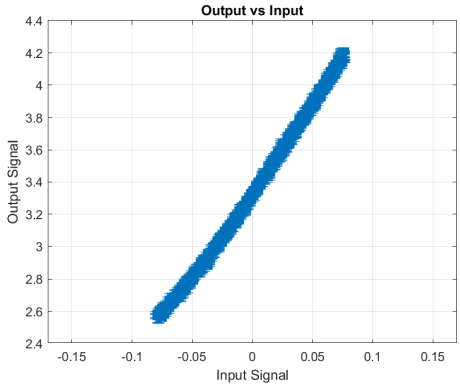
A gradual increase in the gate voltage of M9 results in an increase in current, therefore raising the current flowing through R_{32} and, consequently, increasing the voltage difference between V_{CC} and the collector of Q_{31}.

With V_{G9} set to -1.0 V (see Figure 3.26a), the signal excursion ranges from 5.10 V down to 3.67 V.

Further increasing the voltage to -0.5 V in V_{G9} (see Figure 3.27a), the signal reaches a maximum of 4.65 V and a minimum of 3.00 V.



(a) Output signal at collector Q_{31} in the time domain



(b) Output signal at collector Q_{31} as a function of the input signal

Figure 3.28: Analysis of the signal from the 1st Block with V_{G9}=-0.0 V

Finally, with the gate voltage V_{G9} set to 0 V (see Figure 3.28a), the maximum current that the current source can supply to the differential pair was reached. At this point, the signal excursion ranges from 4.27 V down to 2.52 V.

It is important to note that the reason for the input signal having a lower amplitude of $80mV_{pp}$ is due to the fact that the collector output (see Figure 3.28b) cannot be in saturation. Since the input signal is likely to be modified according to the parameters α and β before entering the gate of the MOSFET M8, it is essential to note that this signal is crucial for the conduction process of this transistor. Therefore, it is considered a best practice to avoid having

the signal in the differential pair already saturated, as it can compromise the performance of the MOSFET M8.

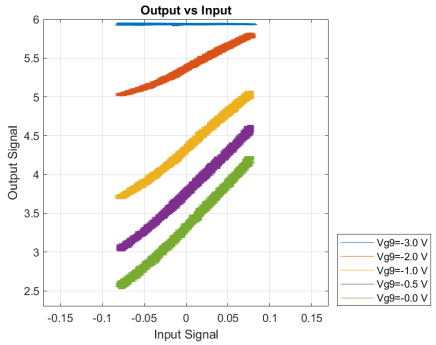
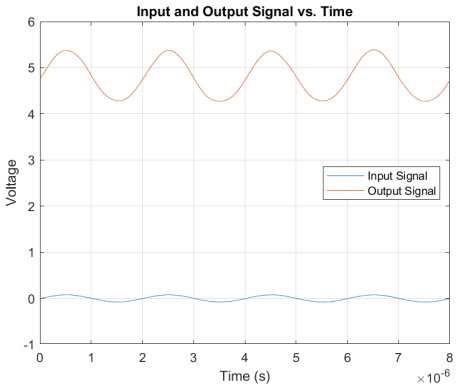


Figure 3.29: Combined XY plots from the 1st block

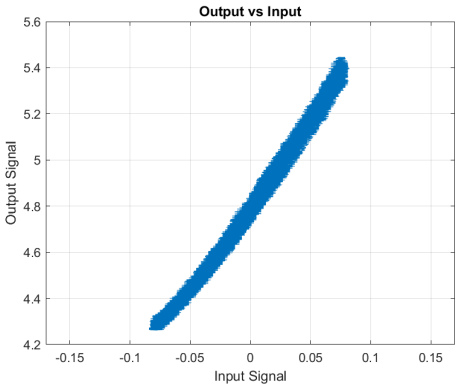
In Figure 3.29 you can see the different XY plots superimposed, here you can see that by changing the voltage at the gate of the M9 MOSFET you can change the gain of the signal, as you can see from the slope of each input-output signal.

3.1.2.2 2nd and 3rd block analysis

The objective of the second and third blocks is to increase or decrease the current passing through the resistor R_{32}. Accordingly, the following graphs were analyzed while varying the two voltages responsible for the β parameter: the voltage at the gate of MOSFET M10 and at M7.

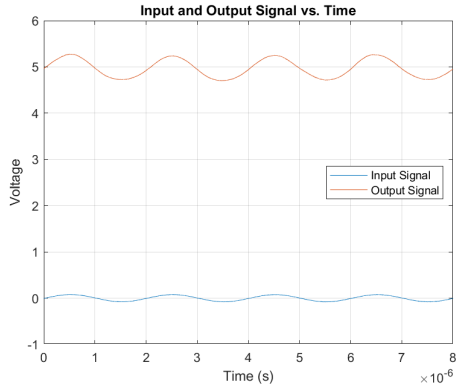


(a) Output signal at collector Q_{31} in the time domain

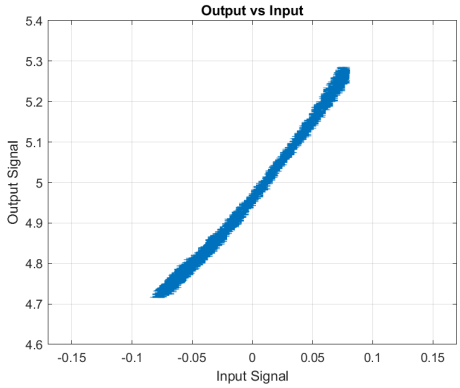


(b) Output signal at collector Q_{31} as a function of the input signal

Figure 3.30: Analysis of the signal from the 1st Block with V_{G9}=-1.41 V,V_{G7}=0.0 V,V_{G10}=-4.07 V



(a) Output signal at collector Q_{31} in the time domain

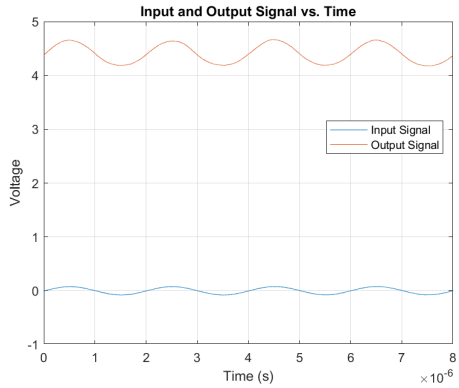


(b) Output signal at collector Q_{31} as a function of the input signal

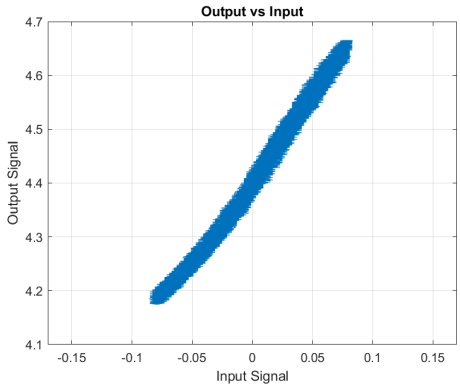
Figure 3.31: Analysis of the signal from the 1st Block with V_{G9}=-1.41 V,V_{G7}=1.84 V,V_{G10}=-4.07 V

At the beginning, the gate voltage of MOSFET M9 was set to V_{G9}=-1.41 V, while the 2nd and 3rd blocks were turned off with V_{G10}=-4.07 V and V_{G7}=0.0 V (see Figure 3.30a).

Maintaining the gate voltage of M9 constant and varying the gate voltage of MOSFET M7 to V_{G7}=1.84 V, the gain remained the same, as can be seen in Figure 3.31a. However, the signal excursion changed due to the decrease in current through resistor R_{32}.



(a) Output signal at collector Q_{31} in the time domain



(b) Output signal at collector Q_{31} as a function of the input signal

Figure 3.32: Analysis of the signal from the 1st Block with V_{G9}=-1.8 V,V_{G7}=2.4 V,V_{G10}=-0.84 V

In Figure 3.32b, we can observe an increase in the voltage drop across resistor R_{32}. This is due to the variation in the gate voltage of M10, V_{G10}=-0.84V, an increase in current in the 3rd block , V_{G7}=2.4 V, and a slight decrease in the gain of the differential pair, V_{G9}=-1.8 V.

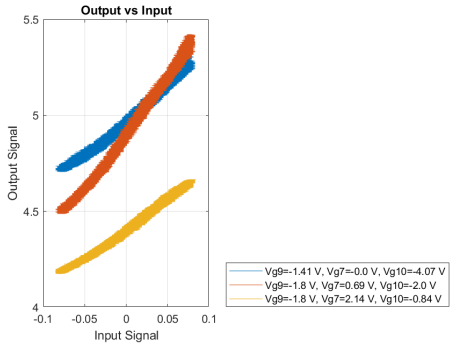


Figure 3.33: Combined XY plots from the 2nd and 3rd Blocks

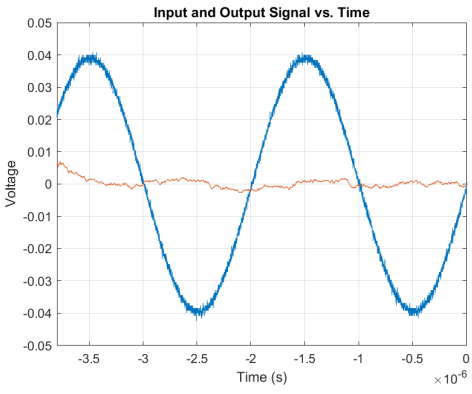
In Figure 3.33 you can see that by changing the voltages V_G9 and V_G10, and thus varying the parameter β, it is possible to compensate the signal.

3.1.2.3 4th block push cell analysis

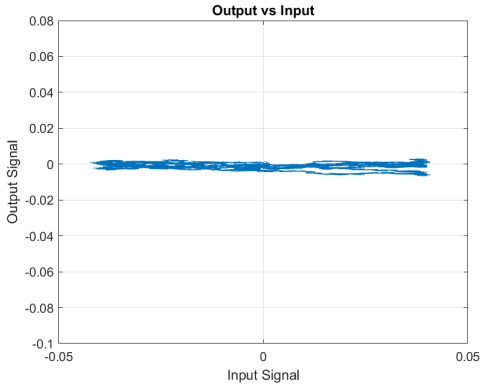
It is important to note that I found a lot more noise in this block than in the others, although an attempt was made to find the source of the noise, it was not possible to identify exactly where it was coming from, and so in this section it can be seen that the graphs have some noise.

The fourth and final block of this cell is the output block, which has the primary purpose of implementing the sigmoid-like function signal, as illustrated in the Figure 3.3. However, this signal is modified accordingly to various parameters of the transfer function, as defined in the equation 3.3. Consequently, after the input signal has been altered based on the parameters α and β, as we have just analyzed in the 1st, 2nd, and 3rd blocks, it is directed connected to the gate of transistor M8.

In the analysis of the output signal, the voltages V_{G9}, V_{G10}, and V_{G6} are changed, to evaluate the impact of each parameter on the output signal.

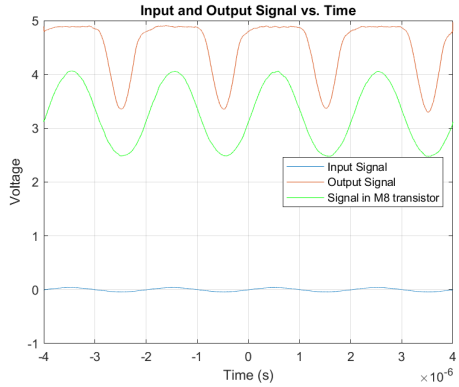


(a) Push unit cell output signal in the time domain

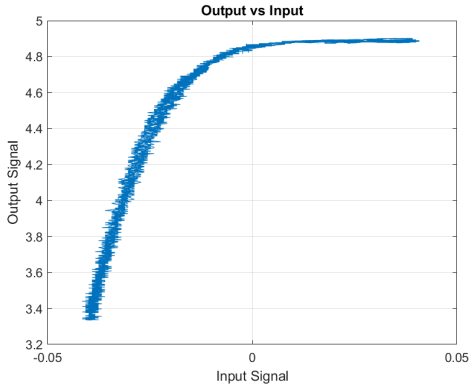


(b) Push unit cell output signal as a function of the input signal

Figure 3.34: Analysis of the signal from the 4th block push cell with V_{G9}=-0.0 V,V_{G10}=0.0 V,V_{G6}=0.0 V



(a) Push unit cell output signal in the time domain

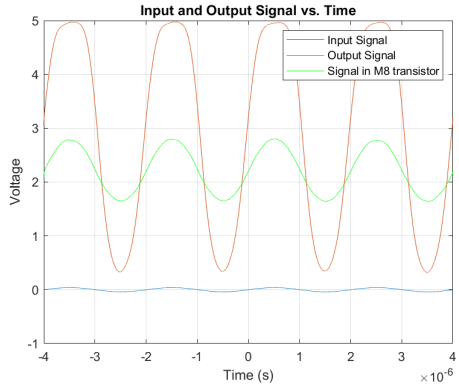


(b) Push unit cell output signal as a function of the input signal

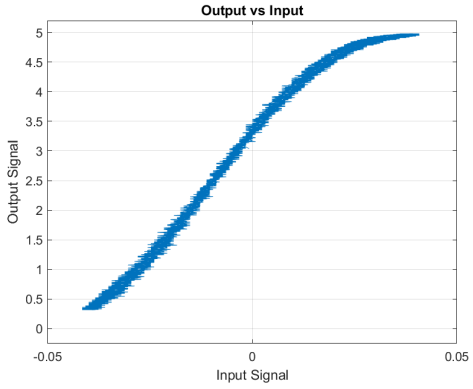
Figure 3.35: Analysis of the signal from the 4th block push cell with V_{G9}=-0.57 V,V_{G10}=-1.30 V,V_{G6}=3.68 V

While in the graph shown in Figure 3.34a, the output signal remains at zero, in the graph depicted in Figure 3.35a, the output signal varies from 3.34 V to 4.97 V. This happens because the voltages V_{G9} and V_{G10} decreased, causing the input signal at the gate of M8 to increase its signal excursion. As a result, the signal reaches such high values that M8 is practically always conducting because $V_{GS_8} > V_{th}$ for most of the signal duration. With V_{G6} at 3.68 V, the M6 MOSFET is also conducting, driving the output signal to saturation due to the high gate voltage applied.

In the graph represented by Figure 3.34b, even when the input signal at M8's gate is sufficient to drive it into conduction, the M6 MOSFET remains turned off, preventing any current flow through the load resistor, R_L. As a result, the output signal remains at zero.



(a) Push Unit Cell Output signal in the time domain



(b) Pull Unit Cell Output signal as a function of the input signal

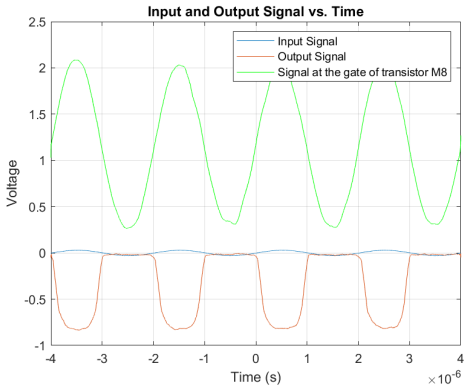
Figure 3.36: Analysis of the signal from the 4th block push cell with V_{G9}=-2.10V,V_{G10}=0.0V,V_{G6}=5.07V

By adjusting the input signal at the M8 gate again, increasing the V_{G10} voltage to 0.0 V and decreasing the V_{G9} voltage to -2.10 V, the output signal's excursion expanded to [0.32; 4.98] V. This is because the input signal at the M8 gate now has a range from 2.47 V to 4.06

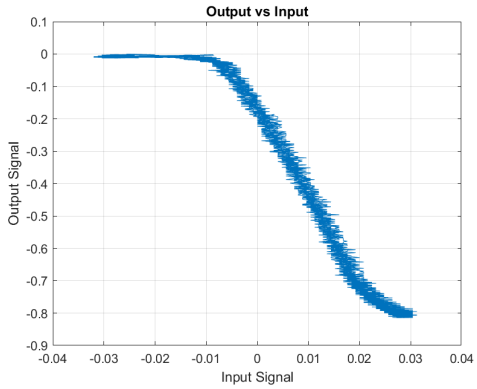
V, as shown in Figure 3.36a. As a result, MOSFET M8 no longer saturates for most of the positive half-cycle of the input signal, reaching V_{GS} values that keep it in the linear region.

3.1.2.4 4th pull cell block analysis

The pull cell is essentially the same as the push cell, but with the addition of an extra current mirror, through which the same current that flows through transistors M6 and M8 passes. This current mirror is responsible for 'pulling' the load current and, thereby, subtracting it from the cell's output current. As in the analysis of the push cell, the voltages V_{G9}, V_{G10}, and V_{G6} were varied to assess how the parameters can alter the output signal's characteristics. The justification for the choice of resistances has been previously discussed in this chapter, in the section on push cell signal analysis (previous section).

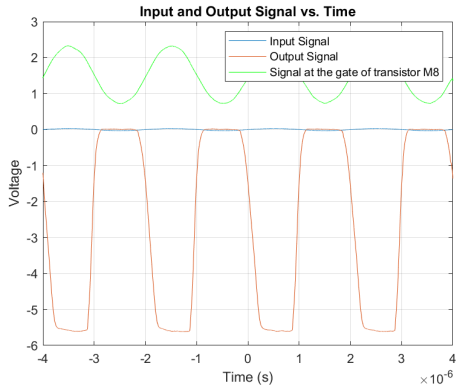


(a) Pull Unit Cell Output signal in the time domain

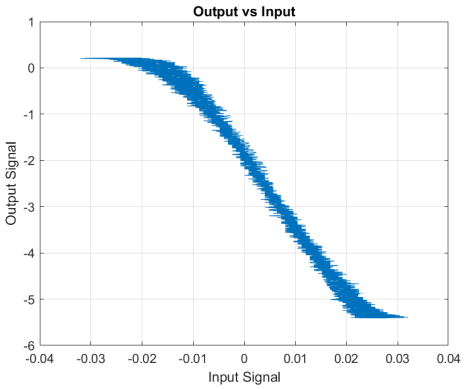


(b) Pull Unit Cell Output signal as a function of the input signal

Figure 3.37: Analysis of the signal from the 4th Block Pull Cell with V_{G9}=0.0V,V_{G10}=0.0V,V_{G6}=1.98V



(a) Pull Unit Cell Output signal in the time domain



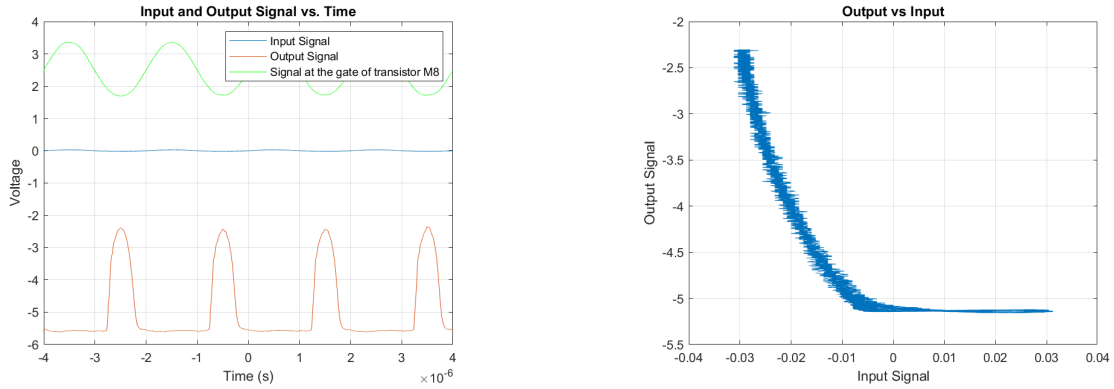
(b) Pull Unit Cell Output signal as a function of the input signal

Figure 3.38: Analysis of the signal from the 4th Block Pull Cell with V_{G9}=-0.46V,V_{G10}=0.0V,V_{G6}=4.31V

In Figure 3.37a, the gate voltages of transistors M9 and M10 are both at zero. As a result, the input signal at the gate of transistor M8 has voltages that allow for a slight conduction of

the transistor. Therefore, if MOSFET M6 is able to conduct (V_{G6}=1.98 V), the output will have a small signal excursion, ranging from 0 V to -0.84 V.

Figure 3.38a shows that the voltage V_{G9} has been lowered, subsequently reducing the current in the differential pair, the input signal at the gate of the M8 MOSFET increases in amplitude. This results in higher conductivity of transistor M8. Additionally, with the gate voltage of transistor M6 at 4.31 V, the output signal exhibits a much larger excursion. Although the signal reaches saturation at the maximum input, where it reaches its maximum absolute value, it ceases to conduct when M8 no longer has $V_{GS_8} > V_{th}$.



(a) Pull Unit Cell Output signal in the time domain

(b) Pull Unit Cell Output signal as a function of the input signal

Figure 3.39: Analysis of the signal from the 4th Block Pull Cell with V_{G9}=-0.46 V,V_{G10}=-0.83 V,V_{G6}=4.31 V

Similarly to the push cell, the same behavior occurs here when the input signal voltage values always remain above the V_{th} threshold. In such conditions, the output signal never reaches zero because both transistors M8 and M6 are continuously conducting (V_{G6} = 4.31 V). Consequently, the output signal saturates for a longer duration, reaching -5.17 V, as can be observed in Figure 3.39b.

3.1.3 Study of the prototype's unit pull cell response with input signal at high frequency

It is important to mention that, ideally, the excursion at the collector of the transistor would range from 6V down to 0.0V. This excursion is possible and has already been achieved using resistors R_{32} and R_{31}, both equal to 3.3 kΩ, while keeping resistors R_{39} and R_{40} at 510 Ω. The problem arises when the circuit's bandwidth was tested, and it was not reaching satisfactory values.

As a result, the initial step was to attempt to reduce the resistances in the differential pair to increase the bandwidth. However, this required increasing the current produced by the current source. The challenge with this approach is that at higher currents, the differential pair loses its symmetry. This means that its behavior becomes less predictable and less favorable for the circuit as a whole.

This issue arises from the fact that the differential pair is a complex circuit to control when it is not in the form of an IC. When the current that flows through the transistors is increased, it leads to a rise in temperature. Consequently, the V_{BE} of each transistor varies differently based on their individual temperatures.

Therefore, a decision was made to reduce the excursion at the output of the 1st block while maintaining a comfortable bandwidth and acceptable behavior for this block.

Since this circuit behaves like a low-pass filter, analysing the upper cut-off frequency is the next step. To test the bandwidth, the peak-to-peak voltage of the output signal in the pull cell was measured at a frequency of 500 kHz, resulting in a value of 1.36 V_{PP}. Subsequently, the voltage value at which the signal drops -3 dB is at 0.9617 V, marking the high cutoff frequency. All the measurements for the different frequencies were made without changing the peak-to-peak voltage of the input signal, which remained at 80 mV_{PP}.

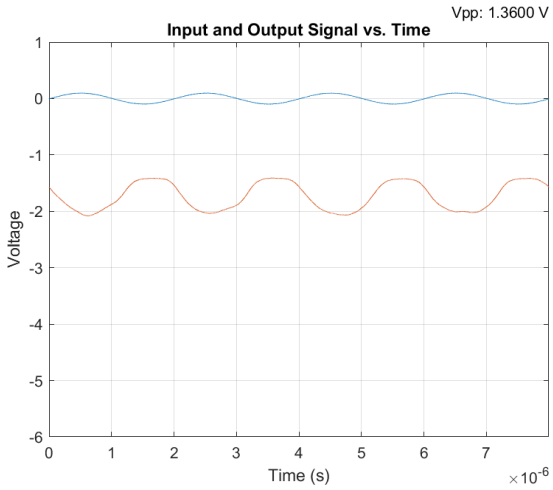
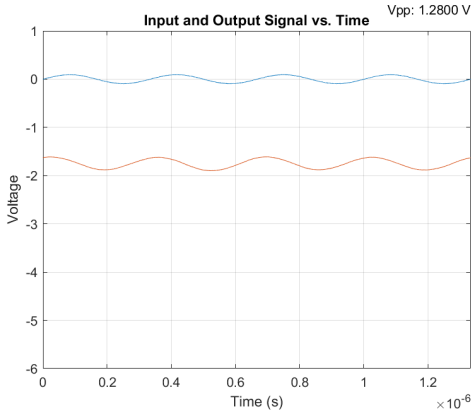
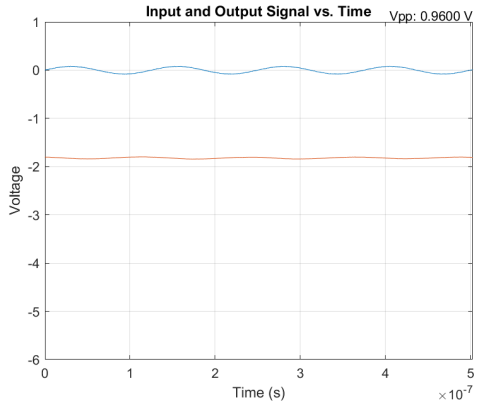


Figure 3.40: Output signal of the pull unit cell with a 500 kHz input signal



(a) Output signal of the pull unit cell with a 3 MHz input signal



(b) Output signal of the pull unit cell with a 7.960 MHz input signal

Figure 3.41: Output signal of the pull unit cell with a 3 MHz and 7.96 MHz input signal

From the Figures above, it is apparent that at an input signal frequency of 3 MHz, the V_{PP} value remains above 0.96 V. It is only at a frequency of 8 MHz that the output signal

reaches the -3 dB drop, signifying an upper cutoff frequency of approximately 8 MHz.

3.1.4 Study of the prototype's unit push cell response with input signal at high frequency

To test the push cell's response to the input signal at high frequencies, the first step was to take the signal's output values at lower frequencies in order to determine the peak-to-peak voltage. Then, following the same procedure applied to the pull cell, we analysed when the voltage dropped by -3 dB.

Unfortunately, due to the fact that this is a prototype divided into blocks, the last one, responsible for adding the push cell, as shown in Figure 3.20, was subject to noise during the measurements. This noise had various origins, such as the connections of ground and the supply voltages of the circuit not being the best, as they involve a lot of wires. This resulted in the bandwidth of this block being significantly lower than that of the other cells.

Given a peak-to-peak voltage of 4.66 V, see Figure 3.42 with a frequency of 500 kHz in the input signal, the voltage when the signal drops -3 db is 3.29 V.

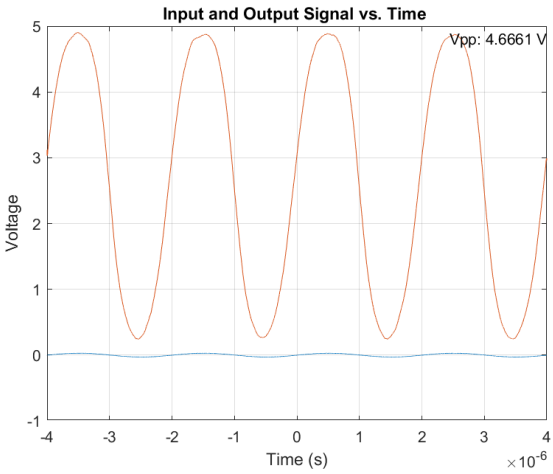
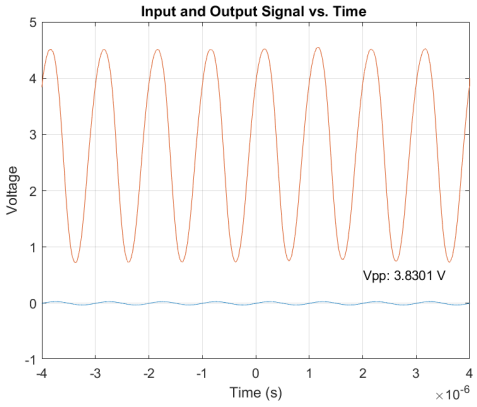
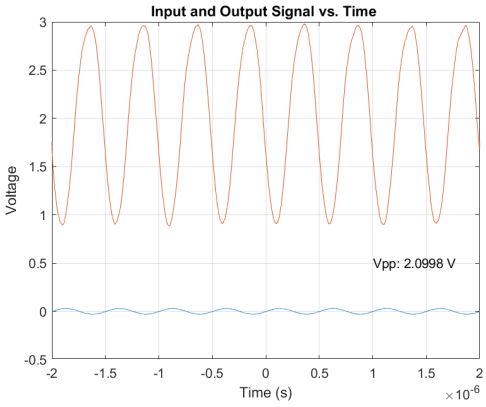


Figure 3.42: Output signal of the push unit cell with a 500 kHz input signal



(a) Output signal of the push unit cell with a 992.9 kHz input signal



(b) Output signal of the push unit cell with a 1.998 MHz input signal

Figure 3.43: Output signal of the push unit cell with a 992 kHz and 1.998 MHz input signal

From the figures, 3.43a and 3.43b, you can see that for a frequency of 992.9 kHz the signal hasn't yet surpassed 3.29 V, as its peak-to-peak voltage is 3.83 V. At a frequency of 1.99 MHz, the output signal is already operating above the upper cut-off frequency, with an peak-to-peak voltage of 2.10 V. This means that this cell has a bandwidth of approximately 1.88 MHz.

CHAPTER 4

Prototype of a Multi-cell Analog Processing Unit

In Chapter 3, a description of the circuit's philosophy and the initial prototype of the unit cell was provided. The following task consisted in developing a prototype of a system that, incorporating several unit cells (of pull and push types), would be able to implement configurable analog transfer functions. For that purpose, these cells needed to be configured through a low-grade microcontroller, which would set the control voltages of each unit cell by means of dedicated DACs. The microcontroller would then be connected to a computer (using an Universal Serial Bus (USB) connection) which, through Matlab, would define the values to be applicable to each configuration voltage of the unit cells. In this chapter, the multi-cell PCB will be displayed, on which five push cells and five pull cells have been incorporated, thus integrating the digital component. Then, following the methodology applied in Chapter 3, we will proceed to analyse the biasing of each block and the signal analysis of the same blocks.

Thus, to implement this multi-cell analog processing unit the following schematics have been drawn in Altium, see Figure 4.1, Figure 4.2 and Figure A.1.

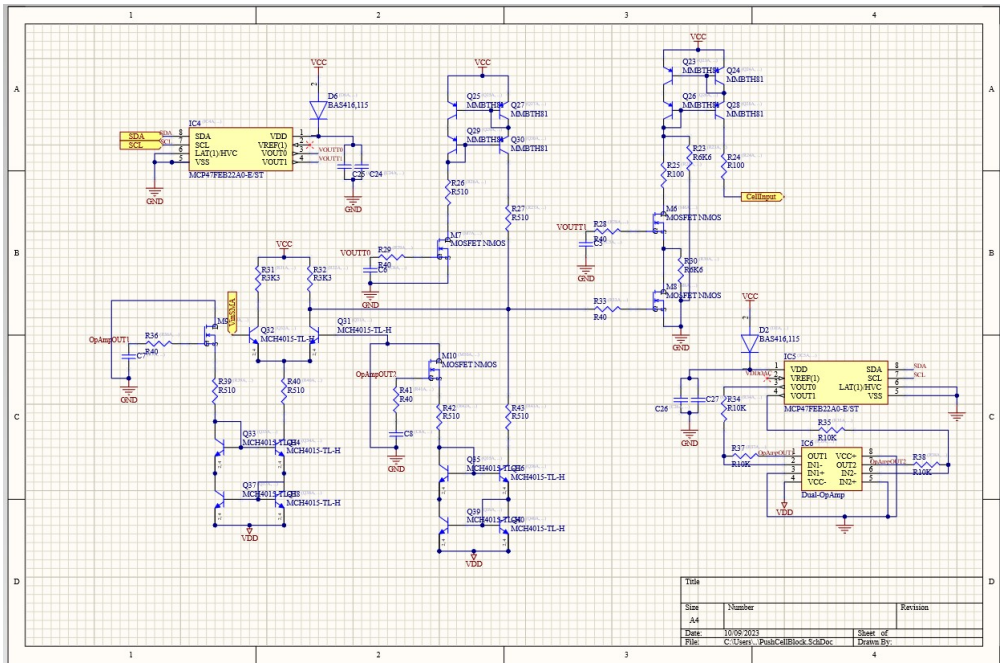


Figure 4.1: Pull cell schematic

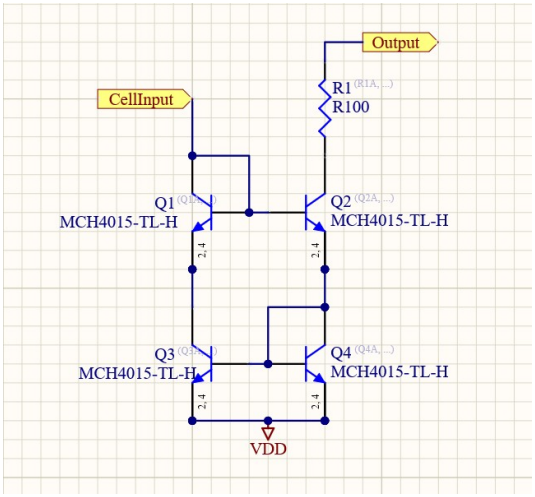


Figure 4.2: Push cell schematic

Following the schematics, the PCB layout was designed, see Figure 4.3.

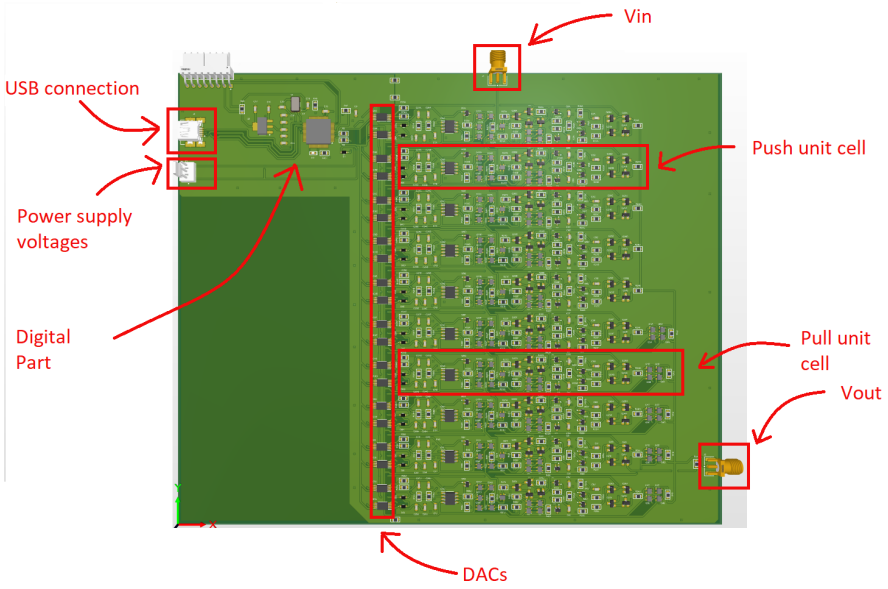


Figure 4.3: Multi-cell analog processing unit 3D layout

Figure 4.4 depicts the PCB with the complete digital section assembled, along with two push cells and one pull cell soldered in place.

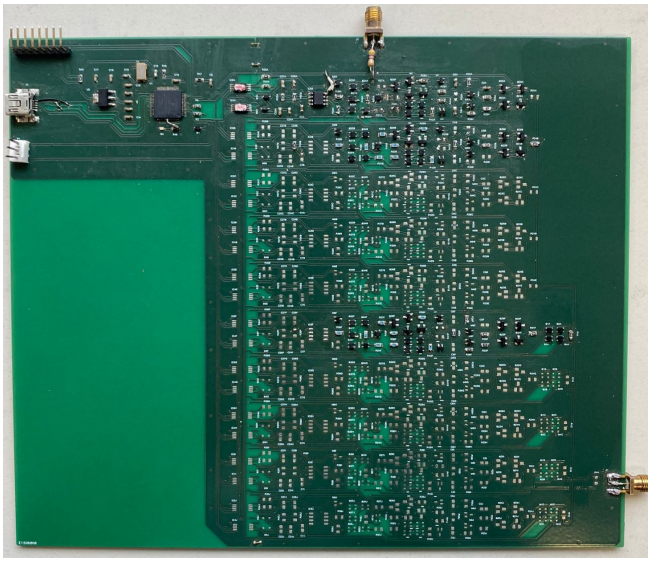


Figure 4.4: Multi-cell analog processing unit PCB

The schematic of the circuit implemented for the digital part of the prototype, the purpose of which is to allow control, using DACs, of all the unit cell configuration voltages, imposed by means of a Matlab script, can be found in the Appendix B, specifically in B.1.

The initial task at hand involved comparing the biasing, therefore, with identical components and resistance values, the output voltages of blocks 1, 2, 3, and 4 (push and pull cells) were measured while altering the configuration voltages using MATLAB.

Although the initial idea was to implement all 10 cells, only one of each was actually implemented. This was due to the ongoing need to carry out detailed tests on the individual

behaviour of each cell after implementation. These tests identified some problems that required corrections. As a result, there was not enough time left in the end to implement the other 8 cells and, consequently, to test the set as a multi-cell prototype.

4.1 Block Bias Analysis

In this section, the detailed results of the individual behaviour of each implemented cell are presented, as well as the results relating to their respective blocks.

A detailed description of how the individual blocks of this circuit work has already been presented in Chapter 3. The aim of this chapter is to provide a comprehensive overview of the final implementation of the prototype and the results obtained from this implementation. Therefore, in this context, it is not necessary to repeat the explanation of the composition of the base cell or the operating principle of each block.

4.1.1 1st block bias

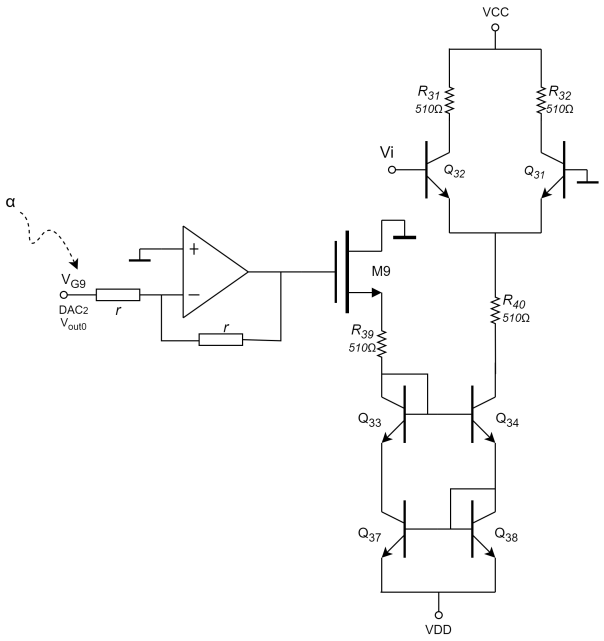


Figure 4.5: 1st Block Diagram

The first block, shown in Figure 4.5, responsible for the input scalling, α, in the transfer function represented in the equation (3.3), causes the output to fluctuate according to the voltage at the gate of transistor M9. This relationship is graphically depicted in the Figure 4.6.

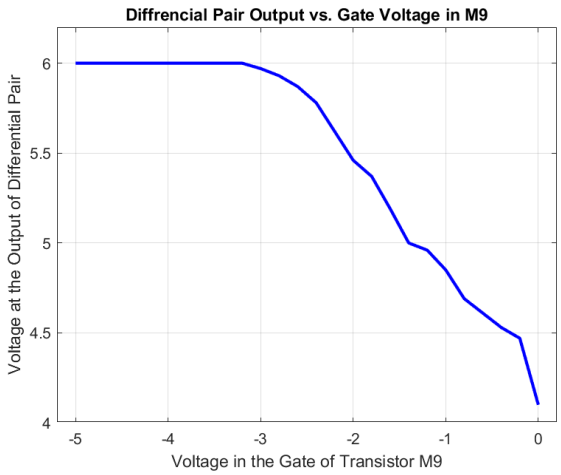


Figure 4.6: Biasing Values Graph of the 1st Block Block

Within the voltage range of -3.2 V to 0.0 V, the behavior of the differential pair exhibits linearity, resulting in a signal swing from 6.0 V to 4.1 V.

4.1.2 2nd and 3rd blocks bias

Figures 4.7 and 4.8 represent blocks 2 and 3 of the unit cell respectively.

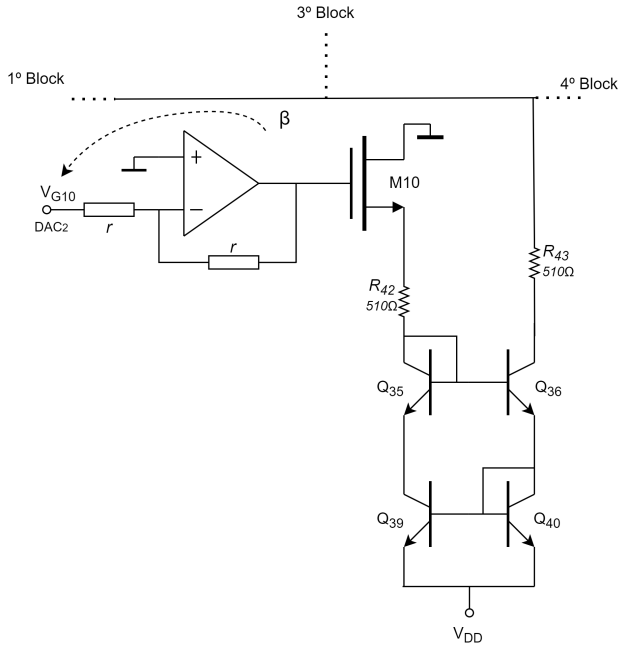


Figure 4.7: 2nd Block Diagram

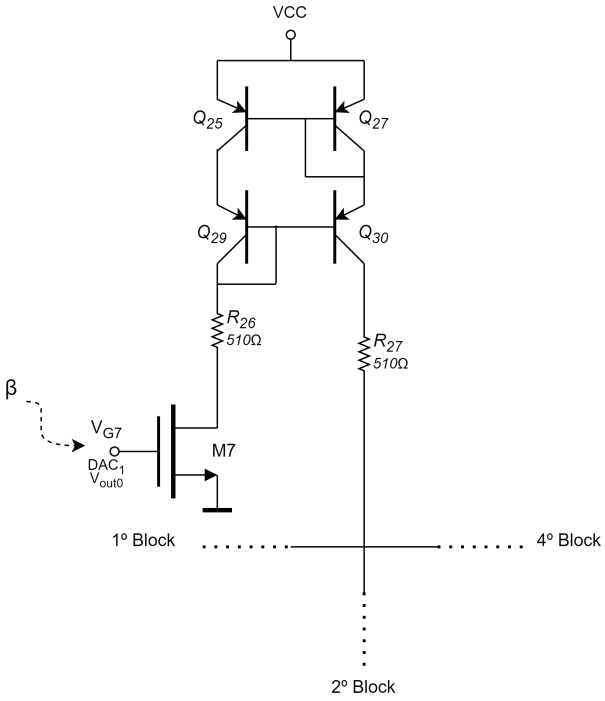


Figure 4.8: 3rd Block Diagram

The bias behavior of the second and third blocks, is shown in Figure 4.9 and Figure 4.10, respectively.

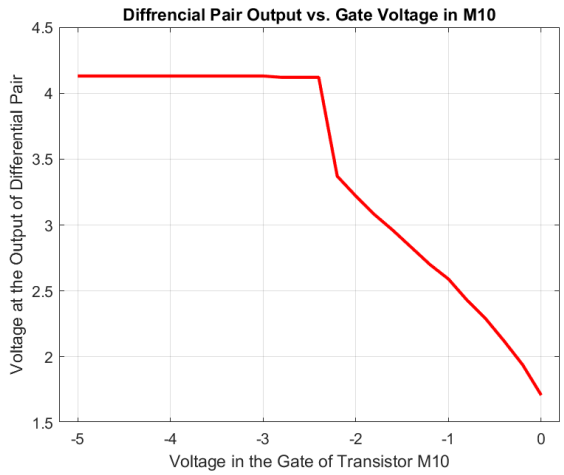


Figure 4.9: Biasing Values Graph of the 2nd Block

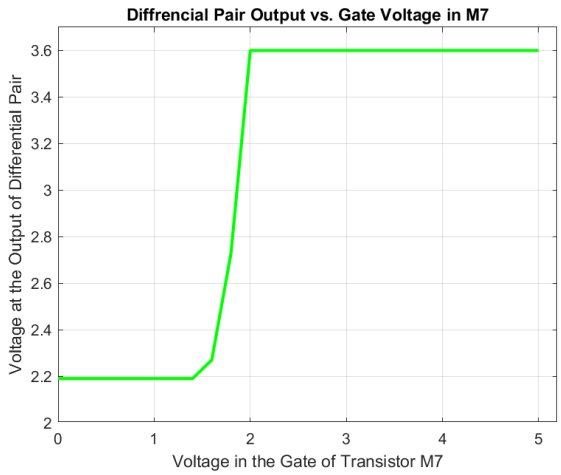


Figure 4.10: Biasing Values Graph of the 3rd Block

To test the second block, a voltage of 0.0 V was applied to the gate of M9 to determine if it is possible, with the assistance of the second block, to achieve a larger excursion. The first block alone allowed a maximum voltage of 4.1 V.

The Figure 4.9 illustrates the polarization of the second block, showing voltage fluctuations between 4.13 V and 1.71 V.

As for the third block, it was tested with V_{G9}=0.0V, V_{G10}=0.0V, and a voltage of 2.19V at the collector of transistor Q_{31}. In consequence, it is noticeable in Figure 4.10 that as the current I_{R27} increases due to the rise in voltage V_{G7}, the voltage at the collector of transistor Q_{31} decreases. The voltage ranges from 2.19 V to 3.60 V.

4.1.3 4th block push and pull bias

Let's proceed to analyze the bias of the push and pull cells, which are shown in Figure 4.11 and Figure 4.12, respectively.

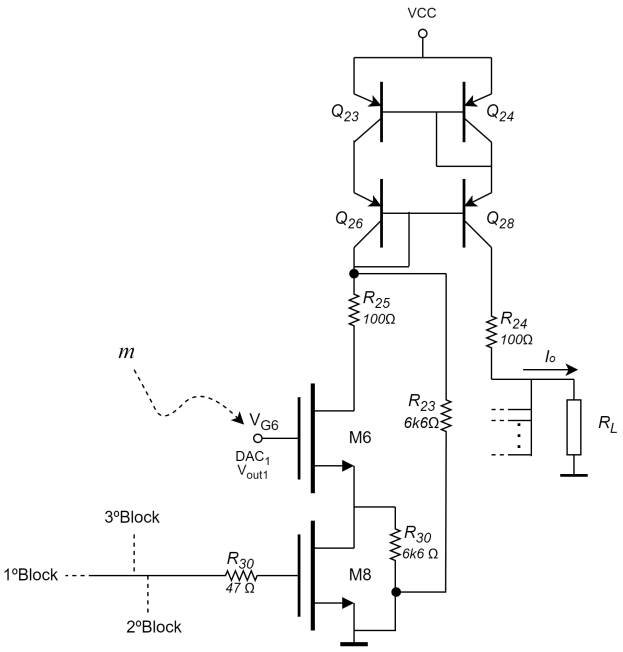


Figure 4.11: 4th Block Push Cell Block Diagram

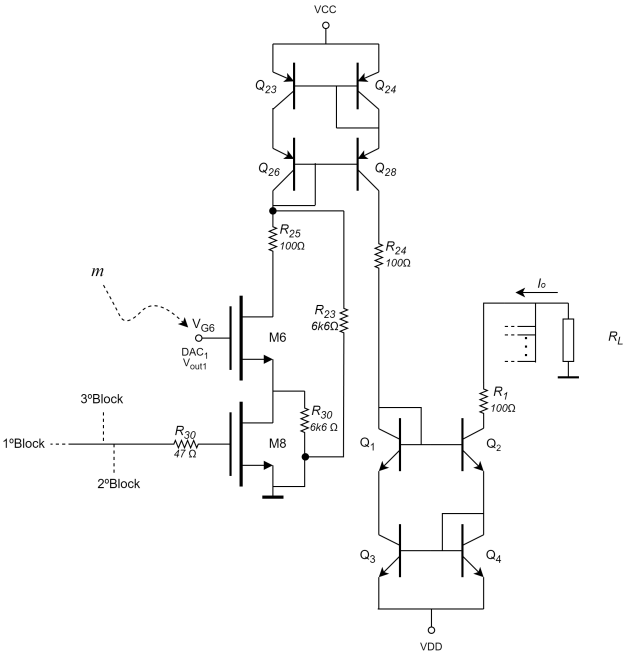


Figure 4.12: 4th Block Pull Cell Block Diagram

Closely resembling the scenario in Chapter 3, the voltage at the collector of Q_{31} is also the voltage responsible for driving MOSFET M8. Therefore, with a constant gate voltage of 4.35 V applied to transistor M8, variations in the voltage at MOSFET M6 yielded an output voltage range at the Push Cell, ranging from 0 V to 4.96 V, see Figure 4.13, and the pull cell with an output range of 0 V to -4.97 V, see Figure 4.14.

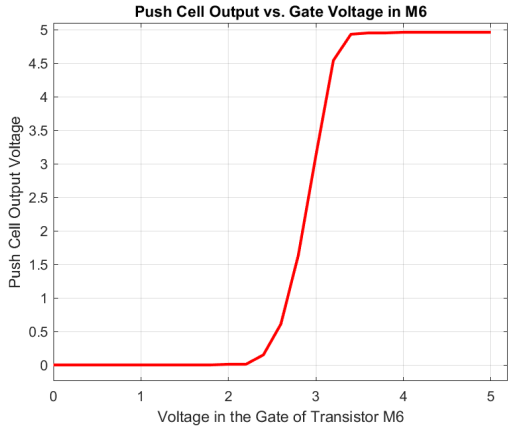


Figure 4.13: Biasing Values Graph of the 4th block push cell

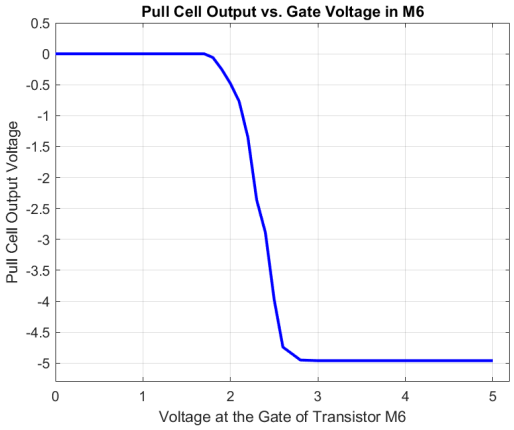


Figure 4.14: Biasing Values Graph of the 4th block pull cell

4.2 Low Frequency Analysis

As a continuation of the study, and with the DC bias of the circuit established in a previous phase, the next step involves applying an input signal to the circuit. This will facilitate the evaluation of the unit cell's dynamic response in the time domain.

4.2.1 Low frequency 1st block analyses

One of the first things to be done in the circuit after changing the resistors to 510 Ω was to analyse the gain of the differential pair, so the peak-to-peak voltage at the output of the Q_{31} collector was also measured in order to analyse the gain imposed by it. The graph in Figure 4.15 illustrates the gradual increase in the output peak-to-peak voltage as a function of the increase in voltage at the gate of the MOSFET M9, which in turn leads to an increase in current in the current source and in the differential pair.

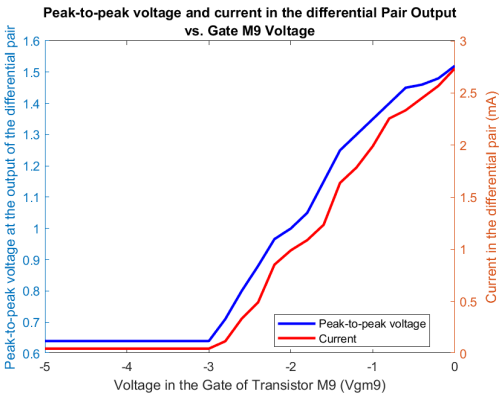


Figure 4.15: Peak-to-peak voltage in the diffrencial pair output vs. gate M9 voltage

Figure 4.16 shows the increase in gain in the differential pair as a function of the current flowing in transistor Q_{31}.

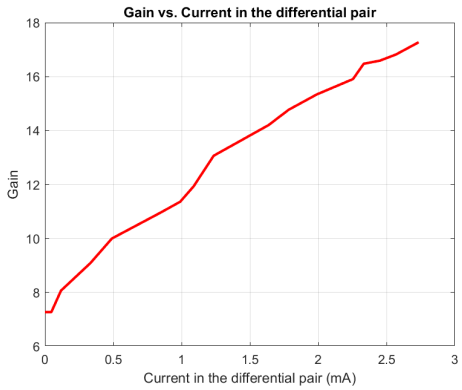
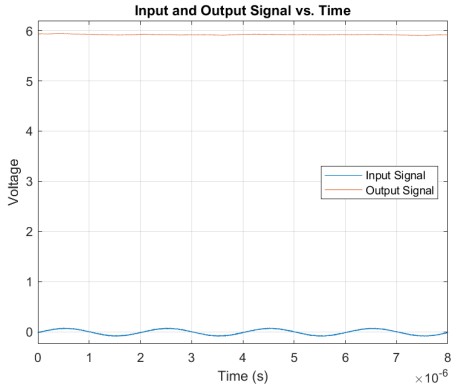
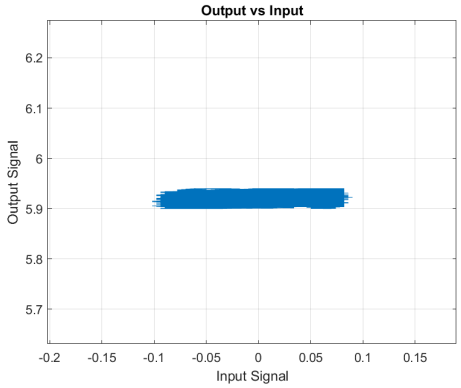


Figure 4.16: Gain vs. Current in the differential pair

A signal with an amplitude of 88 mV_{pp} and a frequency of 500 kHz was applied to the gate of transistor Q_{32}. Following that, the signal at the collector of transistor Q_{31} was measured while varying the gate voltage of M9 transistor. This allowed for the analysis of the input/output behavior of the differential pair, representing the parameter α of the unit cell, which has the capability to modify the signal gain.

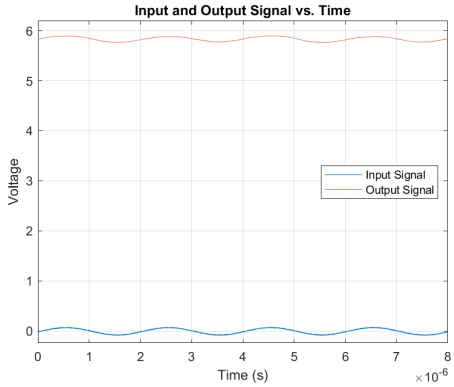


(a) Output signal at collector Q_{31} in the time domain

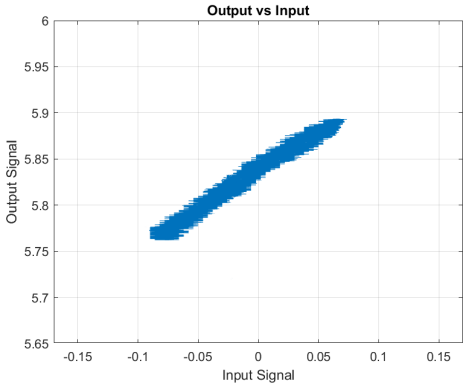


(b) Output signal at collector Q_{31} as a function of the input signal

Figure 4.17: Analysis of the signal from the 1st Block with V_{G_9}=-3.0V



(a) Output signal at collector Q_{31} in the time domain



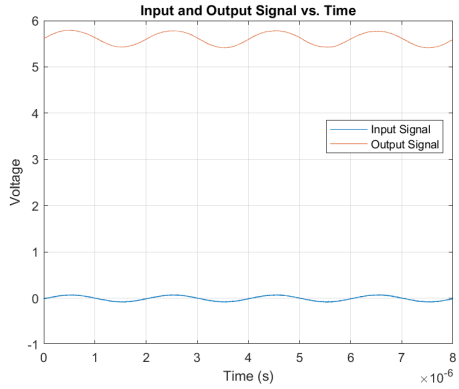
(b) Output signal at collector Q_{31} as a function of the input signal

Figure 4.18: Analysis of the signal from the 1st Block with V_{G_9}=-2.5V

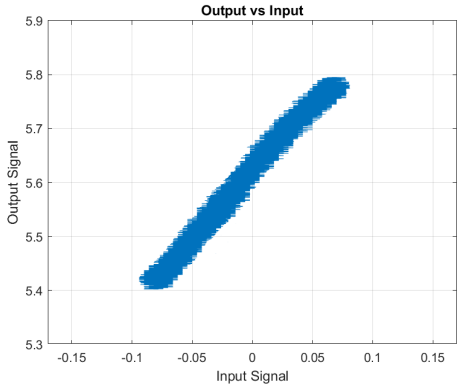
The graph in Figure 4.17a depicts the output at the collector of Q_{31} when a voltage of -3.00V was applied to the gate of MOSFET M9. The output signal remains close to 6 V with a very small excursion, as V_{GS} is less than the threshold voltage V_{th} and the MOSFET is in the cutoff region (see chapter 3).

Figure 4.17b illustrates the output's behavior as a function of the input.

Subsequently, a voltage of -2.5 V was applied to the gate of MOSFET M9. In this graph,4.18a, it is noticeable that the MOSFET starts conducting some current, resulting in a slightly larger signal excursion at the collector of Q_{31}. The signal goes from 5.90 V down to 5.72 V.

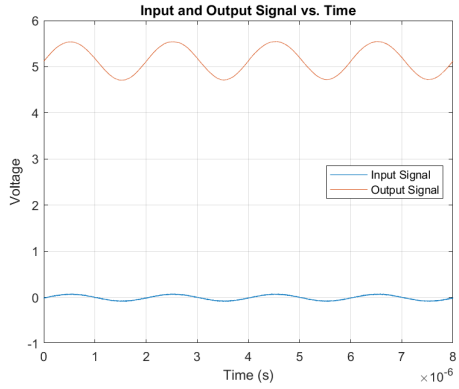


(a) Output signal at collector Q_{31} in the time domain

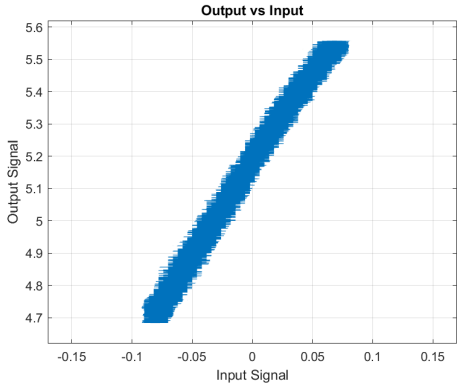


(b) Output signal at collector Q_{31} as a function of the input signal

Figure 4.19: Analysis of the signal from the 1st Block with V_{G9}=-2.0 V



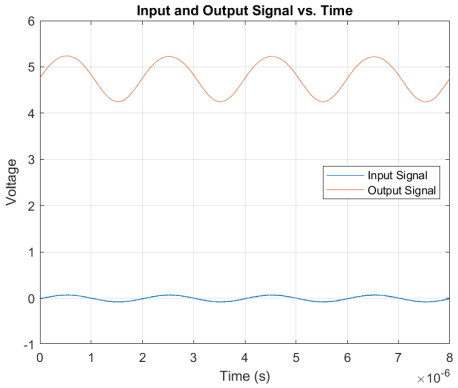
(a) Output signal at collector Q_{31} in the time domain



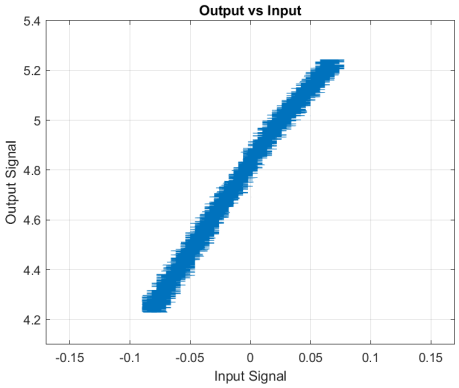
(b) Output signal at collector Q_{31} as a function of the input signal

Figure 4.20: Analysis of the signal from the 1st Block with V_{G_9}=-1.0 V

As the voltage at the gate of M9 transistor changes from V_{G9} = -2.0 V to V_{G9} = -1.0 V, it can be observed in the XY graphs depicted in Figure 4.19b and Figure 4.20b that the signal at the collector of transistor Q_{31} gradually expands until it reaches maximum expansion when the gate voltage of M9 MOSFET is zero. At that moment, not only is the current I_{R32}, as shown in Figure 3.15, at its maximum, but also the gain imposed by the differential pair on the input signal. Figures 4.21a and 4.21b represent the case where V_{G9} = 0.0 V.



(a) Output signal at collector Q_{31} in the time domain



(b) Output signal at collector Q_{31} as a function of the input signal

Figure 4.21: Analysis of the signal from the 1st Block with V_{G_9}=0.0 V

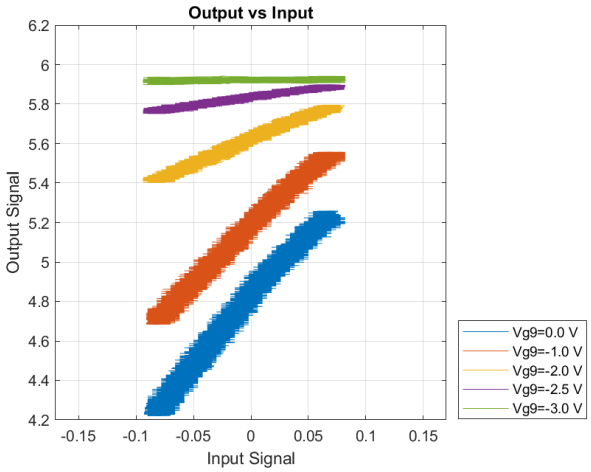


Figure 4.22: Combined XY plots from the 1st Block

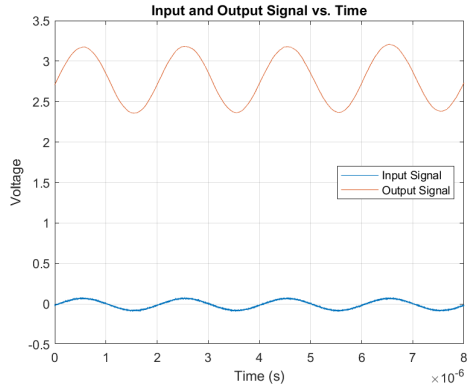
As with the analysis of the first block in chapter 3, it is possible to see in figure 4.22 that the gain of the 1st block depends on the gate voltage of the M9 MOSFET.

4.2.2 Low frequency 2nd and 3rd block analyses

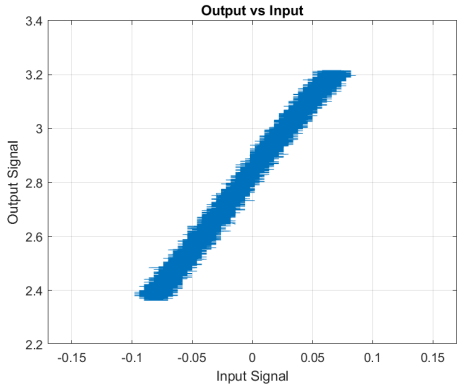
After analyzing the behavior of the first block, it is now time to examine the behavior of the blocks responsible for the β parameter in the transfer function equation (3.3).

In this section, the analysis will cover blocks 2, as depicted in Figure 4.7, and 3, as shown in Figure 4.8, while keeping the gate voltage of MOSFET M9 at V_{G9}=0.0V. This configuration allows the differential pair to conduct with the maximum current from the current source, keeping the gain of the differential pair constant.

Consequently, by adjusting the current flowing through the resistors R_{43} and R_{27}, it becomes possible to increase or decrease the voltage drop across resistor R_{32}, see Figure 3.15.

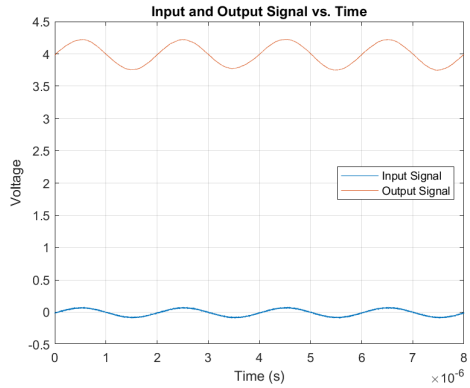


(a) Output signal at collector Q_{31} in the time domain

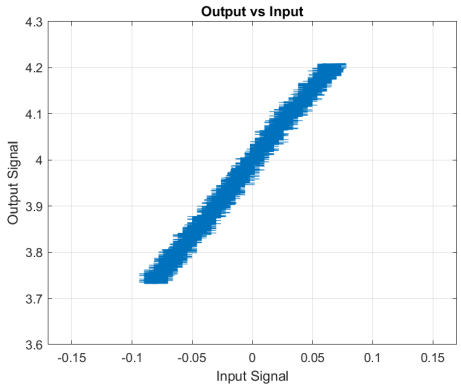


(b) Output signal at collector Q_{31} as a function of the input signal

Figure 4.23: Analysis of the signal from the 2nd and 3rd Blocks with V_{G9}=0.0 V,V_{G7}=0.0 V,V_{G10}=-0.67 V



(a) Output signal at collector Q_{31} in the time domain

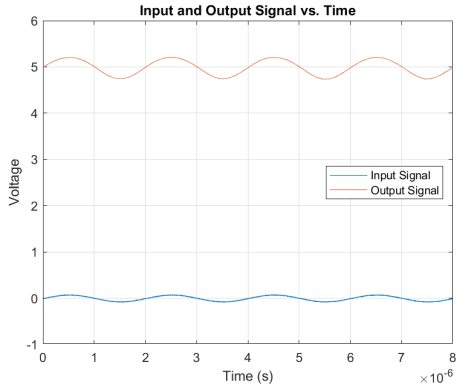


(b) Output signal at collector Q_{31} as a function of the input signal

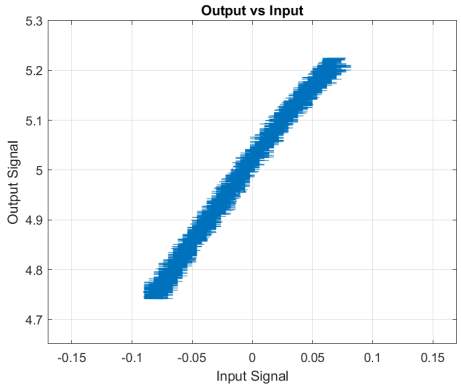
Figure 4.24: Analysis of the signal from the 2nd and 3rd Blocks with V_{G9}=0.0V,V_{G7}=2.0V,V_{G10}=-0.67V

Within Figures 4.23a and 4.23b, the output signal at the collector of Q_{31} is observed when the gate voltage V_{G10} is set to -0.67 V. In this particular operational state, the MOSFET M10 is in the conducting mode, resulting in an increase in the current through the resistor R_{43}. Since M7 transistor remains cut off, with V_{G7} at 0.0 V, the current I_{R32} increases correspondingly, causing the signal to reach a maximum value at the collector of V_{CQ32}= 3.23 V and a minimum value of V_{CQ32}= 2.35 V.

As the gate voltage of M7 MOSFET, V_{G7}, is raised to 2.0 V, the transistor begins to conduct. This leads to an increase in the current I_{R27}. Consequently, the current I_{R32} decreases, and the signal now attains a maximum value at the collector of V_{CQ32}=4.23 V and a minimum value of V_{CQ32}=3.72 V, see Figure 4.24a.



(a) Output signal at collector Q_{31} in the time domain



(b) Output signal at collector Q_{31} as a function of the input signal

Figure 4.25: Analysis of the signal from the 2nd and 3rd Blocks with V_{G9}=0.0V,V_{G7}=2.0V,V_{G10}=-2.2V

In Figures 4.25a and 4.25b, MOSFET M10 is operating in a nearly cutoff mode with a gate voltage of V_{G10} = -2.2 V. As previously explained in the "Block Bias Analysis" subsection of this chapter, this configuration results in a reduction of current I_{R43}, leading to a decrease in current I_{R32} as well,See Figure 4.7 and Figure 4.8 for a more straightforward understanding of the mentioned components. Consequently, the signal at the collector of transistor Q_{32} undergoes a shift along the Y-axis due to the decreased voltage drop.

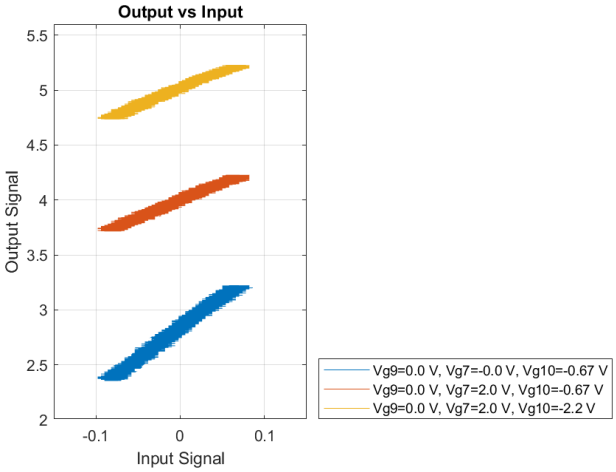


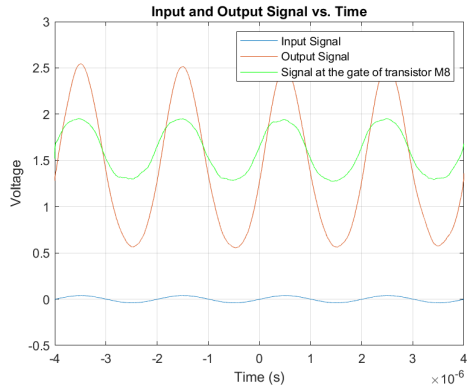
Figure 4.26: Combined XY plots from the 2nd and 3rd Blocks

The graph shown in Figure 4.26, not only shows that by changing the β parameter the output signal undergoes different offsets, but also shows that for lower voltages on the collector of the Q_{31} transistor the signal gain is affected, even though this is not supposed to happen, as the voltage at the gate of the MOSFET M9 has not been changed.

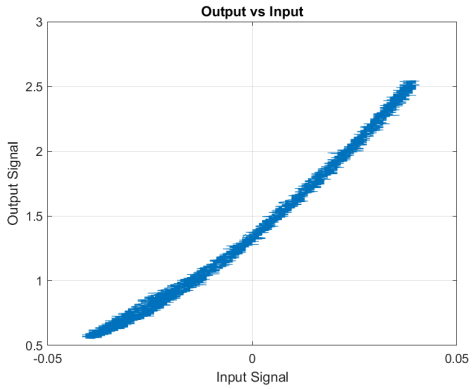
4.2.3 Low frequency 4th push cell block analyses

In the following graphs, the output signal of the push cell is analyzed, as illustrated in Figure 4.11, under various conditions. This includes varying the parameters α and β, which

operate on the input signal, as well as the parameter m, which provides scaling at the output. In this section, the overall performance of the unit cell will be evaluated, and the various resulting signal outputs will be examined. Throughout this section, see the block diagram in Figure 4.11 to keep track of the mentioned components.

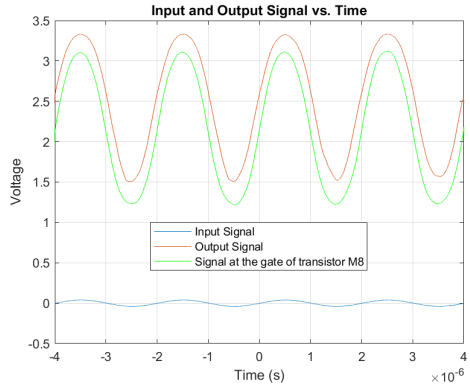


(a) Push Unit Cell Output signal in the time domain

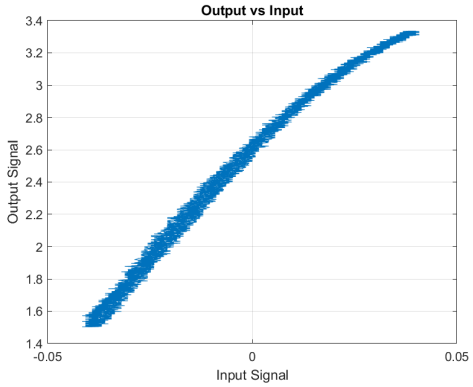


(b) Push Unit Cell Output signal as a function of the input signal

Figure 4.27: Analysis of the signal from the 4th block Push Cell with V_{G9}=-1.76 V,V_{G10}=0.0 V,V_{G6}=4.17 V



(a) Push Unit Cell Output signal in the time domain

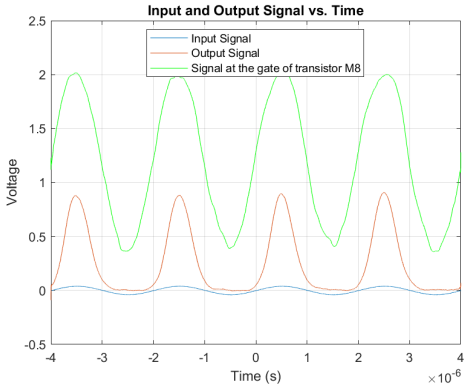


(b) Push Unit Cell Output signal as a function of the input signal

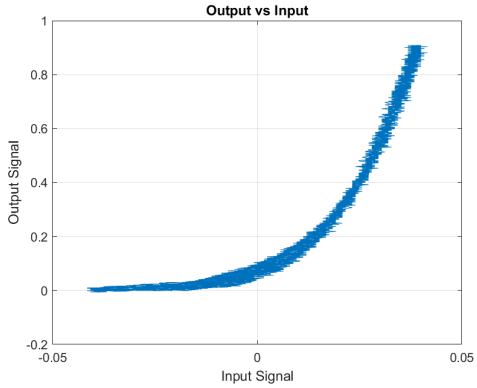
Figure 4.28: Analysis of the signal from the 4th block Push Cell with V_{G9}=-0.76 V,V_{G10}=-1.57 V,V_{G6}=2.51 V

In Figure 4.27a, both the M8 and M6 MOSFETs are conducting, and since the M6 MOSFET already has a voltage of V_{G6}= 4.17 V, the reason for the signal excursion not being higher is due to the fact that the input signal at the M8 transistor gate does not reach values high enough for M6 to conduct more current.

In Figure 4.28b, despite having decreased the voltage to V_{G6}= 2.51 V, the output signal ranges from 1.50 V to 3.33 V, both the maximum and minimum values have increased. This happens because, by reducing the V_{G10} voltage to -1.57 V, the input signal now has higher values due to the decrease of the R_{32} resistor's current, resulting in an increased current conducted by the M8 MOSFET.



(a) Push Unit Cell Output signal in the time domain



(b) Push Unit Cell Output signal as a function of the input signal

Figure 4.29: Analysis of the signal from the 4th block Push Cell with V_{G9}=-1.1 V,V_{G10}=0.0 V,V_{G6}=4.22 V

In the last measurement of the cell, shown in Figure 4.29a, even though the voltage on the M6 MOSFET was increased again, the output signal ranges from -0.09 V to 0.91V. This results from the increase in voltage on the M10 MOSFET, resulting in lower voltage values at the gate of transistor M8. As a result, M8 conducts less current, leading to reduced current flow in the output block and consequently a smaller voltage drop across the resistance R_L.

Similarly to the 4th block of the prototype, when the input signal is in the positive half-cycle, MOSFET M8 conducts because its source voltage is connected to ground, and, therefore, its conduction depends largely on the gate voltage. Thus, for gate voltage values at the M8 gate input below the conduction threshold, approximately $V_{GS} = 1.6$ V, transistor M6 does not conduct.

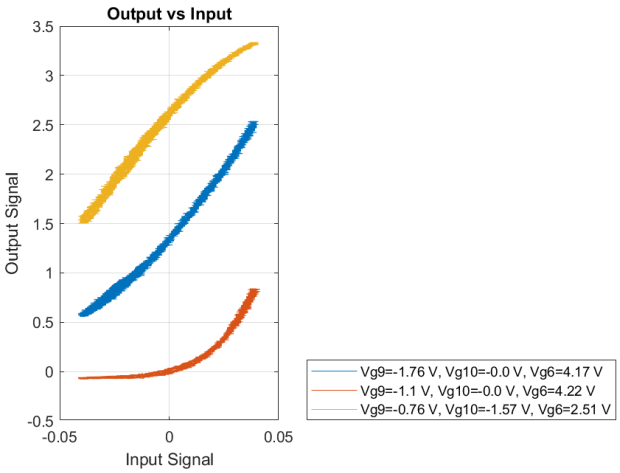
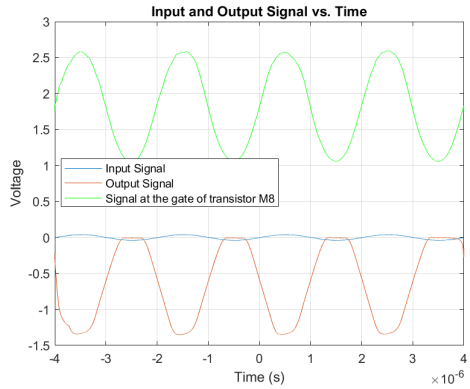


Figure 4.30: Combined XY plots from the push cell

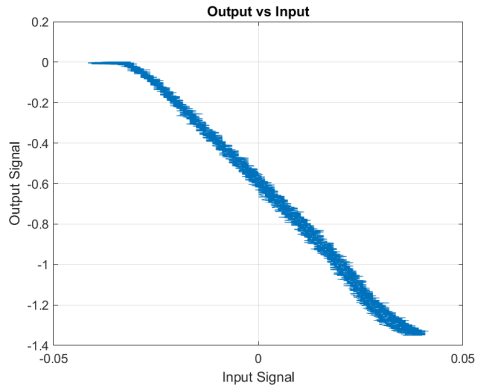
In Figure 4.30, it is possible to see the different waveforms that the push cell can achieve by varying the different parameters, α, β and m.

4.2.4 Low frequency 4th pull cell block analyses

By varying the configurable voltages of the circuit, measurements were taken to demonstrate not only the behavior and impact of the final block but also to assess how changes in the α and β parameters affect the output signal. To better understand this analysis see Figure 4.12, where it is represented de block diagram of the Pull Cell.

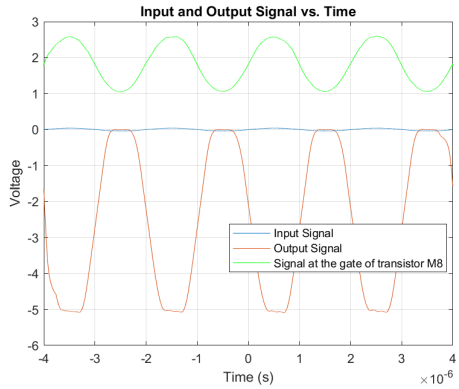


(a) Pull Unit Cell Output signal in the time domain

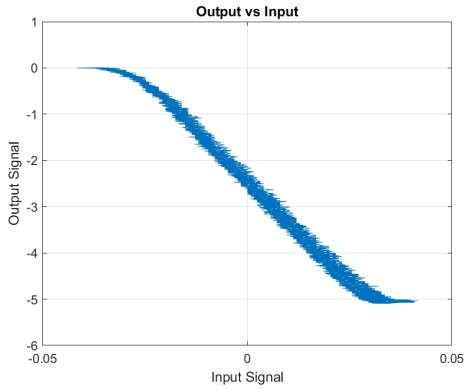


(b) Pull Unit Cell Output signal as a function of the input signal

Figure 4.31: Analysis of the signal from the 2nd and 3rd Blocks with V_{G9}=0.0 V,V_{G10}=-0.13 V,V_{G6}=2.12 V



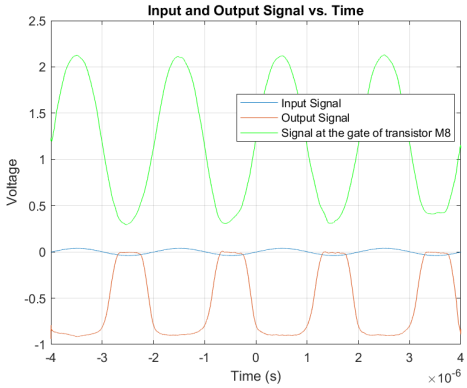
(a) Pull Unit Cell Output signal in the time domain



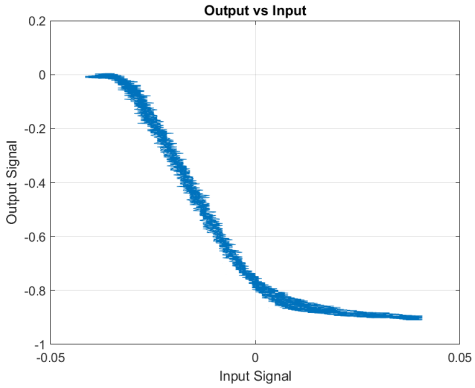
(b) Pull Unit Cell Output signal as a function of the input signal

Figure 4.32: Analysis of the signal from the 2nd and 3rd Blocks with V_{G9}=0.0 V,V_{G10}=- 0.13 V,V_{G6}=3.41 V

The two Figures above, 4.31a and 4.32a, depict the behavior of the last block while keeping the voltages V_{G9} and V_{G10} constant and only varying the voltage V_{G6}. As can be observed, increasing the voltage at MOSFET M6 results in higher current in the branches of the current mirror, leading to a greater voltage drop across the load. Consequently, the output signal reaches a minimum voltage value of -5.09 V.



(a) Pull Unit Cell Output signal in the time domain



(b) Pull Unit Cell Output signal as a function of the input signal

Figure 4.33: Analysis of the signal from the 2nd and 3rd Blocks with V_{G9}=-0.95V,V_{G10}=-0.20 V,V_{G6}=2.0 V

Finally, in the Figure 4.33a, even though the voltage at the gate of MOSFET M10 was altered to V_{G10} = -0.95 V, increasing the current in transistor M8, the voltage at the gate of MOSFET M6, V_{G6}, was reduced to 2.0 V. Consequently, the current conduction decreased, which caused the output signal to reach only -0.94 V in the positive half of the input signal and 0.0 V in the negative half (when M6 is not conducting).

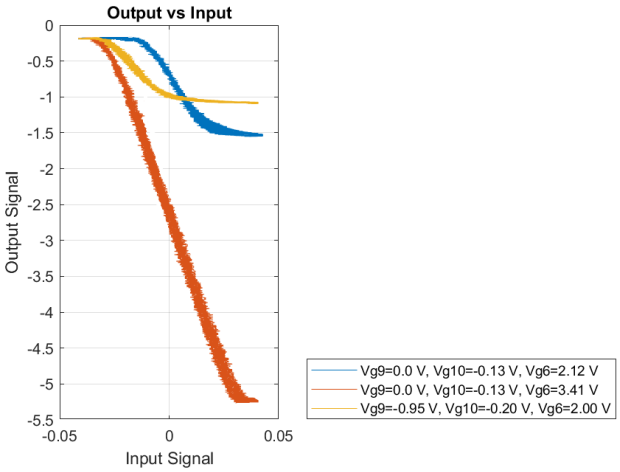


Figure 4.34: Combined XY plots from the pull cell

In Figure 4.34, it is possible to see the different waveforms that the pull cell can achieve by varying the different parameters.

4.2.5 Study of the Push Unit Cell response with input signal at high frequency

Just as it was done in Chapter 3, where the prototype of this circuit was analyzed, testing the circuit at high frequencies involved measuring the peak-to-peak voltage at low frequencies and gradually increasing it until this voltage reached a -3 dB drop.

Applying a 500 kHz input signal with an 80 mV_{PP}, as demonstrated in Figure 4.35, it was possible to verify that the peak-to-peak output voltage is equal to V_{PP} = 2.08 V.

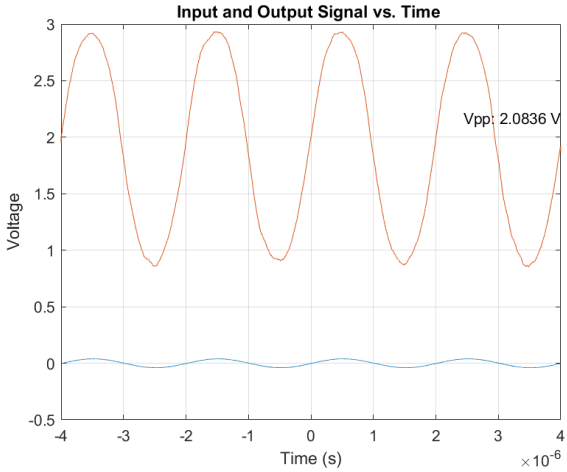
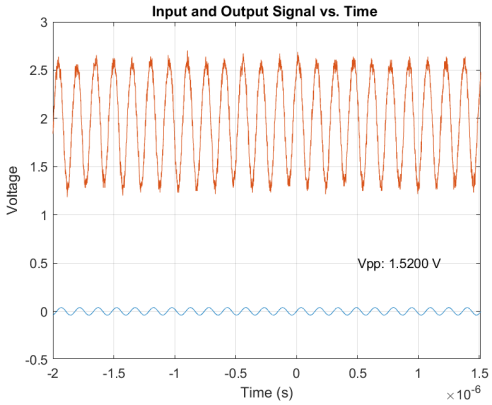
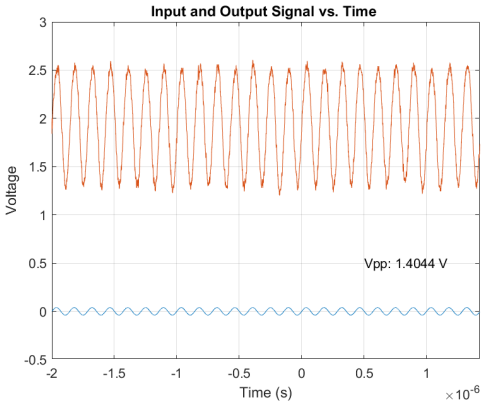


Figure 4.35: Output signal of the push unit cell with a 500kHz input signal

The high cut-off frequency is reached when the signal drops by -3 dB, meaning when the peak-to-peak output voltage is less than the value of 1.47 V.



(a) Output signal of the pull unit cell with a 6.614 MHz input signal



(b) Output signal of the pull unit cell with a 7.02 MHz input signal

Figure 4.36: Output signal of the pull unit cell with a 6.614 MHz and 7.02 MHz input signal

Based on the data presented in Figures 4.36a and 4.36b, it is evident that with an input signal frequency of 6.614 MHz, the V_{PP} value stays consistently above 1.47V. It is not until we reach a frequency of 7.02 MHz that the output signal experiences the -3 dB drop, indicating an upper cutoff frequency of around 7 MHz.

4.2.6 Study of the pull unit cell response with input signal at high frequency

Considering the various modifications to the differential pair resistors and the consequent changes to the bandwidth resulting from these modifications, we can state that the bandwidth is predominantly influenced by the behaviour of the differential pair. Based on this observation and considering that a detailed bandwidth analysis has already been conducted for the push cell in this chapter, it is valid to assume that, due to the structural similarity between this cell and the current one, where the main addition is a current mirror, we can estimate a bandwidth of approximately 7 MHz for the current configuration.

CHAPTER 5

Conclusions and Future Work

After a long and challenging journey, this dissertation has enabled a deeper understanding of various concepts, including analog electronics, circuit design and dimensioning, PCB design in Altium, and component assembly.

A prototype for the configurable analog circuit was developed and tested, with a primary goal of achieving configurability through the application of specific control voltages. This approach resulted in an analog circuit capable of implementing configurable functions. Throughout the circuit's development, the main emphasis remained on the intention of minimizing power consumption, with the focus on maintaining low power usage while achieving configurability and a reasonable bandwidth.

Nonetheless, it is vital to acknowledge the following aspect when aiming for the ideal bandwidth. The prior version of the circuit was simulated to operate up to frequencies of around 100 MHz, with a collector resistance in the differential pair set to $50\,\Omega$. While considering the substantial difference between the initial $50\,\Omega$ resistance and the $510\,\Omega$ resistance implemented in the collector of the circuit, and taking into account an estimated bandwidth of approximately 7 MHz in the circuit, it becomes evident that the primary limitation in achieving a 100 MHz bandwidth stems from the characteristics of the discrete components within the differential pair. Despite being necessary to increase the resistance to accommodate the components, it affected the achievable bandwidth.

There are several aspects that are worth taking into account in the future. Firstly, exploring the possibility of soldering all the cells, including the 5 push cells and the 5 pull cells, in order to generate more complex waveforms. This could provide valuable information on the circuit's performance and extend its capabilities. Additionally, it could be advantageous to contemplate the shift from using discrete components in the circuit towards an integrated circuit approach. An enticing step forward could involve designing a new cell specifically tailored for integrated circuits. For the development of this integrated circuit, the collaboration between the University of Aveiro and EUROPRACTICE, a consortium of renowned European research organizations, is an asset that allows system integration solutions and small volume

production at a reduced cost.

APPENDIX A

Schematics in Altium

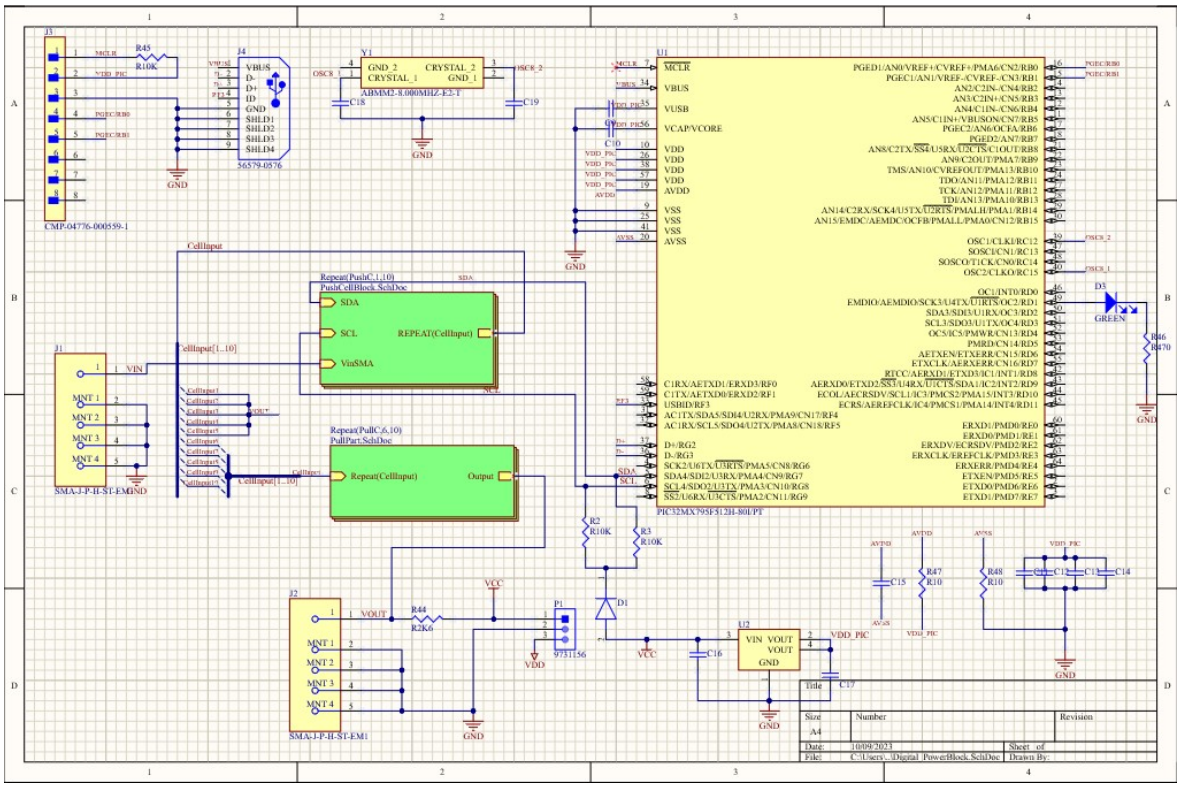


Figure A.1: Digital Part Diagram in Altium

APPENDIX B

MATLAB code

TestScript.m

```
%% Script for testing SetVoltage
clear all
close all
clc

%open the USB link
h = OpenUsbLink();

%Set the voltage
SetVoltage(h,hex2dec('62'),0,0.0); %M7 A DAC 2 é que alimenta as gates dos transistores M6 e M7, não tem OP-AMP inversor
SetVoltage(h,hex2dec('62'),1,0.0); %M6

SetVoltage(h,hex2dec('61'),1,5.0); % OpAmpOut2 M10
SetVoltage(h,hex2dec('61'),0,0.0); % OpAmpOut1 M9

%close the USB link
CloseUsbLink(h);
```

Figure B.1: Matlab Code to control the gate's voltages

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