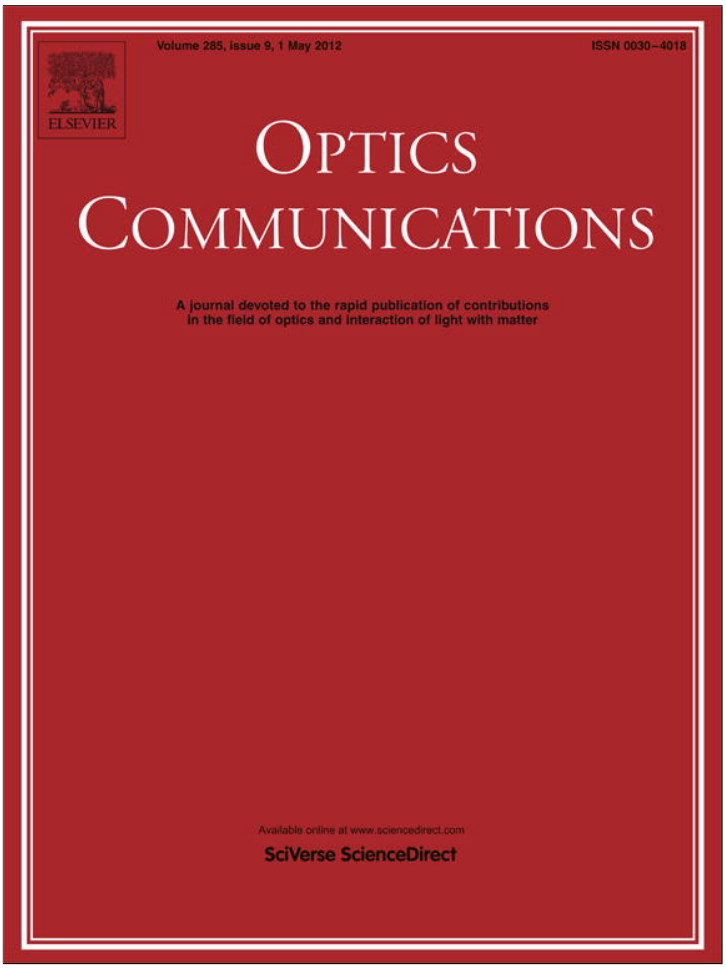

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Theoretical analysis of all-optical clocked D flip-flop using a single SOA assisted symmetric MZI

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ABSTRACT

A novel scheme for an all-optical clocked D flip-flop, with very low complexity, is proposed and numerically demonstrated. This new flip-flop configuration is based on a semiconductor optical amplifier — Mach–Zehnder interferometer (SOA-MZI), with a feedback loop, and presents two stable states determined by the phase shift between the two MZI arms.

1. Introduction

With the fast growth of bandwidth demand from network users, is desirable that switching and routing can be carried out in the physical layer, to enhance the efficiency of the network and to allow higher data rates [1]. The optoelectronic conversion, in the traditional cases required for acting in routing information, may impose a technological bottleneck, which limits the traffic capacity that can be processed [2].

An all-optical flip-flop is a key building block in next generation photonic transmission systems, and it can act as temporary storage of header related information, while the payload of a packet is routed to the output port [3].

In the last few years, considerable research has been done for the development of all-optical flip-flops. In [4] and [5], all-optical flip-flops, based on the gain quenching effect, were demonstrated using two coupled laser diodes and two SOA fiber ring lasers, respectively. In [6], an all-optical flip-flop was proposed based on a Mach–Zehnder interferometer, with distributed Bragg reflectors (DBRs) and saturable absorbers, to obtain single-mode laser operation and hysteresis. The latter flip-flop configuration overcomes the issues of MMI-BLD flip-flop scheme proposed in [7], since the two cross-coupled lasing modes have, theoretically, 100% spatial overlap. In [8], an all-optical one-bit memory was demonstrated using a single distributed feedback (DFB) laser diode, showing a very fast operation speed, with low switching energies. All of these different technologies for optical buffering are all-optical asynchronous flip-flops. Therefore, any change of information in the inputs is transmitted, immediately, to the output, rather than changing in a determined instant.

The all-optical D flip-flop scheme, proposed in this paper, works with a synchronization signal (clock), therefore is capable to control the timing when the information is stored. Since this flip-flop architecture only uses a single SOA-MZI, is significantly simpler to implement than the all-optical clocked D flip-flop that was experimentally demonstrated in [9], which required two coupled SOA-MZI.

The bistability of the proposed configuration is caused by the external feedback loop, and due to the interferometric structure of this flip-flop configuration, its operation principle relies on the dependency of the refractive index on the carrier density of the SOA.

The paper is organized as follows: in Section 2, we describe the proposed all-optical flip-flop concept, showing its theoretical model and the possible operation cases that can occur. The obtained simulation results and further discussion are presented on Section 3. In Section 4 it is shown the effect on the output waveforms of different loop lengths. Finally, in Section 5 the conclusions are drawn.

2. All-optical clocked D flip-flop

An all-optical clocked D flip-flop overcomes some issues of the optical clocked S-R flip-flop, namely it removes the forbidden state that

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occurs when both set and reset inputs are at the high state ('1'). Therefore, it is possible to predict, theoretically, for every possible case, the D flip-flop output, according to Table 1.

The proposed all-optical D flip-flop scheme is illustrated in Fig. 1, and it is based on a single SOA-MZI, with an external feedback between the output Q and the inputs. The scheme actually exploits the possibility of using both output switching ports of SOA-based interferometers, which has been thoroughly investigated in [10]. The loop has an optical delay line (ODL) and an optical attenuator (ATT), in order to synchronize and to equalize the power of the input data signals that enters in the circuit from interferometric ports #B and #C [11]. The objective of the feedback loop is to maintain the flip-flop's previous state, in the absence of the clock input signal. The feedback loop length should be such that the data can reach to the port #C of the MZI when the gain recovery of the SOA takes place, otherwise the optical data can reach to the unwanted port, due to crosstalk. This fact will be investigated and quantified, in more detail, in Section 4. The SOA-MZI used in the numerical simulations is a uniformly symmetric device, with the exactly same optical path on both MZI arms.

In electronics, an input of a clocked D flip-flop is referenced as 'data' and its state can be changed with 'clock' (CLK) input. In this manuscript, we also use the same convention. Here, the incoming signal of MZI is considered as 'data pulse' and the strong control pulse is considered as 'clock (CLK) pulse'. This 'clock pulse' enables the flip-flop to change its state; otherwise it holds the previous state. The power at the flip-flop output Q (port #I) is a result of an interference process, that can be constructive or destructive, depending on the internal phase condition of the interferometer. So, when the control signal (CLK) is 'ON', the data of the input port (D) reaches to its corresponding bar-port (port #I). On the other hand, if CLK = OFF then the incoming signal emerges at its cross-port (port #J).

2.1. Theoretical model

Some assumptions were considered for the theoretical model of the clocked D flip-flop based on a symmetric SOA-MZI switch, namely that the incoming signal (D) should not affect the SOA gain dynamics. So, the incoming signal was selected ten times smaller than the control (CLK) pulse [12]. The gain and group-velocity dispersion were neglected, which is practically satisfied for pulse-width in the picosecond range. This essentially means that the incoming and clock signals travel through SOA at same speed, so their transit times are equal [13]. In [14], it was demonstrated that ASE becomes too high and influence the gain saturation only for SOAs longer than $1500\mu m$. Since the energy of the control pulse was less than 1 pJ, with a very narrow pulse-width, the two-photon absorption (TPA) and ultrafast nonlinear reflection (UNR) were also neglected [15]. Furthermore, the SOA small signal gain, internal loss and saturation energy were assumed to be wavelength independent and hence the same for both control and incoming signal, otherwise we would need to use the second order polynomial of the gain spectrum [16], which would increase the model complexity.

Table 1
Truth table of the optical clocked D flip-flop. Q_n: flip-flop's previous state; Q_{n+1}: flip-flop's next state; X: any logical state, 0 or 1.

D	CLK	Q_n	Q_{n+1}	Remarks
1	1	×	1	Set
1	0	1	1	Unchanged
0	0	1	1	Unchanged
0	1	×	0	Reset
0	0	0	0	Unchanged
1	0	0	0	Unchanged

The saturation energy and unsaturated single-pass amplifier gain of the SOA can be expressed as [13,17,18]:

$$E_{sat} = \frac{\hbar\omega_0 wd}{a_N \Gamma} \tag{1}$$

$$G_0 = \exp[g_0 L - \alpha_D L] \tag{2}$$

$$g_0 = \Gamma a_N N_{tr}\left(\frac{I\tau_e}{qwdLN_{tr}} - 1\right) \tag{3}$$

where, E_{sat} is the saturation energy of the SOA, G_0 the unsaturated single-pass amplifier gain, $\Gamma$the confinement factor, a_N the differential gain, N_{tr} the carrier density at transparency, q the charge of a electron, w and d are, respectively, the width and the depth of the active region of SOA, L is the active length of SOA, α_D the internal loss of the waveguide and $\omega_o$the frequency. $\hbar = h/2\pi$, where h is the Plank constant.

When an optical pulse passes through a SOA, it is amplified and can be defined as [19]

$$P_{out}(t) = P_{in}(t)\cdot \exp[h(t)] \tag{4}$$

where, $P_{in}(t)$ and $P_{out}(t)$ are the power and phase of the input and output pulse, respectively.

From the following differential equation [19]

$$\frac{dh(t)}{dt} = \frac{g_0 L - h(t)}{\tau_e} - \frac{P_{in}(t)}{E_{sat}}\{\exp[h(t)] - 1\} \tag{5}$$

$h(t)$ can be calculated as

$$h(t) = -\ln\left[1 - \left(1 - \frac{1}{G_0}\right)\exp\left(-\frac{E_{cp}(t)}{E_{sat}}\right)\right] \tag{6}$$

When a clock pulse (CLK) is injected into the SOA assisted symmetric MZI switch, it saturates the SOA at time t_s and changes its index of refraction. The gain of the SOA decreases rapidly as [13]

$$G(t) = \exp[h(t)] \tag{7}$$

The energy fraction contained in the leading edge of the pulse until the $t' \le t$is given by

$$E_{cp}(t) = \int_{-\infty}^{t} P_{cp}\left(t'\right) dt' \tag{8}$$

By definition $E_{cp}(t \to \infty) = E_c$ = total energy of the control pulse. After a while, the gain recovers due to injection of carriers and can be obtained from the gain recovery formula [20]

$$G(t) = G_0\left[\frac{G(t_s)}{G_0}\right]^{\exp[-(t-t_s)/\tau_e]} \quad ; \quad t \ge t_s \tag{9}$$

where, τ_e is the gain recovery time.

When a periodic pulse train is injected into the SOA, there is no time for the recovery of the gain to G_0. Instead, it only recovers to a lower gain, G_l [21]. Hence, Eq. (7) takes the following form

$$G(t) = \left\{1 - (1 - 1/G_l)\exp\left[-E_{cp}(t)/E_{sat}\right]\right\}^{-1} \tag{10}$$

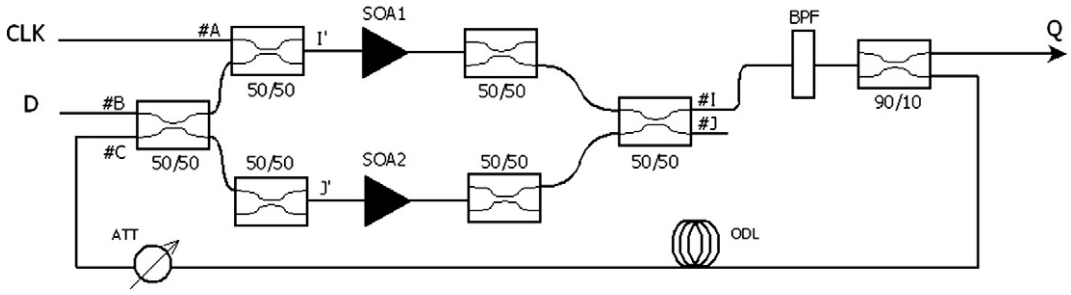

Fig. 1. Schematic representation of the all-optical D flip-flop based on a single SOA-MZI. D: incoming signal; CLK: clock signal; Q: flip-flop output; ODL: optical delay line; ATT: optical attenuator; BPF: band pass filter. The input ports of the MZI are A, B, C, D and output ports are I, J.

Considering a Gaussian pulse $P_{cp}(t)=\frac{E_c}{\sigma\sqrt{\pi}}\exp\left(-\frac{t^2}{\sigma^2}\right)$ as the clock signal and σ related to full width at half maximum (FWHM) by $T_{FWHM}\cong 1.665\sigma$, then we can write [13]

$$E_{cp}(t)=\frac{E_c}{2}\left[1+erf\left(\frac{t}{\sigma}\right)\right] \tag{11}$$

where, *erf*(.) is the error function.

The SOA saturation time is$t_s\approx T_{FWHM}$, then 99% of the pulse transmits through the SOA. So, from Eq. (10) we obtain

$$G_f=G(t_s)=\frac{G_l}{G_l-(G_l-1)\exp(-E_c/E_{sat})} \tag{12}$$

At the next bit period (ξ), SOA gain does not reach toG_0, but onlyG_l. So,

$$G_l=G(\xi)=G_0\left[\frac{G_f}{G_0}\right]^{\exp\{-(\xi-T_{FWHM})/\tau_e\}} \tag{13}$$

For the next pulse, the gain starts to decrease again and the same process is repeated. The output power at bar-port (Ⅱ) and cross-port (×) can be expressed as [22]:

$$P_{\shortparallel}(t)=\frac{P_{in}(t)}{4}\cdot\left\{G_1(t)+G_2(t)-2\sqrt{G_1(t)\cdot G_2(t)}\cdot\cos(\Delta\varphi)\right\} \tag{14}$$

$$P_{\times}(t)=\frac{P_{in}(t)}{4}\cdot\left\{G_1(t)+G_2(t)+2\sqrt{G_1(t)\cdot G_2(t)}\cdot\cos(\Delta\varphi)\right\} \tag{15}$$

where $G_1(t)$ and $G_2(t)$ are the gain of SOA_1 and SOA_2, respectively, at the time t and $\Delta\varphi=-\frac{\alpha}{2}\cdot\ln\left(\frac{G_1}{G_2}\right)$, where$\alpha$ is line-width enhancement factor. Therefore, after they recombine at the input coupler, the $\Delta\varphi\approx\pi$ and data will exit from the bar port (Ⅱ). At same time, the power at the cross port $=P_{\times}(t)\approx 0$.

In the absence of the clock signal (***CLK = OFF***), the incoming signal enters into the two arms of the MZI, propagates through both SOA at the same time, and experience almost the same unsaturated amplifier gain G_0. Therefore, the incoming signal passes through the 3 dB output coupler with $\Delta\varphi\approx 0$ (as $G_1\approx G_2$). So expression for $P_{\shortparallel}(t)\approx 0$ and$P_{\times}(t)\neq 0$.

The D flip-flop output (Q) has two possible states: one is its current state (Q_{n+1}) and the other is its previous state (Q_n). Depending on the different input conditions, the output state Q_{n+1} can be expressed as:

$$P_{Q_{n+1}}(t)\Big|_{Q_n=0}^{D=CLK=1}=\left(0.9P_{\shortparallel}(t)|_{Input=D}\right)_{HIGH} \tag{16}$$

$$P_{Q_{n+1}}(t)\Big|_{Q_n=1}^{D=CLK=1}=\left(0.9P_{\shortparallel}(t)|_{Input=D}\right)_{HIGH}+\left(0.9P_{\times}(t)|_{Input=Q_n}\right)_{LOW} \tag{17}$$

$$P_{Q_{n+1}}(t)\Big|_{Q_n=1}^{D=1,CLK=0}=\left(0.9P_{\shortparallel}(t)|_{Input=D}\right)_{LOW}+\left(0.9P_{\times}(t)|_{Input=Q_n}\right)_{HIGH} \tag{18}$$

$$P_{Q_{n+1}}(t)\Big|_{Q_n=1}^{D=CLK=0}=\left(0.9P_{\times}(t)|_{Input=Q_n}\right)_{HIGH} \tag{19}$$

$$P_{Q_{n+1}}(t)\Big|_{Q_n=0}^{D=0,CLK=0}=P_{Q_{n+1}}(t)\Big|_{Q_n=0}^{D=0,CLK=1}=0 \tag{20}$$

$$P_{Q_{n+1}}(t)\Big|_{Q_n=0}^{D=1,CLK=0}=\left(0.9P_{\shortparallel}(t)|_{Input=D}\right)_{LOW} \tag{21}$$

$$P_{Q_{n+1}}(t)\Big|_{Q_n=1}^{D=0,CLK=1}=\left(0.9P_{\times}(t)|_{Input=Q_n}\right)_{LOW} \tag{22}$$

Note that the 0.9 factor present in the above formulas is due to the 90/10 coupler of the flip-flop setup. Therefore, only 90% of the power is obtained at the D output port; the others 10% are launched into the feedback loop.

2.2. Operation cases

An optical clocked D flip-flop is a sequential circuit; therefore its output (Q) not only depends of the information present at the inputs (D and CLK), in a considered instant, but also depends of the information from the previous state (Q_n). During the operation of the optical clocked D flip-flop, $2^3=8$ possible situations can occur.

The possible operation cases of the proposed flip-flop are depicted in Fig. 2, and will be discussed, in more detail, below.

CASE-I. *CLK = D = 1 and $Q_n=0$*

Let us consider a strong control signal (CLK) injected, through an optical 2×1 combiner, in the port #A of the SOA-MZI. This signal modulates the gain of the SOA_1, which induces a modulation of its refractive index. If the incoming signal (D) is launched into port #B, half of its power appears at each output of the input coupler, with a phase shift of $\frac{\pi}{2}$. However, due to the presence of the control signal, the two even parts of the incoming signal will suffer different gains and phase shifts, which lead to the unbalance of the SOA-MZI. In this case, the modulation of the refractive index are not the same ($n_1\neq n_2$), therefore the light in the upper arm of the MZI presents a different velocity than the lower arm; hence the incoming optical pulse emerges at port #I, as illustrated in Fig. 2 (a). Therefore, in this case, the flip-flop output is Q = '1'.

CASE-II. *CLK = D = 1 and $Q_n=1$*

If, however, in the previous state, the flip-flop output presented the logical value '1', an optical pulse will travel in the feedback loop and will arrive at port #C of the interferometer, at same time of the incoming optical pulse. Again, due to the presence of the control signal, the two even parts of both signals will experience different gains and phase shifts. Therefore, the optical incoming pulse and the optical

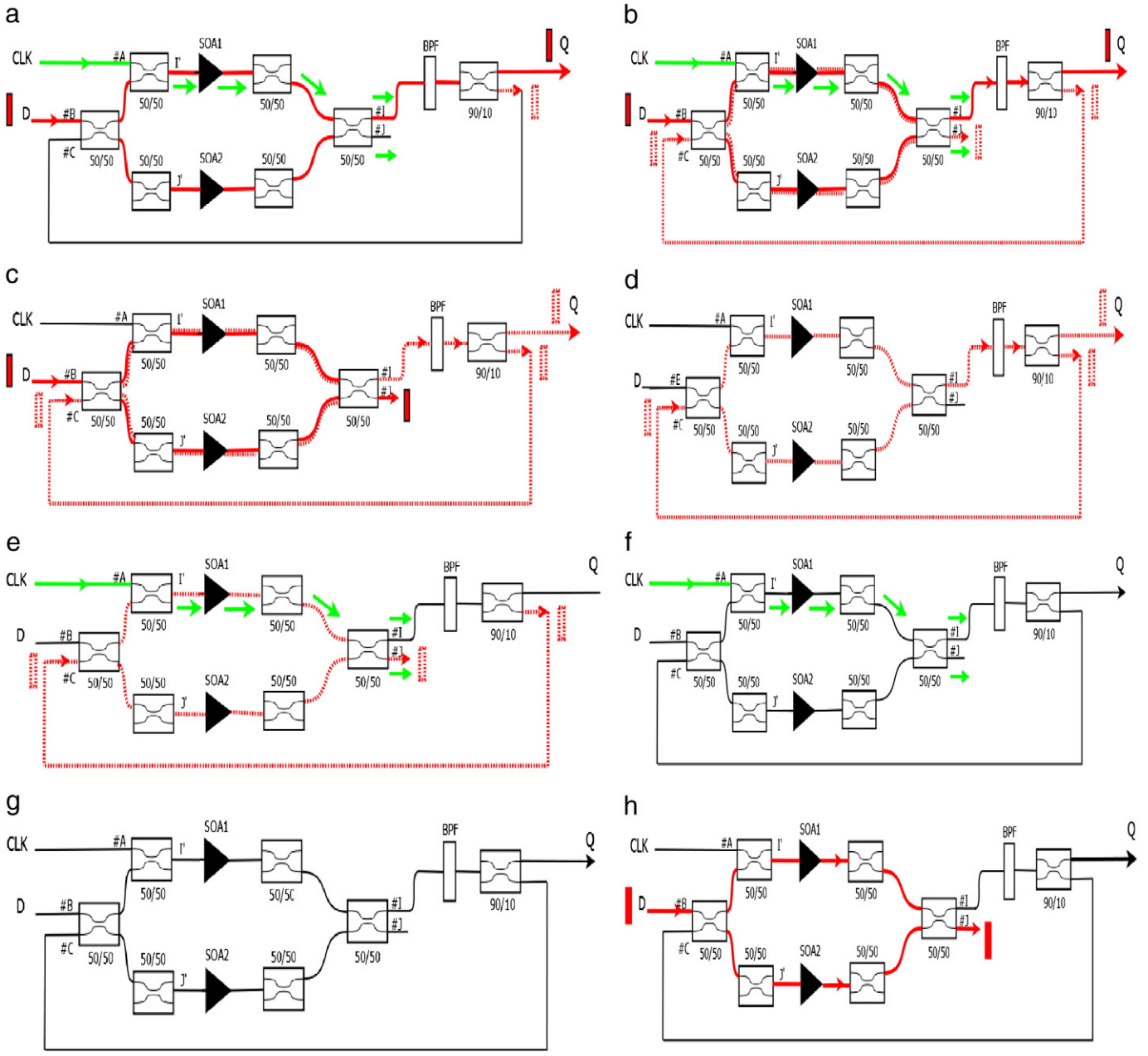

Fig. 2. Power distribution, along the interferometer arms, for different cases. (a) Case-I: D = 1, CLK = 1, Qn = 0, (b) Case-II: D = 1, CLK = 1, Qn = 1, (c) Case-III: D = 1, CLK = 0, Qn = 1, (d) Case-IV: D = 0, CLK = 0, Qn = 1, (e) Case-V: D = 0, CLK = 1, Qn = 1, (f) Case-VI: D = 0, CLK = 1, Qn = 0, (g) Case-VII: D = 0, CLK = 0, Qn = 0, (h) Case-VIII: D = 1, CLK = 0, Qn = 0.

pulse from the feedback loop (last Q) will reach their bar-ports, as it is shown in Fig. 2(b). Therefore, in this particular case, the flip-flop's next state will be the logical value '1'.

CASE-III. *CLK = 0 and D = Q_n = 1*

In the absence of a clock pulse and D = Q_n = 1, a '1' logical level will arrive to interferometer port #C, at the same time of D optical pulse. Both input signals are split equally, with a phase shift of $\frac{\pi}{2}$, by the input 3-dB coupler.

The outputs of the 3 dB input coupler (coupling ratio = 0.5) are given by:

$$\begin{bmatrix} E_{I'} \\ E_{J'} \end{bmatrix} = \begin{bmatrix} \frac{E_B}{\sqrt{2}} + j\frac{E_C}{\sqrt{2}} \\ j\frac{E_B}{\sqrt{2}} + \frac{E_C}{\sqrt{2}} \end{bmatrix}; \left(j = \sqrt{-1}\right) \tag{23}$$

After passing through the input coupler, the signals propagate into the two MZI arms, where they will be evenly amplified by the SOAs. Since the modulation of the refractive index are the same ($n_1 = n_2$), both signals will be affected by the same phase and gain, and no additional phase shift between the two MZI arms is added. Therefore, we can simplify this system analysis, by neglecting the gain and phase contribution provided by the SOAs (since this contribution are the same for both arms).

When the signals arise at the output 3-dB coupler, they will suffer another phase shit of $\frac{\pi}{2}$, and the optical output fields can be calculated by

$$\begin{bmatrix} E_I \\ E_J \end{bmatrix} = \begin{bmatrix} \frac{E_{I'}}{\sqrt{2}} + j\frac{E_{J'}}{\sqrt{2}} \\ j\frac{E_{I'}}{\sqrt{2}} + \frac{E_{J'}}{\sqrt{2}} \end{bmatrix} \equiv \begin{bmatrix} E_I \\ E_J \end{bmatrix} = \begin{bmatrix} jE_C \\ jE_B \end{bmatrix} \tag{24}$$

The output powers can be found by:

$$P_I = E_C \cdot E_C^* = jE_C \cdot (-jE_C) = E_C^2 = P_{Q_n}$$
$$P_J = E_B \cdot E_B^* = jE_B \cdot (-jE_B) = E_B^2 = P_D \quad (25)$$

where the superscript * means the complex conjugate. Therefore, when CLK = 0 and D = Q_n = 1, the D flip-flop holds the information of its last output state, as it is shown in Fig. 2(c).

CASE-IV. *D = CLK = 0 and Q_n = 1*

In the absence of other input signals, if in the previous state Q_n = 1, then a '1' logical level will travel in the feedback loop and will arrive to port #C of the interferometer. After passing through the input coupler, the signal is split in two equal parts and half of the input power appears at each output of the coupler, with a phase shift of $\frac{\pi}{2}$.

$$\begin{bmatrix} E_{I'} \\ E_{J'} \end{bmatrix} = \begin{bmatrix} j\frac{E_C}{\sqrt{2}} \\ \frac{E_C}{\sqrt{2}} \end{bmatrix} \quad (26)$$

The signals travel through the nonlinear media (SOAs) and deplete the carrier density, modulating the refractive index. Since both parts of the signal experiments the same gains and phases ($G_1 = G_2$), the signals are equally amplified and recombine at the output coupler, where experiments another $\frac{\pi}{2}$ phase shift. Since the phase and gain, provided by the SOAs are the same for both arms, again no additional phase shift between the two MZI arms is added, so the system can be calculated as

$$\begin{bmatrix} E_I \\ E_j \end{bmatrix} = \begin{bmatrix} jE_C \\ 0 \end{bmatrix} \quad (27)$$

For this case, the output powers can be defined as:

$$P_I = E_C^2 = P_{Q_n}$$
$$P_J = 0 \quad (28)$$

which means that the output of D flip-flop maintains its previous state when, in the absence of other input signals, the last value of the flip-flop output is '1'. This situation is illustrated in Fig. 2(d).

CASE-V. *CLK = 1; D = 0 and Q_n = 1*

When a strong control pulse (CLK) is injected again into the interferometer, it arises at SOA_1, reducing its carrier density, hence the refractive index of SOA_1 changes. In this situation, if in the previous state Q_n = 1, this optical pulse will be split in two, after passing through the 3 dB coupler, and will suffer different gains and phase shifts in each of the interferometer arms. Therefore, when the clock is in its high state, it saturates the upper SOA and the signal in the upper arm is not amplified, which means that no optical power is obtained at the flip-flop output (port #I), and the pulse from the previous state emerge, at the next state, in its bar port, as illustrated in Fig. 2 (e). In this case, the flip-flop changes its states from '1' to '0'.

CASE-VI. *CLK = 1; D = 0 and Q_n = 0*

This condition, illustrated in Fig. 2(f), occurs when only a clock pulse is injected into the SOA-MZI. Since the filter block the clock pulse, no optical power will be obtained at the D flip-flop output.

CASE-VII. *CLK = D = Q_n = 0*

In this case, it is clear that if no light is injected at the interferometer inputs, no optical signal can be obtained at the interferometer outputs. So, the D flip-flop output presents the logic value '0'.

CASE-VIII. *D = 1 and CLK = Q_n = 0*

When only an incoming pulse (D) is injected into port #B of the input coupler, its power is distributed, equally, through both SOA-MZI arms, but with a phase shift of $\frac{\pi}{2}$ between the two branches of the interferometer.

$$\begin{bmatrix} E_{I'} \\ E_{J'} \end{bmatrix} = \begin{bmatrix} \frac{E_B}{\sqrt{2}} \\ j\frac{E_B}{\sqrt{2}} \end{bmatrix} \quad (29)$$

In the MZI, the two even parts of the incoming signal pass through the two SOAs, where they modulate, equally, the carrier density and thereby the refractive index. Since the length path of the MZI arms and SOA's phase shifts and gains are identical (G1 = G2), no additional phase shift is added in the MZI arms because the light velocity, propagating in both MZI arms, is the same. Therefore, both parts of the incoming signal will be evenly amplified and will recombine at the output of the interferometer destructively (port #I) and constructively (port #J). In this situation, the SOA-MZI is balanced.

$$\begin{bmatrix} E_I \\ E_J \end{bmatrix} = \begin{bmatrix} 0 \\ jE_B \end{bmatrix} \quad (30)$$

The output powers are then given by:

$$P_I = 0$$
$$P_J = E_B \cdot E_B^* = jE_B \cdot (-jE_B) = E_B^2 = P_D \quad (31)$$

where the superscript * means the complex conjugate. Therefore, in this case, no optical signal is obtained at the D flip-flop output. i.e., in the absence of a clock pulse, the output does not change even if in D input is applied logic '1'.

3. Results and discussions

A simulation study of the all-optical clocked D flip-flop was carried out at 50 Gb/s, using the parameters summarized in Table 2 [14,16], of a bulk InGaAsP-SOA operating in 1500 nm spectral region.

The dynamic operation of the all-optical clocked D flip-flop was numerically demonstrated by toggling the state of the flip-flop, through the injection of optical pulses. Fig. 3 presents the time domain traces obtained for the clocked D flip-flop and it is very noticeable that the information at the D flip-flop input is transferred to the Q output, only when the clock signal is enabled.

The switching crosstalk (*XT*) is defined as the ratio between P_{nt} and P_t:

$$XT = 10\log\left(\frac{P_{nt}}{P_t}\right) \quad (32)$$

Table 2
Parameters used in simulation.

Parameters	Symbol	Value
Injection current of SOA	I	600 mA
Confinement factor	Γ	0.48
Differential gain	a_N	3.3×10^{-20} m^2
Line-width enhancement factor of SOA	α	6.5
Carrier density at transparency	N_{tr}	1.0×10^{24} m^{-3}
Width of the active region of SOA	w	0.7 μm
Depth of the active region of SOA	d	220 nm
Active length of SOA	L	150 μm
Internal loss of the wave guide	α_D	2700 m^{-1}
Wave length of light	λ_0	1500 nm
Gain recovery time	τ_e	20 ps
Unsaturated single-pass amplifier gain	G_0	23.142 dB
Clock pulse energy	E_c	15 fJ
Full width at half maximum of control pulse	σ	2 ps
Incoming pulse power		0.2 mW

where P_{nt} and P_t are, respectively, the power of switched non-targeted and targeted signals. The ratio can be calculated from Eqs. (14) and (15). Since no clock pulse is applied to SOA_2, the gain of that SOA is nearly the same as G_0. However, the gain of SOA_1 changes with CLK pulse, as it can be seen in Fig. 4. If we plot the variation of G_1 with the phase shift ($\Delta\varphi$) (as shown in Fig. 5), we get at $G_1 = 8.807$ dB, $\Delta\varphi = 3.14$ rad, so $P_{\times}(t) = 0$, i.e., crosstalk (XT) is very low. This is the ideal situation, but in practical this does not occur. In Fig. 6, we plot CLK pulse energy (E_c) against G_1 and the phase shift ($\Delta\varphi$) and we found that, at CLK pulse energy = 15 fJ, $\Delta\varphi$ = 3.039 rad and $G_1 = 9.084$ dB, which is almost 3.14 rad i.e., is nearly the ideal situation.

The output 'pseudo-eye-diagram' (PED) [23] is shown in Fig. 7. This is not a 'classical' eye diagram because it is not as informative in the sense that degrading effects, normally observed in point-to-point communication links, such as noise source, are added by the detector and optical fibers. The relative eye opening (O) of the PED is defined as [24]:

$$O = \frac{P^1_{\min} - P^0_{\max}}{P^1_{\min}} \tag{33}$$

where $P^1_{\min}$ and $P^0_{\max}$ are the minimum and maximum power at '1' and '0', respectively.

The variation of the relative eye opening percentage (O) with CLK pulse energy (E_c), was calculated and the obtained results are shown in Fig. 8. We obtain O = 91.67% at $_?E_c = 15$ fJ, and it is possible to observe that O decreases for any values of$_?E_c \neq 15$ fJ. Hence, the simulations were carried out for a value of $E_c = 15$ fJ, since this is the optimum operation point, in which the performance of the circuit increases. In Fig. 9, the variation of crosstalk with SOA_1 gain, G_1, is plotted from formula (32) and we obtain XT = -28.997 dB, at $G_1 = 9.084$ dB (for $E_c = 15$ fJ).This is the lower crosstalk value, for other values of G_1 crosstalk is higher.

To assess the performance of this flip-flop configuration, different merit figures were calculated from the 'pseudo-eye-diagram', such as contrast ratio (*C.R.*), extinction ratio (*E.R.*), and amplitude modulation (*A.M.*).

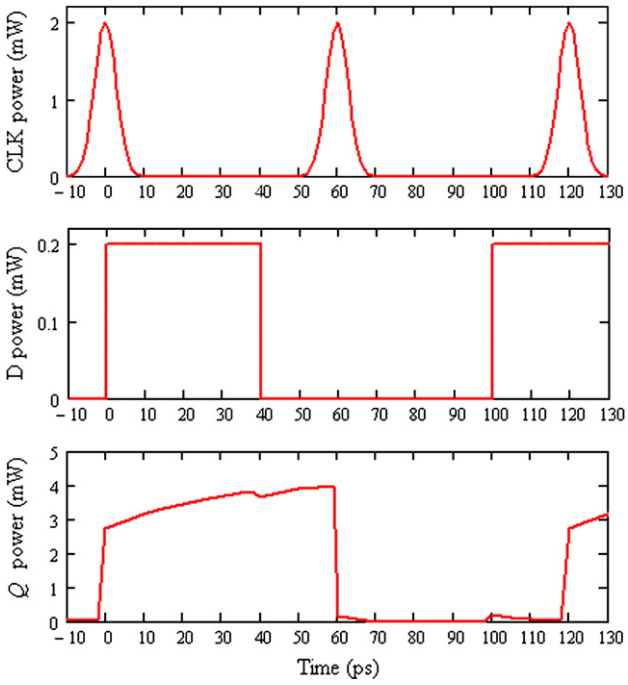

Fig. 3. Simulated output of SOA-MZI based all-optical clocked D flip-flop.

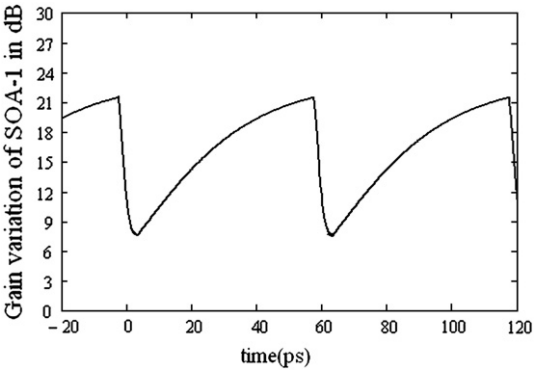

Fig. 4. Gain variation of SOA_1 with time for CLK = '1 0 0 1 0 0 1'.

The output contrast ratio (*C.R.*) is defined as the ratio between the mean value of output peak power for '1' (P^1_{mean}) and the mean output peak power for '0' (P^0_{mean}) in decibels [13] i.e.

$$C.R.(dB) = 10\log\left(\frac{P^1_{mean}}{P^0_{mean}}\right) \tag{34}$$

The amplitude modulation (*A.M.*) is defined as [11,23],

$$A.M.(dB) = 10\log\left(\frac{P^1_{\max}}{P^1_{\min}}\right) \tag{35}$$

where $P^1_{\max}$ and $P^1_{\min}$ are, respectively, the maximum and minimum value of the peak power of 'HIGH' (1).

The extinction ratio (*E.R.*) is defined as [13,25],

$$E.R.(dB) = 10\log\left(\frac{P^1_{\min}}{P^0_{\max}}\right) \tag{36}$$

where $P^1_{\min}$ and $P^0_{\max}$ are the minimum and maximum value of the peak power of 'HIGH' (1) and "ZERO" (0), respectively.

For an optimum gate performance, some conditions should be presented, namely, the *C.R.* should be as high as possible so that the main fraction of input can exist at the output; the *A.M.* should be as low as possible so that output '1' presents the same level and the pattern effect can be negligible and, finally, the *E.R.* should be as high as possible so that the '1' level can be distinguishable from '0'.

The dependence of the output *SNR*, *C.R.*, *A.M.* and *E.R.* with the clock pulse energy (in fJ) is shown in Fig. 10 (a), (b), (c) and (d), respectively. At $E_c = 15$ fJ, we obtain *SNR* ~ 19 dB, *C.R.* = 15.8 dB, *A.M.* = 1.63 dB and *E.R.* = 10.792 dB, respectively. These simulated

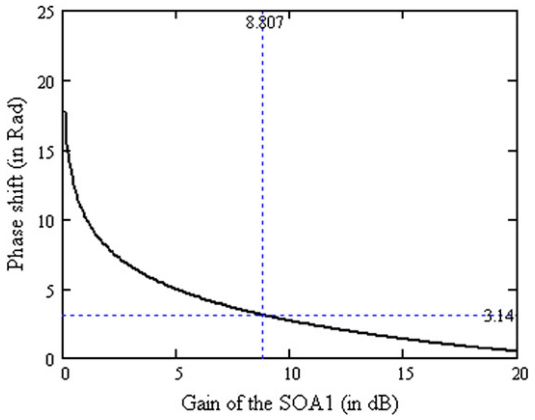

Fig. 5. Gain variation of SOA_1, G_1, with the phase shift ($\Delta\varphi$).

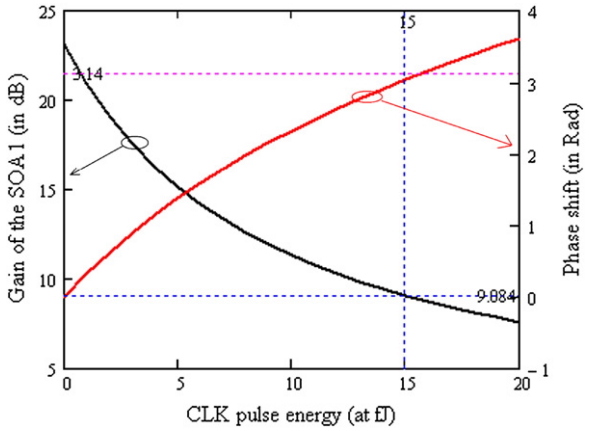

Fig. 6. Variation of CLK pulse energy with SOA_1 gain and phase shift.

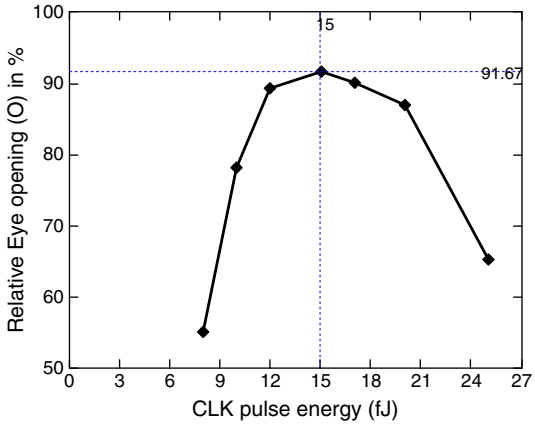

Fig. 8. Variation of relative eye opening (O) with CLK pulse energy (fJ).

results confirm the optimum performance of the proposed configuration, since the CR and ER present high values (>10) and, at the same time, the AM value is low. It should be noted that the AM should not exceed 1 dB. This can also be visualized in the PED of Fig. 7, where the envelopes of the '1's do not coincide but are discernible due to the existence of pattern effect [26].

The ability of an all-optical flip-flop for ultrafast switching is determined by how fast are the rising and falling times [27]. When D = CLK = 1, the flip-flop output starts to rise. When D = 0, the flip-flop maintains its last value due to the feedback loop, but since the SOA_1 gain slowly rises with time, it should continue to rise. But, in practice, we notice that it falls slightly because of the loss of the 3-dB coupler and the losses inside the SOA, which reduces the amplitude. The falling time and rising time, obtained at the flip-flop output, is shown in Fig. 11(a) and (b), respectively. From this figure, we see that switching speeds of ~0.84 ps (59.10 ps to 59.94 ps) and ~1.78 ps (118.19 ps to 119.97 ps) were achieved for fall time and rise time, respectively. The rising time is higher than the falling time because, after the decrease of the gain of SOA_1, the gain increases slowly to its recovery value.

4. Feedback loop calibration

In our proposed all-optical flip-flop, the feedback loop is a very important feature since it maintains the flip-flop's previous state, in the absence of the clock input signal. In this section, we try to make a calibration of the length of the feedback loop by showing the effect on the output waveforms, for different loop lengths. Let us consider that the feedback loop length is *L*. So after emission from port#I, the data will reach to the MZI port#C after the time $\tau = L/v$, where v is the velocity of light inside the fiber.

When data (D signal) enters through port#B, at time t_0, it emits through port#I (if control pulse is 'ON') at time $(t_0 + t_{MZI})$, where t_{MZI} is the time taken through the MZI switch ($t_{MZI}$is very small). After time 'τ', one part of that signal enters again into the switch through port#C and if the control pulse is 'OFF' then, the data emerges again from port#I after the time $(t_0 + 2t_{MZI} + \tau)$.

The flip-flop properties of the proposed circuit depend on some important aspects, such as:

- When data arrives at port#C through the feedback loop, the D signal can be present or not.
- At that time the gain of the SOA_1 recovers or not.
- The loop length delay time (τ) can be small or large.

As it is shown in Fig. 12, we realize numerical simulations to find out the output waveform of the all-optical flip-flop, for different τ. We chose all the possible cases for D and CLK pulse applied, i.e. D = CLK = 1 (at 0 ps in time scale); D = CLK = 0 (at ~0-to-220 ps in time scale); D = 1, CLK = 0 (at ~220-to-300 ps in time scale); D = CLK = 1 (at 300 ps in time scale); D = 1, CLK = 0 (at ~300-to-500 ps in time scale); D = 0, CLK = 1 (at 500 ps in time scale); D = CLK = 0 (at ~500-to-560 ps in time scale) and D = 1, CLK = 0 (at ~560-to-600 ps in time scale).

Case-I. (τ = 5 ps)

This case is illustrated in Fig. 12(a). At first, when D = CLK = 1, the data emits from port#I and reaches to port#C after 5 ps, so the gain of SOA_1 do not recover. Then D = 0 so, from Eqs. (14) and (15), the data

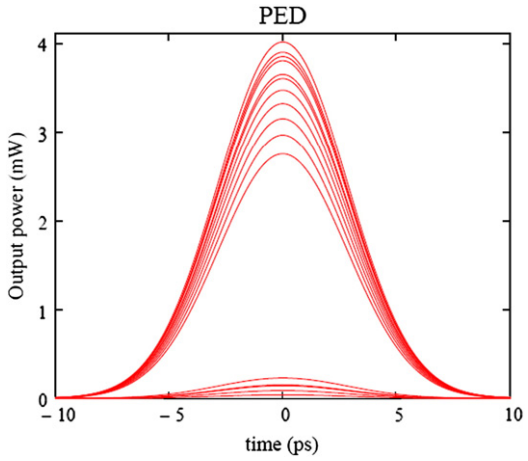

Fig. 7. Simulated pseudo-eye-diagram' (PED) for the proposed all-optical D flip-flop.

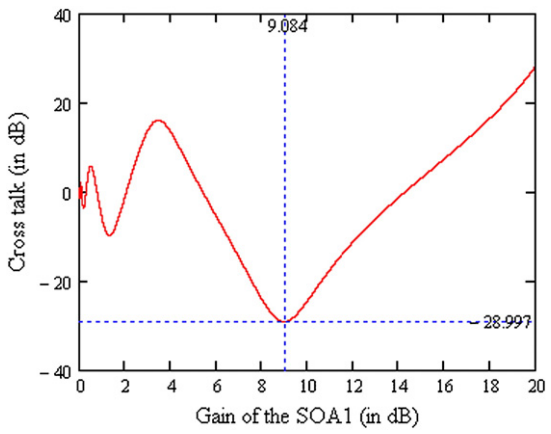

Fig. 9. Variation of crosstalk with SOA_1 gain.

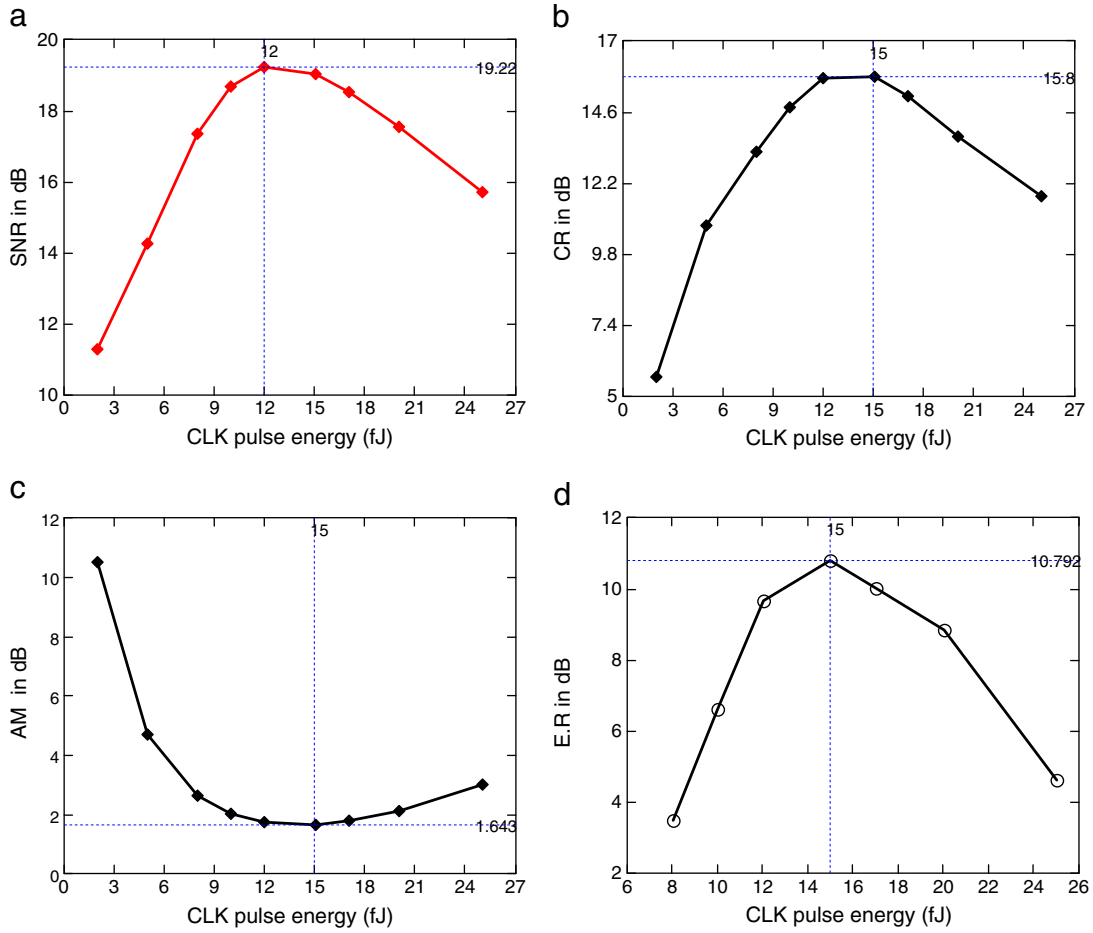

Fig. 10. (a): Variation of signal to noise ratio (*SNR*) with CLK pulse energy (fJ); (b): Variation of contrast ratio (*C.R.*) with CLK pulse energy (fJ); (c): Variation of amplitude modulation (*A.M.*) with CLK pulse energy (fJ); (d): Variation of extinction ratio (*E.R.*) with CLK pulse energy (fJ).

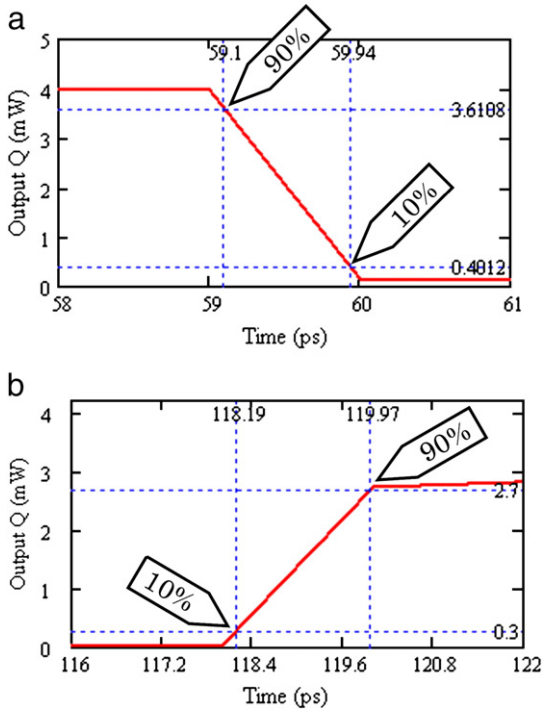

Fig. 11. Switching speeds (a) Falling time; (b) Rising time.

will pass through port#J, which means that $Q \rightarrow 0$and the data is not 'HOLD'.

At 300 ps, D = CLK = 1, and again we obtain $Q = 1$. At 305 ps, the previous phenomena happens again, but since D signal is present, port#I gets the data from D and port#C, which violate the flip-flop condition, so data is not 'HOLD'.

Case-II. ($\tau = 20$ ps)

This situation is shown in Fig. 12(b). When data arrives to port#C after 20 ps, the gain of the SOA_1 recovers. Hence, from Eq. (15), we find out that the output power is not such low as the previous case, so it will increase slowly and saturates up to ~300 ps. At 300 ps, the gain of SOA_1 decreases further (as CLK = ON), and since data at port#C is absent, we obtain low power at the output (but still Q = 1). This two dips are shown in Fig. 12(b) as (i) and (ii). After that it goes to the saturation value. In this case, the 'HOLD' condition of the flip-flop is satisfied.

Case-III. ($\tau = 40$ ps)

The output waveform for $\tau = 40$ ps is shown in Fig. 12(c). In this particular case, we do not found the first dip presented in case-II, because after 40 ps the data reaches to port#C, and SOA_1 recovers its gain higher than 20 ps (shown in Fig. 4). Therefore, we obtain more power at port#I than the previous case, which is obtained from Eqs. (14) and (15). However, after 300 ps, the output power decreases more than case II. This large dip is indicated by (iii) in Fig. 12(c) since at 340 ps, the feedback comes before data at port#B is presented. After that the output increases slowly to saturation value.

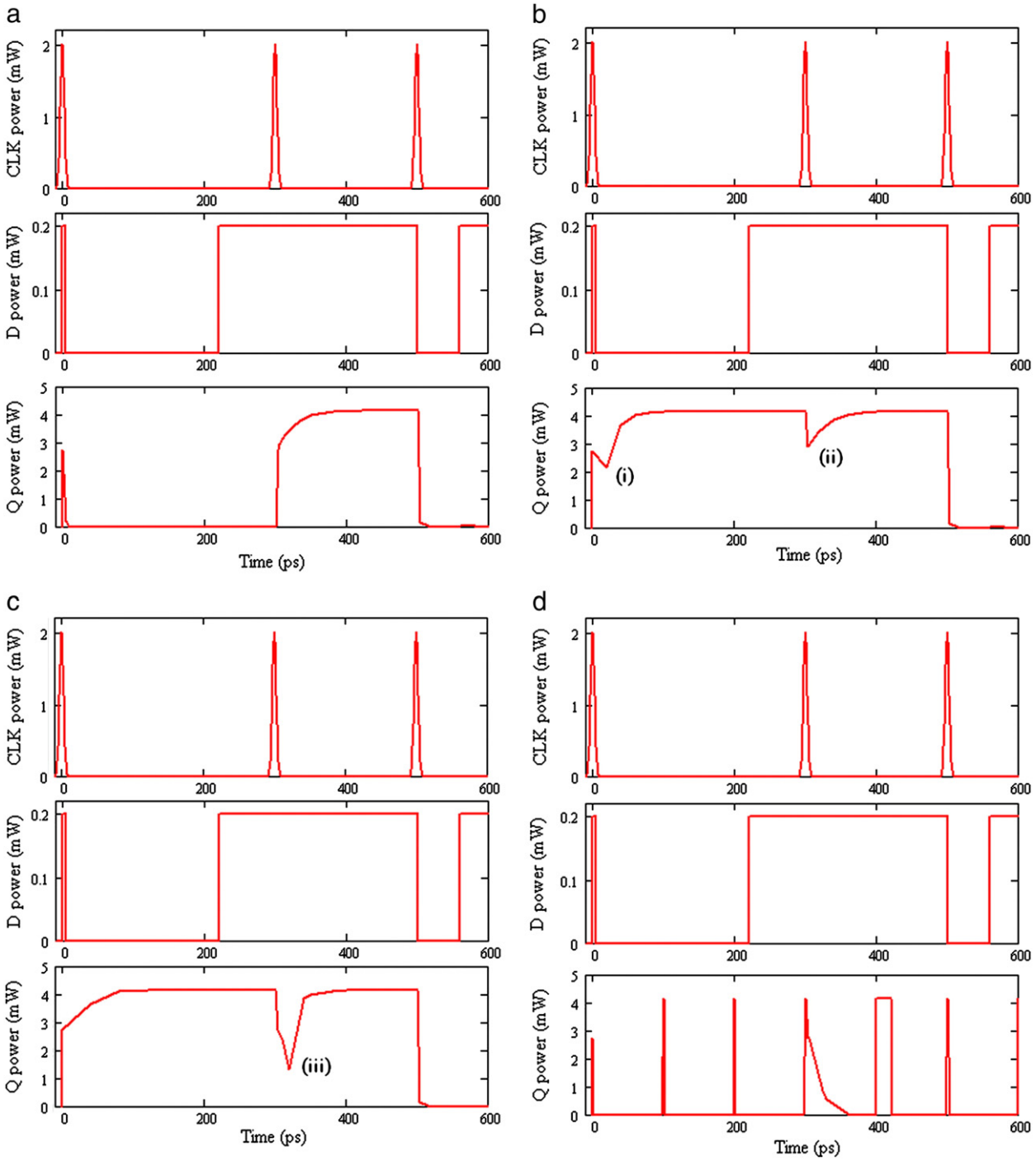

Fig. 12. Output waveforms for different loop length delay time (τ). (a) $_{?}\tau = 5$ ps, (b) $_{?}\tau = 20$ ps, (c) $_{?}\tau = 40$ ps and (d) $_{?}\tau = 100$ ps.

Case-IV. ($\tau = 100$ ps)

If we increase to $\tau = 100$ ps or further more then, we obtain discrete pulses at every 100 ps, because data arrives to port#C after a very large time gap. The output waveform for this case is shown in the Fig. 12(d). We also find an unwanted peak at 600 ps when, according to theory, it should be present the logic value '0'. Therefore, in this case the 'HOLD' condition is not also satisfied. From Fig. 12(c), we verify that if we increase $\tau > 20$ ps there may be a problem at point (iii), since it goes below the threshold value. So, in this condition, the data cannot be 'HOLD'. For $\tau >> 20$ ps, we get unwanted discrete pulses.

From the analysis of the simulations results, we can conclude that the feedback loop length should be maintained comparable with the gain recovery time (τ_e) of the SOAs, otherwise the proposed flip-flop may not work according with its truth table.

5. Complex circuit design by D flip-flop

Every flip-flop circuit requires a feedback loop to hold its output data, permanently or temporary. On the other hand, every all-optical switch cannot operate below its response time. Our all-optical D flip-flop is made of a single SOA-MZI based switch and its operating time is equal to the response time of one MZI switch. The design of the feedback loop length is very important, since the synchronization of data with MZI switching time must be guaranteed.

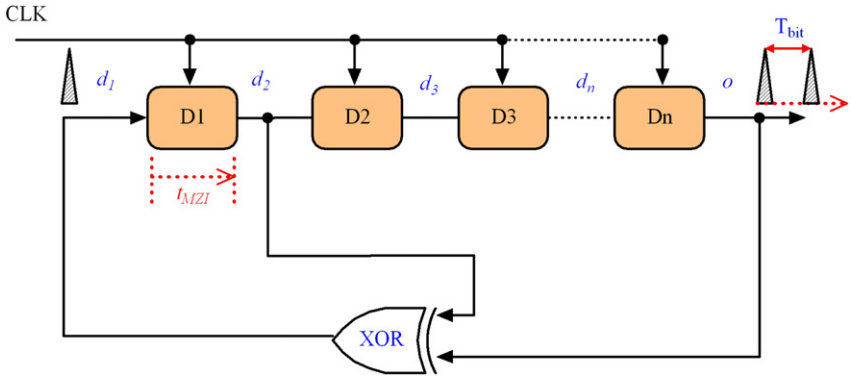

Fig. 13. n-bit degree PRBS circuit using all-optical D flip-flops. T_{bit} = Bit period i.e. time gap between two pulses.

This feedback loop length can be constructed through photonic integration.

In complex circuits, based on D flip-flops, the loop length will not cause any limitation. This can be easily understood with the following example. In the design of pseudorandom sequence generator (PRBS) [28], several identical D flip-flops were serially connected, as shown in Fig. 13. Here the D flip-flops act as shift registers. In the previous section, we see that it takes t_{MZI} time to transmit data from input to the D flip-flop output and to hold the data (without feeding the input signal) it is required $(t_{MZI}+\tau_e)$ time. Hence CLK should be applied to the flip-flops (D1, D2, …, Dn) at least t_{MZI} time or $\geq(t_{MZI}+\tau_e)$ time, respectively. The bit rate depends on the switching time of the D flip-flop. For $n=3$ (feed back polynomial $=x^3+x+1$, period $=2^3\text{-}1=7$) the pulse should be 00101110010111… and the bit period (T_{bit}) should be equal to the response time of one MZI. As our flip-flop is a low circuit design, we think that will support ultrafast bit rates.

6. Conclusions

In this paper, we proposed a new all-optical clocked D flip-flop scheme that dynamically changes its state only when the clock signal is enable. This scheme presents very low complexity since it comprises only a single SOA-MZI, with an external feedback loop.

The concept of this novel flip-flop configuration was demonstrated for each of the possible operations cases and it was proven that this scheme operates according to its truth table.

The performance of the proposed flip-flop was also evaluated, using merit figures such as the extinction ratio and amplitude modulation. The simulation results confirm the effectiveness of our model and that the feedback loop length should be maintained comparable with the gain recovery time (τ_e) of the SOAs.

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