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Performance comparison of all-optical clocked S-R and D type flip-flops

C. Reis[a,*], A. Maziotis[b], C. Kouloumentas[b], T. Chattopadhyay[c], N. Calabretta[d], P. André[a], G. Berrettini[e], G. Meloni[e], A. Bogoni[f], H.J.S. Dorren[d], H. Avramopoulos[b], A. Teixeira[a]

[a] *Instituto de Telecomunicações, Campus Santiago, 3810-193 Aveiro, Portugal*
[b] *National Technical University of Athens – School of Electrical and Computer Engineering, 15773 Athens, Greece*
[c] *Kolaghat Thermal Power Station, 721137 West Bengal, India*
[d] *Eindhoven University of Technology, Eindhoven 5600 MB, The Netherlands*
[e] *Scuola Superiore Sant'Anna, 56124 Pisa, Italy*
[f] *CNIT, 56124 Pisa, Italy*

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ABSTRACT

In this paper, different approaches to implement all-optical flip-flops, working with a synchronization signal, will be presented and compared. In this type of optical bistable devices, the information present at the inputs produces effects on the outputs, throughout all the clock pulse period. The performance of optical clocked flip-flops will be studied in terms of extinction ratio (ER), switching energies and switching times.

1. Introduction

Nowadays electronic routers, based on CMOS technology, can reach over 1Tbps. However, with the increasing demand for bandwidth, scaling electronic routers to higher transmission rates will be extremely difficult, mainly due of its high levels of power dissipation and energy consumption [1].

All-optical packet switching is an attractive solution to increase the routers forwarding capacity, maintaining the efficiency and flexibility of the network. Since this technique realizes switching and routing functions in the physical layer, it will allow the increase of data bit rates, with a small foot-print.

A basic building block of any router, electrical or optical, is the memory circuit. It is essential for storing, temporarily, the header information of a packet and for solving the contention problem that occurs when several packets arrive for the same port, at the same time [2]. In the last few years, different approaches of optical S-R latches memories have been proposed. In this type of optical bistable devices, any change of information in the inputs is transmitted, immediately, to the output, according to its truth table. However, it may happen that input S and R suffer unwanted variation and if we are using asynchronous devices, unwanted information can be stored. Therefore, it is interesting that a higher priority input (clock) exists to control the enabling of the latch, making the latch sensitive or not to the values present in the set/reset inputs. So, if the latch works with a synchronization signal, it is possible to control the way the information is stored. In that case, if a change of information occurs in the inputs, when the clock is at its low state, the Q output will maintain its last value, toggling only at the next clock pulse.

In finite state machines, synchronous D type flip-flop is usually chosen to perform the memory circuit because its input presents the same value as the variables at the next state. However, since it has only one data input, it requires a more complex combinational block.

In this paper, different technologies to realize all-optical clocked S-R and D type flip-flops will be presented and quantitatively assessed.

2. All-optical clocked S-R flip-flops techniques

In the last few years, some approaches have been proposed to implement all-optical clocked S-R flip-flops. These different technologies are briefly discussed below.

2.1. All-optical clocked S-R flip-flop based on coupled SOA-MZI

In [3], an all-optical clocked S-R flip-flop is experimentally demonstrated and all the building blocks of this scheme are based on hybrid SOA-MZIs, which allow photonic integration. The main component of the optical clocked S-R flip-flop scheme, shown

* Corresponding author. Tel.: +351 234 377 900; fax: +351 234 377 901.
E-mail address: creis@av.it.pt (C. Reis).

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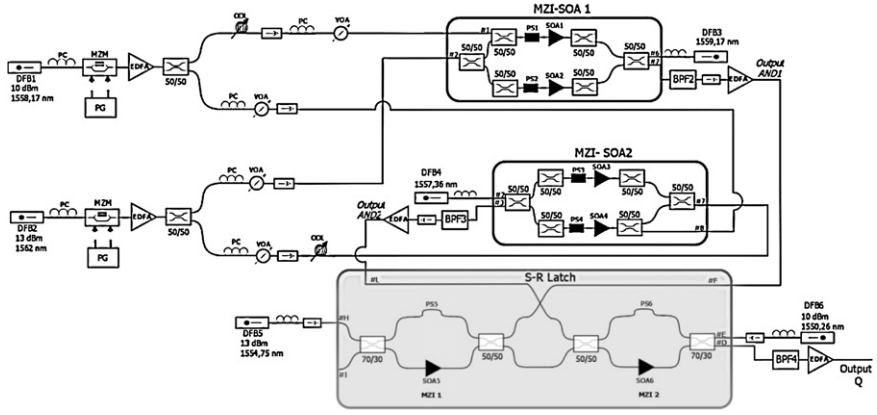

Fig. 1. Scheme of the optical clocked S-R flip-flop based on two coupled SOA-MZI.

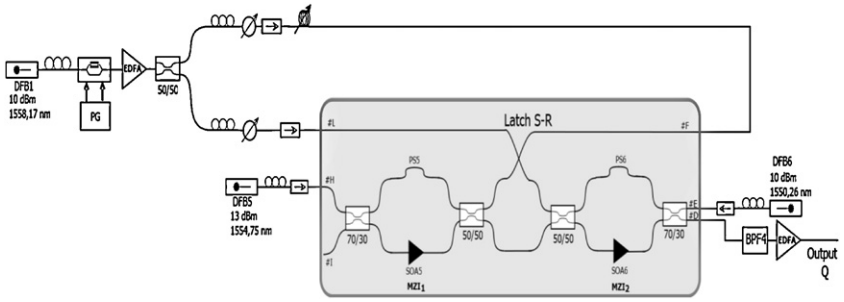

Fig. 2. Optical asynchronous S-R latch scheme based on two coupled SOA-MZI.

in Fig. 1, is the S-R latch, which consists of two coupled SOA-MZI, powered by two continuous wave (CW) signals, at different wavelengths. The latch operation principle is based on the gain quenching concept: when MZI_1 suppresses the output from MZI_2 it becomes dominant and the latch emits a signal at 1554.75 nm; due of system symmetry, when the MZI_2 suppresses the output from MZI_1, the latter one becomes the slave, and 1550.26 nm dominates the output.

The experimental setup of the optical S-R latch is illustrated in Fig. 2 and its dynamic operation is experimentally demonstrated in Fig. 3 by toggling the state of the latch through the injection of set and reset optical pulses. The set and reset optical pulses

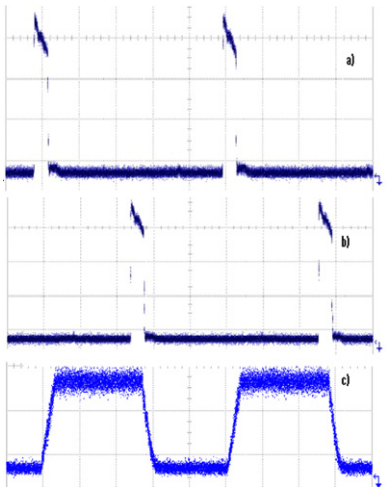

Fig. 3. Experimental results for asynchronous S-R latch: (a) set signal; (b) reset signal; (c) latch output. The vertical scale is arbitrary and the horizontal scale is 5 ns/div.

are generated by an external cavity laser peaking at 1558.17 nm, followed by a polarization controller and a Mach–Zehnder external modulator. The NRZ-OOK data signal, generated by an Anritsu MP 1763C, is then amplified by an Erbium Doped Fiber Amplifier (EDFA), split into two equal parts using a 3 dB coupler and then delayed by 11.6 ns to obtain different set and reset patterns.

The experimental results, depicted in Fig. 3, show that a change of information in the latch inputs is transmitted, immediately, to the output, according to the S-R latch' truth table. The rise and fall times are 1.029 ns and 857 ps, respectively, and these results are limited mainly due to the recovery time of the SOAs.

Contrary to the described S-R latch operation, the optical clocked S-R flip-flop, shown in Fig. 1, allows to control the way the information at set/reset inputs is stored, by working with a synchronization signal (CLK). To implement this all-optical clocked S-R flip-flop scheme, two SOA-based Mach–Zehnder interferometer devices, acting as AND logic gates, are used to enable the S-R latch by the logical level of the clock signal. So, for the cases that the clock signal is in its high level (CLK = 1), the information at the inputs is transmitted to its outputs. On the contrary, if CLK = 0, the flip-flop maintains its previous state, regardless the binary input data. Both optical AND gates are implemented in a co-propagation configuration. The SOA_1-MZI performs the Boolean AND logic operation between the reset and the clock signals. On the other hand, SOA_2-MZI performs the AND function between the set signal and the clock signal. The clock signal is generated by an external cavity laser, peaking at 1562 nm, with 13 dBm of optical power. The set and reset input signals are the same as the ones used to test the asynchronous S-R latch. Fig. 4 illustrates that the all-optical clocked S-R flip-flop switches between two states, by injecting optical pulses into the MZI that is currently dominant, allowing the other MZI to become dominant only when a clock pulse arrives, otherwise the flip-flop maintains its previous value. Depending on the flip-flop state, the bistable device emits a signal at 1554.75 nm or at 1550.26 nm.

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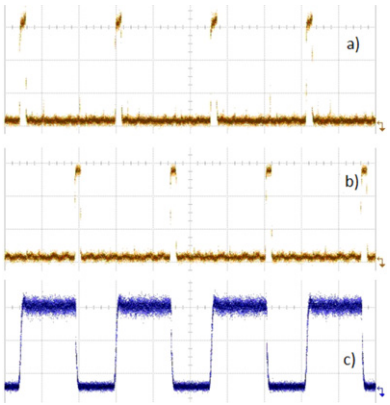

Fig. 4. Experimental results for synchronous S-R flip-flop: (a) set∩clock; (b) reset∩clock; (c) flip-flop output. The vertical scale is arbitrary and the horizontal scale is 10 ns/div.

2.2. All-optical clocked S-R flip-flop based on SOA fiber ring lasers

The optical clocked S-R flip-flop proposed in [4] is also based on the gain quenching effect, thus the signal output from the dominant laser suppresses the other laser from lasing, through gain saturation of the SOA.

Fig. 5 illustrates the experimental setup of the optical clocked S-R flip-flop memory and it consists of two optical AND logic gates and a S-R latch based on SOA fiber ring lasers. The optical latch device has two possible states, depending on which ring laser is lasing. In state 1, the SOA_1 output signal saturates SOA_2 gain therefore the flip-flop output Q emits a continuous wave signal, operating at λ_1 (Q = 1). In state 0, light from ring 2 suppresses lasing in ring 1 and, in that case, ring 2 output ($\bar{Q}$) emits a continuous wave operating at λ_2 ($\bar{Q} = 1$). When the set signal is injected, it will pass through couplers E, B and D, respectively, which suppresses ring 2 due of SOA_2 saturation, setting the flip-flop to state 1. On the other hand, by the injection of the reset signal, ring laser 2 acts as a master, suppressing the emission of ring laser 1, setting the flip-flop to state 0.

The dynamic operation of the S-R latch is changed by providing an additional input (CLK), in order to ensure that only when clock signal is enable (CLK = 1), the information at the inputs is transferred to the output of the flip-flop. Otherwise, the information presents at the inputs do not produces effects on the output. Therefore, the clock acts as a control signal for the latching switch. To enable the optical flip-flop, by a synchronization signal, two AND gates, implemented exploiting the nonlinearities of a SOA, namely four wave mixing (FWM), are used. If the clock signal and the set/reset optical signals are simultaneously '1', the FWM phenomenon occurs. However, if the set/reset signals are equal to '0', the FWM effect is not generated and no light flows out from the AND gates.

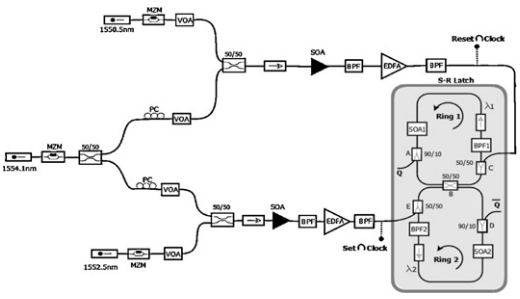

Fig. 5. Scheme of the optical clocked S-R flip-flop based on two coupled SOA ring lasers.

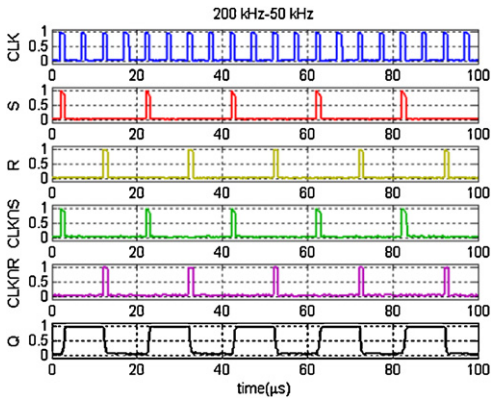

Fig. 6. Experimental results for clocked S-R flip-flop based on SOA ring lasers.

Fig. 6 shows the oscilloscope traces of the S-R flip-flop synchronous operation. The optical clock signal has a repetition rate of 200 kHz, with a pulse-width of 1 μs and is synchronized with the set/reset input signals, driven at 50 kHz, in order they can enter the bistable at the same time. From this figure, is possible to conclude that the switching only occurs in the presence of a clock pulse; otherwise the optical S-R flip-flop output maintains its last value. Therefore, the obtained experimental results are in agreement with the truth table of the clocked S-R flip-flop, which demonstrates the effectiveness of this flip-flop technique implementation.

2.3. All-optical clocked S-R flip-flop based on a Mach–Zehnder interferometer bistable laser diode

The optical clocked S-R flip-flop configuration, proposed in [5], is based on a SOA-MZI, with distributed Bragg reflectors (DBRs) at two interferometric ports, to obtain single-mode laser operation.

Fig. 7 depicts the Mach–Zehnder interferometer bistable laser diode (MZI-BLD), working with an external synchronization signal at 1552 nm. Its operation principle is based on cross gain modulation (XGM) and saturable absorption parts. The MZI-BLD-based flip-flop is composed by two cross-coupled modes, with a perfect spatial overlap (theoretically 100%), which allows a strong interaction between the two modes and the optical input signals. Therefore, the switching between the two modes can be realized with low switching energies. Mode 1 occurs in the right upper port and the left lower port of the active interferometer. On the other hand, mode 2 is between the left upper port and the right lower port. The left output is switched ON with the set optical pulses, throughout all the clock pulse period, and maintain its high state until a reset optical pulse occurs. In that situation, when mode 2 starts lasing, it obtains optical gain at SOAs section, in both MZI arms, which suppresses mode 1 from lasing. Switching from mode 2 to mode 1 occurs when a set pulse is injected at the left lower interferometer port, on the high logical level of the clock signal. Therefore, switching occurs only when a clock pulse arrives, according to the set and reset information at that time, as shown in Fig. 8. By analyzing this figure, although it is noticeable that the flip-flop

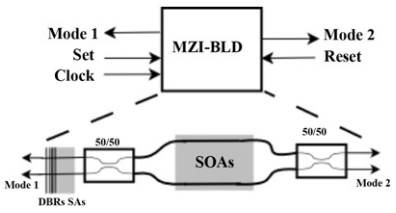

Fig. 7. Scheme of the optical clocked S-R flip-flop based on MZI-BLD.

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Table 1
Quantitative results of all-optical clocked S-R flip-flops techniques.

Technology	ER	Switch times	Switch energies	Integration potential?
Based on coupled SOA-MZI (2.1)	18 dB (dynamic measurement)	≤450 ps	<100 pJ	Yes
Based on SOA ring lasers (2.2)	40 dB (static measurement)	≤1 μs	<20 nJ	Yes
Based on MZI-BLD (2.3)	9 dB (dynamic measurement)	≤300 ps	<30 fJ	Yes

output waveforms show clearly two stable states, they also present several dips, which can be attributed to the XGM effect in the SOAs. However, some of these dips can be removed by controlling the optical passes for set/reset input signals.

The proposed scheme is also studied using clock signals with a wavelength range between 1545 nm and 1559 nm, and similar output waveforms are achieved. Therefore, this optical S-R flip-flop scheme not only presents low complexity but also can work with clock signals with large wavelength range.

2.4. Performance comparison between different all-optical clocked S-R flip-flop techniques

A performance evaluation of the different technologies proposed for the implementation of all-optical clocked S-R flip-flops is demonstrated in Table 1.

The switching behavior of the all-optical clocked S-R flip-flop, based on coupled SOA-MZI, was investigated and although the relatively slow SOA carrier recovery time, a fast operation speed was obtained. Since all the building blocks of the scheme are based on hybrid SOA-MZIs, photonic integration is allowed. A 18 dB extinction ratio performance and low switching energies were also achieved.

Since the output of clocked S-R flip-flops are mainly determined by the S-R latch state, the performance of the optical clocked flip-flop based on SOA fiber ring lasers was evaluated considering the results obtained in the asynchronous S-R latch, ignoring the influence of other elements of the scheme. In this scheme, the total length of each ring laser is few tens of meters due of the use of optical commercially available discrete components, which limits the speed operation of the optical clocked flip-flop. Anyway, 20 ps transition time and 10 Gbit/s operation without any bit loss was demonstrated in [6]. Photonic integration could improve the switching performance of the bistable device, however with today's technology is difficult to obtain optical isolators smaller than 0.8 mm [7].

Regarding the optical clocked S-R flip-flop, based on MZI-BLD, it was possible to distinguish, clearly, the two different stable states of the flip-flop, in spite of the presence of some dips on the flip-flop output waveform. It was very noticeable that the information at the inputs of the S-R flip-flop was transferred to the Q output, only when the clock signal was enabled. The ER, in static measurements, was higher than 14 dB however, in dynamic measurements, only 9 dB was achieved because the output light was monitored from an EDFA, which limited the ER due of the ASE noise. Rising edge of the response was limited by 1 GHz relaxation oscillation, due of the laser cavity length.

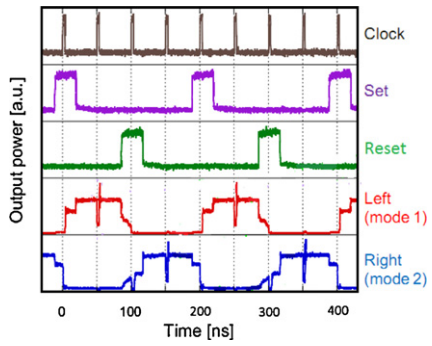

Fig. 8. Experimental results for clocked S-R flip-flop based on MZI-BLD [5].

3. All-optical clocked D flip-flops techniques

The all-optical clocked S-R flip-flop has a forbidden state that occurs when both set and reset inputs are at the high state ('1'). In that situation, it is not possible to predict, theoretically, the flip-flop output. The all-optical clocked D flip-flop is an adaptation of the optical clocked S-R flip-flop and can be implemented using a transparent S-R latch. Since the all-optical clocked D flip-flop only has one data input, the D signal is launched into the S port of the latch and the complement of the D input into to the R input port. Therefore, at the input latch ports are only possible the following combinations: S = 0 and R = 1 (when D = 0) or S = 1 and R = 0 (when D = 1) removing, in that way, the S = R = 0 and the delicate condition S = R = 1.

In an optical clocked D flip-flop, the flip-flop output (Q) is equal to the D input, when the clock signal is at the logic level '1'. When the clock signal is at level '0', the bistable holds the information of its previous state.

3.1. All-optical clocked D flip-flop based on coupled SOA-MZI

Like the optical clocked S-R flip-flop based on two coupled SOA-MZI, the logic level obtained in the output of the optical clocked D flip-flop, depicted in Fig. 9, is determined by the dominant wavelength laser [8].

Since the optical clocked D flip-flop only has one input data, a NOT gate, implemented with one SOA, is needed to realize the complementary signal. To carry out the optical NOT logic gate, based on XGM in a SOA, the NRZ signal at 1558.17 nm is coupled to a continuous wave signal, centered at 1554.75 nm. Then, is injected into SOA_7, which will modulate the gain of the amplifier due to its saturation. Since a co-propagation scheme is used to implement the NOT gate, a band pass filter (BPF_1) is introduced, at the output of the SOA_7, to eliminate the modulated signal wavelength.

Two AND gates are used as the control signals of the S-R latch in order to maintain the flip-flop' previous state, in the absence of the clock signal, independently of the D input information at that moment. Both AND gates are implemented using SOA-MZI structures that are previously balanced in order to obtain the maximum extinction ratio possible between the interferometric outputs. By acting in the polarization controllers, on the SOAs gains and by applying voltage to the phase shifters, SOA_1-MZI and SOA_2-MZI were balanced, showing an ER of 36 dB and 25 dB, respectively. After balancing the SOA-MZI structures, the clock signal, peaking at 1562 nm, with 13 dBm of optical power, is split by a 3 dB coupler and then launched into the ports of SOA_1-MZI and SOA_2-MZI. Due to the nonlinear phase rotation of the SOAs in an interferometer, the logic AND functions are carried out between the clock signal and the inputs data signals. Since both AND gates are implemented in a co-propagation configuration, the wavelength of the data signal and the clock signal are enough separated in order to avoid undesired crosstalk and nonlinear effects such as four wave mixing (FWM).

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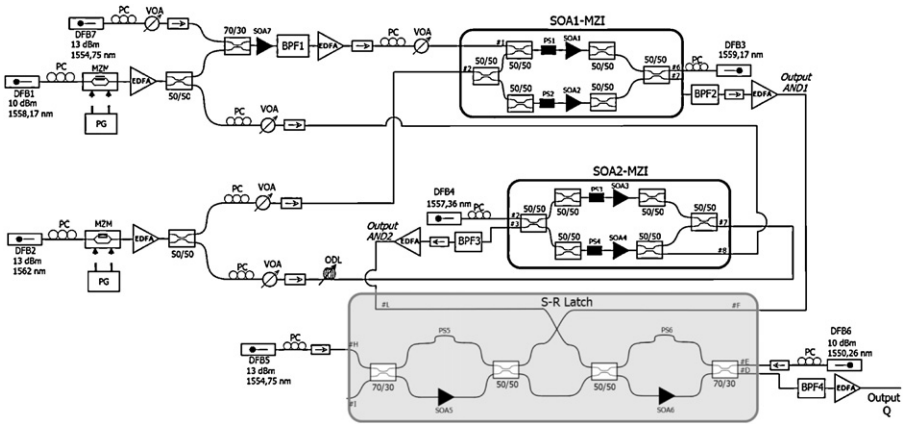

Fig. 9. Scheme of the optical clocked D flip-flop based on two coupled SOA-MZI.

Fig. 10 illustrates time domain traces of the clock, D input and Q flip-flop output signals. The experimental performance analysis shows that if a change of information occurs in the data input, when the clock is at its low state, the Q output will maintain its last value, switching only at the next clock pulse.

3.2. All-optical clocked D flip-flop based on SOA fiber ring lasers

An all-optical clocked D flip-flop is experimentally demonstrated in [4]. The optical clocked D bistable device, depicted in Fig. 11, consists of a SOA-based ring lasers latch and two optical Boolean AND gates. For the experiment, the input D signal, peaking at 1552.5 nm, is generated with a repetition rate of 100 kHz while the clock signal, with a wavelength of 1554.1 nm, is generated with a bit rate of 60 kHz.

The combinational logic of the scheme is carried out by exploiting the nonlinear effects of XGM and FWM in a SOA. Since the all-optical clocked D flip-flop only has one data input, and since its main device is the set/reset latch, there is the need to invert the input data signal before enter in the reset port of the asynchronous latch. A light comes out at 1554.1 nm from the AND between the clock signal and the inverted input signal ($\bar{D}$), because the clock signal is amplified when the input signal is at the low level; otherwise the carriers density of the SOA will be depleted and the clock input signal will be not amplified, due of XGM effect. When the clock signal and the data input signal (D) are simultaneously '1',

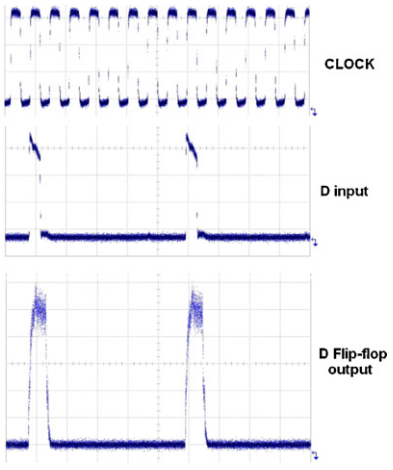

Fig. 10. Optical clocked D flip-flop operation. The vertical scale is arbitrary and the horizontal scale is 5 ns/div.

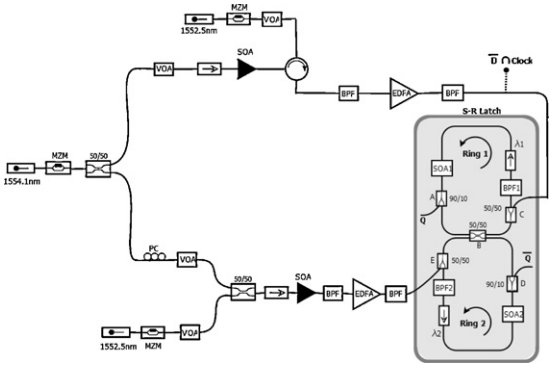

Fig. 11. Scheme of the optical clocked D flip-flop based on two coupled SOA ring lasers.

the FWM phenomenon occurs and the AND that will set the latch is at 1550.9 nm ($2\lambda_D - \lambda_{CLK}$).

In Fig. 12 is depicted the clocked D flip-flop operation. The experimental results show the effectiveness of the proposed scheme since the information presents in the D input is transferred to the flip-flop output only at the arrival of a clock pulse, otherwise if CLK = 0, the flip-flop maintains its last state.

3.3. All-optical clocked D flip-flop using single Terahertz Optical Asymmetric Demultiplexer (TOAD) based switch

In [9], an all-optical clocked delay flip-flop is proposed, using a single terahertz asymmetric demultiplexer (TOAD) based switch, and is shown in Fig. 13. The clock (CLK) and input D signals are

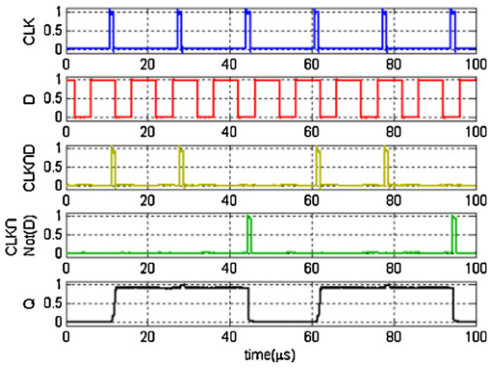

Fig. 12. Experimental results.

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Table 2
Quantitative results of all-optical clocked D flip-flops techniques.

Technology	ER	Switch times	Switch energy	Integration potential?
Based on coupled SOA-MZI (3.1)	12.5 dB (dynamic measurement)	<380 ps	<100 pJ	Yes
Based on SOA ring lasers (3.2)	40 dB (static measurement)	≤1 μs	<20 nJ	Yes
Based on TOAD switch (3.3)	13.64 dB (dynamic measurement)	≤90 ps	≤50 fJ	Yes

selected as two orthogonally polarized lights. CLK is introduced to the TOAD loop with a polarizing beam splitter (PBS) and it is rejected by another PBS such that no unwanted data can pass to the output. When D = 1, the light enters into the TOAD loop through the 50:50 coupler (from port P1) and split into two equal parts (CW and CCW). In that situation, when CLK is ON, the SOA changes its index of refraction. As a result, two counter propagating data signals will experience different gain saturation profiles. Therefore, cross phase modulation takes places when they recombine at the 50:50 coupler, and a–π phase change is introduce between them and data is transmitted to the output Q. This condition is called 'SET'. Partially silvered mirror (PSM, placed between the path P2 and the output) reflects some portion (nearly the same power of input D) of the output data into the loop. In the meantime, the gain of SOA tries to recover.

When CLK is OFF, then the reflected data enters to the TOAD loop through port P2. This is treated as incoming data. As clock is absent, CW and CCW pulses pass through the SOA at different time, but with almost the same gain. Hence, the phase difference between them becomes almost equal to zero and data is reflected towards the source i.e. to P2 port. In that case, the data is locked. This cannot be changed, regardless the information at the D input. After one CLK pulse, clock becomes 'zero' and the TOAD itself behaves like a loop mirror i.e. data will come to the reflected port. Only they are amplified by the SOA. Thus, output pulse power is higher than input D.

When CLK is ON and D = 0, the data is reflected toward the transmitted port (P1). So, no data is found at output Q. This condition is called 'RESET', and no light can be reflected by PSM. This condition maintains the same, even if D = 1 (then, light enters into the TOAD through P1 port and comes again to the incoming port P1, as no clock is present at that time).

Numerical simulation is done using a bulk InGaAsP SOA, operating at 1500 nm spectral region [9] (injection current = 400 mA, confinement factor = 0.48, differential gain = 3.3×10^{-20} m^2, linewidth enhancement factor = 8, carrier density at transparency = 1.0×10^{24} m^{-3}, volume = 150 μm × 1.5 μm × 250 nm, internal loss = 2700 m^{-1}). The simulated waveforms (a) CLK, (c) input D and (d) output Q are shown in Fig. 14. The gain variation of SOA in the TOAD loop is also plotted in Fig. 14(b). Simulation results, at 11.11 Gbit/s, show a high contrast ratio (~16.54 dB) and high extinction ratio (~13.64 dB). Signal to noise ratio is also evaluated and ~14.37 dB is obtained. The switching speed of this device depends on the gain recovery time of the SOA, which can be reduced by applying an 'assist light'.

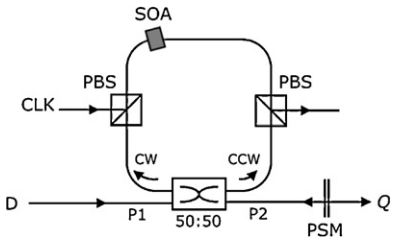

Fig. 13. Physical model of the all-optical clocked D flip-flop using single TOAD based interferometric switch.

3.4. Performance comparison between the different all-optical clocked D flip-flop techniques

The dynamic behavior of the different proposals for optical clocked D flip-flops is analyzed in Table 2.

Experimental results indicate that the technology based on two coupled SOA-MZI requires low energies to operate, presents photonic integration capability and high-speed potentiality. However, the switching speed of this configuration was limited by the recovery time of the SOAs.

As it can be seen in Table 2, the optical clocked D SOA-based coupled ring laser scheme can provide high extinction ratio between the states, however the length of the laser cavities (due to the discrete experimental implementation) affects, negatively, the switching times values.

The D flip-flop scheme, based on a single TOAD interferometric switch, presents less complexity than the other two configurations, because requires fewer components. Besides that, this configuration is also cost effective since it uses only one active element. Due to the fact that a TOAD can be integrated, and a micro mirror can be used for the partially silvered mirror, we believe that is possible to design the device to the chip-level.

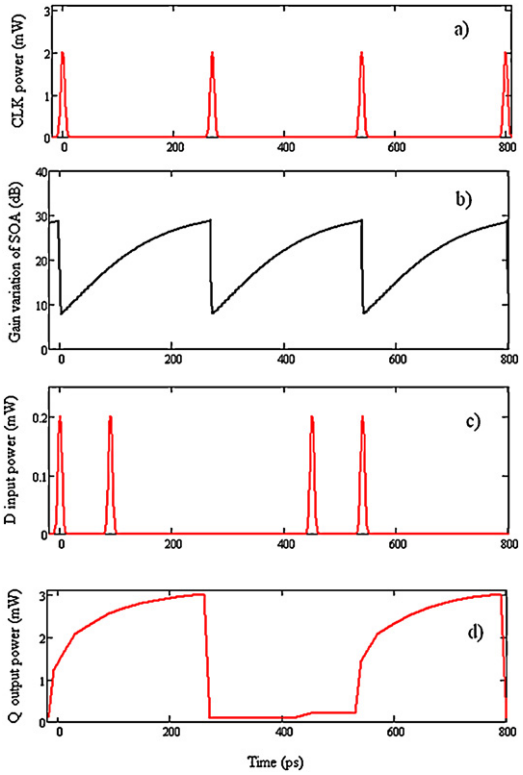

Fig. 14. Simulated waveforms of D-FF. (a) CLK power, (b) gain variation of SOA in dB, (c) D input power, (d) Qn output power.

However, experimental measurements must be carried out to confirm the agreement between the theory and the experimental work.

4. Conclusions

Clocked flips-flops are some of the most used elements in digital VLSI systems, however scaling CMOS sequential logic will be extremely difficult, namely due to the power consumer of their leakage currents. Therefore, it is so important to find high-speed and low-power optical flip-flops capable to overcome the limitations of CMOS technology.

In this paper, different approaches to implement all-optical clocked S-R and D type flip-flops were described and the main results were presented.

We also appraised, quantitatively, the different technologies of all-optical clocked S-R and D flip-flops. The performance of both types of flip-flops was studied in terms of ER, switching energies and switching times and the obtained results demonstrate the suitability of them in next generation communication systems.

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