Universidade de Aveiro Departamento de Electrónica, Telecomunicações e Informática,
2018

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Do Couto Pissarra

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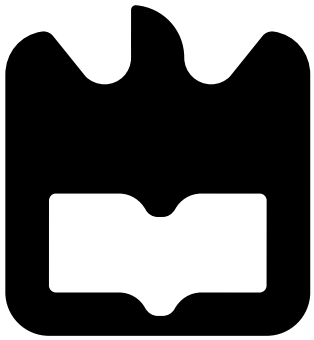
Automatic Calibration Systems for NG-PON2 Transceivers



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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações, realizada sob a orientação científica do Doutor António Luís Jesus Teixeira e do Doutor Mário José Neves de Lima, Professores do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro e do Engenheiro Francisco Rodrigues da PICadvanced S.A.

Dedico este trabalho aos meus pais e irmã.

o júri / the jury

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agradecimentos

Quero agradecer antes de tudo aos meus pais, Fernando e Anabela, e irmã, Diana, pela presença, força, dedicação, amor e educação transmitida bem como, por todas as oportunidades que me proporcionaram com o intuito de crescer e definir o melhor caminho possível.

Ao meu avô, António, a quem infelizmente já não poderei partilhar este momento, e à minha avó, Maria da Luz, pelo amor, ternura, constante preocupação e ensinamento. Um agradecimento especial aos restantes familiares pelo suporte durante esta caminhada, mais concretamente ao meu tio, Alcides, e à minha prima, Ana Celina, pelas brincadeiras e aventuras.

Ao professor António Teixeira e ao Engenheiro Francisco Rodrigues por me terem dado a oportunidade de desenvolver esta dissertação num ambiente empresarial, PICadvanced S.A., disponibilizando todos os recursos bem como aquisição do espírito de autonomia e confiança proveniente dos restantes membros da empresa aos quais também agradeço.

Um especial agradecimento ao Dr.Engenheiro Ricardo Ferreira, pelo seu importante e indispensável contributo para o desenvolvimento da dissertação, demonstrando sempre disponibilidade e, em especial, paciência e compreensão, transmitindo-me sempre uma força adicional para alcançar os objetivos delineados.

Quero agradecer também ao professor Mário Lima e ao Engenheiro Francisco Rodrigues, pela contribuição para a minha formação, ao longo do meu percurso académico, bem como durante a dissertação, ajudaram-me sempre que lhes solicitei ajuda.

Quero agradecer ainda à Sónia, numa perspetiva pessoal, pela alegria, atenção, disponibilidade e preocupação sempre com o próximo, reunindo as mesmas valências a nível profissional. Obrigado, professora Sónia, pelo determinante acompanhando académico e pela excelente ajuda para o término do mesmo.

Àqueles com quem partilhei estes 5 anos, mais concretamente Filipe Costa, João Nuno Maciel, Alexandre Fontes, um muito obrigado por todos os momentos, aventuras bem como partilha de apontamentos, ideias, estudos e trabalhos. À Maria Amaral, Catarina Gama e Carolina Fernandes, pela amizade, apoio e força para ultrapassar certos obstáculos.

À pessoa que não me deixou ir ao fundo nestes últimos 4 anos, por muito que escreva e escreva, nunca vou conseguir agradecer o suficiente por tudo que fez por mim, colocando tudo de lado para me tirar um sorriso. Obrigado por todo o caminho que já percorremos juntos e agradecer-te Adriana não é um gesto que se põe em papel, mas algo que se partilha ao longo da vida.

Este trabalho é financiado pelo Fundo Europeu de Desenvolvimento Regional (FEDER), através do Programa Operacional Regional do Centro (CENTRO 2020) do Portugal 2020 [Projeto HeatIT com o nº 017942 (CENTRO-01-0247-FEDER-017942)];

Palavras-chave Comunicações Óticas, NG-PON2, Transceptores, FPGA, MGTs, SERDES, BERT

Resumo

A sociedade atual depende cada vez mais dos serviços de comunicação, exigindo melhores ligações e mais rápidas, prevendo-se num futuro próximo a necessidade de ligações na ordem das centenas de Gbit/s.

O aumento dos ritmos de transmissão refletem um aumento no que se refere à taxa de erro (BER), uma vez que o impacto associado a fatores como ruído ou interferência entre símbolos, é maior do que para baixos ritmos.

Este trabalho foca-se no desenvolvimento de um sistema de teste BER, tanto para uma transmissão contínua como para transmissão em rajadas, que demonstre a viabilidade da comunicação sobre a tecnologia da próxima geração, Next Generation Passive Optical Network 2 (NG-PON2), que utiliza débitos de transmissão elevados (10 Gbit/s).

Para este efeito foi implementado uma arquitetura em Field-programmable gate array (FPGA) que possibilita para longas distâncias na rede ótica, elevados ritmos de transmissão. Esta escolha reflete uma alterativa mais económica em relação aos equipamentos comerciais e apresenta vantagens tais como a flexibilidade de reprogramar e preparar a arquitetura de acordo com as necessidades do utilizador.

Para cumprir os requisitos propostos o projeto dividiu-se em três partes. Numa primeira parte do projeto desenvolveu-se uma arquitetura que permite adquirir a taxa de erros durante uma transmissão contínua.

Com o intuito de analisar a viabilidade em tempo real da comunicação em questão, bem com o utilizador ter controlo sobre o sistema, alterando certas características do canal de comunicação, desenvolveu-se numa segunda parte do projeto uma interface entre o computador e a FPGA.

Numa última parte do projeto desenvolveu-se uma arquitetura semelhante à anterior, na qual se permite igualmente adquirir a taxa de erros com transmissão em rajadas (Burst), sendo este um dos requisitos de maior interesse na tecnologia NG-PON2.

Por fim, a prova de conceito foi realizada através de uma rede ótica disponibilizada pela empresa PICadvanced, que permitiu a validação das diversas partes do projeto. Estas validações vão permitir a conceção de novos módulos que posteriormente vão contribuir para o projeto fonte que está em desenvolvimento na empresa PICadvanced, que visa a implementação de uma placa de calibração automatizada para os transceptores 10 Gigabit Small Form Factor Pluggables (XFP).

Keywords Optical Communications, NG-PON2, Transceivers, FPGA, MGTs, SERDES, BERT

Abstract

The current society is increasingly dependent on communication services, requiring better and faster connections, predicting in a near future connections in the order of hundreds of Gbit/s. During the data transmissions, the increase of speed reflects an increase of the error ratio due to factors such as noise, reductions of signal or jitter, which for low speed these were not emphasized so much.

This project involves the development of a BER test system for both continuous and Burst mode of the transmission, demonstrating the viability of communication over the next-generation technology, NG-PON2, which uses high transmission rates (10 Gbit/s).

For this purpose, an FPGA architecture was implemented that allows for long distances in the optical network, high transmission rates. This choice reflects a more economical alternative in relation to commercial equipment and has several advantages, such as the flexibility to reprogram and prepare the architecture according to the needs of the user.

To achieve the proposed requirements, the project was divided into three parts. In the first part an architecture was developed that allows to obtain the error rate during a continuous mode transmission. In order to obtain the real-time viability of the communication referred and to have control over the system, an interface was developed between the computer and the FPGA to change certain characteristics of the communication channel. This is the second part of the project.

The last part of the project has an architecture similar to the previous one, that is, instead of the transmission to be done in continuous mode, it is performed in mode Burst, being this the requirement with more interest to the technology NG-PON2.

Finally, proof of concept was performed through an optical network provided by the company PICadvanced that allowed the validation of the different parts of the project.

These validations will allow the development of new modules that will later contribute to the main project that is under development in the company PICadvanced, which aims at the construction of an automatic calibration board for the XFP transceivers.

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Acronyms

B2B	Back to Back
BER	Bit Error Rate
BERT	Bit Error Ratio Test
BWmap	Bandwidth Management
CDR	Clock Data Recovery
CLBs	Configurable Logic Blocks
DFE	Decision Feedback Equalizer
ER	Extinction ratio
FPGA	Field Programmable Gate Array
FS	Framing Sublayer
FSAN	Full Service Access Network
FSM	Finite State Machine
G-PON	Gigabit Passive Optical Network
ITU-T	Telecommunication Standardization Sector
LPM	Low-Power Mode
LUTs	Look-up Tables
MGTs	Multi-Gigabit Transceivers
NG-PON	Next-Generation Passive Optical Network
NG-PON2	Next-Generation Passive Optical Network 2
ODN	Optical Distribution Network
OFDM-PON	Orthogonal Frequency Division Multiplexing PON

OLT	Optical Line Termination
OMCI	ONU Management and Control Interface
ONT	Optical Network Terminal
ONU	Optical Network Unit
OPP	Optical Power Penalty
OSI	Open System Interconnection
PCS	Physical Coding Sublayer
PHY	Physical Interface
PISO	Parallel in Serial Out
PLL	Phase-locked loop
PMA	Physical Medium Attachment
PMD	Physical Media Dependent
PON	Passive Optical Network
PRBS	Pseud Random Bits Sequence
PSBu	Physical Synchronization Block appropriate for Downstream
ROM	Read-Only Memory
SDU	Service Date Unit
SerDes	Serializer/Deserializes
SIPO	Serial in Parallel Out
SMA	SubMiniature version A
TC	Transmission Convergence
TDM-PON	Time Division Multiple
TDMA	Time Division Multiple Access
TEC	Thermoelectric Cooler
TWDM	Time and Wavelength Division Multiplexed Passive Optical Network
TWDM-PON	Time and Wavelength Division Multiplexed Passive Optical Network PON
TWDM-TC	Time and Wavelength Division Multiplexed Passive Optical Network Transmission Convergence
UART	Universal Asynchronous Receiver-Transmitter
VCO	Voltage-controlled oscillator
VOA	Variable Optical Attenuator

WDM	Wavelength Division Multiplexed
WDM-PON	Wavelength Division Multiplexed PON
XFP	10 Gigabit Small Form Factor Pluggable
XG-PON	10-Gigabit Passive Optical Network

Chapter 1

Introduction

This work occurs in the context of the development of the project conducted in the Curricular Unit Dissertation, within the study plan of the Integrated Masters in Electronic and Telecommunications Engineering. In this section, an introductory analysis of the project is made, from its general framework and the motivational point of view. Finally, a description of the problem, of its objectives and the structure of this dissertation is made.

1.1 General Framework

Over the past few years, the demand for high bandwidth has been increasing rapidly due to the emergence of advanced multimedia applications such as video services, online gaming, live streaming, ultra-High Definition and many other services, all of them competing for the same resources. Therefore, upgrading and developing new technologies is necessary to accommodate the new applications. The major topic of concern for telecommunication operators has been the increase of the bandwidth used by the end user[1].

According to Cisco's Visual Networking Index (VNI), from 2016 until 2021 the total amount of data exchanged between mobile and users is expected to increase each year. This will create a networked society, and consequently a tremendous growth in mobile data will place huge pressure on operators. Figure 1.1 illustrates the global mobile data traffic required for next years [2].

Figure 1.1: Global Mobile Data Traffic Drivers[2]

Due to the technological advance, as well as the diversification of services and massification in internet access, there is a need for a modernization of telecommunication access network, particularly in the transition of Fiber technologies, since the requirement of a higher bandwidth and faster speeds are always present, challenging the limits of network capacity [3].

For the last years, operators have expressed interest in the implementation and development of Passive Optical Network (PON), to provide better service to users, such as high rate per client, as well as for providers once PON networks are attractive since they do not depend on active elements between their endpoints, allowing for reduction of maintenance costs and better operational efficiency [4].

PON technologies were standardized and developed across the world, but the increasing bandwidth demand makes the necessity for this type of network to evolve. Therefore, the current standardized technologies Giga-capable PON (G-PON) need to be upgraded to Next-Generation PON2 (NG-PON2), which is the next step on access network evolution and is currently on the process of study and standardization [5].

The NG-PON2 must co-exist on the same optical distribution network (ODN) of the G-PON, so it re-utilizes the already built infrastructures and consequently protects the initial investment and reduces the operation costs [5].

The full service access network (FSAN) group has been using the roadmap to guide the development of PON and according to them, NG-PON2 belongs to the next generation of PONs and is currently being standardised and is expected to be implemented in the near future [6]. Figure 1.2 illustrates the PON evolution.

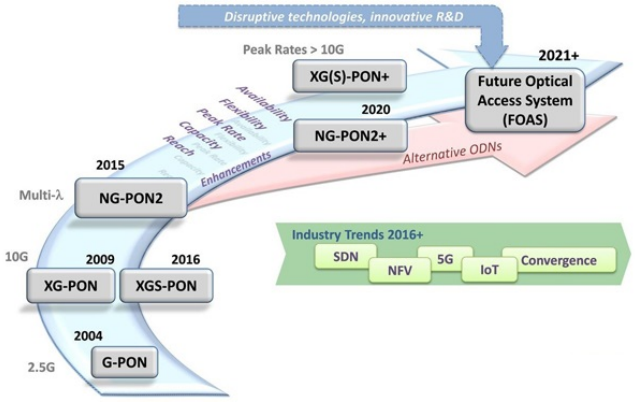


Figure 1.2: Future PON network development[7]

The principle of NG-PON2 is to improve previous technologies, in terms of capacity, ODN compatibility, bandwidth and cost-efficiency. In April 2012, FSAN selected the Time Wavelength Division Multiplexing PON (TWDM-PON) technology as the best solution of choice for NG-PON2 [6][8].

Observing figure 1.1 and 1.2 it is possible to conclude that existing resources are not able to respond to this growing need for high-speed communications. Due to this it is urgently necessary to develop technologies, not only able to satisfy this demand, but at the same time to do it in an energetically and financially efficient way.

In this context the company PICadvanced appeared and has been responding increasingly with the pre-production of its 10 Gigabit Small Form Factor Pluggable (XFP)s for optical

network terminal (ONT) of NG-PON2 technology.

This pre-production is achieved through an automatic board that has been developed at PICadvanced in order to achieve automated calibration of the essential parameters for the final production of the XFPs.

Currently, the calibration board requires the development of some modules for the final step, allowing a greater productivity and yield in the production response of the XFPs, so that they can reach the final customer and consequently respond to the current needs of society.

1.2 Motivation

In the telecommunication market there must be standard for both the networks and the components, so that interoperability is achieved, and several manufacturers for the same technology [9]. The standard that PICadvanced follows for its transceivers NG-PON2 is the XFP that allows 10 Gbit/s in its data lines, which matches the specifications of the network standard [10].

Currently, the company PICadvanced has its XFP for ONT NG-PON2 pre-production and is in the final stage of the automated board development which allows the calibration of XFPs parameters, figure 1.3. As a way to increase its efficiency, this stage requires the implementation of test systems that will allow the control of the optical components and that will later be emulated in an optical network.

Therefore, one of the main requirements for this final stage is the addition of an FPGA to the calibration board referred, in order to implement an architecture for the automatic measurement of the BER levels of the system that will communicate, through inter-integrated circuit (I2C) with the microcontroller.

This microcontroller is already available in the current board and it coordinates all the test systems that aim at the production of the XFP, thus enabling the automation of the calibration board.

The achieved test systems are validated through a firmware environment developed to control the system as a whole.

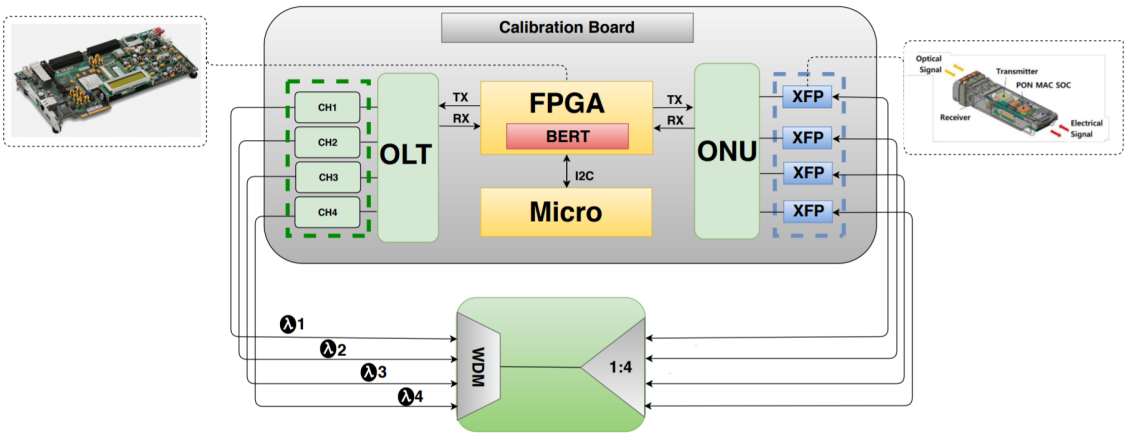


Figure 1.3: Automated board general project for XFPs calibration

1.3 Problem description and objectives

This project has as main objective the development of an architecture capable of providing to the microcontroller of the referred calibration board, the automatic measurement of BER levels in both directions, downstream and upstream.

The development platform used in this project is the Xilinx evaluation board KC705. It is equipped with an FPGA XC7k325TFBG900-2 device, provided with GTX transceivers supporting a line rate up to 10 Gbit/s.

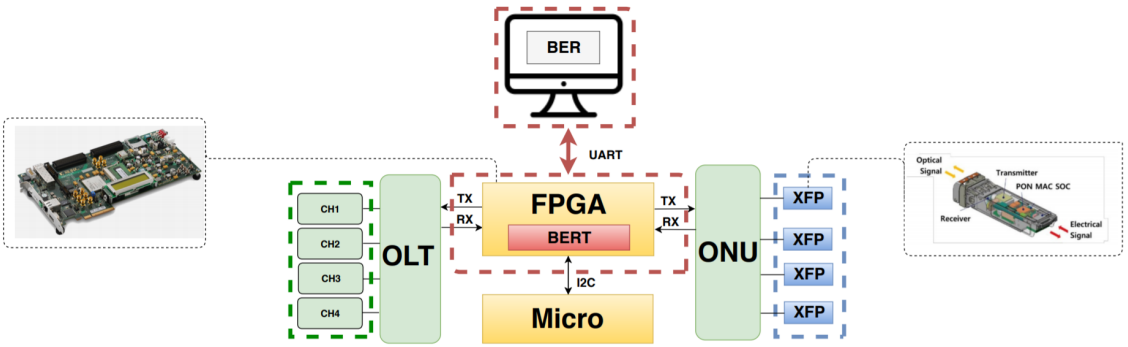


Figure 1.4: General diagram of the proposed problem

Figure 1.4 illustrates the general design of the project to be carried out. To simplify its development, it was divided into 3 stages:

- Design and development of a bit error rate test (BERT) to a communication implemented in:
  - Continuous Mode [11]
  - Burst Mode [12]
- Design of architectures that perform serialization and deserialization of data;
- Design and develop an interface so that the user may control the test system developed;

The first part consists on obtaining an architecture in the FPGA of BERT system that allows evaluating the viability of the communication in future NG-PON2 technology.

This test system reflects on the underlying TWDM technology in the NG-PON2 that makes it possible to evaluate the communication when it is performed in a continuous mode, that is, when the communication is performed in a downstream direction between the optical line terminal (OLT) and optical network unit (ONU), as well as the reverse direction, upstream, when communication is performed in Burst mode [6].

The second part of the project consists on the design of an architecture provided by the FPGA that allows the serialization and the deserialization of the data. This architecture convert the data from series into parallel, throught the deserialization process followed by the inverse process, serialization, that sends the data from parallel to series again, allowing it to be sent to the optical fiber network.

The third and final part of the project consists on an interface from the Universal asynchronous receiver/transmitter (UART) communication protocol between the FPGA and the

computer, in order to allow the control of the BERT system, by changing several parameters made available by the developed firmware application. Once the three parts of the project are completed, the final goal is achieved.

1.4 Structure

- **Chapter 2: Concepts about the Next Generation Optical Networks** It explores important concepts about optical communications for the development of this dissertation. Initially, it gives an approach to the NG-PON2 standard and how the merit figures relate to the NG-PON2 transceivers, followed by the description of the transmission convergence layer that specifies the content of the different frame flows, for both downstream and upstream frames.

- **Chapter 3: FPGAs for Calibration System - Technical Overview** It present an overview of several aspects of the FPGA is presented, exposing the underlying architecture of the available transceivers Xilinx (KC705 Kintex-7) FPGA as well as some considerations relevant to the correct operation of the project in general.

- **Chapter 4: Implementation and Results of BERT in Continuous Mode** It describes the design and development of the all architecture and of interface related to the implementation of the BERT system in continuous mode. This chapter ends with several tests and results in order to get the concept's proof of the architecture presented in 1.3.

- **Chapter 5: Implementation and Results of BERT in Burst Mode** It explores the previous architecture to reach Burst mode, describing the architecture changes required for this mode to be achieved, approaching all issues and problems related to the Burst mode condition. Finally, the results are presented.

- **Chapter 6: Conclusions and Future Work** Presents a description of what was achieved, as well as the main conclusions taken from this project. Suggestions for more work on this topic are also presented.

Chapter 2

Concepts about the Next Generation Optical Networks

2.1 40-Gigabit-capable PON (NG-PON2)

2.1.1 PON General Architecture

In order to support the high usage of bandwidth, optical communication networks that support high data rates had to be developed. Currently, in the access network, the optical communications architecture in use is based on Passive Optical Network (PON).

PONs have a topology that share point-to-multipoint (P2MP) architecture where all the elements should be passive, this is, without power supplies to operate. This architecture consists of the following main elements: the optical line terminal (OLT), the optical distribution network (ODN) and the optical network unit (ONU).

It uses a passive fiber tree topology to maximize the coverage, allow flexibility, and minimize the number of networking splitting, thus reducing the optical power loss and increasing the physical reach. The success of PON relies on its high bandwidth, infrastructure cost sharing, and simple maintenance and operation, which results from the absence of electronic active components between the OLT and the ONUs. Figure 2.1 presents each of the mentioned PON elements [6].

They are defined by the following[10]:

- **OLT**: Is the device located in the telecommunications operator terminal in charge of the management and maintenance of the ODN and its function is to transmit and receive data to several users. It sends the broadcast signal to all ONUs, controlling and synchronizing the data exchange in the access network.

- **ONU**: Is the device that terminates the network on the user side and receives the transmission signal from the OLT and then selects the data desired.

- **Splitter**: from the OLT, a single mode optical fiber is connected to the entrance of a 1: N passive optical splitter, where the N outputs of the splitter are connected to the ONUs of the clients via single mode individual optical fiber. This set of single-mode optical fibers and passive optical components that are installed between the OLT and end users, ONU, is called the ODN.

The two directions for optical transmission in the ODN are identified as follows:

- **Downstream**: Is the direction which the signals are transmitted from the OLT to the ONU. In this case, the OLT is the transmitter and the ONU is the receiver.

- **Upstream**: Is the direction which the signals are transmitted from the ONU to the OLT. In this case, the OLT is the receiver and the ONU is the transmitter.

In both directions of the transmission, Downstream and Upstream, the same components and optical fibers are used.

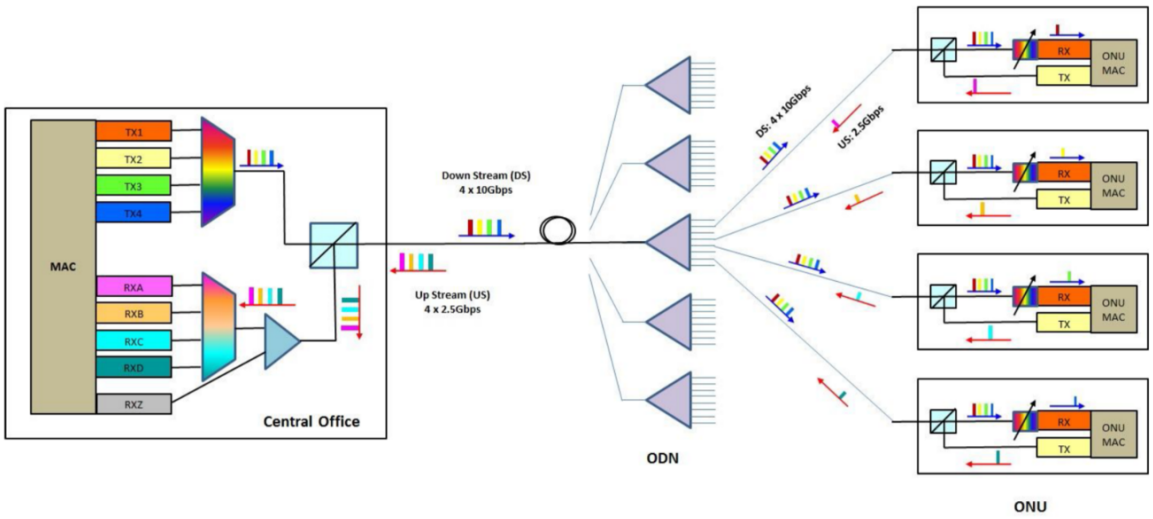


Figure 2.1: Traffic between OLT and ONU [13]

2.1.2 NG-PON RoadMap

FSAN group along Telecommunication Standardization Sector (ITU-T) are the forum standardization with the greatest activity in the study of PON evolution. The network operators have resorted to NG-PON solutions that can transparently coexist with legacy PONs on the existing fiber infrastructure and enable gradual upgrades in order to protect the investments [14].

Also, it is very important that coexistence on the same ODN is supported to satisfy cases where fiber resources are not abundant, and to minimize the interruption of service for users who are not migrating [6][14].

In addition, NG-PON must provide all G-PON legacy services in case of full migration and according to those entities, NG-PON technologies are divided into two parts: first stage NG-PON (NG-PON1), better known as 10-Gigabit Passive Optical Network (XG-PON), and second stage NG-PON (NG-PON2). NG-PON1 is known as the mid-term next generation based on 10 Gbit/s for both downstream and upstream directions [6].

NG-PON2 has been proposed by FSAN as a solution for new services applications, it is considered as the long-term generation of the optical access network which allows providing no less than 40 Gbit/s downstream and must remain backward compatible, figure 2.2 [15].

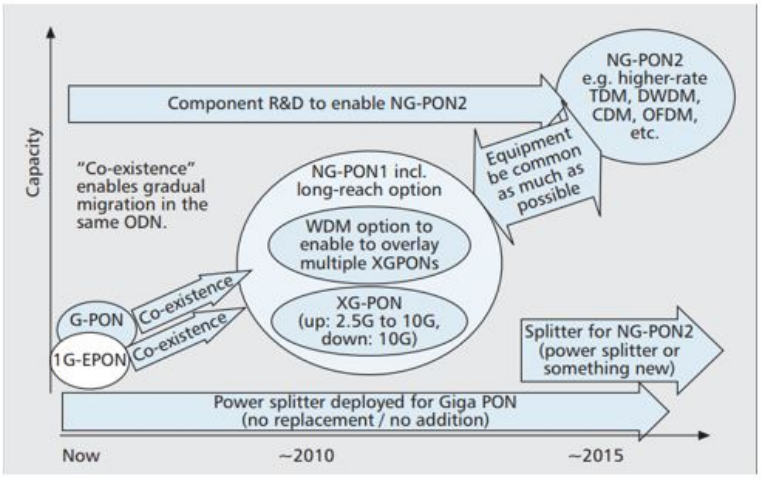


Figure 2.2: NG-PON2 roadmap [15]

2.1.3 NG-PON2 Standard

NG-PON2 is the response of network providers to increase the efficiency through the development of new services only possible with increase of bandwidth, especially the triple-play services, with voice, video, data, file sharing and online gaming that requires higher bandwidth capacity.

This technology is capable of offering higher capacity per customer than current G-PON and XG-PON1 systems, since it is a direct evolution of PON networks, which are a generation of independent PON systems based on the same transmission share part or all of the ODN through several dedicated wavelengths as form of protecting the service provider's initial investment by taking advantages of the existing ODNs [15].

2.1.4 Architecture

NG-PON2 is the latest of the ITU-T standardized PON system. The standard for NG-PON2 was defined by ITU-T in a series of recommendations G.989.x (x = 1, 2, 3) that define characteristics of the NG-PON2 system and the specifications from the Physical Media Dependent (PMD) and the Transmission Convergence (TC) [10][16][17].

The general requirements document (ITU-T G.989.1)[10] was approved in March 2013, addressing some requirements. Then in December 2014 (ITU-T G.989.2)[10] PMD specifications were addressed. The last and most recent was approved in October 2015, addressing TC specifications.

Several technologies were suggested to support the requirements for the NG-PON2, such as 40G TDM-PON, wavelength division multiplexed PON (WDM-PON), time and wavelength division multiplexed PON (TWDM-PON) and orthogonal frequency division multiplexing PON (OFDM-PON) [18].

WDM-PON fails to adhere to the main requirements of NG-PON2, which is backward compatibility and, unfortunately, this feature is not available in this approach since it re-

quires wavelength selective optical ODN. 40G TDM-PON is also excluded due to the costs of implementation for each end user and the high chromatic dispersion over long distances. OFDM-PON, due to its need of time frame, which is a complex technology and its implementation would have high costs as well as risks [18][19].

2.1.4.1 TWDM technology

Amongst these technologies, TWDM-PON has been selected as the best candidate for NG-PON2 and is supported by major telecommunication companies because it supports backward compatibility, flexibility and static sharing. It increases the aggregate PON rate by stacking XG-PONs via multiple pairs of wavelength. On a TWDM-PON architecture, four XG-PON networks are stacked by using four pairs of wavelength which are able to provide 40 Gbit/s and 10 Gbit/s as the present target and 160 Gbit/s and 80 Gbit/s as a future target for downstream and upstream, respectively [10].

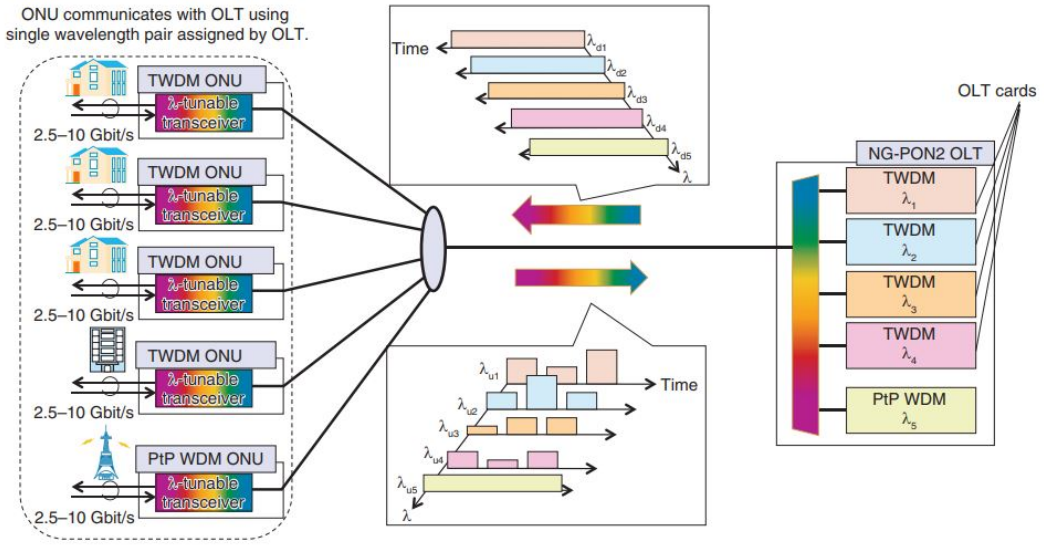


Figure 2.3: NG-PON2 roadmap [7]

Figure 2.3, shows the architecture of the standard TWDM-PON system, which uses both WDM and TDMA. Typically, the architecture has a tree topology, with OLTs at the root of the tree and ONUs as the leaves, already between the OLT and the ONU, there is a new PON ODN (feeder fiber and power splitter) [10].

On the OLT side, a set of laser diodes, such as distributed feedback (DFB) laser diodes operating at different wavelength, serve as downstream laser source, followed by a WDM for multiplexing. The goal of the splitter used in ODN is to distribute power to all ONUs and consequently, each ONU would receive all wavelengths. Therefore, the ONU in TWDM-PON is equipped with a tunable transceiver, so it can selectively transmit or receive upstream/downstream data on a pair of upstream/downstream wavelengths [20].

A tunable filter at the receiver is used to select or tune to any of the four downstream wavelengths. In case of upstream wavelengths, the tunable laser is used to provide colourless ONU [5].

Options to the baseline architecture include more pairs of wavelengths and different rates for stacking. TWDM-PON works with 4 – 8 channel pairs, each consisting of one downstream and one upstream wavelength channel, each channel pair should support nominal line rates of [6][10]:

	Downstream (Gbit/s)	Upstream (Gbit/s)
Basic Rate	10	2.5
Rate Option 1	10	10
Rate Option 2	2.5	2.5

Table 2.1: Relation between TWDM PON line rate options (adapted [10])

2.2 Measurements and Figures of merit in NG-PON2

There are several trade-offs between laser and receiver and, due to it, several figures of merit need to be checked in order to test the transceiver for characterization in NG-PON2. The figures of merit which require more attention for ONUs in this architecture are the Burst-mode operation, laser driving, tunability between four downstream and four upstream channels, and BER measurements.

2.2.1 Burst Mode

In TWDM-PON technology the downstream traffic is continuously broadcast to all ONUs, and each ONU selects the packets needed and discards the ones addressed to other ONUs and the upstream traffic of each ONU is only transmitted during pre-assigned time slots by the OLT, as illustrated in figure 2.4. A Burst mode transmitter requires the following features: fast Burst on/off speed, sufficient power suppression during idle period, and stable, accurate power emission during Burst transmission. These functionalities can be performed by specially designed laser drivers that are the most critical part of Burst-mode transmitters [21].

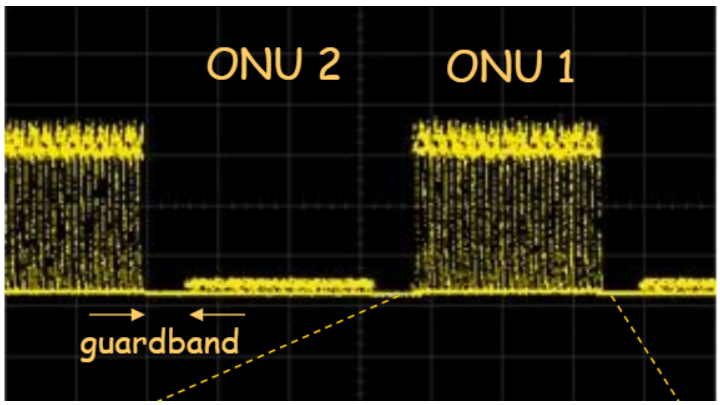


Figure 2.4: Data trace in Burst Mode Operation[22]

In conventional laser drivers, such as direct modulation, the bias current is maintained constant for continuous transmission. Burst mode operation requires the bias current to be

quickly turned on/off before/after Burst is transmitted. When an ONU is not transmitting, its laser is turned off and due to this, the temperature of the laser drifts and consequently wavelength is not the desired one [23].

Therefore, if the laser is turned off it is necessary to introduce a compensation into the driving circuitry in order to compensate the cooling and it will still be kept at the same temperature and wavelength that it had when transmitting. This compensation proves to be important because of the small spacing between the technology channels in NG-PON2.

2.2.2 Laser Driving

In high-speed optical communication systems the laser diode and modulator driver is one of the key components in the transmitter, where it performs the interface between high-speed electronics and the laser diode or modulator.

Therefore, the main goal of driving circuitry is to provide electrical power to the optical source and to modulate the light output in accordance with the signal that is to be transmitted. In semiconductor lasers, the bias current of the laser should be closed to threshold and then modulated by an electrical time-dependent signal. Thus, the driving circuit is designed to supply a constant bias current as well as modulated electrical signal [24].

The power at the output of a semiconductor laser depends on the current injected through the laser diode according to the power/current function represented in figure 2.5 [25].

When the population inversion is achieved, it means that the current reaches the threshold leading to lasing action. The laser output power then increases linearly with increasing current, until some saturation is reached for high bias current values.

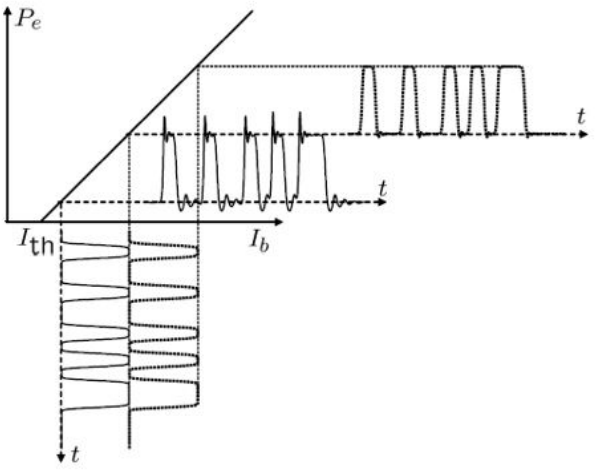


Figure 2.5: Direct current modulation of a semiconductor laser[25]

According to the modulating signal, the laser driving current is assorted resulting into modulation of the emitted power. The modulation optical signal is represented at two different values of the bias current, but an increase in the bias and modulation currents of the laser will increase its output power, resulting in improved dynamic behaviour.

It is important to notice that the laser threshold increases and the power/current function efficiency decreases as the operating temperature goes up. The laser threshold is sensitive to the operating temperature and the bias level control is needed [25].

Extinction ratio (ER) is an important parameter included in the specification of most fiber optic transceivers. It can affect the performance of digital optical communication systems because it transmits binary data using two levels of optical power, where the higher power level represents a binary 1 and the lower power level represents a binary 0. These two power levels can be represented as P1 and P0 where P1 > P0 and the units of power are watts [26].

For a constant temperature the transfer function stays the same, meaning that if bias current were to change, the ER would decrease with the increase of the power of the zero, and ER is given by:

$$ER\ (db) = 10log(\frac{P1}{P0}) \tag{2.1}$$

Changes in the driving current of the laser influence its output power and the maximum allowed power to the standard, needs to be between 4 dBm and 9 dBm upstream direction [10].

- Too much power may cause non-linear effects in the fiber.
- Too low power may produce lacking BER and sensitivity merit figures.

It is necessary to be careful with the increase of the driving current of the laser since it may diminish the ER of the optical fiber and may cause it to become lower than the minimum of 6 dB, which is set by the standard. A lower value of ER will require more optical power penalty which indicates how much more power is needed in the input of the receiver to ensure the same error probability, being this a feature defined by standard, and the value is between 1 and 2.

2.2.3 Tunable transmitter and receiver

In TWDM-PON system wavelength-tunable ONUs are implemented, which realize several attractive functions, such as the load balancing, power saving and colourless ONU, and redundancy [27][28].

- Load balancing:
  - It happens when the ONU communicates with an OLT using the wavelength initially allocated by the OLT. The OLT orders ONU to change its wavelength to another empty wavelength when traffic concentrates on one wavelength.
- Power saving:
  - ONU power consumption can be adequately decreased by the power-saving functions. The OLT side power saving can happen during the time of low traffic load (for example overnight) as all ONUs on an ODN can retune to a common wavelength and allow OLT ports to be powered down.
- Colourless:
  - The colourless ONU means that all ONUs in the system have the same specifications and are wavelength-independent that allow reduced manufacturing and operation costs derived from inventory reduction (management), flexibility.

- Redundancy:

  - ONU can change the wavelength to connect to a healthy OLT if the original OLT fails. Appropriate specifications to realize this are expected.

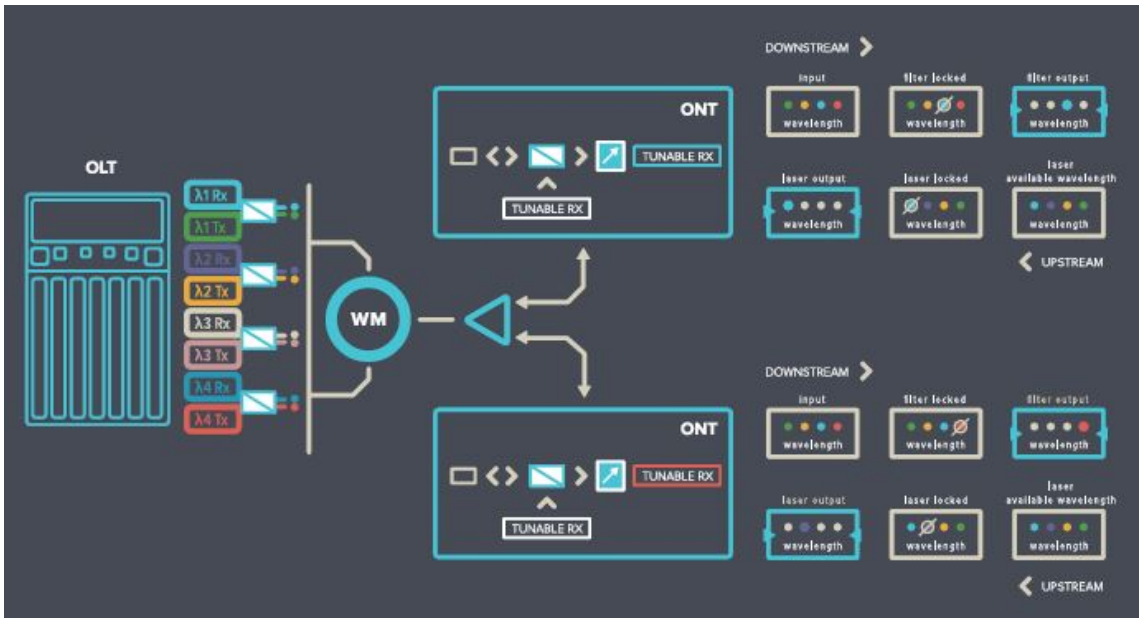


Figure 2.6: TWDM PON Wavelength tuning [29]

Therefore, the ONUs are equipped with tunable transceivers and tunable receivers that function as selectors to any of the four upstream and downstream channels. For each ONU transceiver to be able to tune its reception to one of the downstream wavelength and its transmission to the corresponding upstream wavelength, it is necessary to employ different filters locked to a specific wavelength in each ONU, as shown figure 2.6. [30][29]

So, the transceiver must be able to change the laser parameters in order to allow the wavelength of the spectrum to change to another channel. The main goal of the laser is allowing a change in the band that the photodetector receives, that is, that filters the incoming optical signal to the band desired [30].

It is usually used as a tunable optical filter, the component shown in 2.7, composed of a single cavity and two distributed Bragg reflectors (DBR). The refractive indices of optical layers vary by controlled temperature, shifting the transmission wavelength of the filter.These changes in temperature can be achieved with a thermometric cooler (TEC). It allows to change and maintain a set temperature, and consequently its wavelength, allowing it to tune to a specific channel in architecture with more than one wavelength, like NG-PON2.

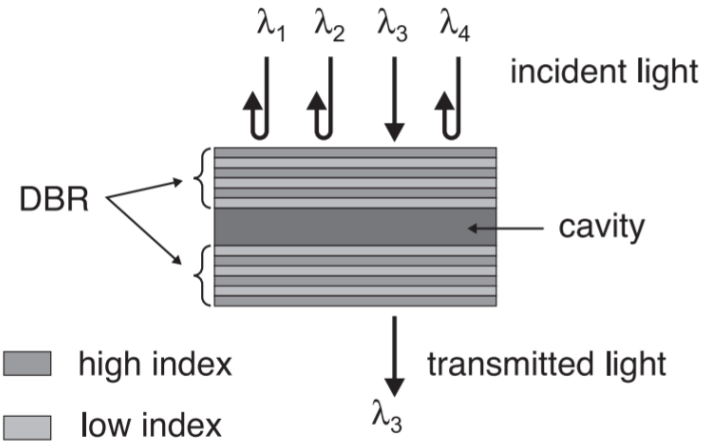


Figure 2.7: Example of a structure transparent to a certain wavelength and reflective to others [31]

One important aspect in NG-PON2 is the tuning time between channels. There are three classes for the wavelength channel tuning time of the ONU transmitter and receiver that are specified in NG-PON2 as shown in table 2.2.

Classes	**Tuning Time**
1	< 10 μs
2	10 to 25 ms
3	< 1 s

Table 2.2: NG-PON2 tunning time classes[10]

2.2.4 BER

BER measurements are used to assess systems that transmit digital data from one location to another.

When data is transmitted over data link, there is a possibility of errors introduced into the system, such as, noise, interference, and phase jitter may cause degradation of the digital signal which affects the integrity of the system [32][11].

Therefore, it is necessary to evaluate the performance of the system and this can be achieved by means of BER measurements. It enables to assess if communication can be supported or if it is difficult or even impossible, rather than testing the component parts and hoping that they will operate satisfactorily when in place.

BER can be defined as the rate at which errors occur in a transmission system. The following equation 2.2 shows the ratio between the number of errors that occur in a string of a stated number of bits [33].

$$BER = \frac{ReceivedBits\ with\ errors}{Total\ number\ of\ bitstransmitted} \tag{2.2}$$

For a fiber optic system, bit errors essentially result from imperfections in the components

used to make system connections, such as the optical driver, receiver, connectors and the fiber itself, but it can also be introduced as a result of optical fiber dispersion and attenuation [32].

In what concerns the receivers, the sensitivity is defined as the minimum optical power required to achieve a specific BER. The number of errors at the output of decision circuit will determine the quality of the receiver and, of course, the quality of the transmission system [34].

In NG-PON2 the merit figure for BER is that the sensitivity, that is the power at which the BER = 1×10^{-3} must be equal or lower than -28 dBm for downstream and -26 dBm for upstream, only to Type A link at 10 Gbit/s [10]. An additional requirement is that power penalty of the 20km of fiber, that is, the difference between sensitivity with or without fiber what is called optical path penalty (OPP), must be lower than 2 dB for downstream and 0.5 dB for upstream [10].

2.3 Transmission Convergence (TC) layer

The transmission convergence (TC) layer is the protocol layer of the NG-PON2 system that is positioned between the PMD layer and service clients. More details will be presented in the following chapter. It builds on the XG-PON recommendations [35], with modifications for NG-PON2's specific features. This subsection was made according to [17].

A NG-PON2 system may contain a set of TWDM channels, a set of point-to-point wavelength-division multiplexing (PtP WDM) channels or both. Each technology uses a different TC layer and only the first will be described in this subsection.

The TWDM-TC layer is a part of the TWDM-PON protocol stack that specifies the formats and procedures of mapping between the upper layer services data unit (SDUs) and bitstream suitable for modulating the optical carrier.

This layer is composed by three sublayers, which are, service adaptation sublayer, framing sublayer and physical adaptation sublayer. It is also responsible for functions such as the performance monitoring, security key management, ONU power management, TWDM channel management and protection.

TWDM-TC layer is present in both the OLT and the ONU side. In downstream direction, the interface between TWDM-TC and PMD layers is represented by the bitstream divided into the frames of 125 μs duration. In the upstream direction, the interface is represented by the series of precisely-synchronized time-bursts.

With the help of figure 2.8, the three layers mentioned will be focused on, referring to some essential blocks and properties in a brief way.

- TWDM-TC service adaptation sublayer:
  - Is responsible for the upper layer SDU encapsulation, multiplexing and delineation. This layer deals with two types of SDUs such as user data frames and ONU Management and Control Interface (OMCI) messages that decompose logically in a XG-PON Encapsulation Method (XGEM) engine and two service adapters: the user data adapter and the OMCI adapter. The user data adapter can also be configured to accommodate a variety of upper layer transport interfaces.

- TWDM-TC framing sublayer:
  - Is responsible for the construction and managing the fields necessary for the data-stream management in PON. The TWDM-TC framing sublayer formats are devised so that the frames, bursts and their elements are aligned to 4-byte word boundaries, whenever possible.
- TWDM-TC PHY adaptation sublayer:
  - provides function to modify the data-stream modulated by the optical transmitter in order to improve the detection and sensitivity. It also describes the properties of the signal transmitted through the optical medium and secures the data by the error-coding techniques.

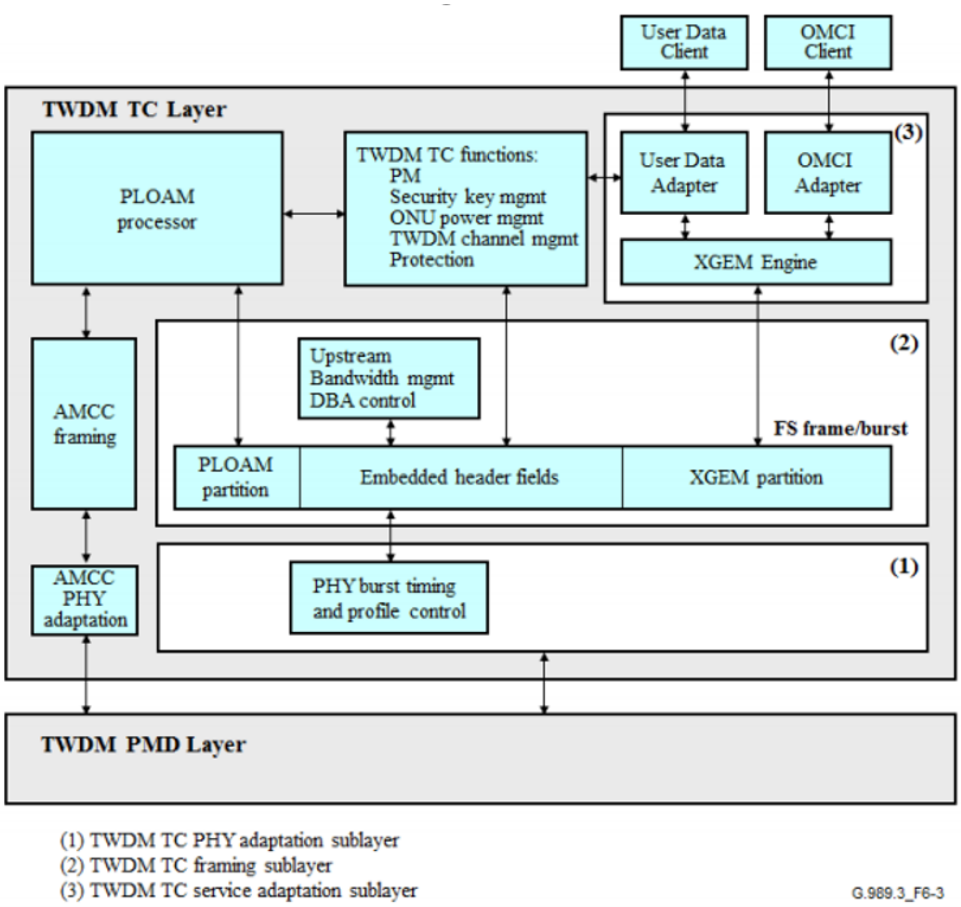


Figure 2.8: Outline of TWDM TC information flow [16]

During this project there will be the need to work on the TWDM physical layer and due to this it is important to understand what this layer essentially contains and what its requirements for its ideal operation are. Therefore, within this layer there are two essential frames such as downstream PHY frame and upstream PHY frame, which will be the frame explored during the last part of the project.

The downstream transmitter of the OLT operates in continuous mode at one of two possible line rates: 9.95328 Gbit/s or 2.48832 Gbit/s.

A downstream PHY layer frame consists of physical synchronization block appropriate for downstream (PSBd) and a PHY frame payload, figure 2.9. The PHY payload is represented by the downstream FS frame whose content is scrambled and optionally protected by forward error correction (FEC), it can be turned on or off depending on the operational considerations.

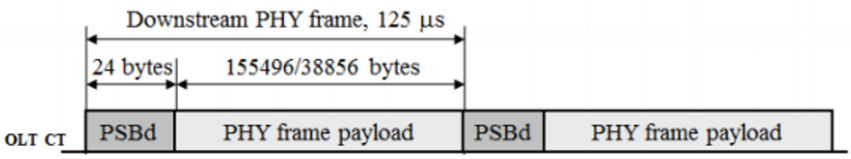


Figure 2.9: Downstream PHY frame [16]

The ONU upstream transmitter operates in the Burst mode at the nominal line rates of 9.95328 Gbit/s or 2.48832 Gbit/s. In the upstream direction, each ONU transmits a series of relatively short PHY bursts and remains silent, disabling the transmitter in between the bursts.

At the PHY layer, each upstream ONU burst contains the physical synchronization block appropriate for upstream (PSBu) and an upstream FS frame containing a header used for identification, status indication and series of individual allocations, among others.

For each upstream ONU transmission burst, the BWmap in the downstream FS frame specifies the start time of the burst and the size for individual allocations within the burst so that the upstream transmissions by different ONUs are non-overlapping.

The PSBu, figure 2.10, contains a preamble and a delimiter. The preamble and the delimiter are employed by the optical line terminal channel termination (OLT CT) Burst mode receiver to determine the presence of a PHY burst and delineate the PHY burst. According to [16], the recommended size of the preamble and the delimiter is 160 bits and 32, respectively.

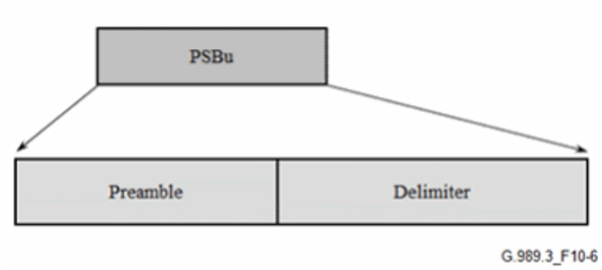


Figure 2.10: Upstream physical synchronization block [16]

Observing figure 2.9 it is possible to conclude that the transmission of OLT is split into fixed size downstream PHY frames, while in figure 2.11 each ONU transmits a series of bursts of different sizes. Both transmission frames have a duration of 125 μs, which corresponds to the maximum size of 38880 bytes at the rate of 2.48832 Gbit/s, and to the maximum size of 155520 bytes at the rate of 9.95328 Gbit/s.

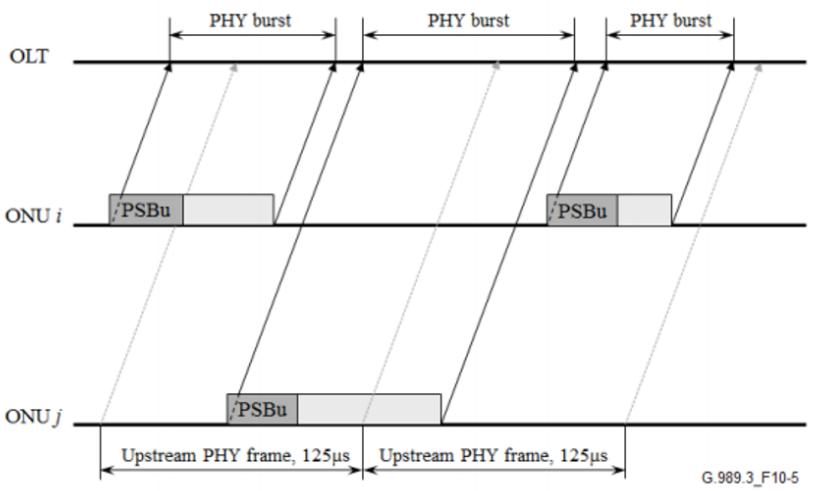


Figure 2.11: Upstream PHY frame and upstream PHY bursts [16]

Chapter 3

FPGAs for Calibration System - Technical Overview

3.1 Field-Programmable Gate Array (FPGA)

FPGAs, are integrated circuits containing logic which can be programmed by the user in the field [11]. Logic blocks contain a wide set of programmable logic gates and memory elements (simple flip-flops or more complex block of memories). FPGAs also contain interconnection resources, which allow the blocks to be wired together and to implement almost any kind of digital circuit or system. [11][36] The logic described in hardware description language (HDL) such as VHSIC Hardware Description Language (VHDL) or Verilog can later be synthesized with software that also implements the design and generates a bit-file which describes how the configurable logic blocks (CLBs) and interconnections are to be configured (to implement the desired logical functions) [11].

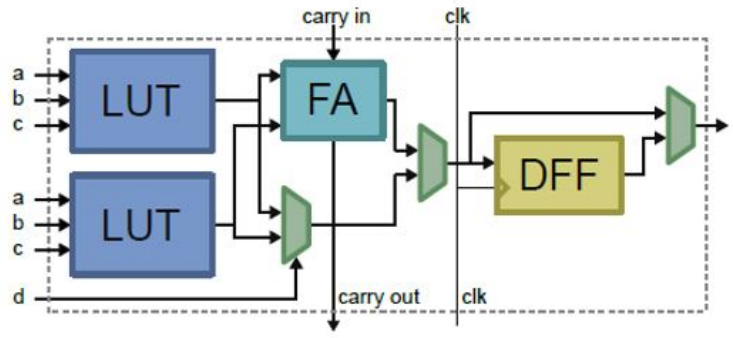


Figure 3.1: A Configurable Logic Block used in FPGAs [11]

The interconnections and look-up tables (LUTs) are configured by 1-bit memory cells, mostly static random access memory (SRAM) based, which make certain connections to CLBs and make LUTs hold certain values. The LUTs can implement all combinational logical functions, i.e., OR, AND, NOT, XOR and their complements as well as any custom behaviour. Figure 3.1 shows an example of a CLBs. CLBs can contain full adders (FAs) for accelerating addition and subtraction and some FPGAs contain special a digital signal processing (DSP) block for more complex mathematical operations, such as multiplication

and division. There are also multiplexers (MUXes) for routing the signal and a d-type flip flop (DFF) for saving one bit [11][36].

The basic structure of an FPGA, figure 3.2, includes the following elements [11]:

- Look-up Tables: block which performs logical operations;
- Flip-Flops: register elements which can store the result of the LUTs;
- Wires: interconnection resources;
- IO pads: physical ports that get data in and out of the FPGA.

Although this structure allows the implementation of a wide range of digital systems in order to improve their efficiency, contemporary FPGAs incorporate additional elements, which implement specific functions such as [11]:

- Embedded memories to distribute data storage (Block RAMs);
- Phase-locked loops (PPLs) to drive the FPGA fabric at different clock rates;
- External and/or embedded microprocessors;
- Digital Signal Processors (DSPs).

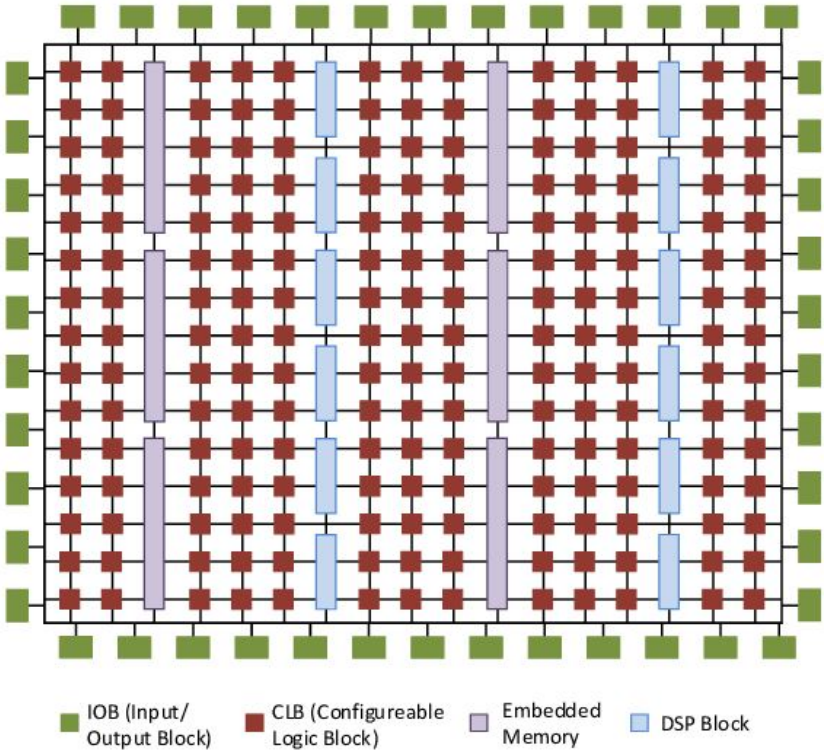


Figure 3.2: Overview of FPGA architecture [11]

3.2 Physical Layer

The open system interconnection (OSI) reference model shown in figure 3.3, was developed by the International Standards Organization (ISO) and defines seven layers in network communication systems. Physical layer in context is the lowest in the hierarchy and is concerned with physical transmission of data over various transmission mediums, such as cabling, fiber optics or wireless. The Application layer is presented to users and the layers in between take care of, e.g., routing data packages over the Internet. The Physical layer includes mechanical, electrical and timing interfaces in its design to make the transferring of bits as accurate as possible. Due to its complexity it can be described by other sub-layers [37].

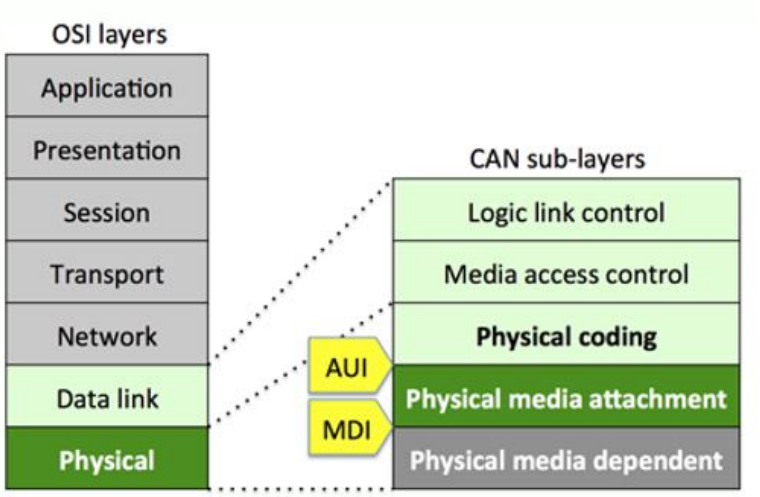


Figure 3.3: The OSI reference model [38]

3.2.1 Physical Coding Sublayer (PCS)

The physical coding sublayer lies below the data link layer (layer two) in the OSI reference model and above the physical medium attachment (PMA) physical sublayer. The PCS performs several functions, such as the encoding/decoding and scrambling/descrambling of data blocks. The encoding of data is performed together with scramblers to ensure enough transitions between logical ones and zeroes so that the receiver can perform clock recovery from a serial link which provides no clock reference. The PCS can insert and remove markers for the alignment of data and can identify blocks of received data streams for encoding schemes, such as 8B/10B [39][37].

3.2.2 Physical Medium Attachment Sublayer(PMA)

The physical medium attachment sublayer connects the PCS to an electrical interface, such as an optical transceiver. Receivers are essentially photo-detectors connected to circuits for amplification and quantization, often sharing any controlling circuit with the transmitter. For high-speed links, the PMA serialized/ deserialized data performs clock recovery from received data streams. The PMA is responsible for taking inputs of parallel data and sending it out at high speed (and vice versa), and the data conversions can be implemented in a Serializer/Deserializer (SerDes) circuit, which is described in the following section. [40][37]

3.3 Serial to Parallel and Parallel to serial conversion: SerDes

The increasing requests for reliable high-speed transmission over long distances has often made serial link preferred over parallel ones. However, since data elaboration is often parallel, data needs to be serialized on the transmitter side and deserialized on the receiver side [41].

A specialized circuit for doing this conversion has been projected and is constantly developing, it is called SerDes. The working principle of a "SerDes" is relatively simple because a parallel data is clocked into the parallel register synchronously to a slow clock and shifted out, one bit at a time, at a higher serial clock rate. These blocks are often called "parallel in serial out" (PISO) and the inverse operation is called "serial in parallel out" (SIPO)[42][41].

Basically, there is a shift register which receives data one bit after the other and transmits its contents to a storage register used to hold the data for the slower, parallel clock. This scheme can only work well if the transmitter and receiver clocks are perfectly synchronized.

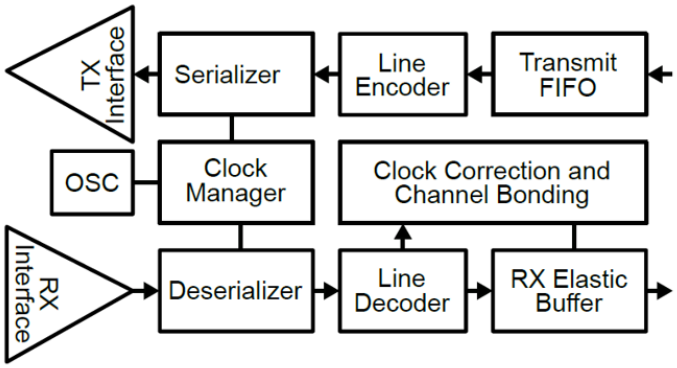


Figure 3.4: SERDES Generic Block Diagram [42]

Description of each block of the Serializer diagram [42]:

- Transmit FIFO (First IN, First Out):
  - Storing the incoming data before transmission.
- Line Encoder:
  - This is an optional block sometimes not included in a SerDes. It encodes the data into a more line-friendly format and usually involves eliminating long sequence of non-changing bits. It may also adjust data for an even balance of ones and zeros.
- Serializer:
  - This is a block that serializes the received data, that is, when it receives a certain number of data in parallel (x data) at a given rate (frequency y), it transforms it into a given stream at a rate of x multiplied by y.
- TX Line Interface:
  - This block turns out to be the final interface of the Serializer with physical cable, and generally it also allows better recovery of the receive-side signal.

Alternatively, the Deserializer must do the whole inverse process that the block Serializer does. The functions of each block are briefly described below [42].

- Rx Line Interface:
  - It is the interface of the Deserializer with the physical cable. It can use some passive or active signal equalization.
- Deserializer:
  - Converts the serial data it receives at a rate of x multiplied by y, in x data parallel to a cadence of y.
- Line Decoder:
  - Decodes data received.
- RX Elastic Buffer:
  - Aligns the incoming data into the proper word boundaries. Several different mechanisms can be used for automatic detection and alignment of a special reserved bit sequence.
- Clock Correction and Channel Bonding:
  - This block allows the correction of differences between clock signals and correction of delays between different channels (if there is a multi-channel transmission).

There is also a block that is common to both the serializer and the deserializer which is the Clock Manager, which is essentially responsible for the various processes that the clock signals need: from frequency multiplication, division and even retrieval [41][42].

This architecture presents the essential blocks for the proper functioning of a serializer and deserializer, however there are other features that can be added: from the different types of possible encodings to detector codes and error correctors that can be added to the architecture. [42]

3.4 High-speed serial data of FPGA KC705

Xilinx Series 7 FPGAs have transceivers capable of high-speed serial communication as required in this project.

Specifically, according to [40], GTX transceivers are available in the Xilinx (KC705 Kintex-7) FPGA which allow a speed of 12.5 Gbit/s. In other models there are other transceivers, such as GTZ (allowing up to 28 Gbit/s), GTH (which allows rates up to 13.1 Gbit/s) and GTP (with debits up to 6.6 Gbit/s). However only the GTX transceivers will be addressed, since they are the most suitable ones for this type of communication and the only ones available in the FPGA used.

In figure 3.5 shows the FPGA to be used in the project and the entries/exits of the GTX SMA Transceiver which will be used for concept's proof.

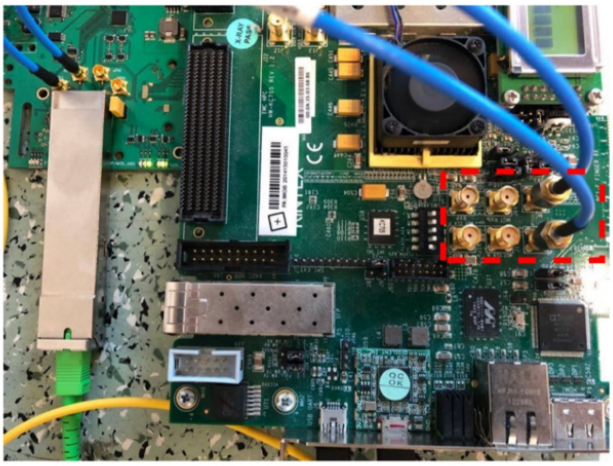


Figure 3.5: GTX SMA Transceiver of Xilinx (KC705 Kintex-7) FPGA [41]

3.5 Architecture of transceivers

The GTX transceiver is essentially a high-speed SerDes developed by Xilinx for Kintex-7 family FPGAs. It is a highly power-efficient configurable module that can produce line rate up to 10 Gbit/s. The GTX transceivers are grouped into four channels described as Quad and these are strategically close in order to minimize the layout size and power consumption [41].

Each GTX transceiver is composed by transmission block (TX) and receiving block (RX) and the figure 3.6 shown the general architecture of FPGA transceivers.

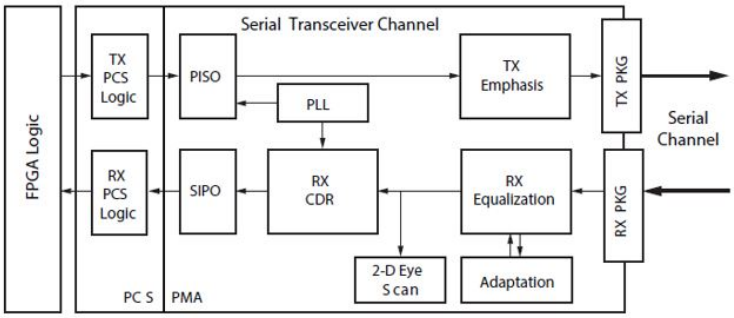


Figure 3.6: General Architecture of Transceivers [40]

Its architecture is briefly described, according to the [40] and [41]:

As you can see from the figure, there are two sublayers (PMA and PCS) which have already been mentioned above.

Each sublayer provides different blocks. The PMA sublayer includes: Serial/Parallel (PISO and SIPO), Phase-locked loop (PLL), Clock Data Recovery (CDR) and Pre/Post-emphasis and provides equalization programming to optimize the received signal integrity.

On the other hand, PCS sublayer includes: 2-byte and 4-byte internal data path to support different line rate requirement, pseudorandom binary sequence (PRBS) generator/checker,

8b/10b encoding/decoding protocol, comma detect and alignment and equalization blocks, among others. Following these sublayers there is FPGA logic interface.

3.5.1 Transmitter

In figure 3.7 the architecture of the GTX transmitter is shown. It has blocks with different functions that allow to maintain the integrity of the signal during a transmission. The data flows from the right side to left side.

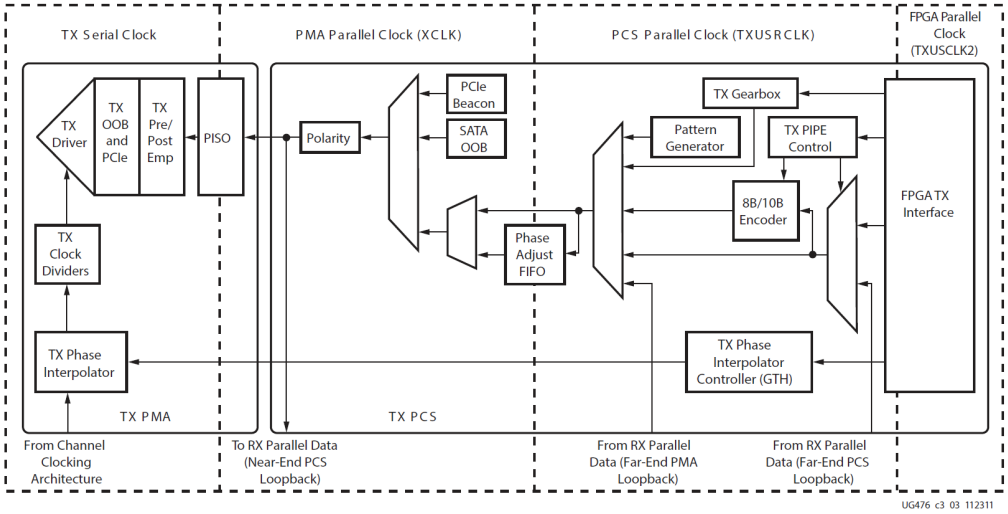


Figure 3.7: GTX/GTH Transceiver TX Block Diagram [41]

The block on the right, TX PCS, is the FPGA TX interface, where the parallel data input of the FPGA will be serialized. The users can define their own TX data pattern in this block, such as utilization of memory or coded-pattern generators as well as the width of TX data (2-byte, 4-byte), according to [41].

Parallel data enters this block at a given well-defined cadence: to the positive edge of the TXUSRCLK2 clock signal, this being the synchronization signal between the data coming from FPGA and the transmitter. However, another clock signal is also required for the PCS internal logic of the transmitter: TXUSRCLK. [41]

The TX data and control signals in this block are running under TXUSRCLK domain (typically below 500MHz). Bear in mind that the PCS internal logic works with the data in parallel, so the value of this clock signal depends, not only on the cadence at which the data enters the transmitter, but also on the chosen datapath.

The PCS block uses two clock signals internally for its correct operation: TXUSRCLK (as already mentioned) and XCLK (parallel data clock signal of the PMA block). Figure 3.7 illustrates the different clock domains present in the GTX transmitter.

When the data is transferred between the TXUSRCLK and the XCLK domains, it is necessary that in addition to having similar frequencies, any phase differences that may exist are resolved. This will be focused on with more detail in subsection 3.5.3.

Lastly the TX PMA block is basically composed by a high-performance serializer and a configurable driver. The PISO block, parallel in and serial out, uses the high-speed serial clock (typical several GHz) to sample coming parallel TX data for serialization [41].

3.5.2 Receiver

In figure 3.8 it is possible to see the architecture of the receiver GTX, that includes several blocks which allow the correct recovery signal, being the operating of certain blocks already mentioned in the subsection 3.3.

The RX actually performs the opposite of the TX side. As the figure 3.8 shows, the data flows from left to right in RX block. Similar to TX block, each RX contains RX PMA and RX PCS blocks. The RX PMA is composed by a high-performance receiver, programmable equalizer, CDR and SIPO block.

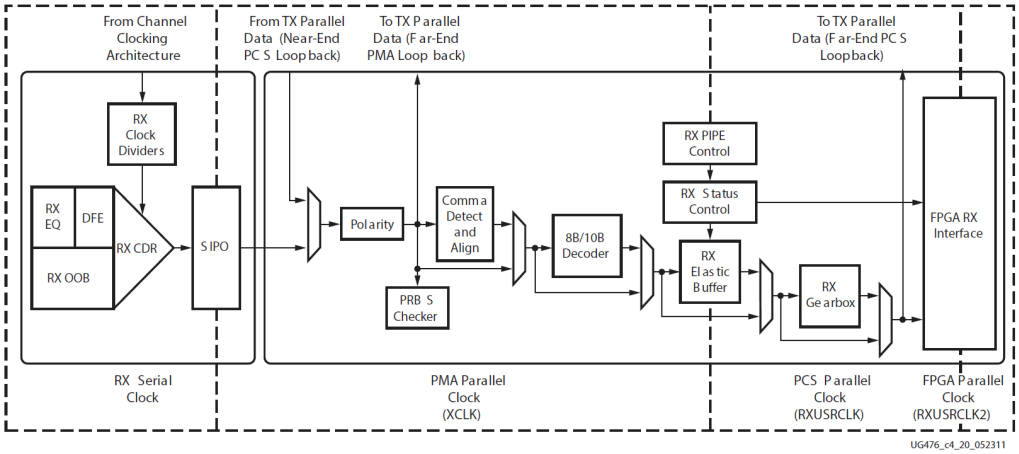


Figure 3.8: GTX/GTH Transceiver RX Block Diagram [41]

The two programmable RX equalizers including decision feedback equalizer (DFE) and low-power mode (LPM) help the CDR circuit to recover received high-speed data stream. These equalizers are selected depending on the system level trade-offs between power and performance.

For a lower-loss channel, LPM mode is chosen for power efficiency. On the other hand, for equalizing high-loss channels, the DFE mode is selected to offer better data recovering quality. The parallel data then flows into the RX PCS block. This RX data usually shares the same bit width with TX data which can be configured by FPGA TX/RX interface block [41].

Also, the comma detect is presented to align the input signal accordingly. These processes are under parallel clock RXUSRCLK domain which is the duplication of TXUSRCLK. The RX PCS block also has built-in loopback paths to receive parallel TX data from TX PCS and the ability of transmitting received data to TX PCS. After passing these blocks, the processed parallel RX data is then provided to the FPGA RX interface [41].

3.5.3 Interface between the different clock signal domains of the transmitter

The PCS block uses two clock signals internally for its correct operation: TX/RXUSRCLK (as already mentioned) and XCLK (parallel data clock signal of the PMA block).

All this functionality also occurs on the receiver side since it operates in different clock signal domains. Figure 3.7 illustrates the different clock domains present on the GTX receiver.

When data is transmitted from one domain to another, all phase differences between the clock signals must be resolved and the frequency should not change much. For this reason, one of the following two blocks must be used: the elastic buffer or the phase alignment block.

Both blocks solve the phase differences between the two domains, however they present their advantages and disadvantages.

On the one hand, according to [41], the buffer is a robust structure and easy to operate, whereas the phase alignment block requires more logic and restrictions regarding the clock sources. But the use of the buffer implies a higher latency since the phase alignment block is designed to decrease the total latency of the system.

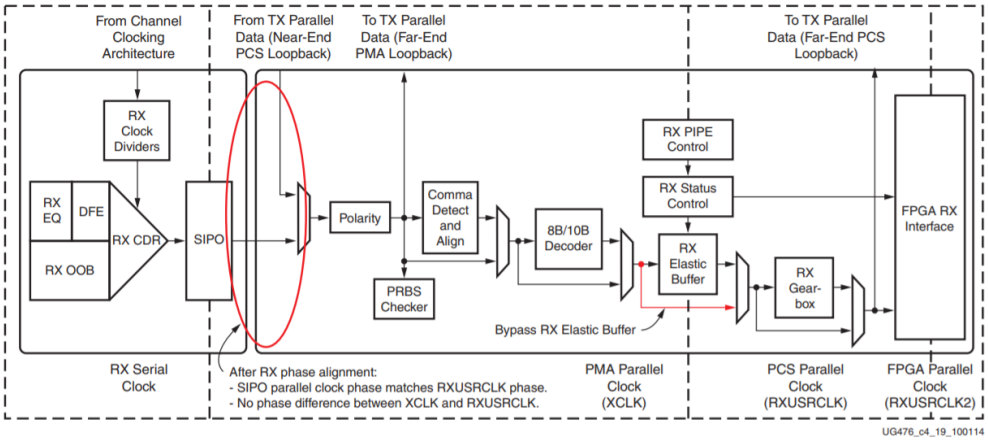


Figure 3.9: Using RX Phase Alignment [41]

3.5.4 Interfaces with the Physical Layer

The interfaces with the physical layers on both sides of the transmission (receiver and transmitter) include analog circuits that allow transmitting and receiving differential signals. However, the signal communicated along the channel may be subject to interference for several reasons which are critical in receiving the signal [43].

Therefore, techniques implemented in these same interfaces are used which, on one side, are responsible for "preparing" the signals to be transmitted to a noisy channel, in order to prevent their change, and, on the other side are responsible for correcting the data received according to certain characteristics.

These techniques are referred to as Pre-Emphasis on the transmitter side and Equalization on the receiver side [42].

During transmission on the physical channel it is normal to have the phenomenon of Inter-symbol interference (ISI), figure 3.10 that occurs due to the fact that there are long periods of transmission of a certain value followed by a short period of time with an opposite value.

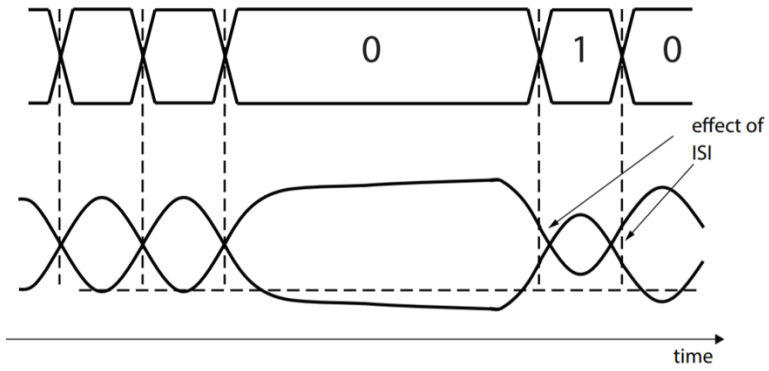


Figure 3.10: Intersymbol Interference during a Transmission [42]

It is important to control this type of interference and because of this the physical channel uses the pre-emphasis/de-emphasis technique. According to [42] it is one of the most important characteristics of the interface with the physical layer, consisting of an intentional overdriving at the beginning of a transition and an underdriving on the consecutive bits that present the same value.

This way, when the phenomenon of intersymbol interference occurs, the capacity of the channel to recover the full amplitude of a small transition will not become a problem.

3.5.5 Interface with the FPGA

Just like in the transmitter there are two clock signals required for the correct operation of the receiver: RXUSRCLK e RXUSRCLK2. The clock signal RXUSRCLK is the internal signal for the logic of the PCS block (which handles the data in parallel) and the second which has already been mentioned as the synchronism clock signal between the receiver and the FPGA logic. It is important to remember that the PCS internal logic works with data in parallel, so the value of this clock signal depends, not only on the cadence at which the data enters the transmitter, but also on the chosen datapath.

TX_INT_DATAWIDTH	Internal Data Width	FPGA Interface Width	TXUSRCLK2 Frequency
0 (2 bytes)	16	16	FTXUSRCLK2 = FTXUSRCLK
0 (2 bytes)	16	32	FTXUSRCLK2 = FTXUSRCLK/2
0 (2 bytes)	20	20	FTXUSRCLK2 = FTXUSRCLK
0 (2 bytes)	20	40	FTXUSRCLK2 = FTXUSRCLK/2
1 (4 bytes)	32	32	FTXUSRCLK2 = FTXUSRCLK
1 (4 bytes)	32	64	FTXUSRCLK2 = FTXUSRCLK/2
1 (4 bytes)	40	40	FTXUSRCLK2 = FTXUSRCLK
1 (4 bytes)	40	80	FTXUSRCLK2 = FTXUSRCLK/2

Table 3.1: FPGA TX Interface Datapath Configuration (adapted [41])

According to 3.1 we can verify the relationship between the two clock signals, as well as, from the port size of the transmitter interface and the size of the datapath to acquire the serial data rate through the equation 3.1. If a line rate greater than 6.6 Gbit/s, it requires a

4-byte internal datapath by setting TX_INT_DATAWIDTH to 1 [41].

$$TXUSRCLKRate = \frac{LineRate}{InternalDatapathWidth} \tag{3.1}$$

In order to understand the difference between these frequencies, a concrete case is shown, which is used in the project.

To achieve an output rate of 10 Gbit/s, a set of 32 bits in parallel was put in the entrance of the transmitter, which makes this data be sampled at a frequency of 312.5 MHz, discarding the 2-byte hypothesis, presented in table 3.1.

This case is valid, according to table 3.1, if it presents the same internal width of the datapath in relation to the port size of the interface since the relation between clock signals is identical, upper branch (figure 3.11).

As an alternative, lower branch (figure 3.11), the relation between clock signals presents twice the previous sampling rate, causing a reduction to half of the internal width of the datapath, which implies adding another datapath to make the 80 bits in parallel to achieve the desired input of the transmitter.

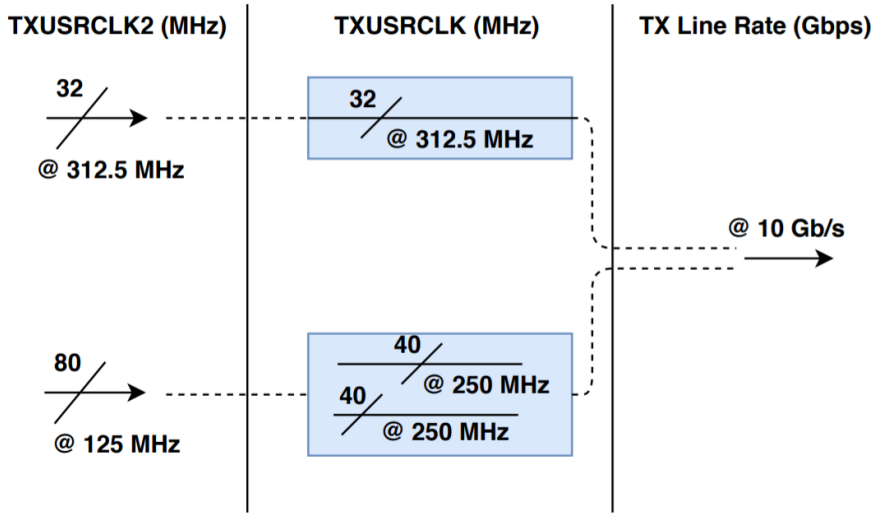


Figure 3.11: Frequency and Datapath Relationship

3.6 GTX Transceiver Structure

This section presents the general intellectual property (IP) structure provided by Xilinx generated in the VIVADO software and, as a way to generate this module, there is an interface that allows to configure various features of both the transmitter and the GTX receiver.

The module shown in figure 3.12 consists of several sub-blocks, as indicated [41]. However, these sub-blocks are internal managements of the transceiver and are not relevant. Only the most important input/output are presented for the development of the project.

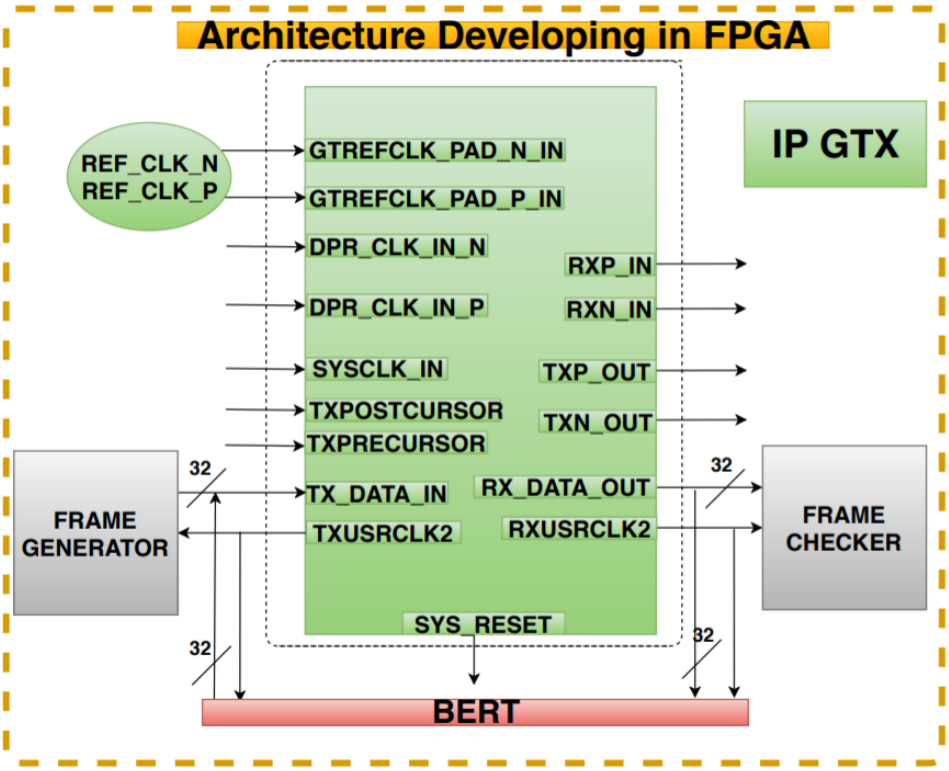


Figure 3.12: GTX structure provided by Xilinx generated in the VIVADO

According to [41], figure 3.12 presents:

- GTREFCLK:
  - Input of the external differential reference clock signal (REF_CLK_P corresponds to the positive signal and REF_CLK_N to the negative signal).
- DRP_CLK:
  - Input of the external differential clock signal to the DRP (Dynamic Reconfiguration Port) interface.
- SYSCLK_IN:
  - Clock signal input from all other architecture blocks other than GTX.
- RX_IN / TX_OUT:
  - Differential input and output pair of the serial data of the receiver and transmitter, respectively.
- TX_DATA_IN / RX_DATA_OUT:
  - Input of the parallel data to be serialized, as well as the output of the data in parallel after received and serialized.

- TX/RXUSRCLK2:
  - Data sampling clock signal for both the transmitter and data from the receiver.
- SYS_RESET:
  - Reset signal activated by the receiver and transmitter states.
- TXPOST/TXPRECURSOR:
  - Pre-cursor and post-cursor transmit pre-emphasis.

In the internal management of the transceiver it is possible to conclude that the input TX DATA_IN and the output RX DATA_OUT are connected to two blocks:

✓ Generator block of frames to send to the transmitter;

✓ Block that verifies the frames arriving at the receiver;

Both operate on the TXUSRCLK2 and RXUSRCLK2 clock signals that are required for the correct operation of the entire system.

For the development of this project these inputs and outputs, as well as the clock signals, will be useful for the development of the BERT system which in the following chapter will be approached step by step in detail.

Chapter 4

Implementation and Results of BERT in Continuous Mode

In this chapter an architecture is presented, that intends to characterize the NG-PON2 system available in the laboratory, in order to verify its performance during communication and to provide reliability to the final user, this is, if the communication can be performed or if it is difficult or even impossible.

In order to implement this architecture, a set of steps were developed following the sequence shown in figure 4.1. Starting off with the creation of the interface between the computer and the FPGA, Interface BERT system, followed by the creation of the GTX module provided by the VIVADO software and lastly the improvement XFP Interface, already created by PICadvanced.

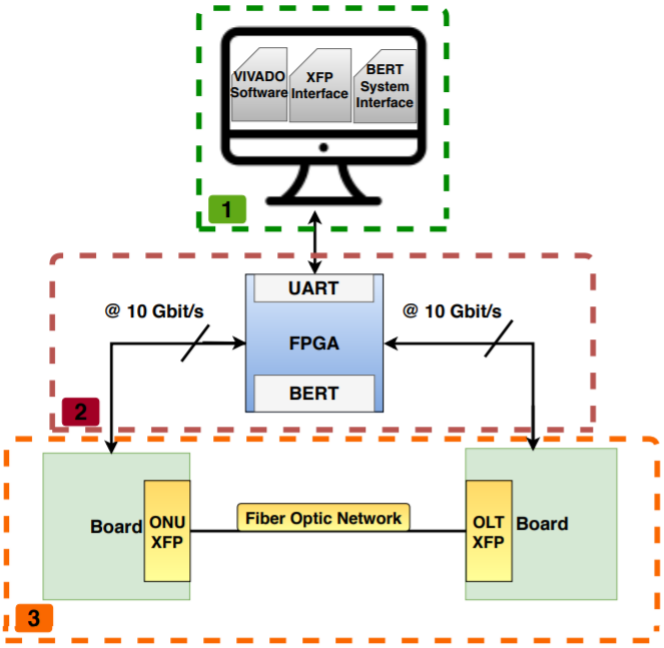


Figure 4.1: Description of the different stages of development performed during the project

In an initial step of the project, an interface between the computer and the FPGA was developed through a serious communication, UART, with the purpose of the user to have greater control over the system.

In a second step, a continuous BERT was developed in which the data transmission in series was realized through the module GTX made available by Xilinx, as already approached in the chapter above, being it quite complex.

Finally, the validation of concept's proof of the global system in which the operational points of the technology were verified with the correspondence of its standards.

4.1 Continuous Mode Communication Interface

In order for the user to have greater control of the system, a communication interface has been developed to transfer the state of the system. The final user can obtain the current bit error rate and the accumulated bit error rate, as well as according to the user's needs be able to change certain parameters which allows optimized communication through pre/post-emphasis.

The Kintex KC705 board has a connector (CP2103GM) which is used to connect the FPGA to a computer [44]. Additional logic is needed for serializing the data, i.e., a UART and a program which presents the data on the computer.

According to [45], Universal asynchronous receiver and transmitter (UART) is a circuit that sends parallel data through a serial line.

In the first step, the general block UART was developed on the FPGA side, figure 4.3, composed of several essential blocks, such as the transmitter and receiver block, and because the communication is asynchronous, that is, without any clock signal, the transmitter/receiver bits have to work at a given cadence in which it is agreed between the receiver and transmitter, which is why there is the baud rate block [45].

The developed UART protocol only sends and receives 8 bits of data. Due to the need of sending more than 8 bits, as well as to safeguard the received data it was fundamental to add two new blocks for this referred effect. This effect was achieved through a finite state machine (FSM).

In general, the transmitter is essentially a special shift register that loads data in parallel and then shifts it out bit by bit at a specific rate. The receiver, on the other hand, shifts in bit by bit and then reassembles the data [46].

In order to avoid any anomaly during communication, there was a need to ensure a correct data flow sequence, figure 4.2, and for this, four crucial states for the ideal operation were developed: idle state, start state, data and stop state [46].

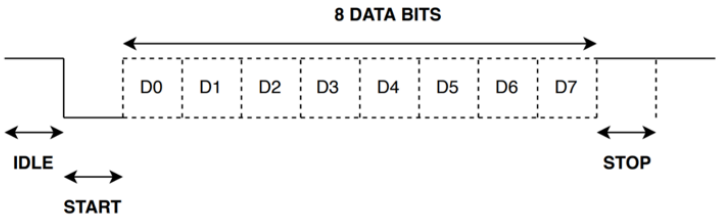


Figure 4.2: Transmission of a byte

Therefore, in the absence of data, idle state, the serial line represents a logical level '1'. When the transmission starts, start state, a transition to a logical level '0' occurs followed by the data state that corresponds to the 8 bits sent until the stop state is reached.

When this last state is reached, a signal is sent, indicating that the transmission/reception has been successful, TX_DONE/RX_DONE respectively. This way, RX FSM allows the storage of the information coming from the PC as well as transmission in an orderly way the stored data coming from TX FSM.

Finally, on the computer side an application that shared the same UART communication protocol was developed, which not only receives/sends data in real time, but also allows to perform all data processing in order not to overload the hardware. This application was developed through the platform Windows Forms Application (Framework 4.6.1), using the programming language C# (C sharp).

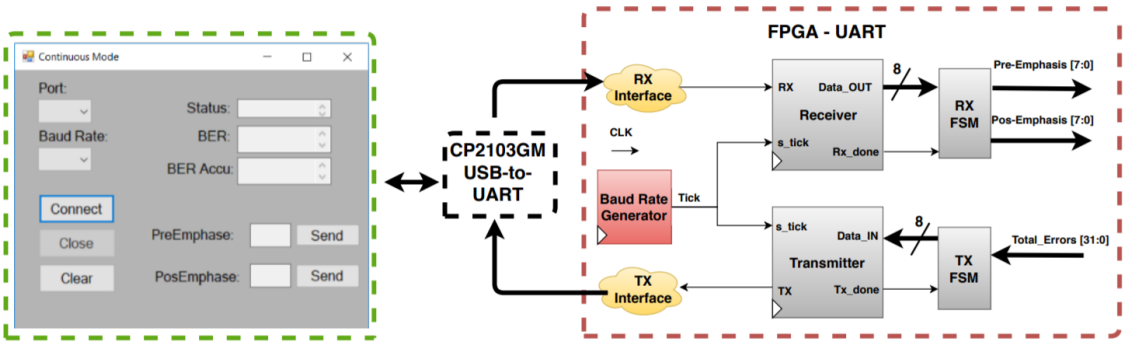


Figure 4.3: Diagram of UART blocks developed in FPGA and interface developed in PC both for continuous mode

4.2 Bit Error Rate Tester (BERT)

4.2.1 Bit Error Rate

As stated in a previous subsection 2.2.4, BER is one of the most important parameters describing the performance of transmission in the digital link.

Because of the random nature of the phenomena involved, BER is also regarded as the probability of errors occurring during data transmission. The standard maximum bit error rates are specified as 1×10^{-9} or 1×10^{-12} for modern fibre optic systems.[47].

Nowadays 10 Gbit/s transmission rate is increasingly common in fiber optic links and individual implementation of BER measurement systems require expensive commercial equipment. Therefore, one of the main purposes of this work is to develop a BER tester for transmission rate at 10 Gbit/s and with the integration of high-speed transceivers inside a FPGA.

This provides a cheaper alternative to commercial equipment and offers the flexibility and data analysis showing if communication can be realized or if it is difficult or even impossible.

4.2.2 Idea of Operation of the BER Tester

Each BERT consists of two main blocks: the transmitter which includes a test sequence generator and a receiver which includes a detector and error analyser. This test sequence generator is intended to produce the stream of the data bits according to some rules that must be known for the receiver as well [48].

Often the PRBS generators are used for this purpose. There are a number of standard polynomials defining different PRBS, developed by standardization bodies for testing telecommunication equipment. Alternately, some bit sequence defined by the user and stored in the tester memory may be periodically generated [47]. PRBS may be generated by means of linear shift registers with appropriate feedback. If the shift register has n stages, the maximum pattern length will be $2^{(n)} - 1$ bits [48]. The receiver contains an error detector that compares the received bits with the original pattern and, in case of mismatch the error counter increases.

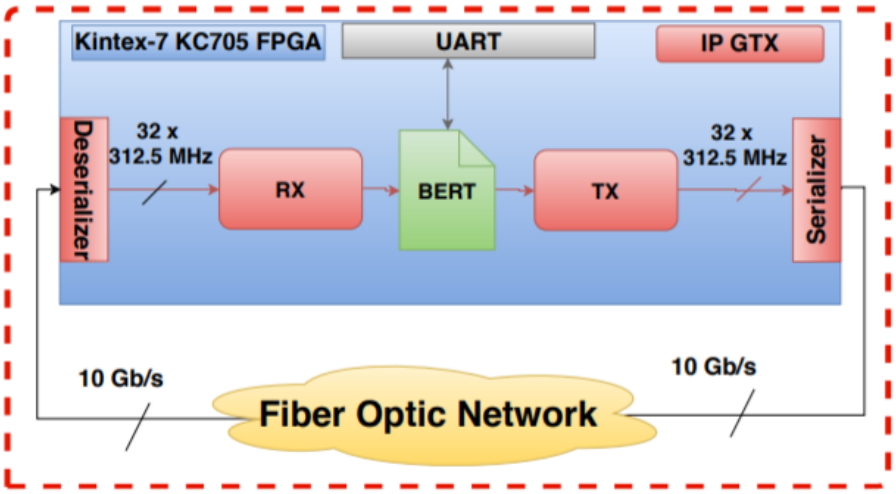


Figure 4.4: Block diagram of 10 Gbit/s BER tester

The described solution is achieved through the Multi-Gigabit Transceivers (MGTs) provided by the Xilinx (KC705 Kintex-7) FPGA [44].

As already discussed in the previous chapter, the MGTs is a SerDes, capable of operating at serial bit rates above 1 Gigabit/second. Currently, MGTs are used increasingly for data communications because they can run over longer distances, use fewer wires, and thus have lower costs than parallel interfaces with equivalent data throughput [49].

These MGTs allow the transmission of data in parallel, at a substantially reduced speed (312.5 MHz) and convert them into a stream of serial bits [47]. Figure 4.4, shows the process.

4.2.3 BER Tester

4.2.3.1 Block Diagram of system

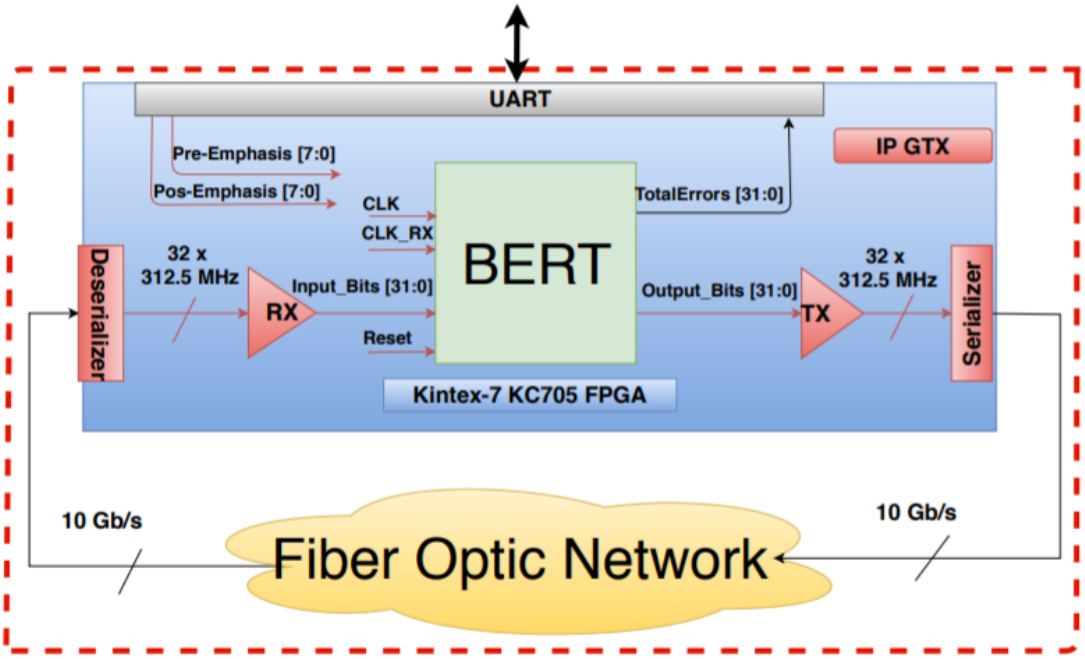


Figure 4.5: The basic block diagram of a BERT design

The block diagram of figure 4.5 is in agreement with the block diagram of figure 4.4 of the previous section, that is, it demonstrates all the essential blocks of the system, which clearly shows which are the inputs and outputs of the BERT system, as well as the number of underlying bits.

Through figure 4.5 the BERT system is composed of an input and output data of the GTX module provided by the software VIVADO and the respective clocks, as already mentioned in the previous chapter, as well as an output corresponding to the BERT system feedback. Some of these inputs and outputs are presented:

- RX DATA:
  - Receives the PRBS via the optic fiber link (Data of fiber optic network), with data rate of 10 Gbit/s.
- TX DATA:
  - Transmits the test pattern sequence via the optic fiber cable (Data transmitted to the fiber optic network).
- Total Errors:
  - Number of errors that can ensue during communication, i.e., errors between transmitted data and received data.

- CLK/CLK_RX:
  - Signal coming from TXUSRCLK2 and RXUSRCLK2, respectively.
- Reset:
  - Signal coming from SYSRESET.

The total number of errors is sent through a serial communication interface, UART, which shares the number of errors of the system in real time and through the two input parameters (Pre/Pos-Emphasis) the communication channel can be adjusted as a way to obtain a better system feedback.

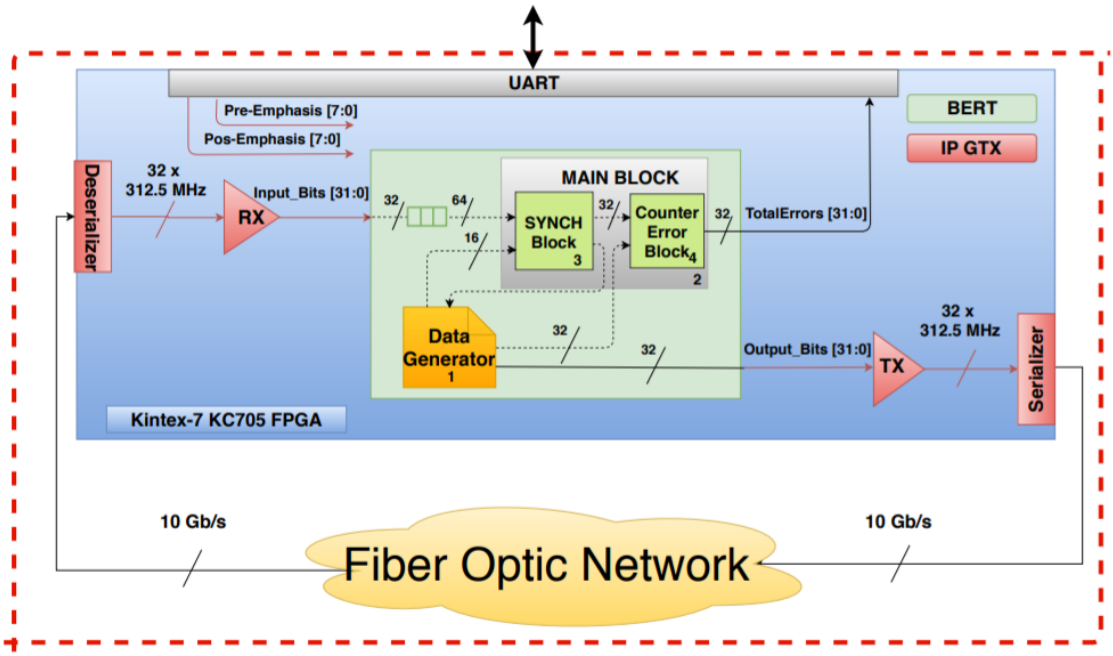


Figure 4.6: Diagram of logic function modules implemented in the FPGA

As a way of illustrating the contents of the inputs and outputs of the BERT system block, a new block diagram was developed, which demonstrates a lower layer that clarifies the sub-blocks regarding the system, as shown in figure 4.6.

There are two blocks within the BERT, such as:

- Data Generator:
  - PRBS with a rate of 10 Gbit/s.
- Main Block:
  - Which handles the data in a critical way so that it is possible to verify the viability of the transmission system in question.

The last sub-block (Main Block) has two underlying blocks:

- Synchronism Block:
  - Most important block of the BERT system (this will be discussed with more detail in the following subsection 4.2.3.4). Without this block it would not be possible to start counting errors.
- Counter Error Block:
  - Analyses the number of errors occurred throughout the system.

4.2.3.2 Explanation of the Blocks

To exemplify how the development of the BERT system was approached a global layer is divided into several sub-layers.

Until now it has been possible to demonstrate all different layers, such as an upper layer, two layers at an intermediate level, as well as the last layer that has not yet been addressed but will be explained in detail in the following subsections.

- The upper layer (figure 4.4):
  - Composed by 5 essential blocks: the receiver, the transmitter, the SerDes, as well as the block containing the BER system.

As a way to substantially reduce the clock speed, data from the BERT system will be introduced into the high-speed transceivers that enable serialization as well as deserialization of the data.

It is desired to have 32-bit in parallel at the output of the transmitter with a total aggregate rate of 10 Gbit/s. For this to be valid it is necessary to reduce the clock speed rate to a frequency of 312.5 MHz (frequency represented by FTXUSRCLK2 of figure 3.12).

- The first intermediate layer (figure 4.5):
  - Composed by the main inputs and outputs of the BERT system and the adjacent bits.
- The second intermediate layer (figure 4.6):
  - Shows, in general, which are the main blocks behind the inputs and outputs of the first intermediate layer.
- Finally, the last layer (figure 4.7):
  - Shows a more detailed content of the main blocks delineated by the second intermediate layer, that is, the **Data Generator block**, the **Synchronization block** as well as the **Counter block**.

The operation of the several blocks will be presented individually in the subsections below.

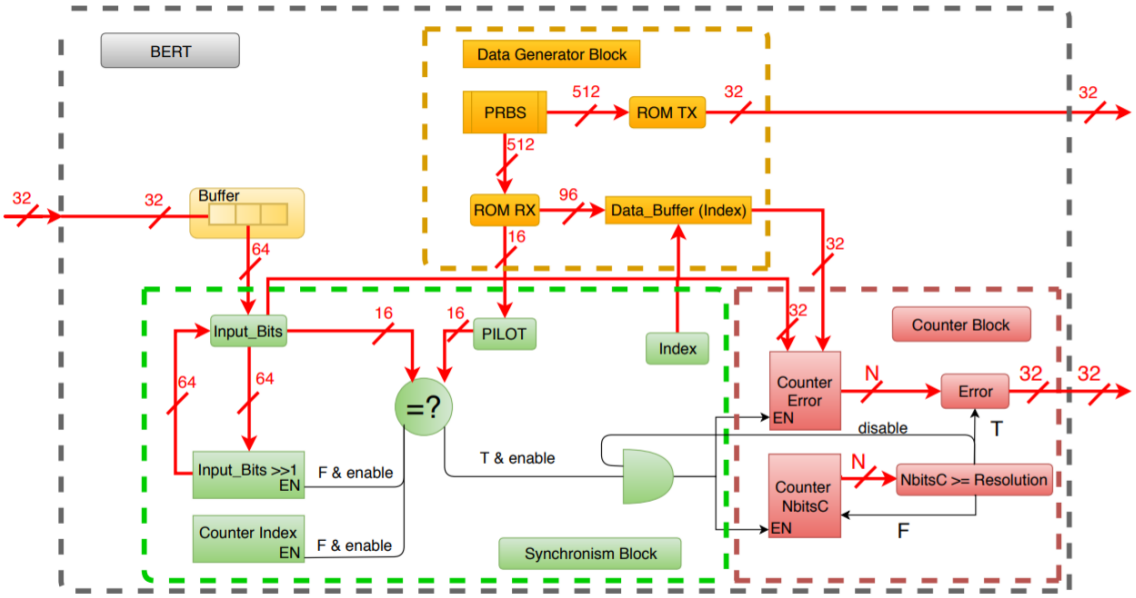


Figure 4.7: Simplified block diagram of BERT in Continuous Mode

4.2.3.3 Data Generator Block

In BER measurement, a pseudorandom data sequence is used, as we can not create a truly random signal using deterministic methods. To simulate the actual measuring BER by the BERT system was designed a PRBS with a maximum pattern length ($2^{14} - 1$ bits) by means of a linear-feedback shift register (LFSR) to simulate the transmitted signal. Over an endless period of time, we can assume that the data transmission is a random process [33].

The transmitter of BERT is responsible for generating a predictable data pattern (ROM TX) to simulate the signal transmitted in the real communication channels, then sending the pattern to the optic fiber network.

On the receiver side it is needed to generate the data pattern (ROM RX which we call the default reference), which must be identical to the pattern generated on the transmitter. The receiver uses the default reference to compare with the received data and performs BER statistics, depending on the result of the comparison.

A data buffer composed of 96 input bits from ROM RX and 32 bits of output was generated, which will be the input of the counter block. These 32 bits will be delineated by the input argument (Index) from the synchronism block.

4.2.3.4 Synchronism Block

The transmission channel is not ideal and due to it, the data stream along the optical fiber during communications present impairments such as attenuations, dispersions, as well as noise and delays that promote the incompatibility of the received data. In other words, not all the data received corresponds to the transmitted data, which may condition the viability of the system. However, in order to obtain a viable response, the data must be compared at the correct time.

This way, the synchronization block has the function of synchronizing the data coming from the fiber optic network, in order to calculate the errors correctly and then to show the performance of the communication link.

As mentioned in the previous subsection, two identical ROMs (TX and RX) were generated in which they contain a known delimiter (PILOT), in this case, a 16 bit sequence. It allows identifying the initial time of the data for the counting block to be able to start.

Figure 4.7 shows that the synchronization block has as input 64 bits of data from the data storage buffer that is constantly receiving data of 32 bits in parallel, coming from the receiver, figure 4.8.

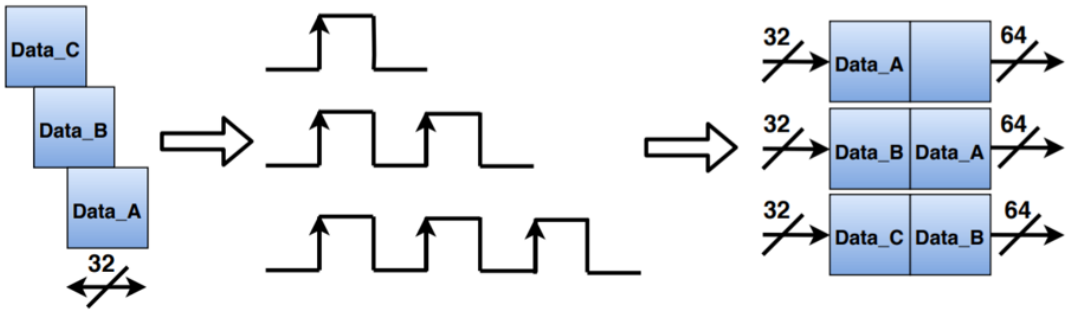


Figure 4.8: Constantly reception of 32 bit data in parallel from the receiver

Due to the factors mentioned above, the data during the communications may change and therefore the initially designated delimiter may not appear at first instant, i.e. in the first 16 bits, which implies a delay of the data. The existence of this delay implies a constant search of the delimiter along the data storage buffer.

During the search, there is an index that will constantly increment, indicating the offset of the data. So the data filtering decision in Data Buffer will match the offset that occurred as shown throughout the following examples, figure 4.9, 4.10, 4.11.

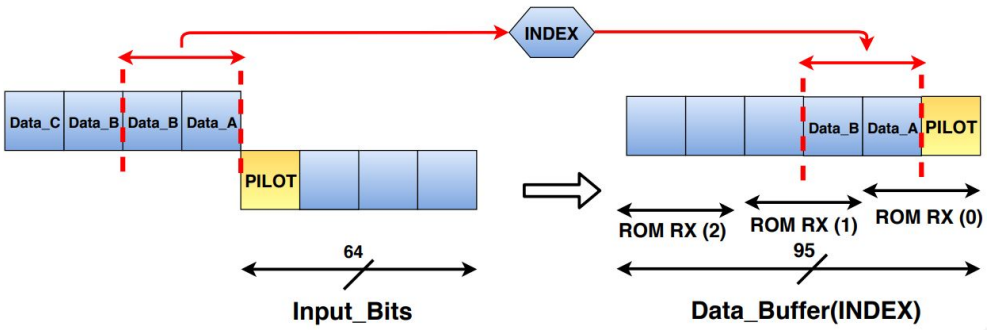


Figure 4.9: Synchronization Block (INDEX = 16)

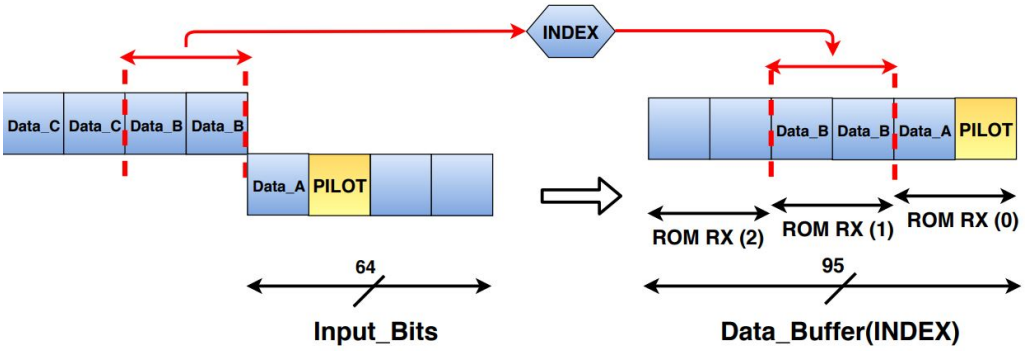


Figure 4.10: Synchronization Block (INDEX = 32)

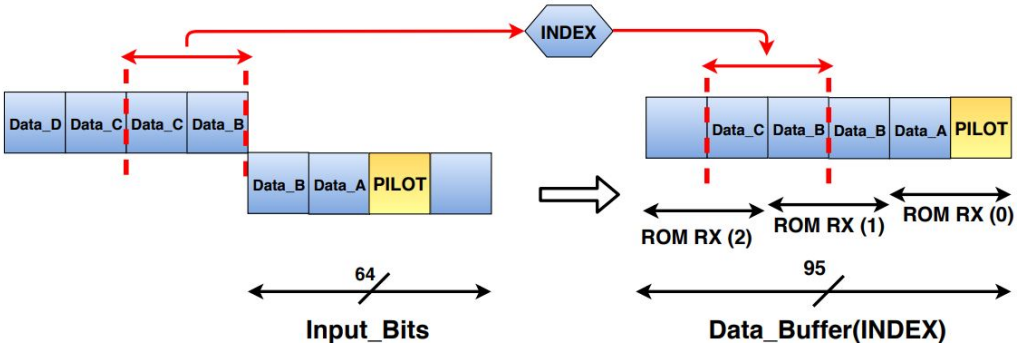


Figure 4.11: Synchronization Block (INDEX = 48)

4.2.3.5 Counter Block

Having defined the synchronization between the transmitted and received data, the counter block is achieved.

This way, this block will compare the received data, Input_Bits, with the transmitted data that corresponds to the default reference data coming of Data_Buffer filtering, figure 4.11

Due to the fact that the transmission rates are continuous, there is a need to understand how the data is circulating and thus behind the error counter, there is another counter that will match the resolution. When the resolution is reached, the user receives the total number of errors, since a control signal is activated in order to stop the count, as well as reset all the counters for a new cycle to start.

4.3 Experimental Results

This subsection intends to explore the last layer of the diagram initially presented in figure 4.1 as a way of characterizing the NG-PON2 technology available in the PICadvanced laboratory.

The developed BERT system was properly synthesized and implemented in the FPGA with the purpose of validating the concept's proof described in the previous subsections by verifying the operational points of the technology using the optical network topology present in the block diagram, figure 4.12, followed by a validation setup 4.13.

This topology consists of:

- Xilinx Kintex-7 FPGA KC705;
- ONU XFP and OLT XFP;
- Optical Power Meter;
- Variable Optical Attenuator;
- 4 SMA Cables;
- Fiber length of 10km and 20km;

Firstly, the differential TX and RX pairs coming SMA connectors from the FPGA, figure 3.5, were connected to the boards that will later support the OLT and ONU XFPs.

These boards, created by PICadvanced, have an interface which allows the user to read the values of several registers on the transceiver and change their values.

The interface XFP enables the verification of the driving currents as bias current, as well as modulation, Burst mode compensation and TEC compensation, among others. During this experimental state, this interface will allow activating the corresponding laser of the XFP, as well as of the channel desired to transmit.

Next step, a VOA was added between the ONU and OLT XFP in order to vary the optical power received in the OLT, controlled by means of a power meter, in order to validate the BERT system developed.

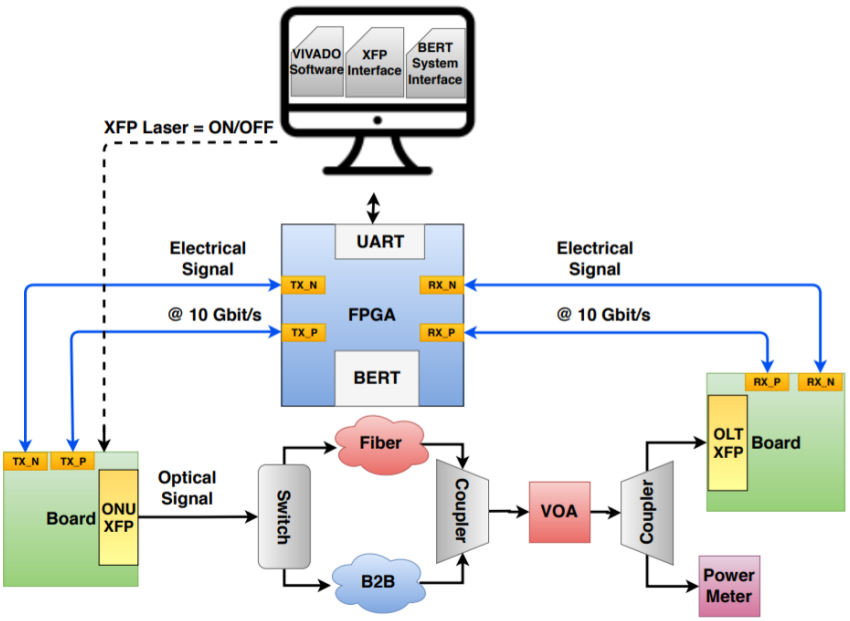


Figure 4.12: Block diagram for the BERT system over the NG-PON2 technology

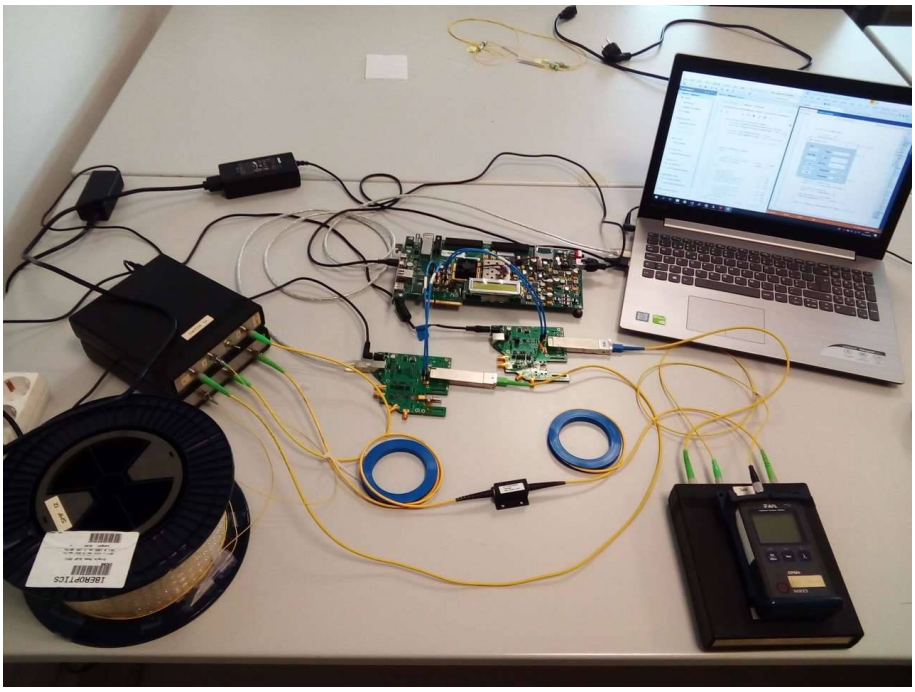


Figure 4.13: Validation setup of the BERT system over the NG-PON2 technology

The following subsections, through the presented topology, intend to explore the BERT system developed with evaluation of their performance during upstream transmission in back to back (B2B) condition, as well as the introduction of fiber in the optical network.

It intends to make a comparative study of a BERT reference system, available in PICadvanced, and what are the effects of the Pre/Post-emphasis parameters introduced by the user on the performance of the BERT system.

Finally, an analysis of the transmission signal present in the optical network is performed, in order to realize the difficulties that are inherent in the receiver side.

4.3.1 Performance evaluation of upstream transmission

In this context, the first scenario studied was the condition of B2B in order to characterize the sensitivity of the system developed. As discussed in Chapter 2.1, NG-PON2 technology operates at four different wavelengths, both upstream and downstream, which forces the transceiver to be tuned to the wavelengths of each channel.

In order for this tuning to be achieved, the transceiver must be able to change the laser parameters, allowing the wavelength of the spectrum to change to another channel, thereby altering the laser bias currents.

Figure 4.14 shows the evaluation of the BER as a function of the optical power received at the receiver of the OLT for the different channels of the NG-PON2 technology. It is possible to conclude that the developed BERT system complies with the values established by the NG-PON2 technology standard, that is, for BER $= 1 \times 10^{-3}$ the required received optical power is lower than -28 dBm for downstream, as discussed in 2.2.4.

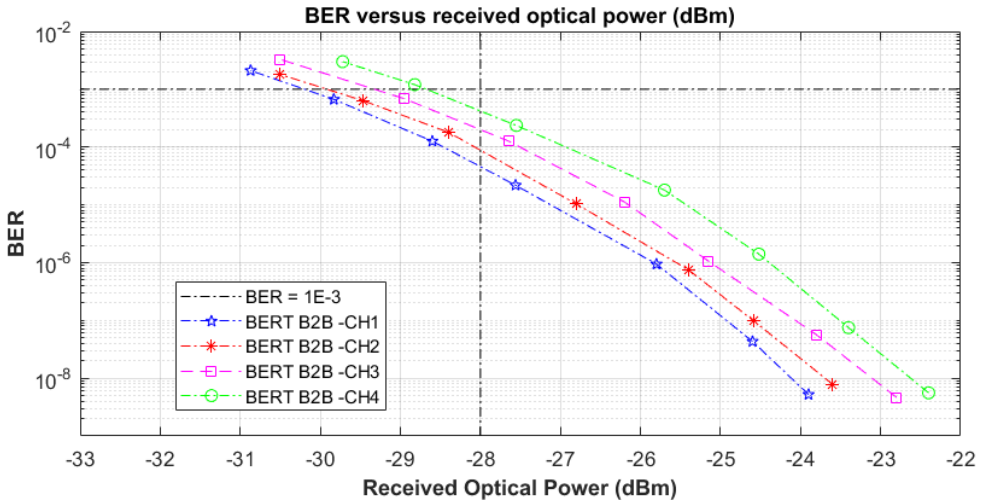


Figure 4.14: BER as a function of received optical power for the different channels B2B

4.3.2 Impact of System Sensitivity when using fiber

The following scenario demonstrates the behaviour of the characteristic curves when using fiber. This way, the BER values were estimated by varying the fiber length from the B2B condition until 20km. These results are illustrated in figure 4.15.

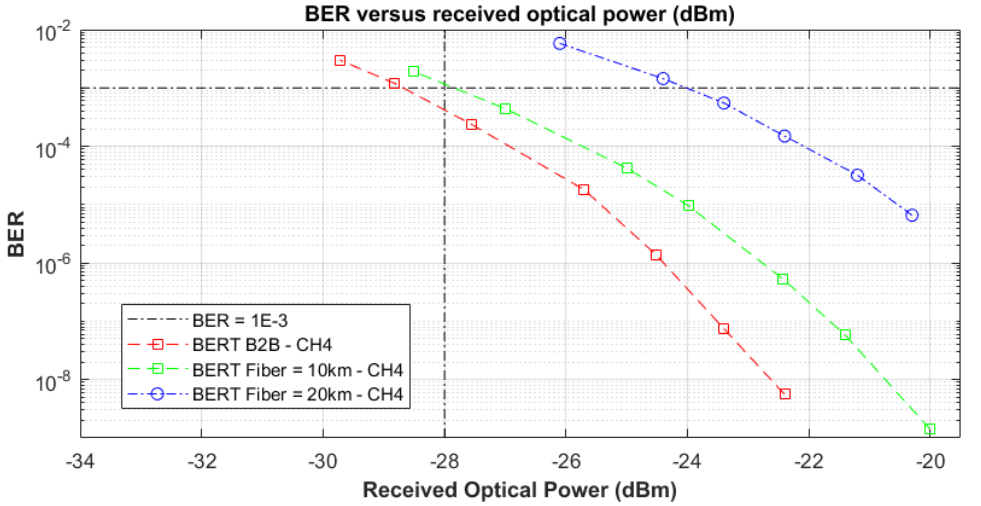


Figure 4.15: BER as a function of received optical power for the different fiber length

According to [16], the NG-PON2 technology standard restricts the optical power penalty range from 0 to 2 dB. Figure 4.15 showed a penalty difference on average 0.40 dB, being within the measurement error of the power meter, for 10km of fiber instead of 20km of fiber that completely exceeds the defined range.

The excess OPP to 20km can be explained by the introduction of undesirable system errors, as well as greater difficulty in recovering data from the optical network by the FPGA, leading to an invalid characteristic curve.

This greater difficulty can be reflected in two aspects that can aggregate and compromise the overall performance of the system.

One of the strands reflects the quality of the signal coming from the optical network observed by the receiver, being it an important factor when the introduction of the fiber is present. The fiber degrades the performance of the transmission signal in relation to the B2B condition, as can be seen in figure eye diagram 4.20.

The other strand reflects the physical behaviour of the FPGA transceivers, which requires a favourable environment for this to be able to recover the signal that was degraded during the optical network. This 20km curve was only achieved with the addition of a fan over the fan already existing in the FPGA, verifying that the behaviour of the transceivers is influenced by the temperature at which they operate.

4.3.3 Comparative study of the BERT system with a reference BERT system

In order to evaluate the performance of the BERT system developed, a test of a reference system was performed, available in PICadvanced, to compare the performance of the development BERT system.

Figure 4.16 presents the performance associated to channel 4, the worst case, considering the BERT system and a reference. This performance difference is approximately 0.3 dB, within the measurement error of the power meter, thereby validating the BERT system developed.

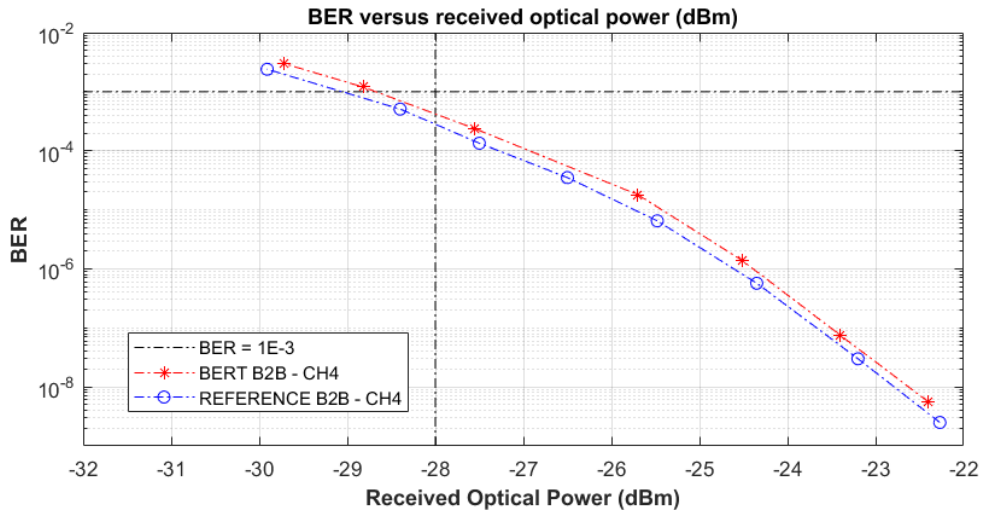


Figure 4.16: Comparison between the BERT system and reference BERT system

Although the developed BERT system performs lower, it fully complies with the values established by the NG-PON2 technology standard, since the required received optical power is lower than -28 dBm for downstream, as discussed in 2.2.4.

4.3.4 Impact of Effect of Pre/Post-Emphasis Parameters

As a way to fully explore the developed BERT system by improving the communication channel and consequently the performance of the system, certain parameters were adjusted.

One factor to be taken into account in this experimental part of this project is that high transmission rates promote an increase in channel driven distortion, which may cause a high BER to be observed on the receiver side.

Therefore, it is necessary to use techniques on the transmitter and receiver side to compensate for the noise/distortion input. These techniques are called emphasis in transmit domain and equalization in receiver domain.

In this context, techniques are implemented in the physical layer of the FPGA transceivers that "prepare" the signal to be transmitted to the channel, preventing its modification.

According to [50], TX-Emphasis is a technique which boosts high-frequency components or suppresses low-frequency components. 7-series FPGA transceivers have pre-tap and post-tap de-emphasis capabilities which help to compensate for the loss of signal over the channel.

These improvements of the communication channel can be reached through the inputs TX PRECURSOR [4:0] and TX POSTCURSOR [4:0] from the generated GTX module, subsection 3.6, and with the developed Continuous Mode interface, subsection 4.1, the user has the possibility to adjust the Pre/Pos-Emphasis values according to needs.

Figure 4.17 shows the improvement of the performance of the BERT system developed, to the worst case, with the adjustment of the Pre/Post-Emphasis parameters, allowing an approximation for the reference BERT system.

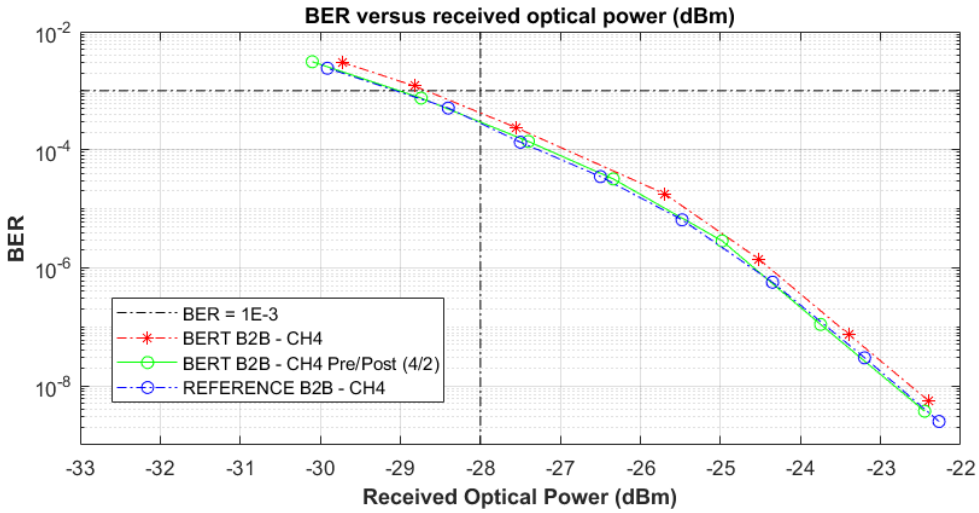


Figure 4.17: System behaviour with Pre/Post-Emphasis parameter introduction

4.3.5 Analysis of the Transmission Signal in the Optical Network

As a last scenario, it was intended to demonstrate the quality of the transmission of the signal present in the optical network, in a first condition of B2B followed by the introduction of fiber, in order to understand the difficulties that may be inherent in the side of the receiver for later recovery of the data.

This way, the eye diagram responds to the quality that is inherent in high-speed digital transmission. This eye diagram is achieved through an oscilloscope which overlays sweeps of different segments of a long data stream, allowing to have a perception of the quality of the system in terms of threshold level in amplitude and time [51].

The following eye diagrams were achieved, through the topology present in the block diagram, figure 4.18, followed by a realistic perception of the topology, figure 4.19.

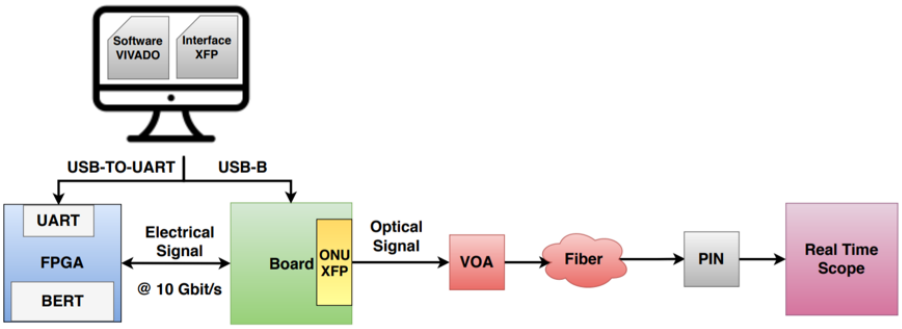


Figure 4.18: Block diagram for transmission signal characterization

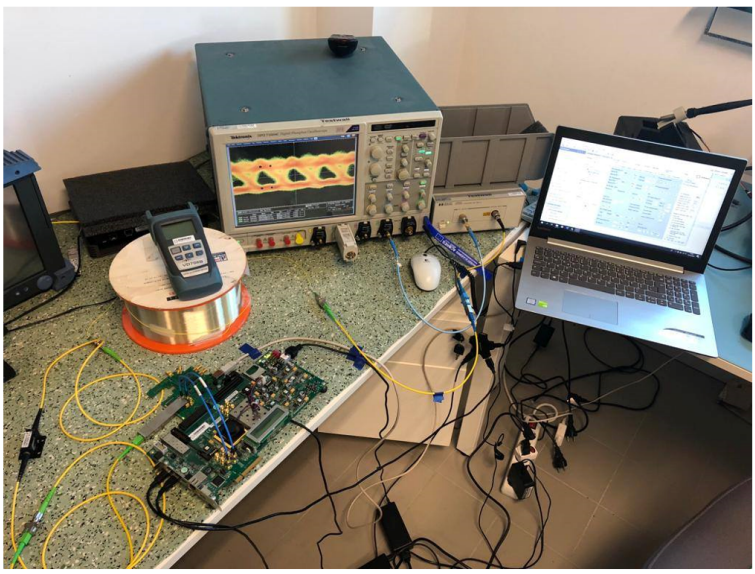


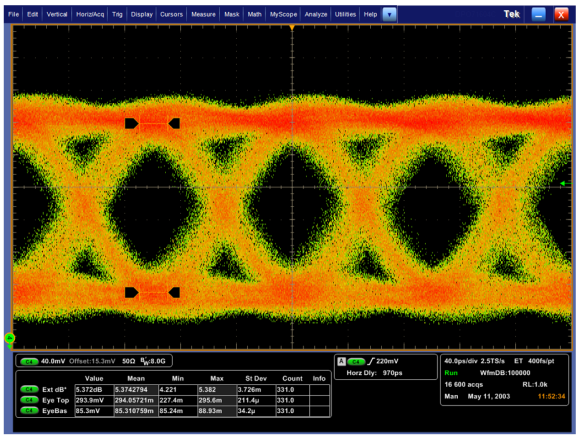
Figure 4.19: Setup for transmission signal characterization

Figures 4.20 present the eye diagrams for B2B condition, 10km and 20km, respectively. These eye diagrams are achieved through a digital phosphor oscilloscope (DPO), Tektronix DPO MSO71604C , at 10 Gbit/s transmission rate coming from FPGA.

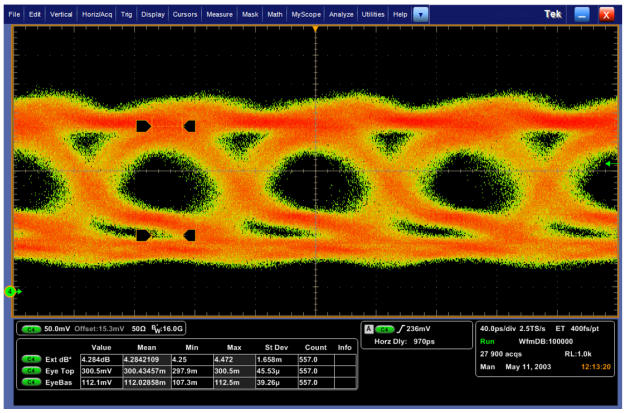
Concerning the eye diagrams, the differences between the back to back and 10km and 20km of fibre are more visible. In the B2B case, the eye diagram is open in terms of amplitude and time which respectively lead to good threshold level and good sampling time. The jitter (time taken in the crossing states) is small, as well as the noise for the '1' and '0' level. On the other hand, the eye diagram of the system with 10km and 20km of fibre has more noise in the '1' and '0' levels which lead to a worse decision level when compared to the previous case. Moreover, the jitter in these cases is higher and is caused by the dispersion of the fibre.

It is possible to check throughout these eye diagrams that the ER value is influenced by the opening of the eye diagram, since aperture of the eye diagram decreases as the ER level decreases, thereby making it difficult decision level the receiver.

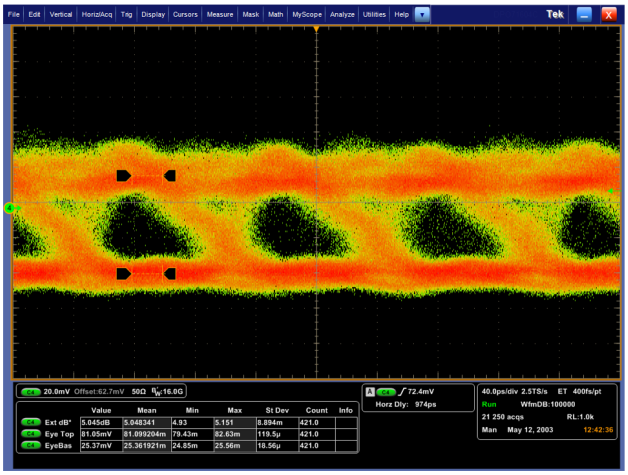
For the different conditions, B2B, 10 and 20km, eye aperture and consequently the ER value complies with the available upstream interval, in the subsection 2.2.2, as dictated by the NG-PON2 standard.



(a) 10 Gbit/s + B2B.



(b) 10 Gbit/s + 10km.



(c) 10 Gbit/s + 20km.

Figure 4.20: Eye diagram results for the transmission tests

Chapter 5

Implementation and Results of BERT in Burst Mode

In this chapter an architecture is developed, that intends to characterize one of the requirements of major interest in NG-PON2 technology, in order to verify its performance during the communication performed upstream instead of downstream.

According to 2.2.1, when the communication is performed upstream the lasers corresponding to the ONU transmitters are active during the time intervals predefined by the OLT and deactivated in the remaining instants, figure 2.4. Thus, one of the main objectives of this architecture is the implementation of a BERT system that allows, for each time interval predefined, the viability of communication.

This architecture contains most of the architecture structure previously developed, with the addition of new blocks, both from the application side and from the BERT system developed through the FPGA. All these steps are appropriately detailed, and the main results are also presented.

5.1 Burst Mode Communication Interface

As previously mentioned, it was necessary to change certain blocks to achieve the Burst mode condition. A new parameter was added giving the user greater control over the OLT, allowing the definition of the time interval to perform the communication between ONU and OLT in upstream.

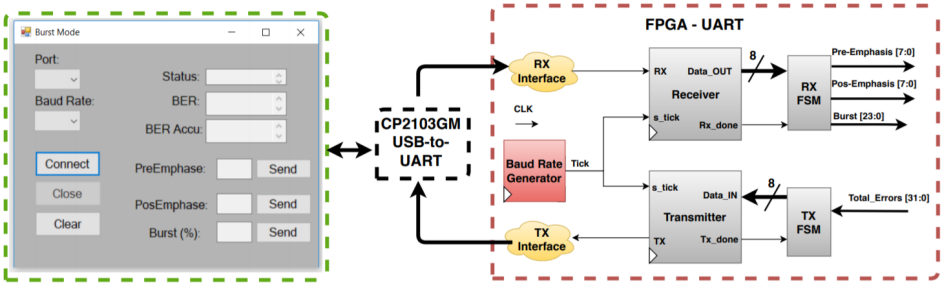


Figure 5.1: Diagram of UART blocks developed in FPGA and interface developed in computer both for Burst mode

Figure 5.1 demonstrates the referred parameter, designated as Burst, on both application and FPGA sides. This parameter, Burst, has a value defined between 0 and 100 %. When in the maximum percentage the continuous mode is reached, as referred to in the previous section.

5.2 Burst Mode Architecture

Although the architecture of Burst mode has most parts of the architecture previously developed, it is necessary to change certain structures like the frame structure that defines the data transmission.

As it can be seen from figure 5.2, the Burst mode has data transmission for a time interval predefined by the OLT, interrupting the following data transmission, in contrast to the continuous mode architecture in which it requires a continuous transmission of data.

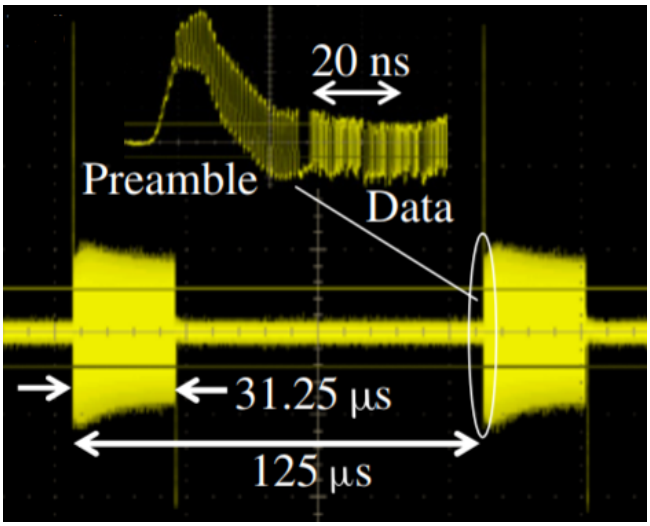


Figure 5.2: Burst-mode traffic for the upstream transmission [52]

According to subsection 2.3: the frame structure in burst mode has a duration of 125 μs and is composed by a preamble, a delimiter followed by a payload for a correct operation of the system. The preamble and delimiter allow the OLT optical receiver to adjust to the level of the optical signal and to delineate burst. The recommended size of the preamble and the delimiter is 160 bits and 32 bits, respectively.

Regarding the payload, the OLT is able to coordinate the time intervals of the Burst of each ONU, providing a dynamic payload. So, the time interval of each Burst can be defined by the introduction of the parameter Burst, referred to 5.1.

5.3 Bit Error Rate Tester (BERT)

This subsection presents the internal architecture of the BERT block developed in subsections 4.5, with the addition of a new input in the BERT block. This new input, designated Burst, allows to define the time interval of the Burst transmission and consequently define the number of bits present in the output, TX_DATA.

5.3.1 Block Diagram of system

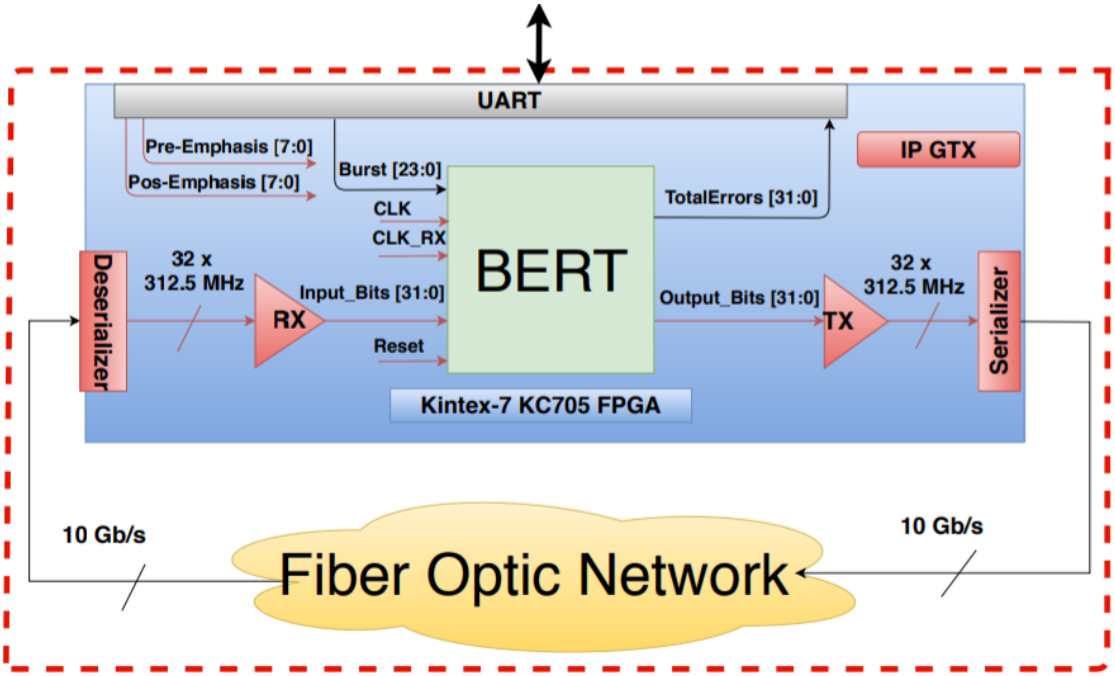


Figure 5.3: Block diagram of the Burst-mode BERT

5.3.2 Explanation of the blocks

One of the main changes made was data transmission, promoting the change of the data generator block, which compared with the previous architecture, needs to comply with the structure approached in subsection 5.2.

Although not changing the idea presented in the previous architecture, the synchronism block requires an extension of the delimiter from 16 bits to 32 bits. The counter block needs to add a new sub-block, designated as Counter Nburst.

This new sub-block indicates that if the Burst defined by the OLT is reached, the count of the number of errors so far will be stagnant until the next Burst input, sending this way a control signal.

Finally, the rest of the operation is similar to the previous architecture, in other words, when a given resolution is reached, the control signal is sent in order to stagnate the count and transmit it to the application, followed by the restoration of all counters for a new cycle to start.

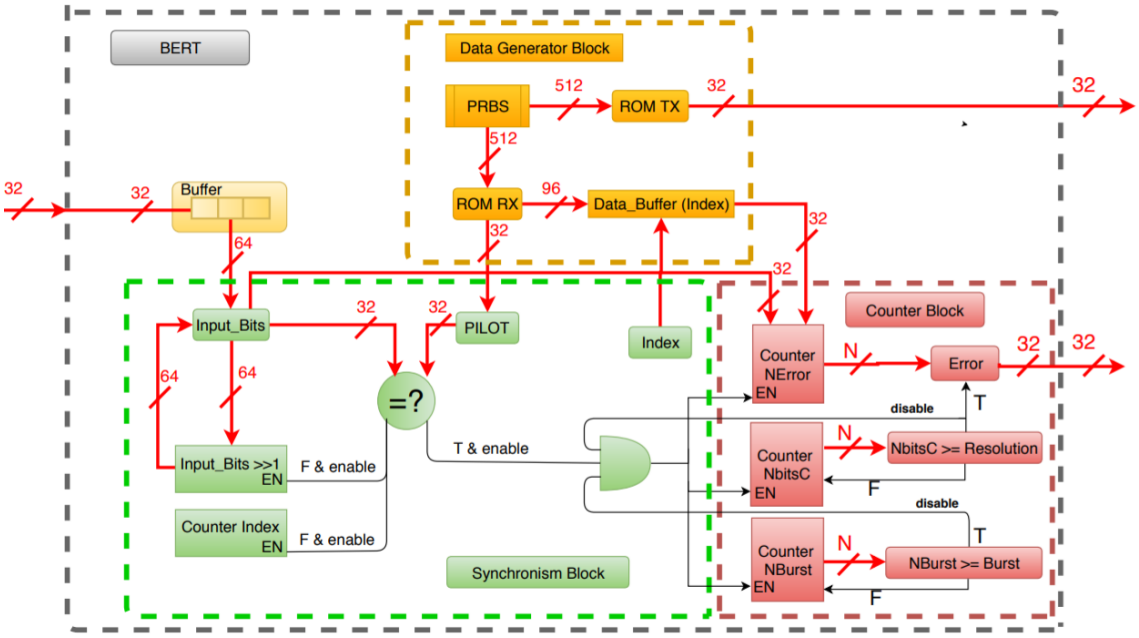


Figure 5.4: Simplified block diagram of BERT in Burst Mode

5.4 Experimental Results

This subsection intends to explore the last layer of the diagram initially presented in figure 4.1, as a way of evaluating the viability of the communication when it is performed upstream and consequently in Burst mode on the future NG-PON2 technology environment.

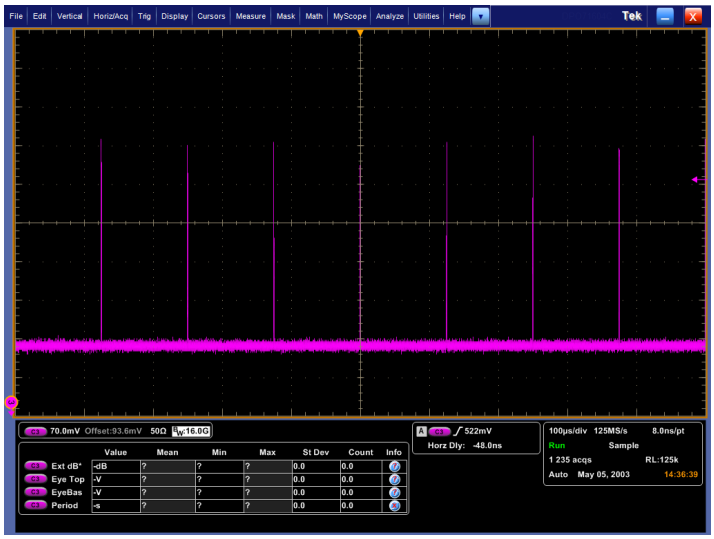
For this communication, certain difficulties were detected in the design and development, which compromised the development of the BERT system for this scenario. However, the system was properly synthesized and implemented in the FPGA in order to validate part of the concept's proof described in the previous subsections.

The results obtained, and the difficulties evidenced will be presented below.

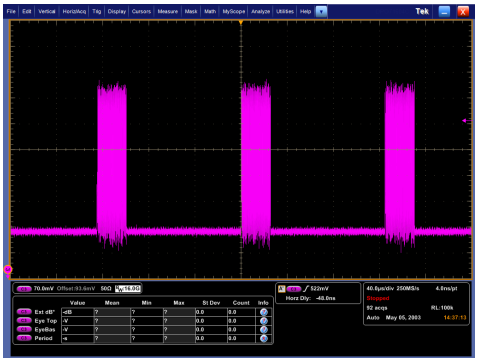
Firstly, it was necessary to modify the data generator block, since upstream communication is performed in Burst mode and it must comply with the structure already discussed in 5.2.

Figure 5.5a demonstrates the compliance of the Burst frame structure, validating the duration of 125 us. The developed Burst mode interface gives the users the opportunity to manage the OLT, defining the different Burst time intervals according to their needs.

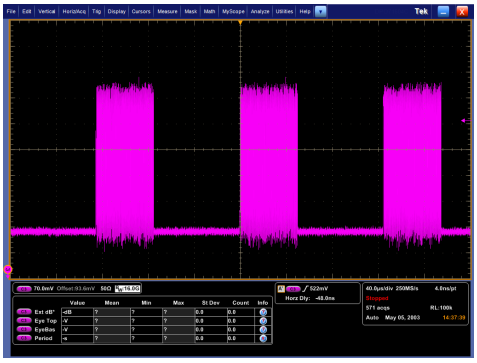
Observing the figures 5.5 it is possible conclude the different outputs of the transmission signal from the data generator block which will be present in the optical domain by converting the electrical signal into the optical signal which is done by the XFP transceiver.



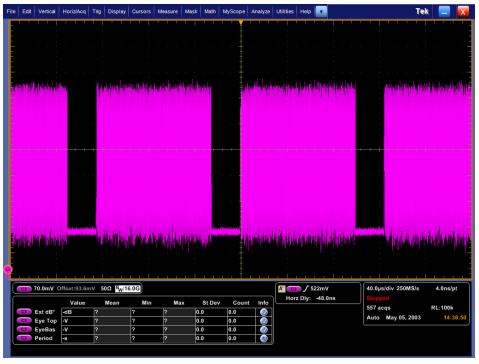
(a) Burst mode = 0 %



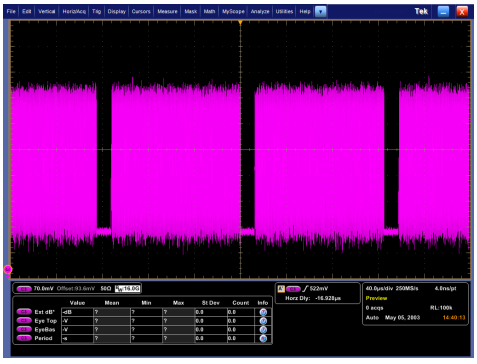
(b) Burst mode = 20 %



(c) Burst mode = 40 %



(d) Burst mode = 80 %



(e) Burst mode = 90 %

Figure 5.5: Behaviour of the different transmission signals of the Data Generator Block state

After validation of the data transmission signal, the synchronism block is reached. This synchronism shows difficulties in working in a Burst mode environment but not in a continuous mode.

As a way of evaluating the correct operation of the referred synchronized block, a closed-loop control test was performed between the transmitted and the received data, as shown in the figure 5.6.

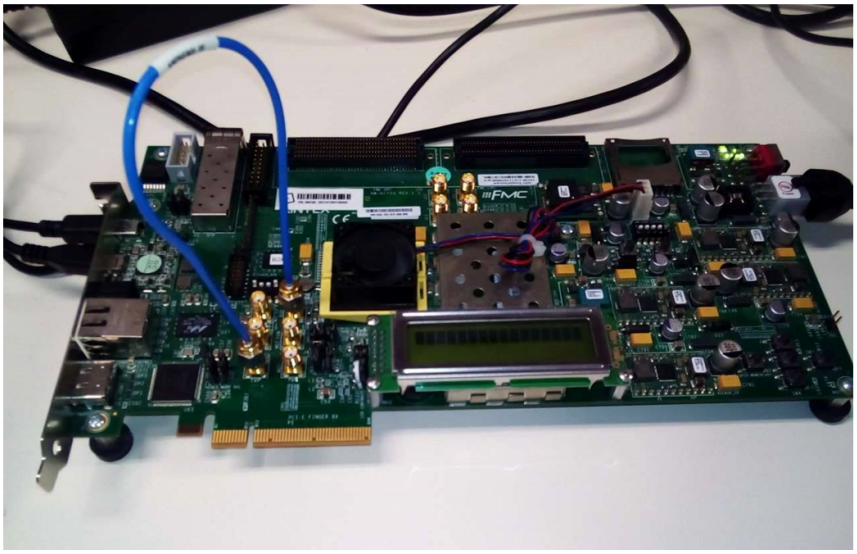


Figure 5.6: MGTs closed loop (blue SMA cable)

Figure 5.7 demonstrates the behaviour of the system when submitted to a given time interval, Burst = 95 % defined by the user, as a way to demonstrate the difficulties presented.

It is possible to verify an undesirable behaviour of the system, since it presents a BER value different from zero, something unexpected, since the transmitter and receiver are directly connected.

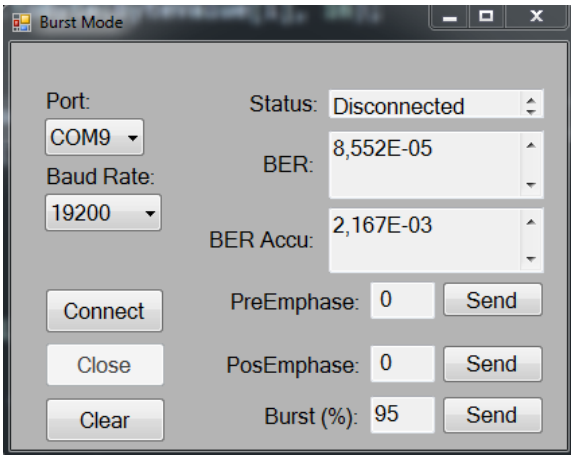


Figure 5.7: Invalidate BER for Burst mode = 95 %

Since the result does not meet expectations, several changes were made in the development of the Burst mode architecture, in order to identify the problem.

These changes had a greater focus in the data generator block and consequently in its interruptions, since this architecture demands the absence of data during the deactivation of the laser of a referred ONU.

The Burst mode architecture initially defined in 5.2, sends a set of zeros until reaching 125 μs, after the playload figure 5.8.

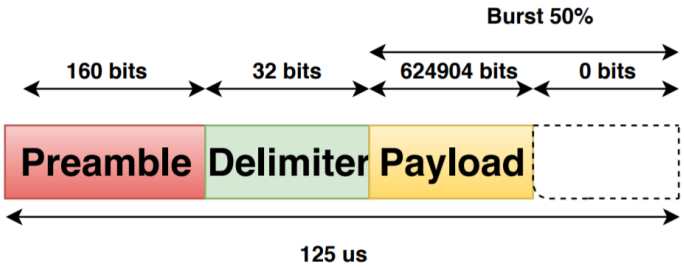


Figure 5.8: Upstream PHY frame

In a first instance, the structure of the Burst was modified, replacing the set of zero, defined after the payload, by preamble violating the premise of the Burst mode in order to understand the behaviour of the system, figure 5.9. In this first premise, the system was able to synchronize ideally for any defined time interval, demonstrating the expected feedback.

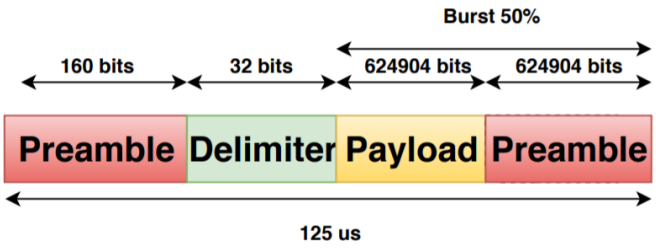


Figure 5.9: Upstream PHY frame that replaces the set of zero by preamble

In a second instance, the structure of the Burst frame, more precisely the preamble, was modified, expanding the size of the same from 160 bits to 8000 bits, 16 ns to 800 ns respectively, figure 5.10. This second premise, although not having solved the problem, has shown insignificantly an improvement in the Burst value, but still with a high time interval to reach the desired value BER.

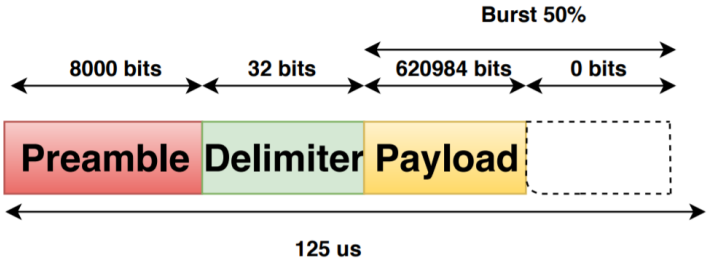
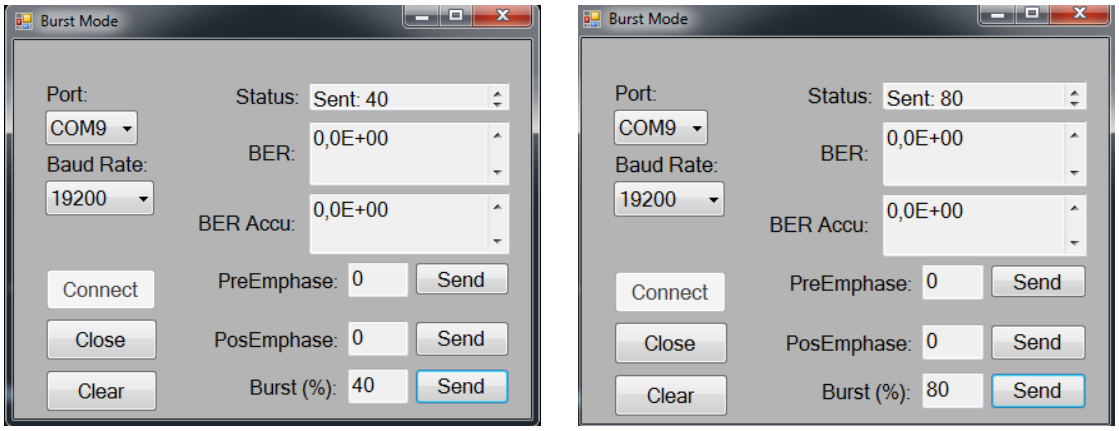


Figure 5.10: Upstream PHY frame expansion from preamble to 8000 bit

Since the second instance showed some improvement, the last instance was defined using the same reasoning, increasing the preamble until it reached synchronism. This last premise offered better performance allowing the user to set the Burst time interval according to needs.

This way, figure 5.11 show the user defined Burst time interval of 40 and 80 % respectively. As it is possible to visualize, the behaviour of the system is the desired, since it presents a feedback of BER equal to zero, something that is expected, due to the closed loop electrical connection between the transmitter and receiver present in figure 5.6.



(a) BER = 0 for Burst mode = 40 %. (b) BER = 0 for Burst mode = 80 %.

Figure 5.11: System behaviour for different user defined Burst mode

As a way of validating these different Burst time intervals, the Burst mode architecture was subjected to an overall system test. This test intends to demonstrate the flow of the system through flags to check the different transitions between the different states of the block diagram 5.4: **Data Generator block**, the **Synchronization block** as well as the **Counter block**.

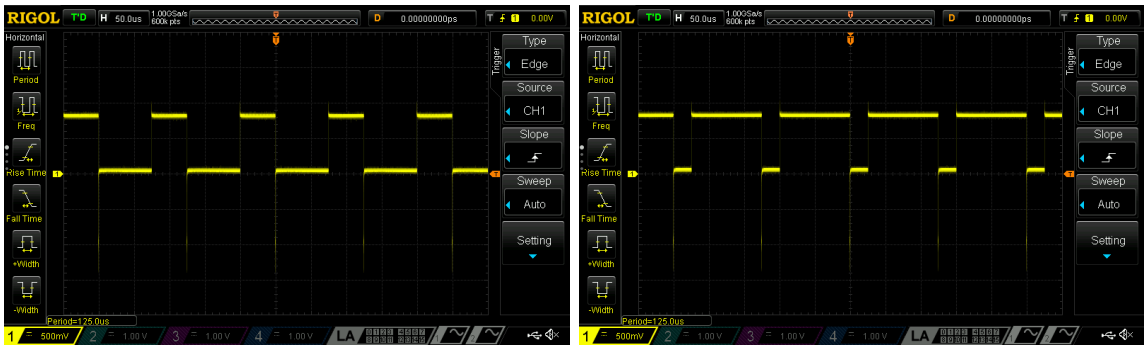
The respective state transitions were sent to LEDs of the FPGA and subsequently these were sampled through the oscilloscope, RIGOL DS1104z, as it can be seen in figure 5.12.

The obtained figures intend to validate, more specifically after the synchronism, the present state of the Counter Block for the different Burst time intervals, in order to validate the BER value seen in the figure 5.11.

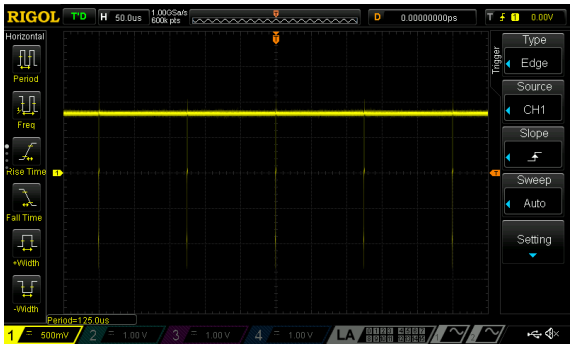
The continuity in the counter block allows to identify:

- Logical level '1':
  - The respective comparison between the data received and the reference data that will subsequently be counted and sent to the user;
- Logical level '0':
  - The state transition, in this case for the initial state;

It is expected that, the longer the user defines Burst time interval, the more extended is the logical level '1' of the counting block.



(a) Burst mode = 40 %. (b) Burst mode = 80 %.



(c) Burst mode = 100 %.

Figure 5.12: Behaviour of the different transmission signals signals of the Counter Block state

This last premise offered a better performance promoting the desired synchronization, allowing the users to define Burst time interval according to their needs.

However the last premise evidences the invalidation of the developed Burst mode architecture, since, with the reduction of the Burst time intervals, the system needs a higher recovery time of the clock, requiring huge preamble bits as shown in figure 5.13, thus violating the frame structure defined by the NG-PON2 standard.

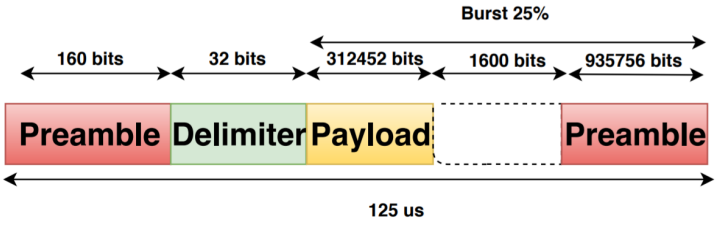


Figure 5.13: Upstream PHY frame expansion from preamble until the achievement of the synchronization

These premises identified the referred difficulties. This way, it is perceptible that the receiver of the generated GTX transceiver has difficulties during the clock data recovery and consequently the identification of the respective delimiter at the correct time.

These difficulties are influenced by the modulation format underlies since the developed system has an Non-return-to-zero (NRZ) modulation format, defined by the NG-PON2 stan-

dard. This format for long sequences of 0's and 1's promotes the absence of transitions, leading to loss of time reference of the receiver.

As mentioned in subsection 3.5.4, during transmission on the physical channel it is natural to have the phenomena of intersymbol interference when subjected to long periods of transmission of a certain value.

This interference reduces the margin of error, i.e., it reduces the signal-to-noise ratio (SNR) present at the receiver input, resulting in a significant degradation of the receiver's capacity to correctly identify the symbol, thereby increasing the reception error rate.

→Knowledge about PLL-CDR

Due to the difficulties presented, a detailed study of the transceivers general architecture was performed, subsection 3.6. This way, this subsection intended to explore the PLL which belongs to the PMA sublayer of the general architecture of transceivers.

The receiver generates a clock from an approximate frequency reference, and then phase-aligns the clock to the transitions in the data stream with a PLL. This is one method of performing a process commonly known as CDR [53].

The PLL is one of the most important circuits in telecommunications electronics that enables clock recovery, data synchronization, frequency multiplication, among others. [54]

According to [55], the basic principle of PLL operation is to continuously correct the phase and/or frequency difference between the reference signal (input) and the feedback signal from the voltage-controlled oscillator (VCO). This occurs through the interaction between 3 basic blocks: Phase/Frequency detector, Low-pass filter and a VCO, figure 5.14.

The output of the phase detector (PD) is proportional to the phase difference between the input signal and the feedback signal. If there is a difference in the frequencies of the two signals, the phase error will increase, and the output of the phase detector will reflect it.

This output is then filtered and applied to a VCO, which "adjusts" the feedback frequency until it is identical to the input frequency; under these conditions the phase error is constant and thus also constant the signal applied to the VCO, which maintains the synchronism of the frequencies. The time the PLL takes to synchronize both signals at the same frequency and phase is known as "Lock time".

Figure 5.14 shows the block diagram the PLL structure:

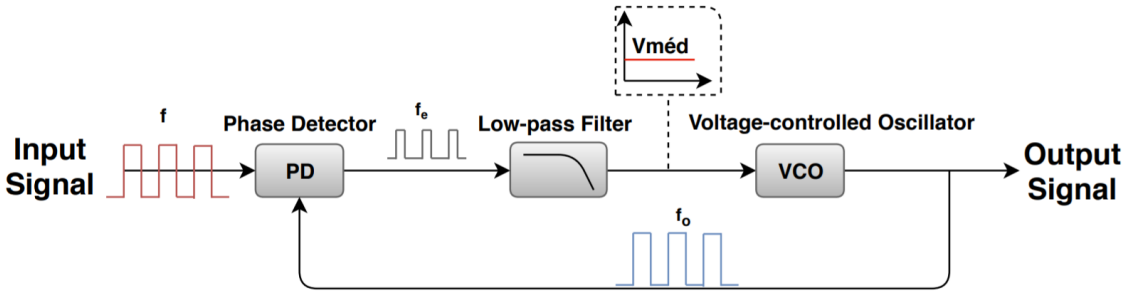


Figure 5.14: Detailed PLL Block Diagram (adapted [55])

The most important characteristics of a PLL are its acquisition range, that is, the range of frequencies in which the PLL can achieve synchronism; the range of synchronism, i.e. the range of frequencies that the PLL can follow, being initially synchronized; and the characteristics of the transitory PLL response (establishment time and overshoot).

If the frequency deviates too much from the original data clock, recovery will be problematic, especially with long transitions of 0's and 1's, since the acquisition time is relatively high due to the closed loop configuration. In contrast, open-loop systems can have a very fast lock time, and need only a few or even no preamble bits to lock the clock to the incoming data.

Observing figure 5.15, it is possible to conclude that the PLL-based architectures become unsuitable for applications that require very fast or immediate acquisition time, as is the case of Burst mode architecture.

	PLL-based	Burst-mode
Lock time	Very slow	Fast
Frequency range	limited	Fixed data rate
Jitter	Stochastic, depends on noise/mismatch	Stochastic, depends on noise/mismatch
Scalability	Bad	Good

Figure 5.15: Comparison between PLL-based and Burst-mode CDRs [55]

Chapter 6

Conclusion and Future Work

In this chapter a summary is presented on the project developed, as well as certain final considerations taking into account the results obtained. Finally, some proposals for future work are presented that aim to improve the work already developed.

6.1 Conclusion

The developed project consists of three parts, the first two being the most interesting, since they support the development of two different architectures that allow contributions to the source project, with the design of new structures into FPGA that will later be used on the calibration board of NG-PON2 transceivers, under development at PICadvanced.

The main objective of the first part of the project is the exploitation of two different architectures, continuous mode and Burst mode, with the aim of developing a BERT system, on NG-PON2 technology that demonstrates the feasibility of communication.

The different architectures, together with the generated GTX module, allowed to reach the second part of the project, providing the validation of the architectures through the sending/receiving of data correctly in closed loop.

According to feedback from the architectures, the objective of the third part of the project is to obtain results from the optical network topology, provided by the company PICadvanced, through the communication interface developed, allowing the user to control BERT system, validating its characteristics with the respective NG-PON2 technology standard.

Regarding the continuous transmission of data, the architecture of the BERT system reached the third part of the project, validating its performance through characteristics, such as the sensitivities, the OPP and the ER. It presented difficulties when submitted to the introduction of long fiber lengths, such as 20km, thereby exceeding the OPP range established by the NG-PON2 standard.

The BERT system for a Burst mode presented difficulties in reaching the third and last part of the project on the behaviour of the system for different sizes of Burst in upstream transmission of the NG-PON2 technology.

As discussed in subsection 5.4, this last architecture shows the impossibility in obtaining the desired synchronism, that compared to the previous architecture, there were difficulties in an initial step in the synchronism but these were successfully overcome.

In a general perspective of the project, the objectives were achieved:

- Communication interface between the FPGA and Computer;

- Graphical user interface (GUI) to control the experiments;
- The BERT system for the continuous transmission of data was achieved:
  - Data generation at 10 Gbit/s;
  - Data reception at 10 Gbit/s validated in B2B and 10km;
- The BERT system for the Burst mode transmission of data presented a positive contribution to the subsequent completion:
  - Compliant Burst mode profiles with NG-PON2 generation validated;
  - Definition and implementation of architecture;

Afterwards, the integration of these architectures will allow responding to the modules required by the source project, with the introduction of them in the calibration board, bringing it closer to the desired automated calibration board and consequently obtaining a greater productivity and yield in the production response of the XFP over the NG-PON2 technology.

6.2 Future work

The work of this thesis was developed, having as motivation its inclusion in the source project, with the goal of PICadvacned developing an automated calibration system and testing. Consequently, in order for this inclusion to be performed definitively, it is necessary to make some improvements to the work, which are listed below:

- To develop a dynamic PRBS and Preamble adjustable to the user's needs.
- To progress to the Kintex UltraScale FPGA:
  - This FPGA allows reaching the burst-mode clock data recovery (BCDR), which obtain the lock time in a very short time.
  - To characterize the BERT system for both architectures to validate the operation points of the NG-PON2 technology.

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