Samuel Santos Pereira

Exploração de Transmissores Integralmente Digitais em Cenários C-RAN

Exploration of All-Digital Transmitters in C-RAN Scenarios

Samuel Santos Pereira

Exploração de Transmissores Integralmente Digitais em Cenários C-RAN

Exploration of All-Digital Transmitters in C-RAN Scenarios

Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Meste em Engenharia Electrónica e de Telecomunicações, realizada sob a orientação científica do Prof. Doutor Arnaldo Silva Rodrigues de Oliveira, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro e do Prof. Doutor Paulo Miguel Nepomuceno Pereira Monteiro, Professor Associado do Departamento de Electrónioca, Telecomunicações e Informática da Universidade de Aveiro

o júri / the jury

presidente / president

Professor Doutor Armando Carlos Domingues da Rocha
Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro

vogais / examiners committee

Professor Doutor João Paulo de Castro Canas Ferreira
Professor Auxiliar da Faculdade de Engenharia da Universidade do Porto (arguente)

Arnaldo Silva Rodrigues de Oliveira
Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro (orientador)

agradecimentos / acknowledgements

Antes de mais gostaria de agradecer à minha mãe pois foi dela que aprendi o mais importante da vida. Foi também ela que me ajudou incessantemente neste percurso que começou muito antes da universidade. Obrigado, mãe.

Gostaria também de agradecer ao resto da minha família e amigos e a todos aqueles que de alguma forma me ajudaram não só neste percurso académico como em todos os aspetos da minha vida.

Um agradecimento em especial para o Ricardo Figueiredo, que foi como um segundo professor em todas as cadeiras que tive. De realçar também a ajuda dada pelo Daniel Dinis e Abel Lorences-Riesgo, com os quais trabalhei e me diverti imenso.

Queria agradecer também aos professores Arnaldo Oliveira e Paulo Monteiro por me terem dado esta oportunidade, bem como ao Instituto de Telecomunicações e a todo os seus funcionários e colaboradores pela disponibilidade e auxílio prestado.

A todos, muito obrigado.

Este trabalho é financiado pela FCT/MEC através de fundos nacionais e quando aplicável cofinanciado pelo FEDER, no âmbito do Acordo de Parceria PT2020 no âmbito do projeto UID/EEA/50008/2013 e pelo Fundo Europeu de Desenvolvimento Regional (FEDER), através do Programa Operacional Regional de Lisboa (POR LISBOA 2020) e do Programa Operacional Competitividade e Internacionalização (COMPETE 2020) do Portugal 2020 [Projeto 5G com o número 024539 (POCI-01-0247-FEDER-024539)] e pelo Fundo Europeu de Desenvolvimento Regional (FEDER), através do Programa Operacional Competitividade e Internacionalização (COMPETE 2020) do Portugal 2020, Projeto RETIOT, POCI-01-0145-FEDER-016432.

FCT Fundação para a Ciência e a Tecnologia

RETIOT

Cofinanciado por:

Lisb@20 20 COMPETE 2020 PORTUGAL 2020 UNIÃO EUROPEIA Fundo Europeu de Desenvolvimento Regional

Resumo

De modo a acompanhar a sempre crescente exigência de maiores taxas de transmissão, a próxima geração de telecomunicações móveis (5G) irá necessitar de maiores larguras de banda, bem como novas frequências de transmissão com espectro livre capaz de acomodar tais larguras de banda. A subida em frequência é apontada como uma solução para este problema, contudo as baixas áreas de cobertura apresentadas por estas bandas de frequência (mmWave) irão necessitar de uma nova forma de implementar estações base. Estas, por sua vez, terão de existir em maior número e mais próximas. É aqui que a nova arquitetura de redes de acesso radio, C-RAN, pode permitir cumprir com estes requisitos, além de poder baixar o custo de cada estação base e aumentar a sua eficiência energética.

Esta dissertação tem como objetivo a criação de uma ligação ponto a ponto baseada em transmissores integralmente digitais (ADTs) capaz de ser usada para a transmissão de dados no *fronthaul*. Aproveitando os desenvolvimentos recentes nos ADT, a criação de um transmissor integralmente digital com largura de banda elevada é agora possível. Além disto, os agregados de células lógicas reprogramáveis (FPGAs) têm vindo a fornecer cada vez uma maior capacidade de processamento, usando menos energia, tornando o produto final, mais barato e mais eficiente. O recurso à modelação delta-sigma ($\Delta\Sigma$M) no ADT poderá reduzir consideravelmente a complexidade da cabeça remota de rádio (RRH).

Neste trabalho a ligação ótica que irá ser usada para enviar os dados no *fronthaul* será baseada num SFP, mas outras técnicas de rádio sobre fibra (RoF) poderão ser também usadas de forma a possibilitar, por exemplo, *upconversion* ótico.

Da conclusão deste trabalho resulta uma ligação ponto a ponto baseada num ADT com um *Error Vector Magnitude* (EVM) sempre abaixo dos 5%, bem como duas arquiteturas de *upconversion* ótico com uma gama possível para o sinal de saída que pode variar entre os 27 GHz e os 63 GHz.

Abstract

In order to accommodate the ever-growing demand for higher transmission rates, the next generation of mobile telecommunications (5G) will need larger bandwidths, as well as, new frequencies with available spectrum capable of accommodate such bandwidths. The rise in frequency is being pointed out as a solution for this problem, however, the low coverage areas presented by these frequency bands (mmWave) will require a new way of implementing base stations. Those, in their turn, will exist in higher numbers and closer together. It is where that the new radio access network architecture, C-RAN, may allow for the fulfilment of these requirements, besides also allowing for the reduction in cost of each base station as well as providing an increase in its energy efficiency.

This dissertation aims to create a point-to-point optical link based on All-Digital Transmitters (ADT) capable of being used for data transmission in the fronthaul. Taking advantage of recent developments in ADT, it is now possible to create one with large bandwidths. Besides, the field programmable gate arrays (FPGAs) have been providing each time higher processing capacity using each time less energy, making the final product cheaper and more efficient. Recurring to delta-sigma modulation ($\Delta\Sigma$M), a reduction in the complexity of the remote radio head (RRH) can be achieved.

In this work the optical link that will be used to transport the data through the fronthaul will be based on an SFP. However, other techniques of radio over fibre (RoF) can be used to enable, for example, optical upconversion.

From the conclusion of this work, a point-to-point optical link based on an ADT was achieved with an Error Vector Magnitude (EVM) always lower than 5%. Also, from this work, two optical upconversions were developed with an output frequency range from 27 GHz up to 63 GHz.

Contents

List of Figures

List of Tables

List of Acronyms

ΔΣM	Delta-sigma Modulation
ADT	All-Digital Transmitters
BBU	Baseband Unit
C-RAN	Cloud Radio Access Network
CPRI	Common Public Radio Interface
DAC	Digital-to-Analogue Converter
DDS	Direct Digital Syntheses
eCPRI	Evolved Common Public Radio Interface
EDFA	Erbium Doped Fibre Amplifier
EVM	Error Vector Magnitude
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
Gsps	Gsamples per second
HDL	Hardware Description Language
IIR	Infinite Impulse Response
ILA	Integrated Logic Analyser
IoT	Internet of Things
MASH	Multi-Stage Noise shaping
MGT	Multi-Gigabit Transceiver
MIMO	Multiple Input Multiple Output
mmWave	Millimetre Wave
Msps	Msamples per second
NTF	Noise Transfer Function
PWM	Pulse-width Modulation
QAM	Quadrature Amplitude Modulation
RAM	Random Access Memory
RF	Radio Frequency
RoF	Radio over Fibre
ROM	Read Only Memory
RRH	Remote Radio Head
SDR	Software Defined Radio
SFP	Small Form-Factor Pluggable Transceiver
SNR	Signal to Noise Ratio

SOA	Semiconductor Optical Amplifier
SQNR	Signal-to-Quantization Noise Ratio
STF	Signal Transfer Function

Chapter 1

Introduction

1.1 Background and Motivation

The ever-growing demand for bandwidth in the mobile communications systems has triggered a huge wave of research and development in the field. This, accompanied by environmental issues, has led developers to find not only solutions capable of delivering wider bandwidths, but also to find the ones which use less energy. These two concerns, paired with the need for more flexible architectures, are the backbone of the next generation of wireless communications (5G).

For a successful 5G implementation and deployment, data rates higher than one gigabit per second are expected to be deliver to each user, and, due to the rise of the Internet of Things (IoT), ten thousand or more devices could be connected to a single macrocell [1]. From [1], it is explained that the increase in data rate per user accompanied by the rise in the total connected devices could represent a thousand fold increase in the so called aggregated data rate, which refers to the total data rate in bit/s per unit of area. Another target for 5G is the low latency which is expected to be less then 1 ms. An overview of these requirements for 5G can be seen in the Figure 1.1. A solution to all these problems could arrive from the combined gains of extreme densification of base stations, of larger bandwidth, mostly by migrating into the millimetre wave band, and of the increased spectral efficiency provided

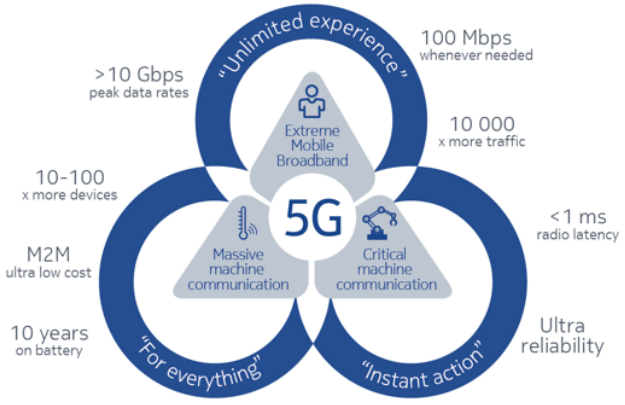


Figure 1.1: 5G vision and key performance indicators, copied from [2].

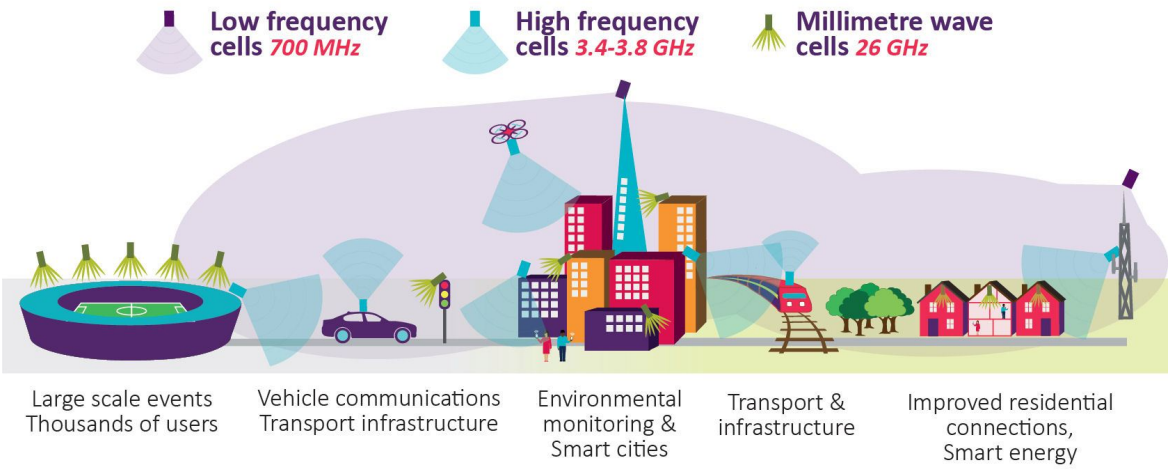


Figure 1.2: Different 5G bands and their applications, copied from [3].

by Multiple Input Multiple Output (MIMO). The use of multiple frequency bands will also ensure that all scenarios are covered by 5G. The use of low frequencies can give large coverage areas, which are important for rural areas, the high frequency band will provide most of the bandwidth needed in cities specially when inside cars and other transports and finally the millimetre wave band will allow for coverage of large scale events and some other specific cases where high bandwidth is the bigger problem. A depiction of these various frequency bands and their use cases can be seen in Figure 1.2.

To achieve the solutions mentioned in the previous paragraph, many authors have pointed to Cloud Radio Access Network (C-RAN) as an enabler for the densification of base stations and for the increase in bandwidth [4]. C-RAN is divided into three blocks: the Baseband Unit (BBU), the fronthaul and the Remote Radio Head (RRH). Figure 1.3 is a depiction of a typical C-RAN architecture, where the BBU is connected to one or several RRHs through the frontahul. The BBU is responsible for the baseband processing and the routing of the data to and from the core network. The fronthaul is normally based on an optical fibre or microwave link, however, there are research to make a packages based fronthaul using ethernet. Some of the more conventional architectures for fronthaul implementation also use analog radio over fibre, Common Public Radio Interface (CPRI) or Evolved Common Public Radio Interface (eCPRI) to transmite data between the BBU and RRH. Finally, the RRH is responsible for receiving and sending data to the fronthaul and for the amplification and radiation. This centralized architecture allows for one BBU to control several RRH, which allows for savings in the BBU regarding the air conditioning, site rent and also for a more effective use of the BBU's computational resources. The reduced cost of the RRH makes its massive deployment a possibility, essentially enabling the densification of base stations that was mentioned in the previous paragraph. Despite these advantages, the CPRI architecture presents a few characteristics that may present some challenges and in this work, the focus will be those presented by the fronthaul, where a flexible and low cost solution is needed. Some authors have pointed to a solution based on All-Digital Transmitters (ADT) with a Radio over Fibre (RoF) connection to the RRH [5, 6]. In this work an implementation based on this concept will be implemented and tested.

ADTs are an attempt of reaching the ideal Software Defined Radio (SDR) concept intro-

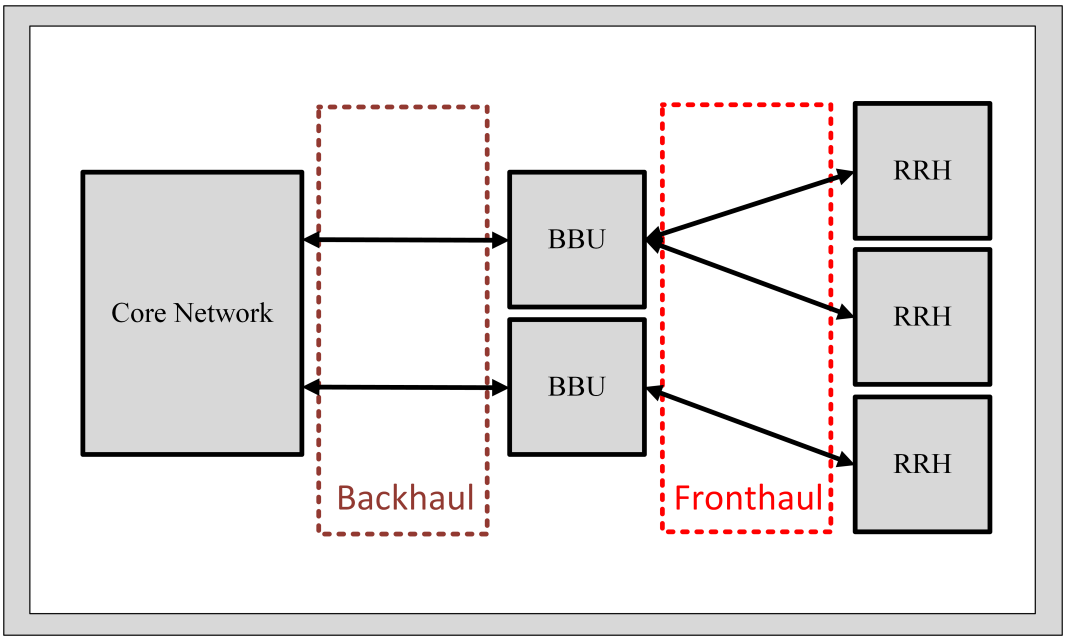


Figure 1.3: Cloud radio access network architecture.

duced by Mitola [7] and have been proposed as an alternative for the traditional transmission chains [8, 9]. Facilitated by the rapid rise in capacity of FPGAs, ADTs have become an hot topic [10–16] and many improvements have been made in order to reduce their size and power consumption, while delivering a larger bandwidth and more flexibility in terms of carrier frequency and waveforms. These improvements made to the ADTs are in line with the core problems to be addressed by 5G. The gain in popularity of ADTs had another consequence in the increased number of their use cases and now they can vary from a simple way of replacing a conventional Digital-to-Analogue Converter (DAC) and Radio Frequency (RF) mixer [9], to a noise and dispersion resilient way of transmitting an RF signal through optical fibre [5]. The architecture of an ADT can be seen in Figure 1.4. The ADTs architecture is composed of a baseband processing block, a pulse encoder and an upconverter. In the baseband processing block the received data is divided in the I and Q signals that are than sent to pulse encoder where the m-bit data is transformed into an 1-bit equivalent that is then upconverted to RF in the upconversion block. The pulse encoder can be designed based on Pulse-width Modulation (PWM) or Delta-sigma Modulation ($\Delta\Sigma$M). Pulse encoders based on PWM are simpler, while $\Delta\Sigma$M based pulse encoders present higher performance at the cost of a higher resource usage.

As mentioned above, the use of optical fibre transmission in conjunction with ADT has already been proposed and some literature have been publicized. In [5], a practical experiment was designed to test the feasibility of such architecture. In the end, the authors of that paper concluded that the use of ADT to create a simple RoF RRH was not only feasible, but also presented characteristics that benefit the signal's propagation in the optical fibre. This type of architecture shows promising features for the use in an optical fronthaul application, and as such some of this work will be dedicated to it.

Another advantage of combining an ADT with optical fibre is the possibility of using optical upconversion in order to migrate the signal created in the ADT into the Millimetre Wave

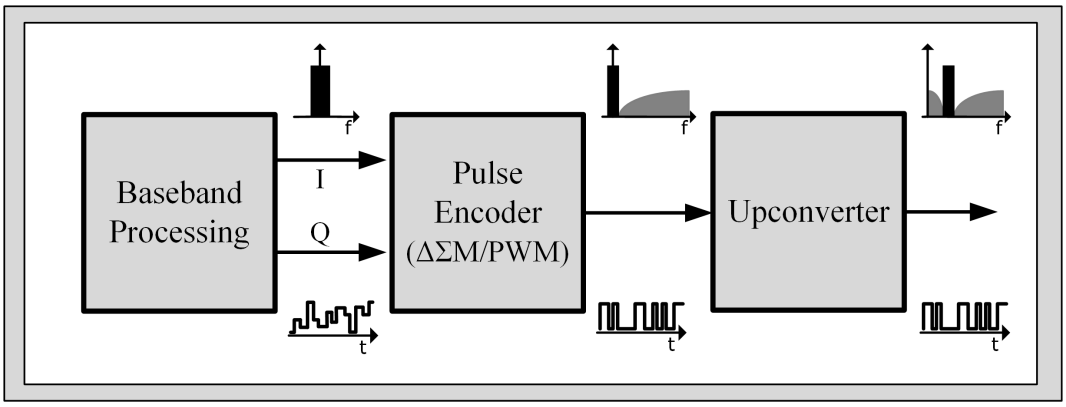


Figure 1.4: All-digital transmitter architecture.

(mmWave) band. This technique can reduce the complexity when creating an upconverter. This is due to this technique being simpler than a radio frequency mixer for this band.

1.2 Objectives

The general objective of this work is the creation of a fronthaul based on delta-sigma modulation with transmission over optical fibre. To achieve this goal, several smaller objectives, or milestones have been created in order to have a guideline as well as a mean of evaluating the development of the work. Those milestones were the following:

- Creation of an all-digital transmitter based on delta-sigma;
- Incorporation of optical fibre transmission in the created transmitter;
- Creation of a receiver for the all-digital transmitter (all-digital receiver);
- Incorporation of both, the transmitter and receiver, in the same project;
- Addition of fibre transmission between the transmitter and receiver.

For the second milestone, several fibre transmission techniques were explored. Two of those techniques will be presented in this document because they provide a easy way of upconverting the signal from an ADT into the mmWave band. These techniques also resulted in publications which will be describe in the next section.

Finally, with the achievement of all these milestones the author produced an optical fibre point-to-point link with an ADT based on ΔΣM.

1.3 Publications

The work done in the scope of this dissertation resulted in the publication of some papers that focused on the use of ADTs paired with optical upconversion and transmission in order to create transmitters to be used in C-RAN scenarios. The two published papers are listed bellow:

- **Millimetre-Wave Real-Time All-Digital Transmitter with Electro-Optical Upconversion**

  S. S. Pereira, A. Lourences-Riesgo, D. C. Dinis, A. S. R. Oliveira, J. N. Vieira, and P. Monteiro in ICTON 18 - International Conference on Transparent Optical Networks, pp. 1-4, July 2018.

  In this first paper, an optical upconversion technique is used to upconvert the signal from the ADT into mmWave frequency band. Several carrier frequencies were tested from 27 GHz to 63.2 GHz, proving the flexibility of the architecture in terms of the range for the carrier frequency. This technique greatly reduces complexity when compared to transistor based upconverters for this frequency band, while maintaining an equal or higher carrier frequency flexibility.

- **Real-Time FPGA-Based Delta-Sigma-Modulation Transmission for 60 GHz Radio-over-Fiber Fronthaul**

  A. Lourences-Riesgo, S. S. Pereira, D. C. Dinis, J. N. Vieira, A. S. R. Oliveira, and P. Monteiro in ECOC 18 - European Conference on Optical Communications, pp. 1-3, September 2018.

  In this paper, a working fronthaul based on radio over fibre is presented with upconversion to 60 GHz. This upconversion is used to sift the signal from an ADT into the mmWave band. The use of an ADT in conjunction with optical upconversion has the potential to significantly reduce the RRH complexity when used in a C-RAN scenario. This potential comes from the fact that when the signal reaches the RRH the upconversion happens in the photodiode and the recovery of the original signal from the ADT only needs a bandpass filter. At this point the signal is ready to be amplified and transmitted.

Also in the scope of this dissertation, the work done resulted in an invitation to present at the Vehicular Technology Conference, VTC2018-Spring. The presentation was entitled "C-RAN Enabled Lab Testbeds (from CPRI to Ethernet)" and it was focused on the Flexicell testbed and the subsequent work lines that were in development. Among one of those work lines is the work that was developed during this dissertation, specially the use of ADTs with optical fibre transmission in order to build an all digital based optical fronthaul.

Both the above mentioned publications, as well as the remaining of the work done during this dissertation resulted in the following major contributions:

- Utilization of ADT to the implementation of a point-to-point link;
- Development of two optical upconversion architectures capable of being used with ADT.

1.4 Document Organisation

This dissertation is divided into five chapters. Chapter 1 presents the background, motivations and objectives for this dissertation, it also presents the publications that resulted from this work.

Some concepts that will be needed for a complete understanding of this dissertation are reviewed in chapter 2.

In chapter 3 the simulation and implementation of the optical point-to-point link will be explained. At the end of this chapter there will be a section dedicated to the analysis of the results.

Chapter 4 introduces two different optical upconversion architectures. The two architectures are compared and practical results of both are shown and analysed.

Finally, chapter 5 draws some conclusions about this work and sets some guidelines for possible future work.

Additional information about the implementation of the point-to-point link can be found in Appendix A at the end of this document. In there, the reader can find more details about how the transmitter and receiver were implemented using System Generator.

Chapter 2

Background

2.1 Introduction

For a more easy understanding of this dissertation, this chapter presents an overview of some concepts that will be the focus of this work. Starting by an introduction to the ADTs that will contain a description of a typical architecture and a more in-depth review of two types of pulse encoders used, the PWM and the $\Delta\Sigma$M. Then, there will be a brief introduction to the concept of radio over fibre accompanied by a theoretical description of some modulation techniques, some modulators and some optical amplifiers. Finally, a section entitled "Practical Considerations" will introduce some concepts such as the concept of Multi-Gigabit Transceiver (MGT) and the importance of using a polyphase implementation instead of a monophase one. Also in this section, the concept of Error Vector Magnitude (EVM) will be reviewed due to its large importance when analysing the results.

2.2 All-digital Transmitters

There are several drivers behind the rise in the adoption of ADTs and one of the most important is the ability of an ADTs to implement a compact radio transmission chain, missing only the amplifier and the bandpass filter. Figure 2.1 has a depiction of a radio transmission chain based on an ADT. Another driver that favours the adoption of ADTs is the capacity of rapid reconfiguration, which makes possible the use of a single ADT to be able of transmitting and receiving several protocols with a vary wide range of characteristics such as different frequency, different bandwidth and different coding. This flexibility of the ADT paired with

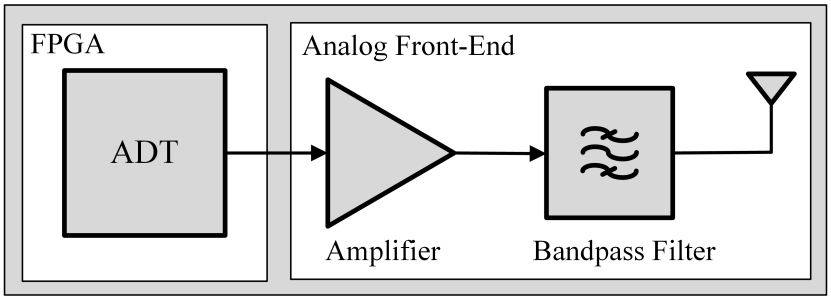


Figure 2.1: Transmission chain using an ADT, based on Fig.1 from [12].

the huge capacity of FPGAs allows for the saving in resources, both in capital expenditures and operational expenditure, by not only allowing for a single FPGA to implement several ADT that can be reconfigured as needed, but also because systems not being used can be shut down or passed to other FPGAs which are less occupied.

ADTs, as briefly mentioned in chapter 1, are comprised of three blocks, a baseband processing block, a pulse encoder block and an upconverter block. The relative position of these last two blocks determine if the ADT is an baseband-stage modulator or an RF-stage modulator. If the pulse encoder is placed before the digital upconversion block, the modulator is called a baseband-stage modulator, case depicted in Figure 1.1, when the pulse encoder is placed after the upconversion block, the modulator is called an RF-stage modulator. The choice between the two cases significantly influence the properties of the final ADT. While an RF-stage modulator may presente challanges in terms of layout and timing constrains due to its high sampling rate pulse encoders, acording to the state of the art, this is the only configuration that can give some agility in terms of carrier frequency [12]. On the other hand, the use of a baseband-stage modulator can significantly reduce the time and costs of building an ADT. However, the use of a traditional upconversion stage would not maintain the constant envelope presented in the output signal of the encoder block. This problem can be solved by choosing the carrier frequency as one fourth of the serializer's sampling frequency [12]. In this specific case as $fc = \frac{1}{4}fs$:

$$e^{\frac{j2\pi fc}{fs}n} = e^{\frac{j\pi}{2}n} = cos(\frac{\pi}{2}n) + jsin(\frac{\pi}{2}n) \tag{2.1}$$

and,

$$cos(\frac{\pi}{2}n) = [1, 0, -1, 0], n \in [0, 1, 2, 3] \tag{2.2}$$

$$sin(\frac{\pi}{2}n) = [0, 1, 0, -1], n \in [0, 1, 2, 3] \tag{2.3}$$

the final upconversion to this frequency is equivalent to do a replica of the I and Q samples and then arrange the output word in the form: $[I, \overline{Q}, \overline{I}, Q]$. With this technique the constant envelope of the signal is preserved.

Nowadays the main research focus is on the pulse encoder and despite the existence of many techniques that can be used in an ADT. Due to their efficiency, PWM and $\Delta\Sigma$M are the two most used techniques [17]. These type of pulse encoding techniques rely on oversampling the original signal and then reducing its levels of quantization to a one bit representation. More than one bit representations exist and are applied when a better signal quality is required [18] . In the next sections a brief description of PWM and $\Delta\Sigma$M will be presented alongside some advantages and disadvantages of each technique.

2.2.1 Pulse Width Modulation

The PWM technique is based on the comparison between the input signal, x(n), and the reference signal, r(n), normally a sawtooth or triangular wave, which results in a two level output signal. Figure 2.1 depicts the working principle of a PWM. In the digital implementation this comparison is really easy to perform and, as long as the input signal has been oversampled, the output contains a good representation of the original signal, which can be recovered using a low-pass filter. The oversampling ratio is a key factor for a good performance of a PWM and the higher it is the better the final result will be. This improvement in the quality

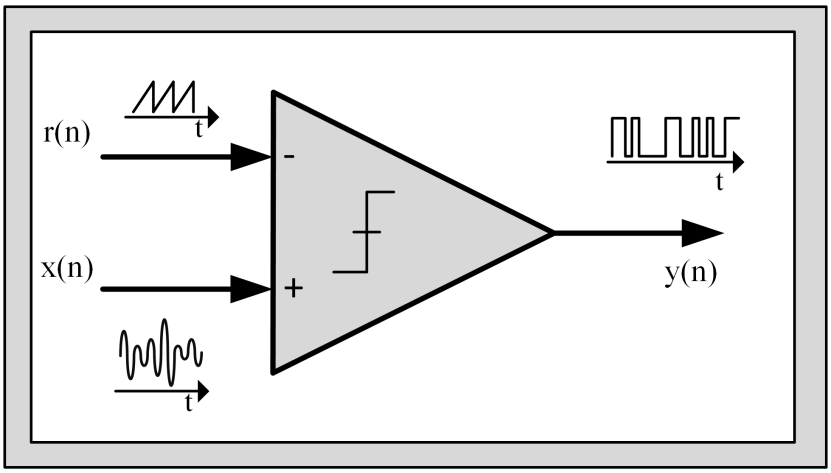


Figure 2.2: Pulse width modulation.

of the output signal is mainly due to the reduced noise floor caused by the oversampling ratio, but there is another advantage of using a higher sapling frequency, which is that, in the frequency domain, the harmonics of the square wave signal are further apart from the original signal making it easier to low-pass filtering the signal. In a practical implementation it is not always possible to increase the sampling frequency, especially when dealing with broadband RF signals. In these cases, polyphase implementations can be used to reduce the clock rate of each phase while maintaining the desired equivalent sampling rate. This approach has the disadvantage of increasing the total digital logic used [17].

In an ADT implementation, the output signal should have as low noise as possible to reduce the analogue filter requirements. When a PWM-based pulse encoder is used in an ADT, the output signal's spectrum contains not only the original signal's spectrum, but also the harmonics of the square wave of the PWM. A typical PWM spectrum can be seen in Figure 2.2, in it, the quantization noise can be seen in both sides of the original signal's spectrum. This type of output signal's spectrum is not ideal because it requires an analogue filter with an high quality factor. A technique to reduce these harmonics was introduced in [19] and it was able to reduce the first harmonic in more than 50 dB without introducing more complexity than was previously present in a typical PWM based ADT. The solution consists in dividing the time in which the signal is on, t_{on}, in smaller blocks while preserving the relation t_{on}/T, where T is the period. This essentially creates square waves with a smaller period and it is known that square waves with smaller period have their harmonics in higher frequencies. Hence the final PWM spectrum will have its quantization noise shaped into higher frequencies, away from the original signal's spectrum.

Other state of the art implementations allow for a continuous adjustment of the carrier frequency in the digital domain [12], giving an extra point of flexibility to the ADT. In that paper, the authors were able to achieve a frequency agility in the range from 100 MHz to 6.2 GHz with a frequency resolution of 1.5625 MHz. This kind of frequency agility may be useful for sub-6 GHz 5G applications.

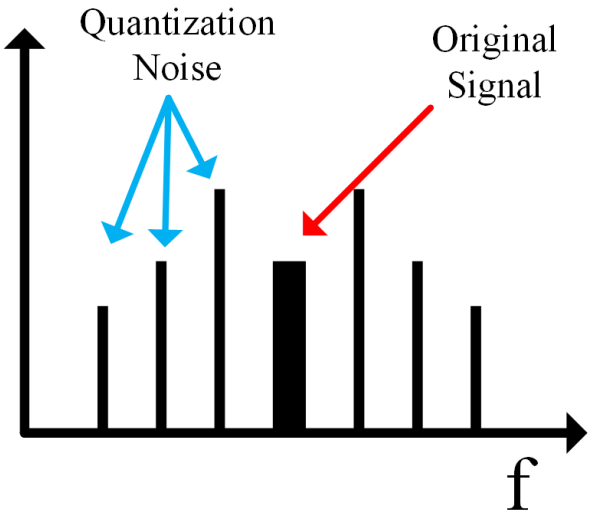


Figure 2.3: PWM typical spectrum.

2.2.2 Delta-Sigma Modulation

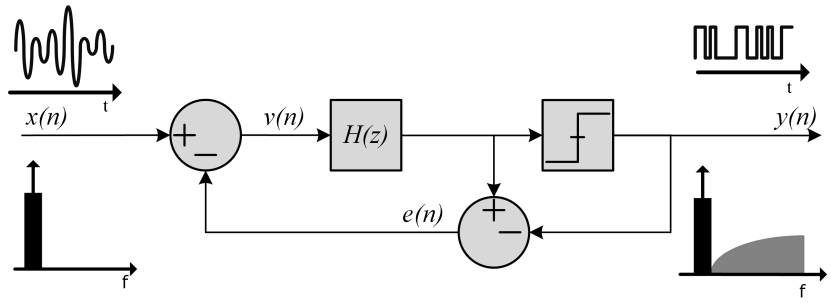
Another technique that is very used in the literature as a pulse encoder for ADTs is the delta-sigma modulation. This kind of modulation relies in most of the same principles as PWM, such as oversampling the original signal followed by a reduction in bits per sample. Despite these similarities, ΔΣM presents some advantages such as a good SNR, scalability and the general lower quantization noise levels near the desired signal, which makes possible to relax the analogue filtering [12]. This is essential for a good ADT implementation.

ΔΣM relies on an error feedback to reduce the added quantization noise to the signal band. This reduction in the quantization noise present in the signal band is determined by the filter, which applies a shaping mechanism to the noise. The type of noise shaping created by the filter imposes the maximum signal bandwidth to a specific Signal to Noise Ratio (SNR). In Figure 2.4, two topologies of a ΔΣM are depicted, one with the filter in the feed forward path, a), and other with the filter in the feedback, b). Both are called error feedback structures, because there is a path that feeds the error back into the input. Due to its simplicity these architectures are very attractive for the digital loops of ΔΣM [20]. The two topologies have different frequency response characteristics due to the position of the filter. In the figures the input signal is represented by $x(n)$, the output signal is represented by $y(n)$, the filter is represented by $H(z)$ and the error signal is represented by $e(n)$. Considering the z-transform of $x(n)$, $v(n)$, $e(n)$ and $y(n)$ as $X(z)$, $V(z)$, $E(z)$ and $Y(z)$, respectively, the frequency response of the modulator depicted in Figure 2.4 a) can be determine by the following equations:

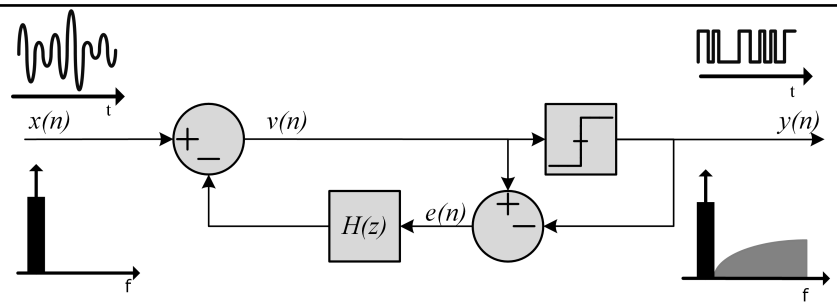
$$V(z) = X(z) - E(z) \tag{2.4}$$

$$E(z) = V(z)H(z) - Y(z) \tag{2.5}$$

substituting $V(z)$ in 2.5 for the one calculated in 2.4, the frequency response of the output



a)



b)

Figure 2.4: Delta-sigma modulation with: a) filter in the feed forward; b) filter in the feedback path.

signal is:

$$Y(z) = X(z)H(z) - E(z)(1 + H(z)) = STF(z)X(z) - NTF(z)E(z) \tag{2.6}$$

The modulator represented in Figure 2.4 b) has a slightly different frequency response, but the core equations which describe its behaviour are almost identical:

$$V(z) = X(z) - E(z)H(z) \tag{2.7}$$

$$E(z) = V(z) - Y(z) \tag{2.8}$$

substituting $V(z)$ in 2.8 for the one calculated in 2.7, the frequency response of the output signal is:

$$Y(z) = X(z) - E(z)(1 + H(z)) = STF(z)X(z) - NTF(z)E(z) \tag{2.9}$$

Doing a quick comparison between equation 2.6 and 2.9, it is easy to notice the difference, i.e., in 2.6 the input signal $X(z)$ comes multiplied by the filter, H(z), while in 2.9 the input signal is unaltered, this makes the Signal Transfer Function (STF) in equation 2.6, $STF(z) = H(z)$, while in the equation 2.9, $STF(z) = 1$. Having a STF equal to one means that the signal does not suffers any alteration in the modulator, apart for any delay caused by the adders or by the quantizer. This is very useful when the signal is already in the desired form to be transmitted and only the pulse encoding modulation is missing. In the other hand, having a filter in the feed forward may allow for a simultaneous filtering and pulse encoding of the signal. However, in this case the design of the filter may be more difficult in order to ensure

not only the correct noise shaping but also a good filtering of the signal. Analysing now the Noise Transfer Function (NTF), it can be seen that it is the same in both equations, 2.6 and 2.9. This means that both implementations will have the same noise shaping characteristics provided that they have the same filter.

One of the most important characteristics to have in mind when designing a ΔΣM is the type of noise shaping that the final implementation will have. As was referred before, the filter is the main block responsible for the NTF and it is possible to derived the type of noise shaping by analysing the NTF. From equation 2.6 or 2.9, it was concluded that the NTF provided by the topologies depicted in Figure 2.4 has the form: $NTF(z) = 1 + H(z)$. With this equality, the filter can be calculated to have the desired frequency response. One of the independent variables that are available for the designer is the order of the filter. A higher order filter will present a more abrupt noise cancellation pattern and also a larger notch, which allows for more useful bandwidth and higer signal quality also known as Signal-to-Quantization Noise Ratio (SQNR). Of course, that choosing a higher order filter modulator will have an increase in the total amount of resources used as well as an increase in the time and effort needed to make the implementation. The implementation of a higher order filter in a ΔΣM is a well studied subject [20] and many implementations like the cascade Multi-Stage Noise shaping (MASH) structure have already been successfully implemented [12, 14].

The search for more bandwidth while maintaining a high SNR has lead researchers to increase the sampling rate of the ΔΣM. This quickly reached the limit imposed by the clock rate of the digital systems and new solutions were developed in order to increase the sampling rate of the modulator, while maintaining a relative low clock rate. One of these solutions was the use of a multi-core ΔΣM. This solution, while looking simple at fist, imposes some challenges such as how to maintain the temporal continuity in the samples processed by each ΔΣM core and how to make the initial conditions of each ΔΣM core be the same as the core which had computed the previous samples. The first problem was addressed in [21], where two blocks called deinterleaving and interleaving make sure that each core was fed with k samples with time continuity. However, this means that in every k samples a discontinuity in the state of the core ΔΣM would occur. This discontinuity causes a decrease in performance by introducing noise spikes in the time domain. This problem was solved in [14] by the introduction of a block called "Synchronous Start-up Control Logic". This block is responsible for saving the final state registers of every modulator and pass it to the next one. This operation occurs every k samples.

Many researchers have been made improvements to ΔΣM's figures of merit such as bandwidth [16], SNR [14], and frequency agility [12], others improvements in these figures of merit may be possible with the implementation of techniques such as the lock-ahead time interleaved ΔΣM [15] and the borrow-save logic [22]. These techniques will not be explored in this work.

2.3 Radio over Fibre

RoF consists in the modulation of a light source, typically from a laser, with an RF signal, which is then propagated through an optical fibre. The large bandwidth offered by optical fibre made this technique very attractive. This has enabled optical fibre to dominate modern telecommunications, with applications in longhaul (core network, metropolitan network and access network), fronthaul (from the antenna to the base station and in C-RAN scenarios),

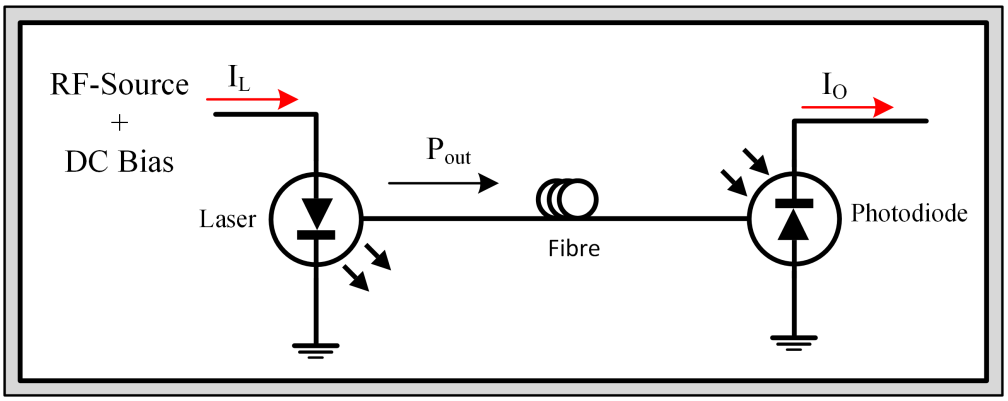


Figure 2.5: Optical direct modulation.

inside servers and more recently even inside buildings, offices and homes.

The modulation in a RoF scenario has two main methods, direct modulation and external modulation [23]. Each method has its own advantages and use cases. The direct modulation is the cheapest of the two and it's applied for low bit rate and low distances of transmission. The external modulation presents a better performance in terms of extinction ratio, which is the relation in terms of power between the on and off state, and also allows for complex modulation, which increases the spectral efficiency at the expense of cost.

The use of a direct modulation allows for a simple and cheap implementation of a RoF. Figure 2.5 ilustrates the working principle of a direct modulation. The use of an LED makes its implementation very cheap and easy, while also making it reliable when used for low bit rates applications. However, the use of direct modulation using a led is only aplicable in very specific scenarios such as visible light applications. The more typical aplications use a laser such as a VCSEL in order to increase bit rate without adding too much complexity and cost. However, most of these cheap lasers work at a wavelength of 850 nm and at this wavelength transmissions over long distances are not possible. In order to increase the transmission distance it is needed to switch the VCSEL at 850 nm to another laser with an wavelength in the 1550 nm range. This might increase the cost and potentialy making the implementation harder. However, it allows for the transmission over large distances and also enables the transmission of larger data rates, both by increasing the symbol rate and by using higher order modulations. The versatility achieved with this modulation called for a lot of attention and soon various use cases for this technique started to emerge. In radio communications, this enabled the start of the C-RAN research [5], which now has evolved to use more complex modulations schemes due to the ever growing demand for larger bandwidth and to enable the use of optical upconversion to reach the millimetre wave band needed for 5G [24, 25]. Other areas also implemented fibre optics based solutions, and in the car and plane industry plastic fibre optics were adopted due to their electromagnetic immunity and their lighter weight compared with copper solutions [26, 27]. The biggest limitations of the direct modulated lasers are its limited bandwidth, the linearity of the laser, the lower achievable extinction ratio and the frequency chirp, which causes a spectral stretching. All these effects are related to the bias point which must be carefully selected.

Although the use of a good laser enables larger bandwidths and higher order modulations to be transmitted by direct modulation, there are cases where an even better performance

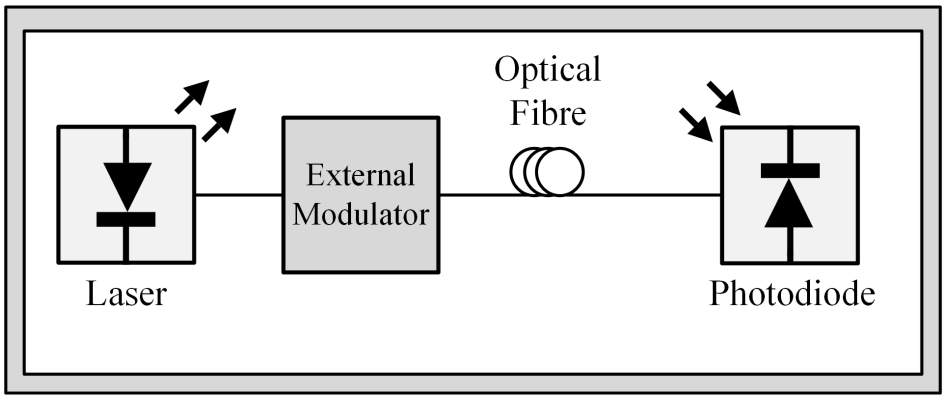


Figure 2.6: Optical external modulation.

is needed, especially when large symbol rates are to be transported through long distances. An improvement in performance can be made by switching to external modulation. This type of modulation enables the achievement of the best performance possible from the light source. The use of an external modulator also allows for an higher extinction ratio, in the case of an amplitude modulation, and it also allows for amplitude and phase modulation or just phase modulation. In the case of the amplitude modulation, the use of an electro-absorption intensity modulator allows for varying the absorption of the light in response to a voltage signal. This modulator works by changing the material absorption coefficient in function with an applied voltage. For the phase modulation the use of a phase modulator allows for a change in the phase of the signal by changing the material refractive index in function with the signal's voltage. Finally, the case which has more advantages, but is also more complex is the IQ modulation. Only with this type of modulation it is possible to achieve higher order modulations like Quadrature Amplitude Modulation (QAM) and so, despite the added complexity and cost, it is the modulation of choice for most telecommunications applications where a high performance is needed. This technique allowed for the exponential increase in the data rates of the backhaul, which enabled the construction of the modern Internet, where video streaming is already possible in both fix or mobile connections.

For the cases used in this work, amplitude modulation is the easiest modulation to implement and doesn't introduce much loss in the RF signal. This good conservation of the signals characteristics is due to the output of the FPGA being a simple two level amplitude-shift keying. For these kinds of signal a simple SFP is enough and, as will be demonstrated later, this is the modulator used for the final project. However, this modulator does not allows for more complex techniques like optical upconversion. For that reason some experiments with the ADT were done using a Mach-Zender Modulator.

A Mach-Zehnder modulator can be single-drive or dual-drive. The modulator depicted in Figure 2.7 is a single-drive Z-cut Mach-Zehnder modulator and it is made up of a phase modulator and two three dB couplers. The change in the phase of the signal in the upper arm caused by the phase modulator will interfere with the unaltered signal that travels through the lower arm. This interference is what causes the amplitude modulation part of a Mach-Zender modulator. The relation between the output power of the modulator and the input voltage $V(t)$ is given by the following equation:

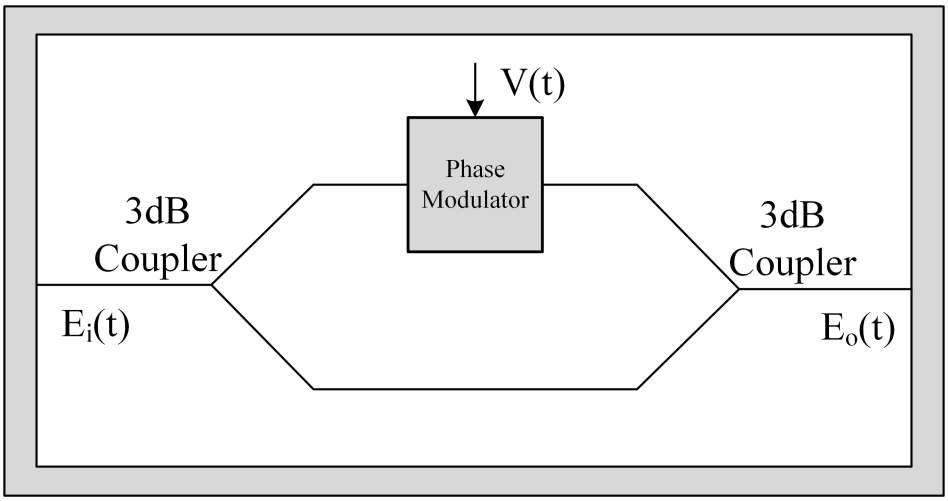


Figure 2.7: Single-drive Mach-Zehnder modulator.

$$E_o(t) = E_i(t)\frac{1 + e^{\frac{j\pi V(t)}{V_\pi}}}{2} \tag{2.10}$$

where V_π is the input voltage needed to create an 180 degrees inversion in the output signal. In this case, external modulation, the laser is not changed and so the value of $E_i(t)$ is a constant.

Despite also being used, the single-drive Mach-Zehnder is not the most used Mach-Zehnder, this title goes to the dual-drive Mach-Zehnder. The architecture of the dual-drive is depicted in the Figure 2.8. This modulator has an extra phase modulator in the lower arm which grants it some advantages over the single-drive, like the easy determination of the RF range of the input signal to achieve the best extinction ratio. To have a better understanding, lets first look to the equation describing the change in the output according to the change in $V_1(t)$ and $V_2(t)$:

$$E_o(t) = E_i(t)\frac{e^{\frac{j\pi V_1(t)}{V_\pi}} + e^{\frac{j\pi V_2(t)}{V_\pi}}}{2} \tag{2.11}$$

if the value of $V_2(t)$ is change to $V_2(t) = -V_1(t)$, the resulting equation is:

$$E_o(t) = E_i(t)\frac{e^{\frac{j\pi V_1(t)}{V_\pi}} + e^{-\frac{j\pi V_1(t)}{V_\pi}}}{2} = E_i(t)cos\left(\frac{\pi V_1(t)}{V_\pi}\right) \tag{2.12}$$

as can be seen, the resulting equation has the waveform of a cosine function. This mode of operation is called push-pull and can be very useful in the way it has no inherent chirp. This property makes the dual-drive Mach-Zehnder more appealing for high performance telecommunications when compared with the single-drive Z-cut Mach-Zehnder. However, the Z-cut is not the only single-drive Mach-Zehnder and the single-drive X-cut Mach-Zehnder is an alternative single-drive architecture that also presents no chirp [28].

In a radio over fibre implementation, after the modulation, it is normal to implement two more operations before the signal is sent to the fibre, these operations are the amplification and filtering, however, the implementation of such operations is not a rule and there are cases

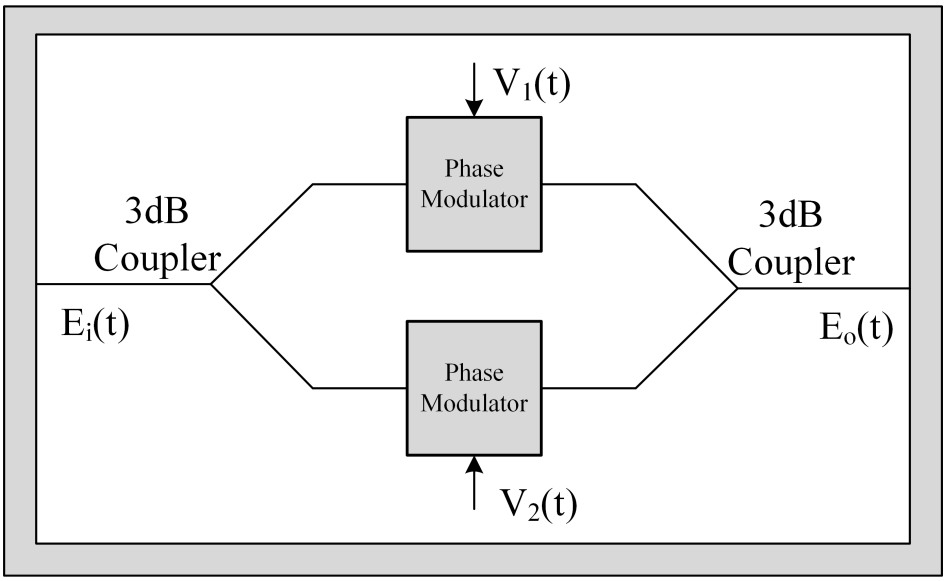


Figure 2.8: Dual-drive Mach-Zehnder modulator.

where none is implemented. When implemented, such operations serves to accommodate the signal for transmission in the fibre. The amplification makes sure that the signal has enough power to travel through the fibre and reach the receiver above the sensitive power level of the photo-diode. After amplification there's always an increase in the noise floor, to remove it and others unwanted frequencies this signal must be filtered.

There are a few ways to amplify an optical signal, but the two ways that are more important for a RoF scenario are done using an Erbium Doped Fibre Amplifier (EDFA) or a Semiconductor Optical Amplifier (SOA). The EDFA amplifier uses a laser pump as a power source, the output of this laser is combined with the signal using a coupler and then both wavelengths travel through an erbium doped fibre. A different configuration of an EDFA can have the light from the pump travelling in the opposite direction compared to the light from the signal. In this configuration the coupler is placed after the doped fibre instead of before, as was the case of the previous configuration. In both configurations the coupler does not attenuate the signal because the light from the laser pomp is in a different wave length than the light that transports the signal and so the coupler can be design to have the power from both its inputs be sent to the same output. After the coupler both wavelengths travel through an erbium doped fibre, in this fibre the pump wavelength excites electrons to an upper energy levels. As the photons from the signal pass through this doped fibre with the excited electrons, stimulated emission occurs and new photons are released. These photons have the same characteristics as the ones that triggered the stimulated emission and so the final result is an amplification of the original signal. This type of amplifier has good characteristics in terms of low distortion and low added noise, this makes then the ideal choice for high performance applications. However, they tend to be expensive and bulky due to the length of dope fibre that is necessary.

The SOA amplifier relies on the same principle of functioning as a semiconductor laser, but without the reflective coating in the chamber. In a SOA, as in a semiconductor laser, a semiconductor material has its electron population inverted by an electrical source. As the

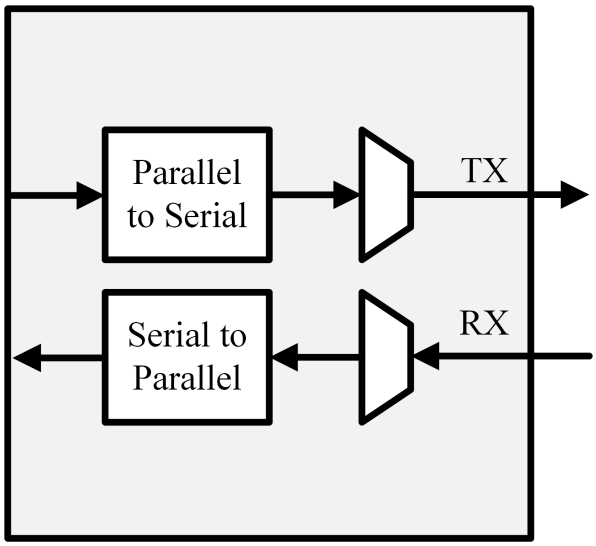


Figure 2.9: MGT's data path.

input signal travels through the chamber, stimulated emission occurs releasing new photons with the same characteristics as the ones from the input signal. Because the power source is now electrical, a SOA is much cheaper and small than an EDFA. However, SOAs tend to be more non-linear and introduce more noise. Recent developments have resolve the relative small bandwidth of SOAs when compared to an EDFA. In [29] a SOA with 100 nm of optical bandwidth is implemented and tested, achieving a data rate of 115.9 Tb/s.

2.4 Practical Considerations

In this section some concepts related to the implementation of the ADT will be reviewed. Starting with the concept of MGT, then the concept of polyphase implementation and finally the concept of EVM.

2.4.1 Multi-gigabit Transceiver

An MGT is an one-bit transceiver that can operate at frequencies higher than 1 gigabit per second. Due to its high frequency output it is normal for this blocks to incorporate both a parallel to serial converter, as well as a serial to parallel converter, as can be seen in Figure 2.9. This types of transceivers are typically arranged in groups of four transceivers called Quads. This Quads have an input clock port in order to have all MGTs being driven by the same clock source. The clock structure of an MGT's Quad can be seen in Figure 2.10.

2.4.2 Polyphase Implementation

When dealing with high sampling frequency signals it is also required to have a high clock frequency. However, there is a technique that allows for the reduction of the clock frequency, maintaining the high sampling rate. This technique is caller polyphase implementation and it is essentially a way of making the processing of the signal in a parallel way. With this type of implementation the clock of the FPGA can be reduced by a factor equal to the number of

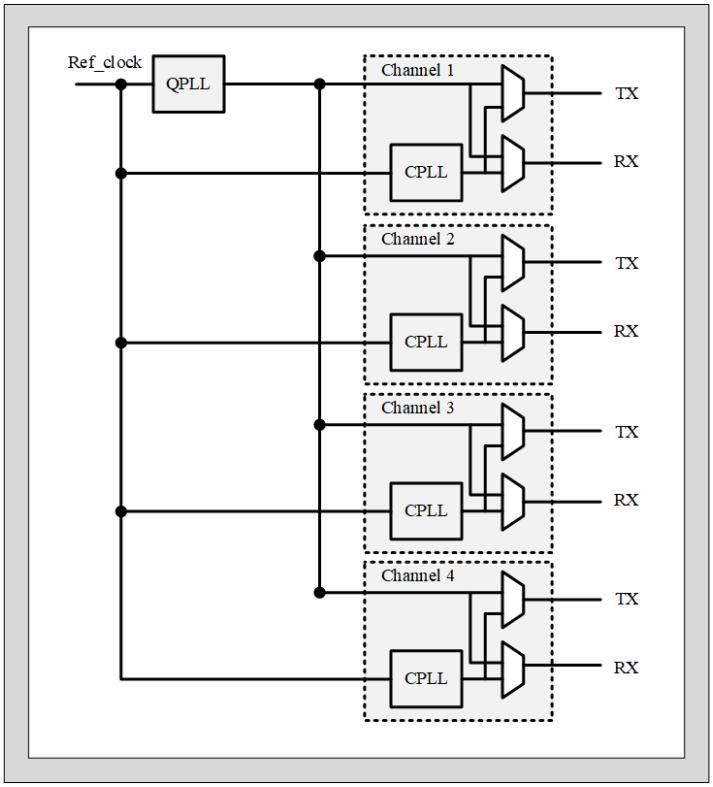


Figure 2.10: MGT's Quad's clock architecture, [30].

parallel phases used. This enabled the processing of signals with sampling frequencies in the order of GHz to be processed in FPGAs with clock running at only a few hundreds MHz.

2.4.3 Error Vector Magnitude

EVM is a way of measuring the how close is a received constellation in comparison to the ideal one. During this document, the EVM measurements will be presented in percentage. This type of EVM is calculated using the following equation:

$$EVM(\%) = \sqrt{\frac{P_{error}}{P_{ref}}} \times 100 \tag{2.13}$$

Where P_{error} is the average of the error vector power and P_{ref} is the average ideal reference vector power [31].

2.5 Final Remark

In this chapter some basic concepts were reviewed. These concepts will be the foundation of the work presented in this document, and despite not all of them being directly used in the final implementation they were crucial to the author's understanding of concepts such as ADTs and RoF.

Chapter 3

Point-to-Point Link

3.1 Concept

The general idea of this work is the development of an optical fibre point-to-point link with an all-digital transmitter based on delta sigma modulation. This link serves the function of the fronthaul in the implementation of C-RAN architectures for 5G. In order to have a successful fronthaul implementation, this link needs to be capable of receiving the IQ data from the BBU, modulate it, send it through the fibre and retrieve the original information in the other side, RRH. This completes the downlink path, the final implementation should also be capable of sending data from the RRH to the BBU. The maximum length of the fibre transmission is also important because it enables the placement of the RRHs several kilometres apart from the BBU.

A top-level block diagram of the proposed architecture for this link can be seen in the Figure 3.1. It includes two main parts, the FPGA and the optical transmission. The implementation of the transmitter and receiver was chosen to be made in an FPGA due to its reconfigurability properties, which allied with its huge processing capacity, make the FPGA a convenient platform to test and implement the proposed architecture. Inside the FPGA there are four blocks: the interface with the computer; the all-digital transmitter; the downconverter and the filter. The last two blocks constitute the receiver. In the optical transmission an electro-optical converter is used to convert the signal from the electrical domain into the optical domain. This is followed by an optical fibre which, at the end, has an opto-electrical

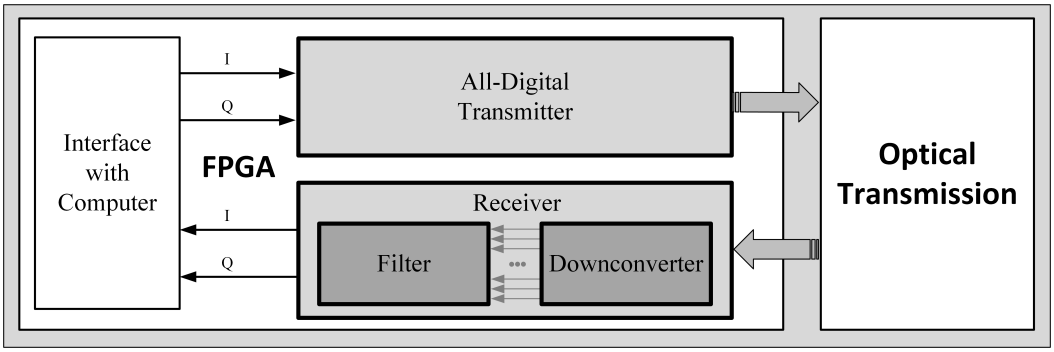


Figure 3.1: Top-level architecture of the proposed point-to-point link.

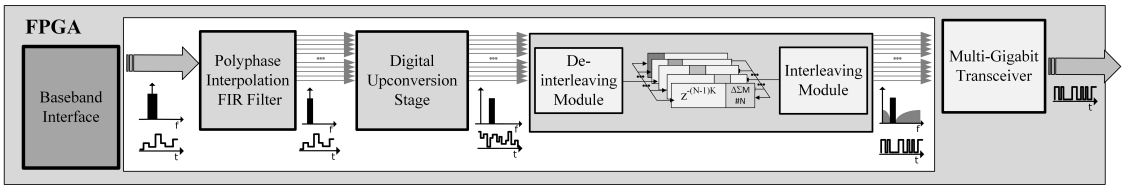


Figure 3.2: ADT's architecture.

converter to return the signal from the optical into the electrical domain in order to be sampled by the FPGA.

In the following sections a detailed description of the implementation process will be discussed, starting with the modelling and simulation part, than the hardware implementation, followed by the optical link description and finally a discussion of the results. The modelling and simulation part of this work was done using System Generator. This was really important because it allowed for a quick iteration process that wouldn't be possible otherwise. This is due to the fact that System Generator runs over Matlab, which allows for a simple and fast testing, as well as an easy visualisation of the results. Another option was to use an Hardware Description Language (HDL), however, both the implementation and testing would be more difficult and time consuming. In the hardware implementation it will be discussed the choices made to the implementation, which, due to the FPGA used in this work being a Xilinx Virtex UltraScale, was done in Vivado. In this section will also be presented a description of the method used for transmitting data to and from the FPGA. In the optical link section an analysis of the optical link's architecture will be made and some other topologies will be compared to the one that was chosen for implementation. Finally, the results obtained when testing this architecture will be presented and analysed.

3.2 Modelling and Simulation

For a more easy understanding, this section will be divided into two subsections: one devoted to the transmitter and other to the receiver. The transmitter subsection will also be divided in topics, one for each component in the transmitter and the same will be done for the receiver.

3.2.1 Transmitter

The transmitter subsection will be divided according to the blocks that constitute the transmitter: the filter, the upconverter, the de-interleaving, the $\Delta\Sigma$M core and the interleaving. A block diagram of the proposed ADT can be seen in Figure 3.2. The division of this subsection was made so that the order in which the blocks appear in the text is the same as the order that they are arranged in the ADT. The ADT used here is an RF-stage modulator, due to the fact that the upconverter block comes first than the $\Delta\Sigma$M core, used as the pulse encoder in this work.

3.2.1.1 Filter

The filter in this transmitter has two functions, interpolate the signal to the sampling frequency imposed by the MGT serialization frequency, in this case 8 GHz, and filter the

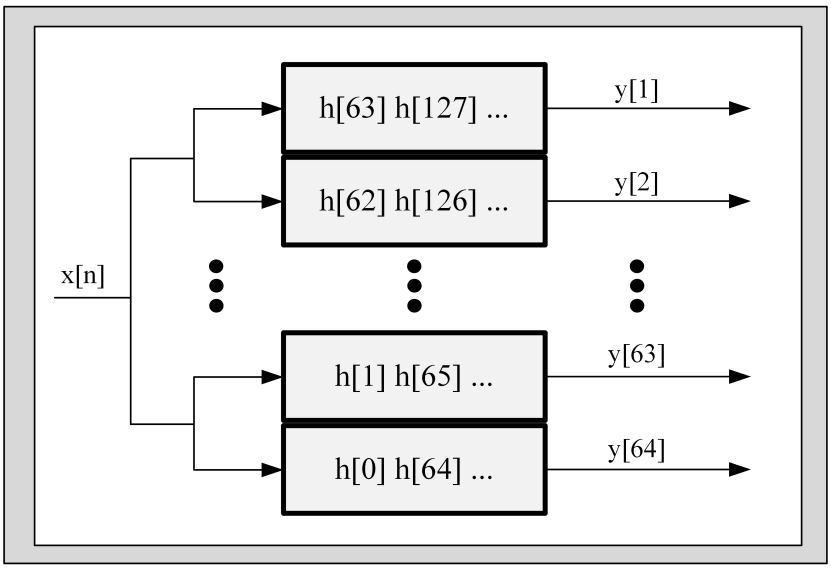


Figure 3.3: Interpolation polyphase filter.

images created by this interpolation. Due to these requirements imposed on the filter, as well as the fact that the output of the filter needs to have the same number of parallel outputs as the number of $\Delta\Sigma$M cores, the chosen architecture for the filter was the interpolation polyphase filter. The architecture for this filter can be seen in the Figure 3.3. In it, the input signal is replicated and then fed to all the smaller Finite Impulse Response (FIR) filters, which all have specific coefficients. These coefficients originate from a larger order single phase FIR filter which was previously designed to have the bandwidth equal to the clock rate of the FPGA, 125 MHz. After the design of the original FIR filter, which must have an order satisfying: $Order = n * Number\ of\ Phases - 1$, where n is a natural number, the coefficients of the original filter are distributed to the smaller filters as depicted in Figure 3.3. This rearrangement of the coefficients of the filter allows for a transformation from a single phase filter to a polyphase one. This polyphase filter has the same frequency response as the single phase with the advantage that each adder and multiplier can work at a frequency n times lower than the multipliers and adders of the single phase filter would have to work. This reduction in the working frequency is crucial to enable the implementation of such filter in an FPGA.

In the final project two filters were used, one for the in phase data (I) and other for the quadrature data (Q). The simulation results of the implemented filters can be seen in Figure 3.4. The data presented in this figure was retrieved from the System Generator using the block "To Workspace" which sends the data to the Matlab workspace. Already in Matlab the only modification done to the signals was the transformation from two real matrices into a single complex matrix followed by a reshape of the matrix into a vector, this transformation is the equivalent of a parallel to serial transformation. Referring once again to Figure 3.4, two signals are visible, one in blue, which represents the original signal given as input to the filter and other in red, which represents the output signal of the filter. Comparing both signals, an increase in the noise floor is clearly visible, but despite the perception that this increase could be a bad thing, in the end, most of it will be under the noise created by the $\Delta\Sigma$M, making the attempt to reduce it not a priority for this work. However, this increment in the noise

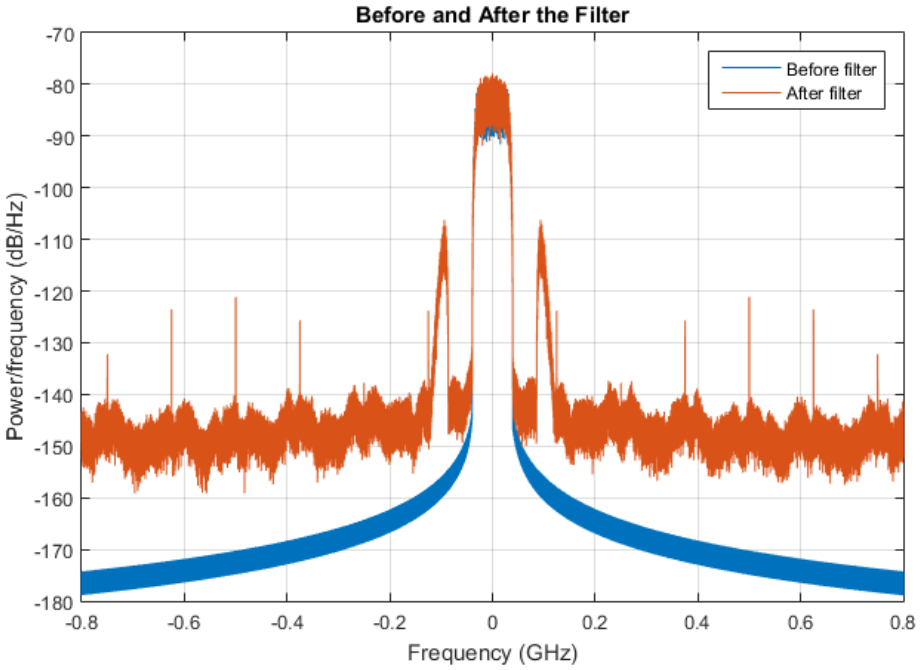


Figure 3.4: Spectrum before and after the transmitter filter.

floor does influence the performance of the ADT and its suppression could be advantageous for the accomplishment of more demanding requisites. In a closer view, it can be seen that the noise floor's increase results in a slightly decrease in SNR. A second difference between the two signals is the appearance of the two noise spikes near the pass-band. These spikes will reflect in the output, being a limiting factor in the overall performance of the ADT. Finally, a crucial difference between both signals is present in-band. This is observable by the blue stain below the red curve. This means that the filter is distorting the original signal resulting in a reduction of performance.

3.2.1.2 Upconverter

After the filtering stage, the signal is divided into two signals, I and Q, this is not ideal due to the fact that it will need twice as much resources than if it was just one signal. However, the combination of the two signals can not be done in base band due to the overlapping of frequencies. A solution to this problem is presented in the implementation of this upconverter, which is depicted in Figure 3.5. As can be seen in the figure, both I and Q signals are multiplied by a sine and a cosine wave, respectively. Then the result of the multiplications is subtracted from one another. This process is equal to the following equation:

$$U(n) = sin\left(2\pi n\frac{fc}{fs}\right)I(n) - cos\left(2\pi n\frac{fc}{fs}\right)Q(n) \tag{3.1}$$

where U is the upconverted signal, fc is the carrier frequency that the signal is being upconverted to and fs is the sampling frequency. The equation results in a real signal that contains the information of both I and Q signals.

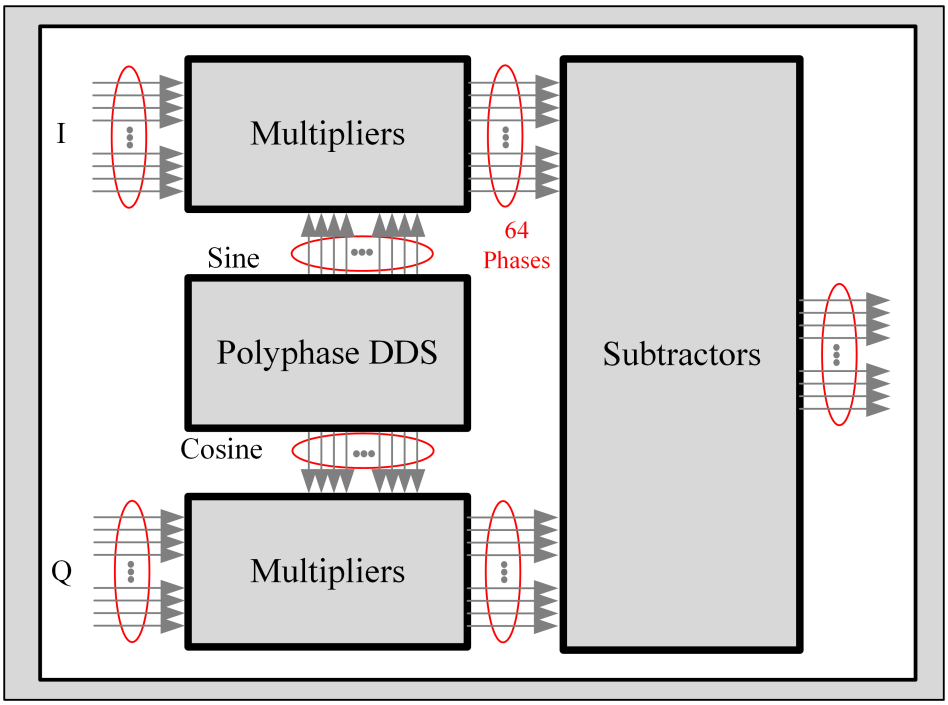


Figure 3.5: Upconverter's architecture.

The block named Polyphase DDS, in Figure 3.5, is a polyphase implementation of a Direct Digital Syntheses (DDS). This block is constituted by 64 sub-blocks each one implementing two Read Only Memories (ROMs), one for the sine and other for the cosine wave, and their respective control logic. The implementation of one of these sub-blocks can be seen in Figure 3.6. In each of the ROMs is stored a discreet version of the sine and cosine waves. The control logic makes sure that at each clock 64 consecutive phases from the sine and cosine waves are available at the output of the polyphase DDS. Then the 64 phases of the sine wave go to the multiplication block, where 64 multipliers multiply these inputs with each phase of the I input signal by the each phase of the sine wave. The same is done for the cosine phases and the Q signal.

The Polyphase DDS block also receives a value called *Step*. This value is then fed to the

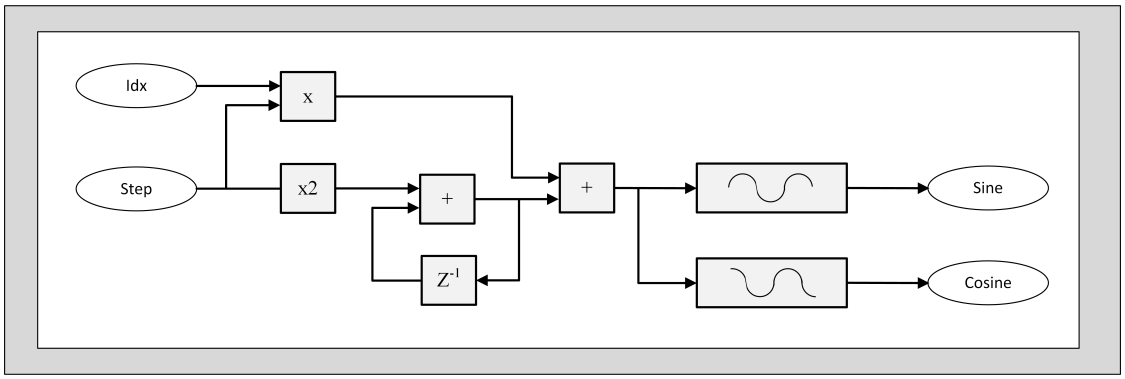


Figure 3.6: DDS ROM's implementation and control.

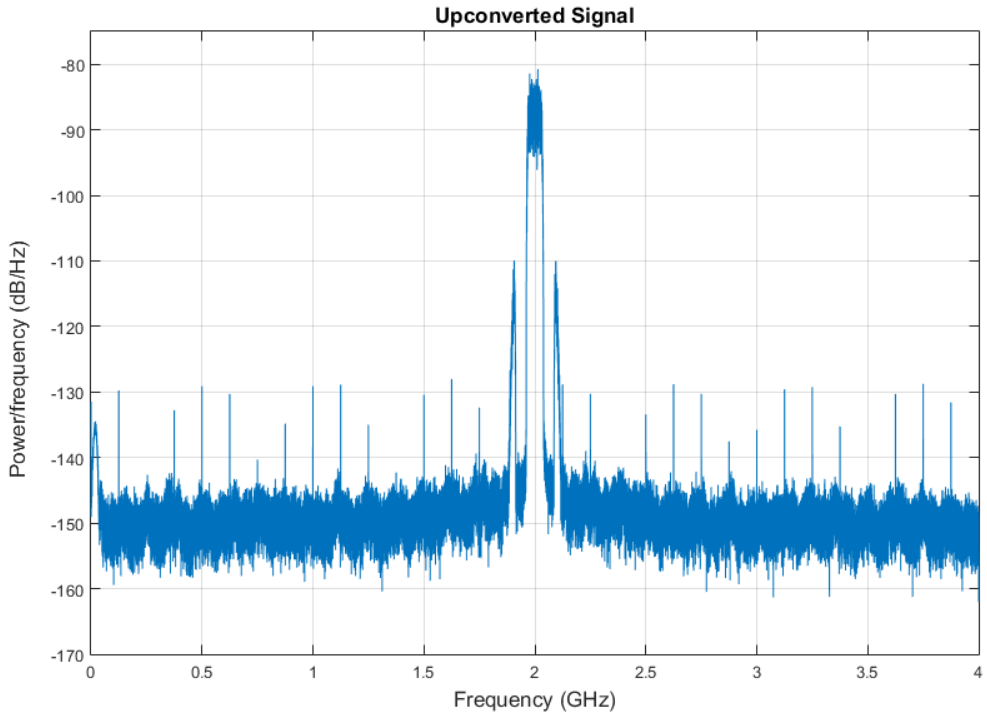


Figure 3.7: Spectrum after the upconverter.

DDS and it controls the output frequency of both sine and cosine waves. The way it can control the frequency of both waveforms is by changing the positions of the ROMs that are being read. Both the ROM that stores the cosine and the ROM that stores the sine wave just have a single period stored in them. The way in which the samples from this single period are read is that determines not only the frequency but also the 64 different phases.

The output signal's spectrum of the upconverter can be seen in Figure 3.7. Comparing this spectrum with the one in the Figure 3.4, its is apparent that they look the same, apart from the change in the frequency axis. In fact, a more careful analysis reveals only some negligible deterioration in SNR.

3.2.1.3 De-interleaving

The de-interleaving block serves a very specific function, which is rearranging the samples in order to make sure that each delta sigma core receives k continuous samples in the time domain. In the implemented case, k has the same value of the number of parallel phases, 64.

For a better understanding of the concept behind the implemented de-interleaver, an example with only two phases is presented in the Figure 3.8. In the figure each color represents a different clock cycle, from black to yellow. The implemented counter increases its output value by one every clock cycle, starting at zero and counting until the value of the number of phases minus one. In the example, the number of phases is two, so the counter goes from zero to one and then wraps around to zero and so on. This counter value is used as an input for the multiplexers and it is delayed by one clock cycle for every consecutive multiplexer. This means that the first multiplexer receives the current counter value, the second multiplexer

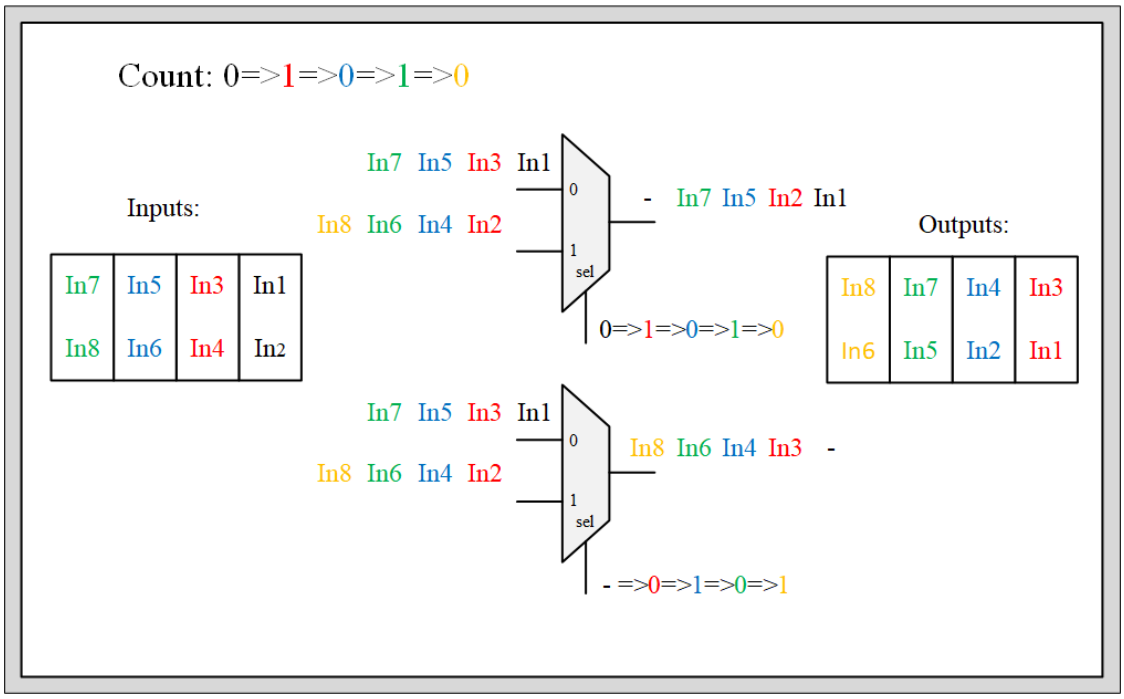


Figure 3.8: Schematic of the de-interleaver with two phases.

receives the counter value with a delay of one clock cycle and so on.

In the example, the multiplexer in the top is the first multiplexer and so its input is synchronous with the counter value, in contrast, the lower multiplexer is the second multiplexer and so it receives a delayed version of the same counter value. The input values come in parallel, which means that every clock cycle a number of samples equal to the number of phases arrives at the input of the de-interleaver. These samples are placed one in each phase and each phase is sent to each input of each multiplexer. However, not all phases are connected directly to the inputs of the multiplexers. Each phase receives a delay equal to its order number, i.e., the phase zero does not receive any delay, the phase one is delayed by one clock cycle and so on. This delay in the samples combined with the delay in the selection input of each multiplexer makes sure that each modulator outputs a number equal to the number of phases in consecutive samples intercalated by $(Number\ of\ Phases - 1) * (Number\ of\ Phases)$ skipped samples.

At this point, the output of each multiplexer already contains the k samples continuous in time. However, each output phase has a different delay. This different delay can be seen in the Figure 3.8, where the first two continuous samples in the first multiplexer are one clock ahead in comparison to the first two contiguous samples of the second multiplexer. To resolve this problem, the final part of the de-interleaver applies another delay to each phase. However, now the delay applied to each phase is equal to: $(Number\ of\ phases) - 1 - (Order\ of\ the\ phase)$. For the exemplified case, this results in the phase zero having a delay of 1 and the phase one having a delay of zero. This final transformation concludes all the required specifications for the de-interleaver, making sure that the delta-sigma core receives k samples continuous in time and each phase has no delay compared to the others.

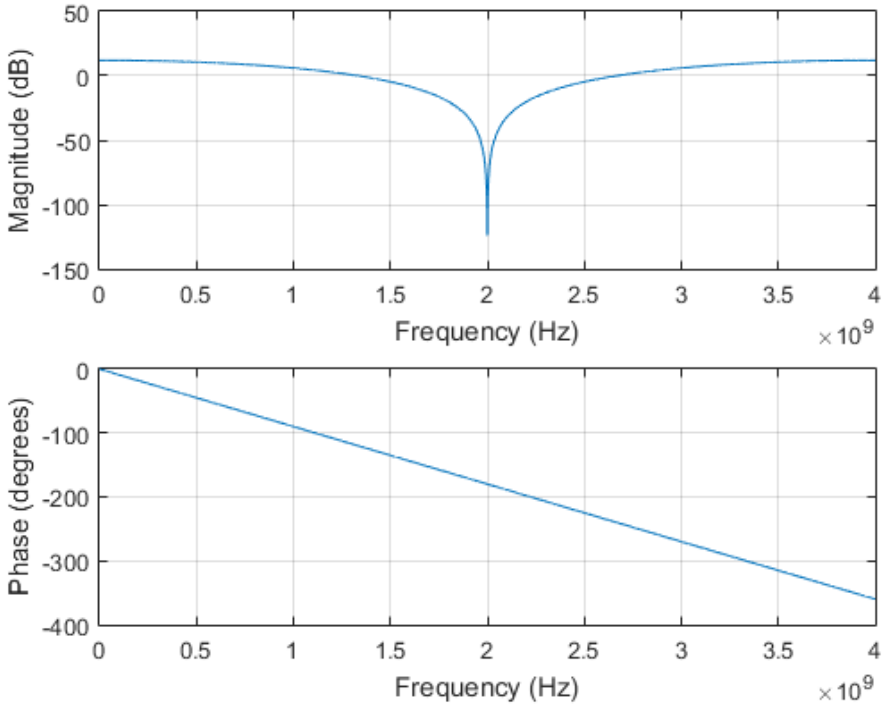


Figure 3.9: Frequency response of the NTF.

3.2.1.4 Delta-Sigma Modulation Core

The type of ΔΣM used in this work is the error feedback architecture, this architecture was described without much implementation details in subsection 2.2.2 and its block diagram can be seen in Figure 2.4 b). In this section a more careful analysis of the practical implementation will be made and some simulation results will be shown.

The choice of an error feedback structure with the filter in the feedback path was due to its simplicity and ease of implementation that combined with its short critical path make this architecture very appealing for implementation in an FPGA. The positioning of the filter in the feedback allows for a more easy determination of the STF and NTF of the modulator, this conclusion can be derived by comparing the following equations:

$$Y(z) = X(z)H(z) - E(z)(1 + H(z)) = STF(z)X(z) - NTF(z)E(z) \tag{3.2}$$

$$Y(z) = X(z) - E(z)(1 + H(z)) = STF(z)X(z) - NTF(z)E(z) \tag{3.3}$$

These two equations were first derived in chapter 2 (equations 2.6 and 2.9). Equation 3.2 describes the STF and NTF of the implementation with the filter in the feed forward, while equation 3.3 describes the STF and NTF of the implementation with the filter in the feedback. As can be concluded by analysing the equations 3.2 and 3.3, the STF of the implementation with the filter in the feedback is already equal to one and so it eliminates the problem of designing a filter that respects both the required characteristics of the STF, which is equal to $H(z)$ and also respects the target characteristics of the NTF, which is equal to $(1 + H(z))$.

The design of the filter was done offline, having always in mind the final objective: creating an NTF that rejects the noise in the 2 GHz band. In the creation of the filter, the first step was the development of a reject band filter with the characteristics wanted for the NTF. Than having this filter, which is equal to the final NTF, the filter to implement in the ΔΣM core would be found through the equation:

$$H(z) = NTF(z) - 1 \tag{3.4}$$

The creation of the filter for the NTF started with this generic filter equation:

$$H_{tmp}(z) = \frac{\left(z^2 + \alpha z + 1\right)^2}{\left(z^2 + \alpha R z + R^2\right)^2} \tag{3.5}$$

where R determines the position of the poles, relative to the zeros and α determines the position of the notch of the filter, which is related to the position of the zeros. The value of α can be calculated by: $\alpha = -2cos(2\pi fc/fs)$, where fc is the center frequency of the notch and fs is the sampling rate. For the proposed case $fc = 2\ GHz$ and $fs = 8\ GHz$. Substituting the values of fc and fs in the equation for the α results in:

$$\alpha = -2cos\left(2\pi\frac{2 * 10^9}{8 * 10^9}\right) = -2cos\left(\pi\frac{1}{2}\right) = 0 \tag{3.6}$$

with the value of α already determined, the only remaining unknown variable is R. From equation 3.5, it is possible to see that with $R = 0$ the filter H_{tmp} can be transformed from an Infinite Impulse Response (IIR) filter into a FIR filter and so the value chosen for R was zero. Finally, making the substitution of both α and R in equation 3.5 gives:

$$H_{tmp}(z) = \frac{\left(z^2 + 1\right)^2}{z^4} = \frac{z^4 + 2z^2 + 1}{z^4} \tag{3.7}$$

dividing both the numerator and the denominator by z^4 gives:

$$NTF(z) = 1 + 2z^{-2} + z^{-4} \tag{3.8}$$

With the NTF already calculated, a validation using the $freqz$ command in Matlab was made. The result of this verification can be seen in Figure 3.9 where the required notch in the 2 GHz band is present. With the verification that the NTF is well calculated, the final H filter can be derived from equation 3.4, resulting in the final filter:

$$H(z) = 2z^{-2} + z^{-4} \tag{3.9}$$

With the filter already calculated, the architecture of one block of the ΔΣM core is completed and so the next step is the replication of this core, 64 times. Some adjustment of the delays prior to each core are needed to ensure that the final state of one ΔΣM core can be passed to the next. These delays were implemented as depicted in Figure 3.10, as can be seen, each ΔΣM core received its input data with a delay that respects the following equation: $N \times k$, where N represents the order of the core, i.e., the first ΔΣM core has $N = 0$, the second core has $N = 1$ and so on, the k represents the number of consecutive samples continuous in the time domain given by the de-interleaver.

If the states were not passed from one core to the next, a noise spike every k samples would be present in the time domain. The final state propagation of each modulator consists

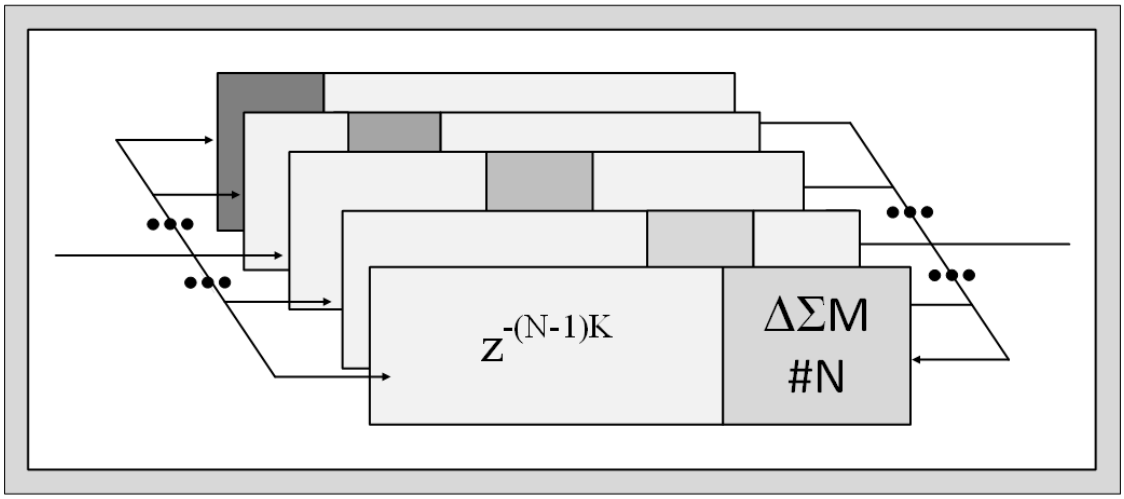


Figure 3.10: ΔΣM core implementation, figure from [14] .

in sending the values saved by each delay of the FIR filter. These are the values that have to be initiated at the beginning of every set of new samples. However, not all of these noise spikes can be eliminated, this is due to the fact that the state of the last core can not be passed to the first core. This happens because, when the last core ends the processing of the first set of samples, the first core has already processed the second set of samples, in fact it has processed a $Number\ of\ phases$ sets of samples at that time. This impossibility results in a noise spike every ($k \times Number\ of\ phases$) samples, which is a good improvement when compared to having a noise spike every k samples. The technique presented here is called state propagation and was firstly introduced in [14].

The delays added after the ΔΣM core have the function of synchronise the phases so that they can go to the interleaver block. The value of each delay was calculated by: $k \times (Number\ of\ phases - N + 1)$. After this operation the samples are once again arranged in blocks of k samples, as depicted in the Inputs in the Figure 3.11.

3.2.1.5 Interleaving

The interleaver block performs the exact opposite operation as the de-interleaver, i.e., the interleaver is the block responsible for taking the samples that are arrange in k samples continuous in time in each phase and rearrange them so that the k samples have their continuity in the different phases.

Once again for a more easy understanding, a two phase version of the interleaver used in this work is presented in Figure 3.11. In the figure, it is visible four boxes with the inputs, where samples 1 and 2 arrive in different clock cycles, but in the same phase, and samples 1 and 3 as well as 2 and 4 arrive in the same clock, but in different phases. At each clock cycle, the parallel samples are passed to the inputs of all multiplexes and, as it was described for the de-interleaver, the sample of the phase zero has no delay and the sample of the phase one has a delay of one clock cycle. In the full implementation the delays will continue to rise one clock cycle for every consecutive phase. This delay is visible in the figure, where samples 1 and 3 reach the interleaver at the same time, but enter the multiplexer in a different clock cycle.

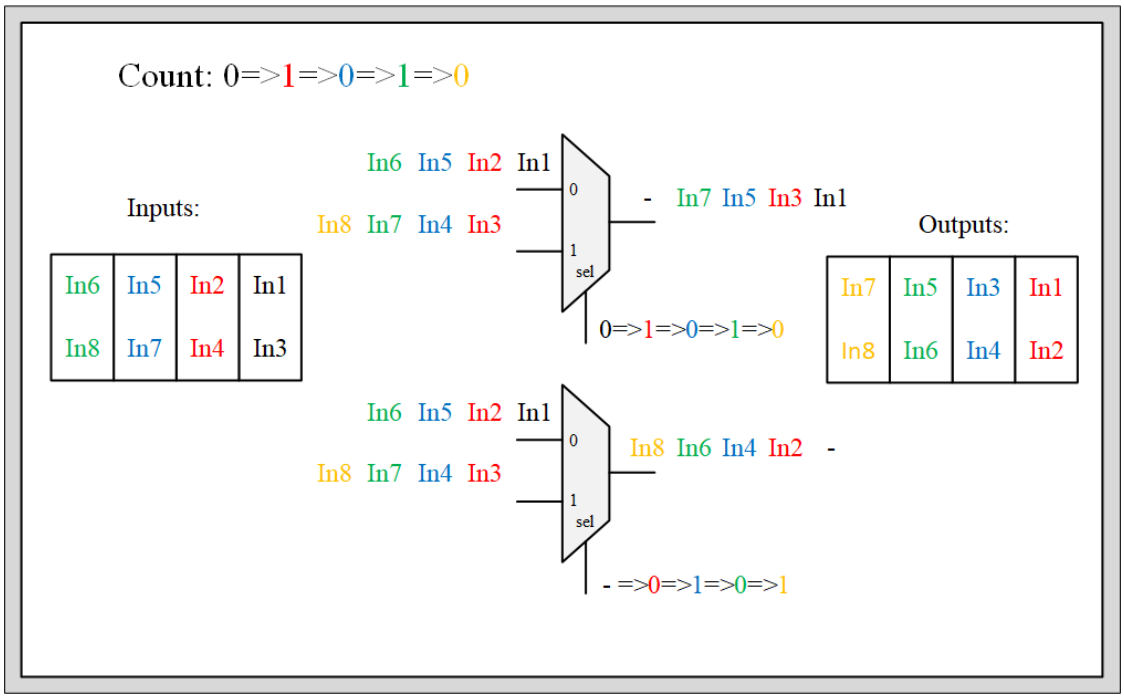


Figure 3.11: Schematic of the interleaver with two phases.

The counter that drives the selection signal for the multiplexers behaves in the same way as it was explained in the de-interleaver section, i.e., it counts from zero to a value equal to the number of phases minus one and then wraps around to zero. Once again, in the depicted case, the counter goes from zero to one, returns to zero and so on. The signal from this counter is then connected to every multiplexer to select the input that is forwarded to the output. However, the signal does not reach all multiplexer at the same time. The signal is delayed by one clock cycle in each consecutive multiplexer. In the example, the multiplexer in the top of the figure is the first multiplexer, so it receives a synchronous version of the counter. In the other hand, the multiplexer in the bottom of the figure is the second multiplexer and so the signal it receives is a delayed version of this counter. The conjunction of the delay imposed on the inputs of the multiplexes with the delay of the counter signal creates a wave like pattern. This counter signal acts as the selection signal of the multiplexers. Each multiplexer outputs a sample that came first from the phase zero, then in the second clock cycle the output sample comes from the phase one and in the third clock cycle the sample comes again from phase zero and so on. This pattern guarantees that at the output of each multiplexer the samples are spaced with a gap equal to the number of phases. Due to the example having two phases, the samples at the output of each multiplexer display the pattern: 1,3,5,7... at the first multiplexer and the pattern: 2,4,6,8... at the second multiplexer.

The only operation that is missing at this point is aligning the phases. Once again this operation is merely a delay in each phase, where phase zero has a delay equal to the number of phases minus one, phase one has a delay equal to the number of phases minus two and so on. In the example, phase zero has a delay of one clock cycle and phase one does not have a delay. After this operation the samples are once again in parallel and they are ready to be sent to the MGT for serialization and transmission.

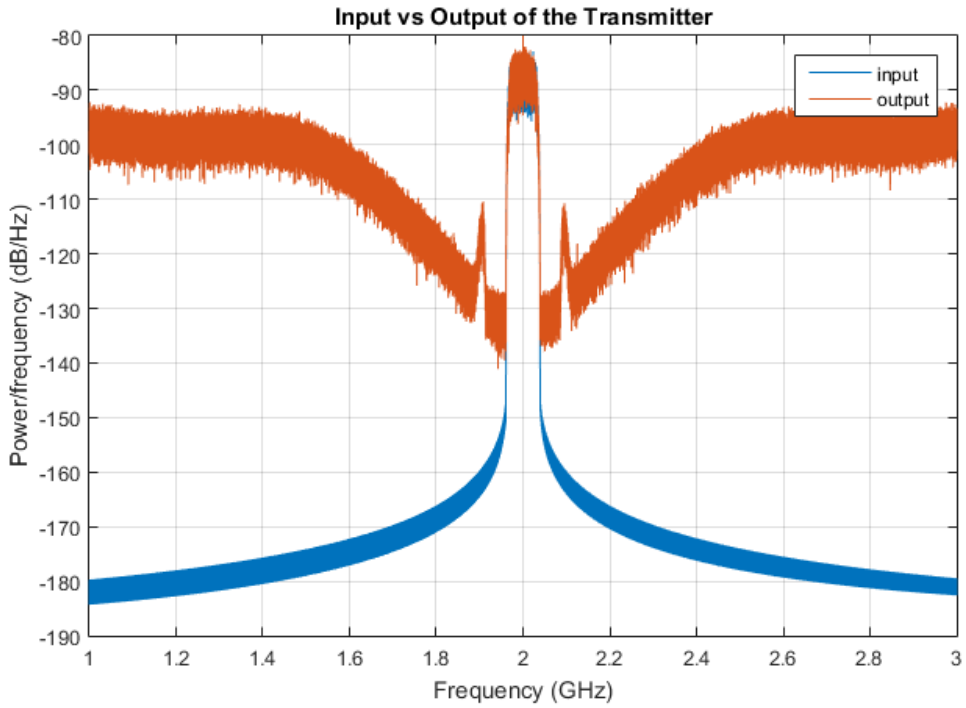


Figure 3.12: Comparison between the input and output spectrum in the transmitter.

3.2.1.6 Transmitter Simulation Results

For a final analysis of the performance of the transmitter an in-depth comparison between the input and output signals of the transmitter will be made. This comparison is key in the determination of how much distortion the $\Delta\Sigma$M, the filter, the upconverter and all other blocks that constitute the transmitter introduce in the output signal. Figure 3.12 represents both the input and output spectra of the transmitter. In blue it is depicted the input spectrum and as can be seen, this signal has a high SNR, of about 60 dB. The input signal was shifted in frequency in order for the signal to be in the same frequency as the output signal, this operation was done in Matlab at the time of figure's creation. In red it is depicted the output spectrum, in this signal it is clear a reduction in SNR, with this parameter being reduced to just less 50 dB. Other signal degradations can also be seen in the figure. One of those degradations can almost pass unnoticed, however, a careful look to the 2 GHz region reveals an in band distortion with peaks of 1 or 2 dB. This distortion is represented in the figure by the little bit of blue that is visible underneath the red portion of the signal. Finally the most clear difference between the two signals is the added noise present in the output signal. This added noise has the consequence of rising the noise floor which decreases the SNR, as well as, it hinders the filtering of the signal in the analogue domain.

All the signal deformations that were analysed in the previous paragraph have a measurable impact in the overall performance of the transmitter. Another way of analysing the signal degradation is recurring to the plot of the constellation and also to the determination of the EVM.

The Figure 3.13 shows a graphical representation of the constellation of the input signal.

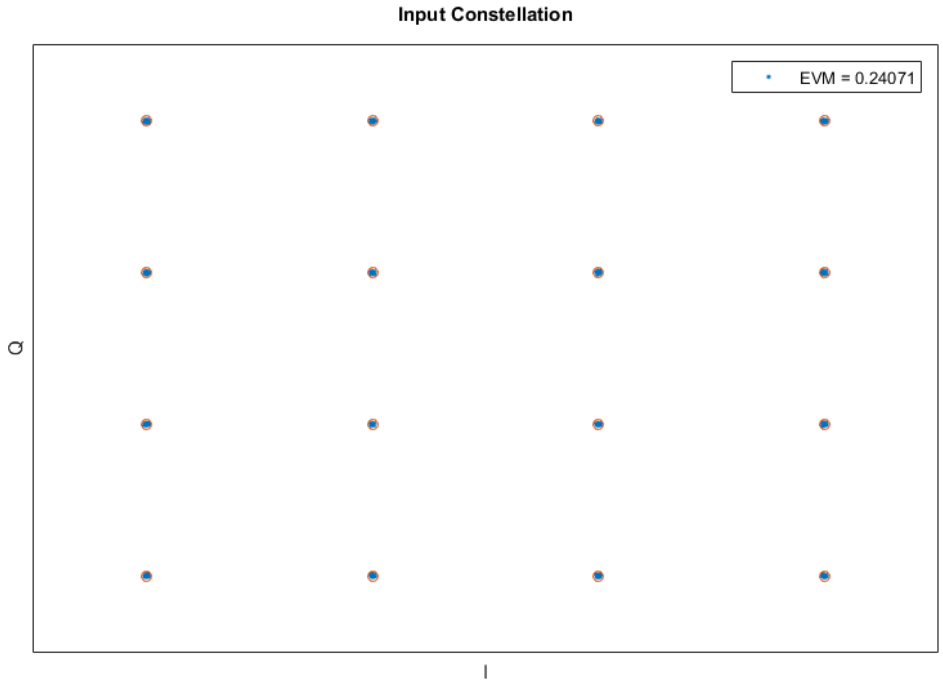


Figure 3.13: Input constellation with EVM measurement.

The obtained EVM has a value of 0.24%, this means that the obtained constellation is very well defined and close to the ideal constellation. Focusing now on Figure 3.14, the signal degradation is clearly visible by the dispersion presented in the points of the constellation. This increase in dispersion is also reflected in the worst EVM value that was obtained, when compared to the one from Figure 3.13. In the end, the EVM measured was 0.92%. With this value a more quantitative assessment of the total degradation introduced in the signal by the transmitter can obtained. In the end, despite the fact that the final EVM is still low, the truth is that this value was tripled when compared to the value obtained for the input signal.

Despite the final result pointing to a EVM of 0.92% in the output signal. This is merely a simulation value and the practical value is expected to be higher, in part by some imperfections in the FPGA's transmitter and others introduced by the oscilloscope used to obtain the signal.

3.2.2 Receiver

As it was done for the case of the transmitter, the receiver section will also be divided into subsections, one for the filter and other for the downconverter.

3.2.2.1 Downconverter

In the receiver's architecture the first block in the signals path is the downconverter, only then the signal goes to the filter. This configuration allows for the use of a simple low pass filter configuration instead of a band pass filter. However, this simplification of the filter block comes at the cost of an increase difficulty in the implementation of the downconverter. One of the biggest challenges is the design of a polyphase DDS. However, this block could be reused

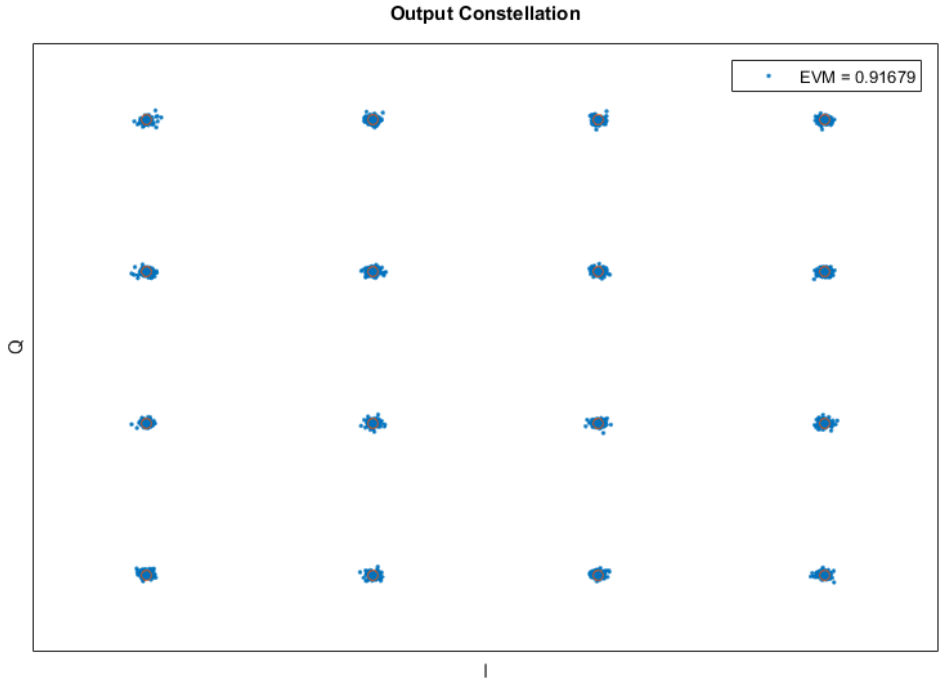


Figure 3.14: Transmitter's output constellation with EVM measurement.

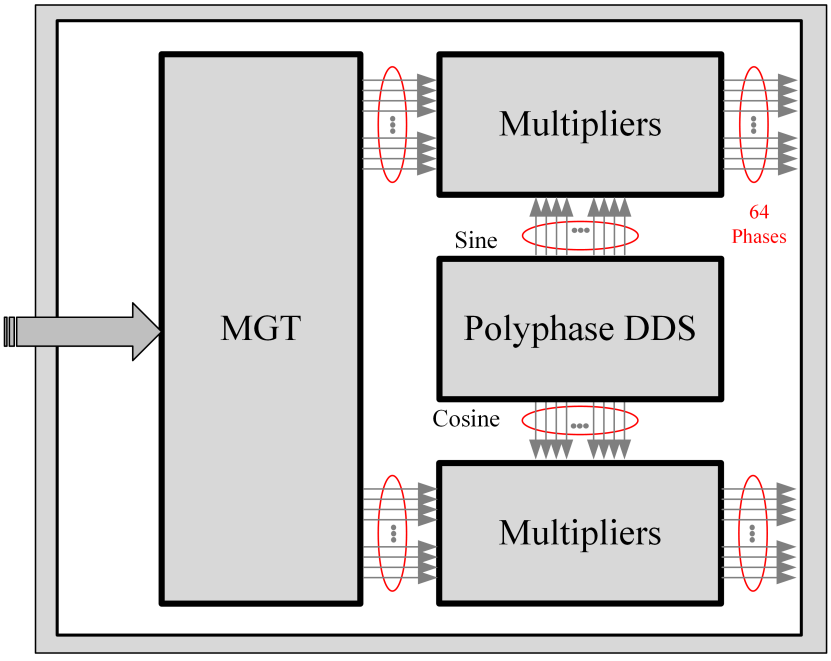


Figure 3.15: MGT and downconverter architecture.

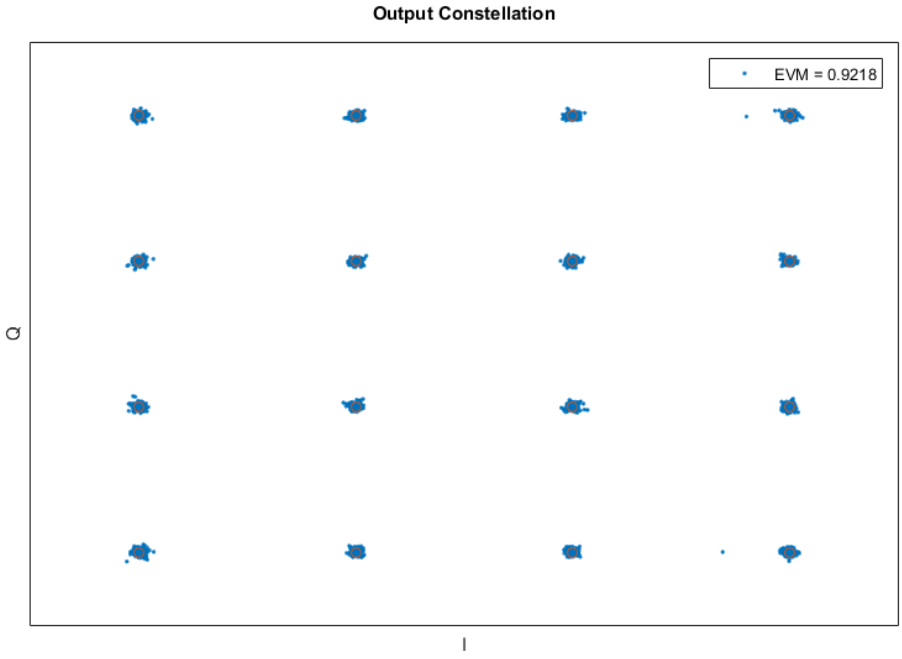


Figure 3.16: Downconverter output constellation with EVM measurement.

from the transmitter's upconverter. This arrangement also as the advantage of being able to simplify the multiplication part of the receiver, as it will be explained later.

The polyphase DDS implemented for the downconverter used the same architecture as the one used for the upconverter, with 64 sets of two ROMs. Each ROM was pre-filed with the values of a cosine or sine function. Once again this architecture provided 64 different and consecutive phases of both the sine and cosine functions to be available at the output of the DDS in each clock cycle.

At the output of the MGT, the samples are just digital zeros and ones, so in the multipliers an optimisation can be made by switching each multiplication block for a multiplexer. Each multiplexer would receive one of the 64 phases of the received signal and use it as a selection signal between the two other inputs. Those two other inputs are a zero constant for the input zero and the value from the DDS for the input one.

A block diagram of the downconverter can be seen in Figure 3.15. Starting from the left of the image. The MGT block receives samples at a sample rate of 8 Gsamples per second (Gsps) in a single phase. Then it divides then into 64 phases, each one with a sample rate of 125 Msamples per second (Msps), and forwards these 64 phases towards both multiplication blocks. The samples that go into the top multiplier are the same as the ones that go to the bottom multiplier. After this point begins the downconverter itself and, as it was already explained, it is constituted of two multiplication blocks and a poliphase DDS block.

3.2.2.2 Filter

The filter in the receiver has two main purposes, filtering the out of band noise present in the signal that comes from the transmitter and decimate in order to pass the signal from

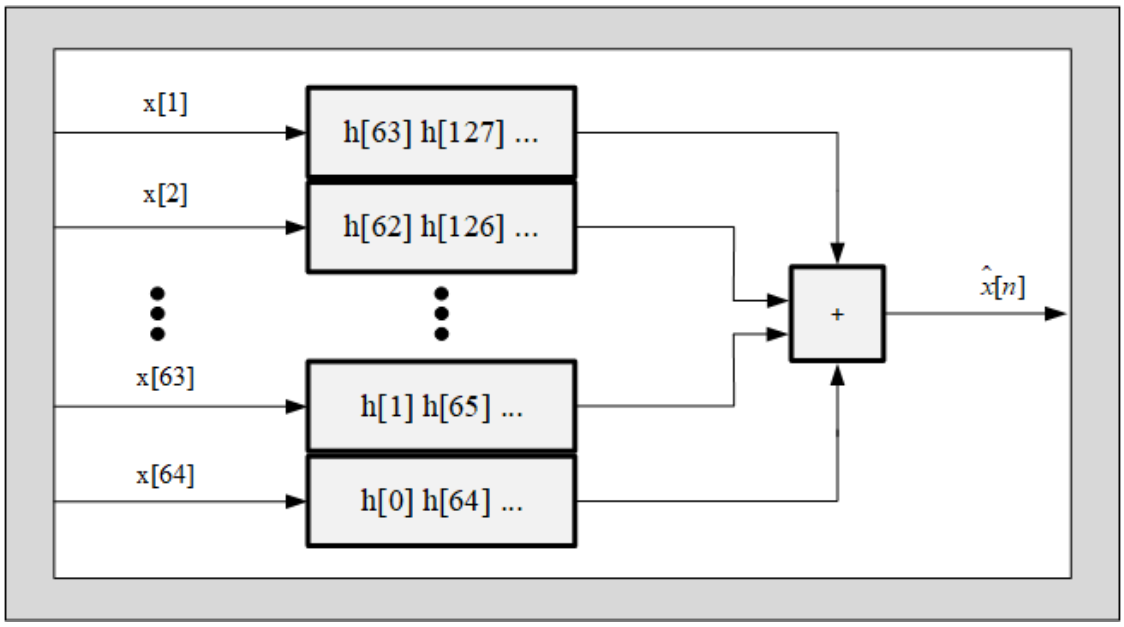


Figure 3.17: Decimation polyphase filter.

a polyphase representation into a single phase representation. In order to achieve both goals in a simple manner, a decimation polyphase filter was implemented.

A block diagram of the implemented filter can be seen in Figure 3.17. In the left side of the picture the input of the signal is represented by the signal $x[n]$. In each clock cycle k samples reach the input of the filter, where k is equal to the number of phases. Then the samples are passed to the k smaller FIR filters. These smaller filters have their coefficients derived from a high order single phase FIR filter which was previously designed to have a bandwidth equal to the bandwidth of a single phase, which is also equal to the clock rate of the FPGA. As can be seen in the figure, the way of rearranging the coefficients from the original filter to the smaller filters consists in giving the first coefficient, $h[0]$, to the first smaller filter and then the next coefficient, $h[1]$, to the next filter. This is repeated until the coefficient $h[k-1]$, where again k is equal to the number of phases. After the coefficient $h[k-1]$ is reached, the process circles back to the first filter and the coefficient $h[k]$ is given to it. The process of giving consecutive coefficients to consecutive filter is repeated until once again the coefficient $h[2*k-1]$ is reached and another cycle may start. From this way of rearranging the coefficients it is clear that for a maximum efficiency of the overall decimation polyphase filter the original single phase filter should have an order equal to $n*k-1$, where n is a natural number. If this condition is fulfilled, the single phase filter will have $n*k$ coefficients and so each smaller filter will have order $n-1$.

After the signal has passed through the filters all phases are summed up into a single phase. This operation was implemented using the two port adder provided by Xilinx and so it required a total of 63 blocks. The number of bits used in each adder was determined by experimentation until the level of signal degradation was negligible or the level of improvement gained by adding resolution to the adders was imperceptible.

Comparing Figure 3.18 with Figure 3.16 it is possible to see that the filter introduced some noise into the constellation. This noise also caused the deterioration of the EVM when

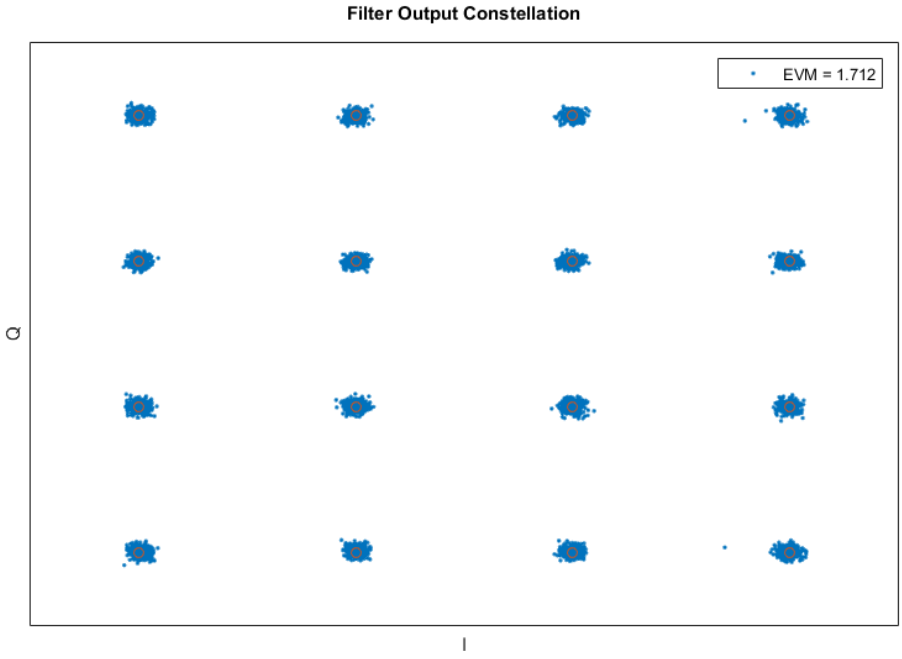


Figure 3.18: Output constellation from the filter.

compared to the output of the downconversion. In the end, the total EVM almost doubled. This could rise some problems in the practical implementation where the noise coming from the output of the transmitter is already high.

3.3 Hardware Implementation

In order to create the FPGA's hardware implementation, the Vivado software from Xilinx was used. This software allows for the integration of custom IP blocks with already provided IP blocks from Xilinx. This flexibility in the type of blocks that can be used combined with the variety of provided blocks from Xilinx, made the process of implementing the hardware much easier. For the FPGA kit, one from Xilinx was used, the VCU1283, Figure 3.19. This FPGA kit is an engineering sample and so its not documented in the Xilinx website, however, the reader can look for the VCU1287 that is similar.

With the simulation process done, two custom blocks were created in System Generator. The System Generator tool allows for the creation of IPs that can then be integrated in Vivado's block design environment and so this is what was done in order to create the transmitter and receiver blocks. These blocks were then imported to Vivado and the process of implementing the hardware begun. The confidence that these blocks would work as they were supposed was high because the simulation was already carried out using Vivado's blocks and so an IP could be generated directly from the same implementation that was used in the simulation.

As can be seen in the Figure 3.20, the transmitter and receiver blocks are connected to the microprocessor. This microprocessor serves several functions, like giving the reset

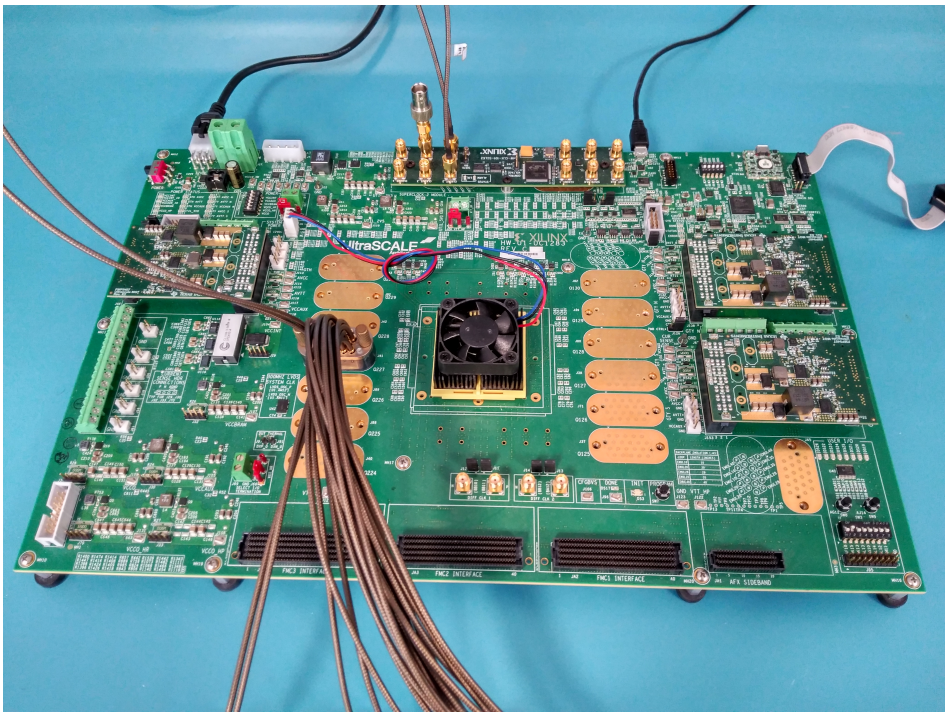


Figure 3.19: FPGA kit used in this implementation, Xilinx VCU1283.

commands to all registers in the transmitter and giving the value of the *Step* needed for both the upconversion and downconversion's DDS. For sending the *Step* value, a custom IP was used that enabled the microprocessor to write in a register that then could be accessed by both the transmitter and receiver blocks. A code to run in the microprocessor was used in order to communicate with the UART and received the value through a serial port. This value was calculated in Matlab and sent to the microprocessor using again the same serial port.

The MGT hardware was done using the UltraScale FPGAs Transceiver Wizard. In this tool the general configurations like the line rate, the reference clock frequency and some optional signals and buffer were specified. Also in this tool, it is possible to chose the Quad in which to implement the MGT. The Quad is the name given to a group of four MGTs which are placed together. It is also possible to choose the QPLL to be used and the clock which drives the QPLL, where QPLL means Quad phase lock loop. Some other configurations are possible and the author already has plans to test if some of them could improve the performance, mostly of the receiver.

For the transmitter path the MGT works as a parallel to serial converter, in the implemented case, the MGT takes the 64 phases, which have a bit rate of 125 Mbit/s and that are the output of the transmitter block, and outputs a single signal with a bit rate 64 times higher, in this case 8 Gbit/s.

In the receiver path, the MGT does the opposite function and acts as a serial to parallel converter. The output of the MGT are the 64 phases with a bit rate of 125 Mbit/s. These phases are then all connected to the receiver block in order to recover the original signal.

Due to the high data rate in the output of the receiver block it is not possible to send the data directly through USB to a PC. A solution based on the Integrated Logic Analyser (ILA)

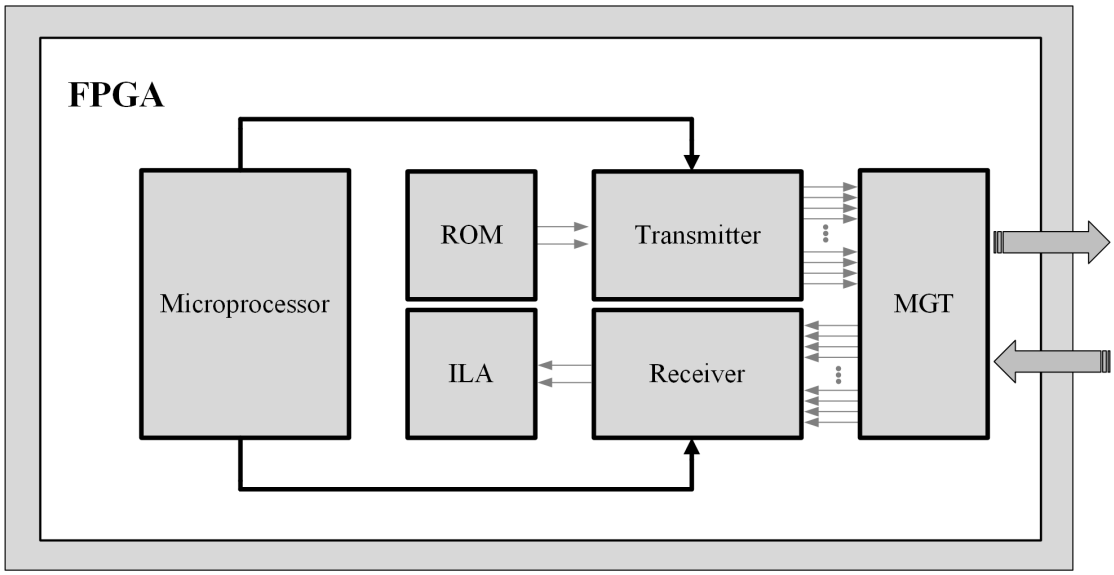


Figure 3.20: Top-level view of the hardware implementation.

Table 3.1: Utilization values of the FPGA.

Resources	Utilization	Available	Utilization %
FF	61690	1075200	5.74
LUT	153415	537600	28.54
Memory LUT	49489	76800	64.44
I/O	11	832	1.32
BRAM	265.5	1728	15.36
DSP48	768	768	100.00
BUFG	11	960	1.15
MMCM	1	16	6.25
GT	2	65	3.08

block from Xilinx was implemented. This block allows for the temporary storage of the data coming from the receiver block and then also allows for the retrieval of that data through USB.

In Table 3.1, the values of the resources used by this implementation can be seen.

3.4 Optical Link

The first idea for the implementation of the optical link was to use a SFP+ with a wavelength of 1550 nm and a supported bit rate of at least 8 Gbit/s. This SFP would allow for the achievement of both a simple and inexpensive solution, while providing a relative long transmittion range. However, due to laboratory limitation there were no SFP that could fulfil all requirements. The SFP that could fulfil the most important requirement, the line rate, was the one depicted in Figure 3.21. This SFP is a Finisar FTLX8571D3BCV, with a line rate of up to 10.3 Gbit/s and a wavelength of 850 nm. This wavelength has a disadvantage

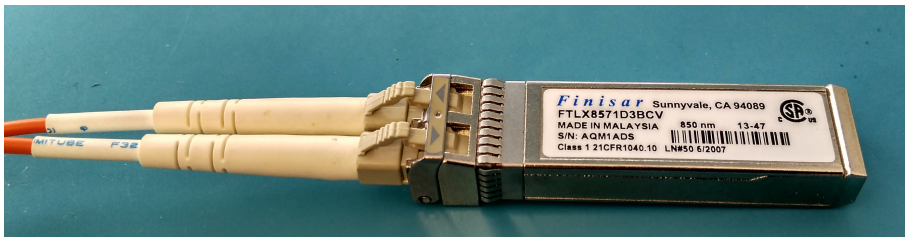


Figure 3.21: Image of the SFP+ used.

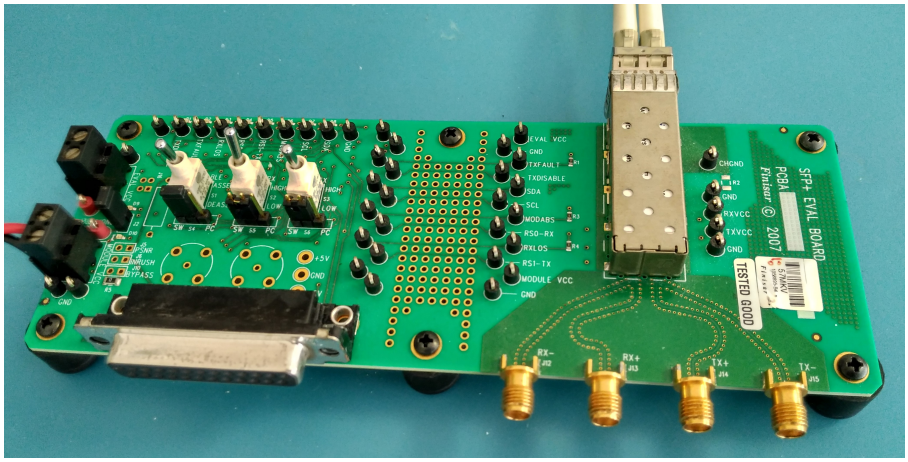


Figure 3.22: Evaluation board used for the housing of the SFP.

---

in the small total distance that can be achieved by the optical link, in the case of this SFP the manufacturer specifies a maximum of 400 m [32]. Just to have a term of comparison, a SFP from the same company, but with a wavelength of 1550 nm has a maximum link length of 40 km [33].

In order to power the SFP, as well as, connect it to the input and output of the FPGA's MGT, an SFP+ Eval Board from Finisar was used. This board presented a slot for the SFP and four SMA connectors to link with the FPGA. A photograph of the board can be seen in Figure 3.22, where in the top right conner is visible the housing for the SFP with the SFP plugged in and in the bottom right conner of the board are visible the four SMA connectors. All four connectors were used, two for connecting with the FPGA's transmitter and the other two for connecting with the receiver. The FPGA's transmitter cables were connected with the Tx ports, where the P cable from the FPGA was connected to the Tx+ and the N cable to the Tx-. The same was done for the receiver, where the P cable was connected to Rx+ and the N cable to the Rx-. Prior to the initialisation of the setup, a multi-mode optical fibre was connected to the SFP in a loopback configuration. A depiction of the final implementation can be seen in Figure 3.23. Finally, the board was powered using a DC voltage of 3.3 V.

With the optical link operational, the measurements began. The next section presents and analysis the measurements done in four different points of the proposed architecture.

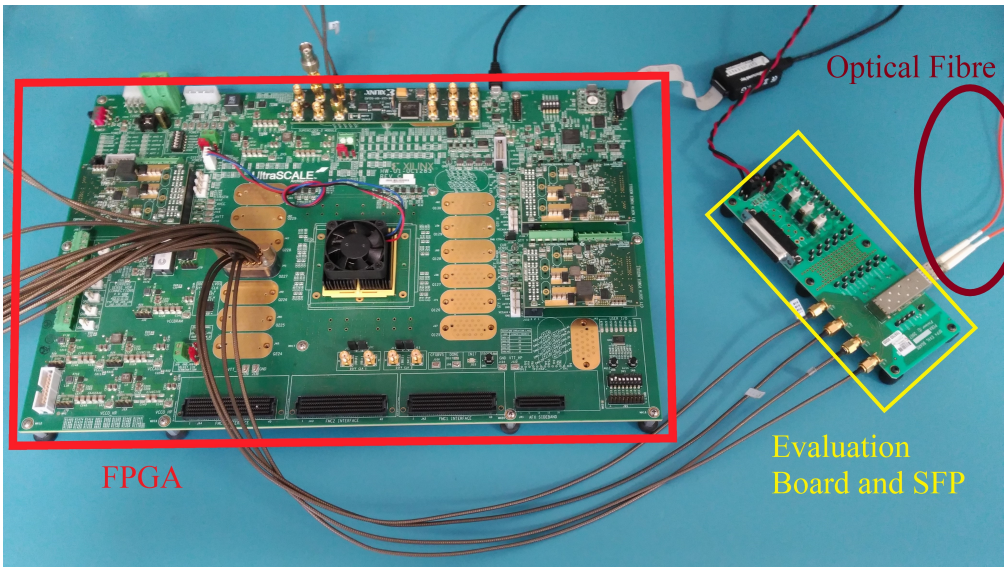


Figure 3.23: Experimental setup with the FPGA (red square), evaluation board and SPF+ (yellow square), and optical fibre (brown circle).

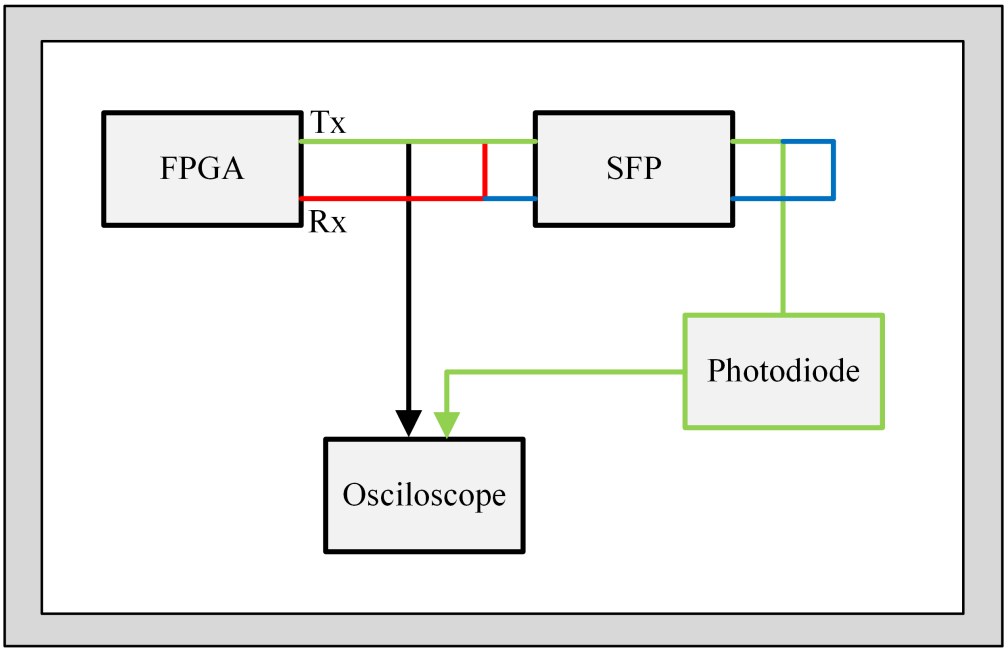


Figure 3.24: Block diagram of the four measurement points: in black, electrical transmission, in red, electrical back-to-back, in green, optical transmission and in blue, the point-to-point link with optical transmission.

3.5 Measurements

From the simulation, a high level of trust in both transmitter and receiver blocks was achieved, however, problems in the interconnection with other FPGA blocks could result in unexpected behaviours. Another problem that was already noticed in the simulation was the high level of noise introduced by the receiver block. In the simulation, this noise was so high that it almost doubled the EVM. This increase in EVM could be even worse in the practical implementation due to the already high noise and also due phase shifts and or delays present in the received signal.

A block that could decrease the performance of the overall system and that was not simulated is the MGT, specially when working as a receiver. Tests prior to this work were done using the MGT in loopback mode. Those tests consists in sending a stream of ones and zeros in an alternating pattern and, after its reception in the MGT with an ILA block, the received pattern was compared with the original one. In the end, no errors could be found. However, the signal was not representative of the real signal to be transmitted in the final work and potential problems with delays and phase shifts caused by the fibre transmission were not covered by those tests.

In this work, the most important parameter to be measure is the total amount of distortion and noise introduced by the link in the signal. In the end, this is the only measurement that determines how good the final link actually is. However, having intermediate measurement may reveal useful information, such as where the distortion is being introduced and how to reduce such distortion. That was the thinking at the time of deciding the type of measurements to be done in this work. Finally, it was settle that four measurement points would be done. The block diagram that represents the experimental setup with the four measuring points can be seen in Figure 3.24.

The fist measure would be at the output of the FPGA's transmitter and would be done using a high frequency oscilloscope from Tektronix, (DPO77002SX). This oscilloscope was chosen because it can sample signals up to 70 GHz and also because it was already used. This measurement point was chosen in order to provide a baseline of the transmitter performance that could than be compared with the final link's performance.

The second measurement would be an electrical loopback test, where the transmitter and receiver from the FPGA would be directly connected and the signal would then be retrieved from the FPGA using the same method as in the final link, i.e., using an ILA block. This measurement would allow for the distinction between the added noise in the optical link and the added noise in the FPGA's receiver.

The third measurement point would be at the end of the fibre transmission and would be done using the same oscilloscope as in the first measurement point. This is an important measurement for determining the performance of the optical part of the work. In the end, the EVM measured at the end of the optical transmission, when the fibre length is small, can not be much higher than the initial EVM at the output of the FPGA.

The final measurement point and also the most important is the evaluation of the overall performance of the link. In this measure, the signal is sent from the FPGA to the SFP, which then converts the electrical signal into the optical domain. The signal travels then through the fibre and returns to the SFP once again. This time the SFP is used as an opto-electrical converter that turns the optical signal back into the electrical domain. After that the signal is redirected to the FPGA's receiver which performs the filtering and downconversion. Then, the signal is retrieved from the FPGA using the ILA block.

Table 3.2: EVM Results obtained at the FPGA's output for both 16- and 64-QAM cases.

EVM (%) 16-QAM	EVM (%) 64-QAM
1.0993	1.1917
1.1991	1.1439

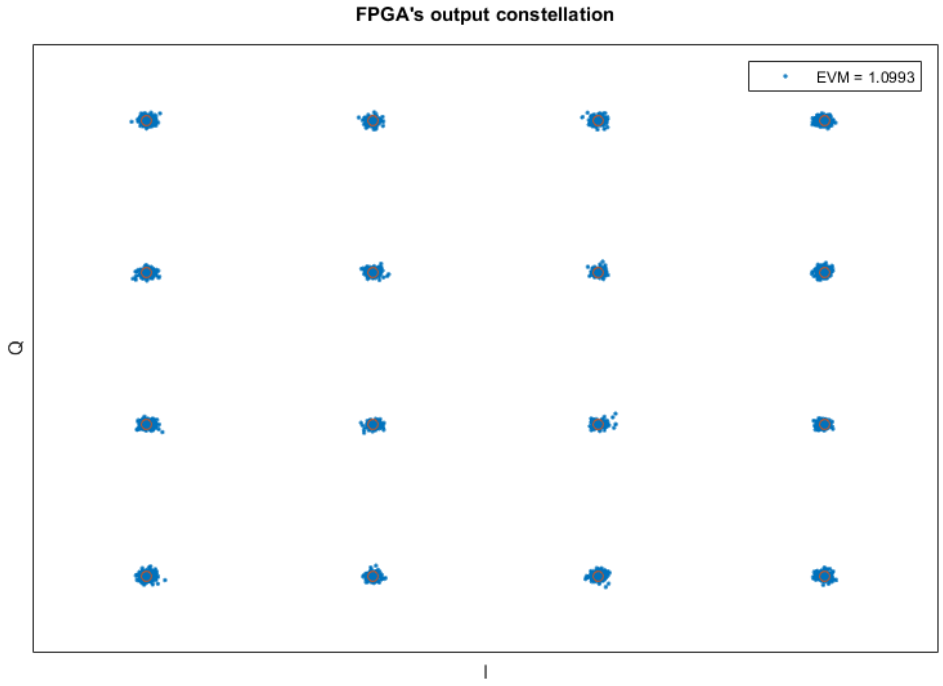


Figure 3.25: FPGA's output with 16-QAM constellation measured in an oscilloscope.

Finally, two projects were created in Vivado each one with a different signal constellation, 16 and 64-QAM. These were the two constellations tested. The following sections will show the results obtained for both constellations in each measuring point.

3.5.1 Electrical Transmission

The results obtained in the first measuring point were very similar to what was expected and already presented in the simulation section. In Figure 3.25, the obtained constellation for the 16-QAM signal can be seen. Comparing this figure with Figure 3.14, a slight increment in noise is visible, however, the total degradation is very small. This slight deviation is expected because of the oscilloscope's finite resolution, of cable and connector's losses and of additional FPGA's transmitter's imperfections. In the end, the total increase in EVM, from the simulation to the practical tests, was at worst 0.28%, which, in the author's opinion, is a reasonable value due to the already mentioned imperfections.

The same scenario was obtained for the 64-QAM constellation. The results for this case can be seen in Figure 3.26, which presents a slightly higher EVM than the 16-QAM case. A

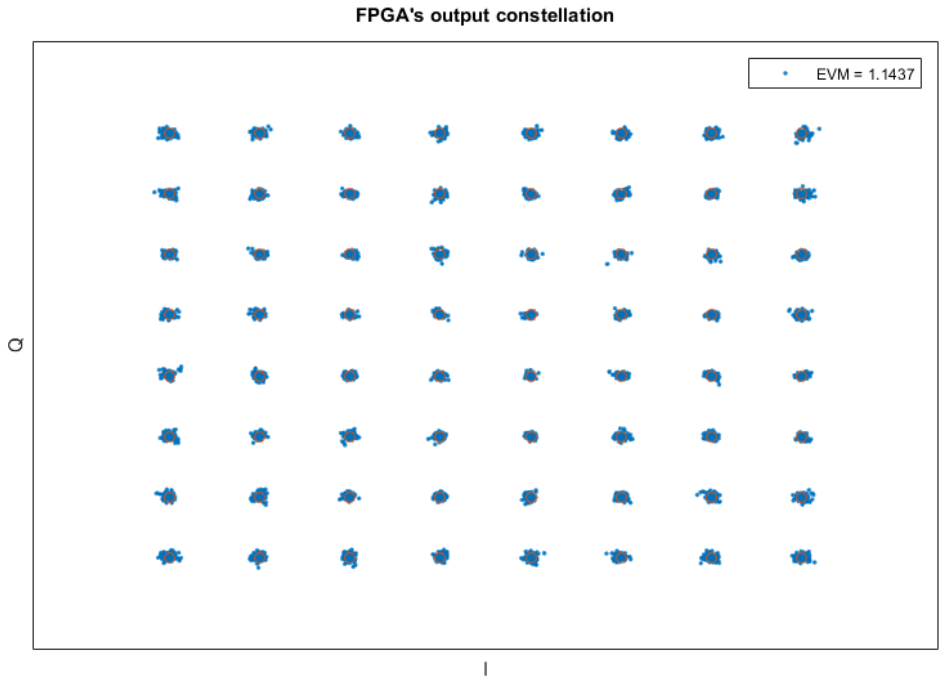


Figure 3.26: FPGA's output with 64-QAM constellation measured in an oscilloscope.

deeper analysis of the Figure 3.26 reveals a pattern in the noise, which increases from the inner to the outer points. This pattern was not visible in the 16-QAM constellation.

The final results for this measuring point can be seen in Table 3.2. A closer inspection of the obtained results reveals that EVM values for both constellations are not too disperse and the worst variation that is observed happens for the 16-QAM case, were a difference of 0.1% was detected.

From this measurement point, a good matching between the simulation and the practical results was obtained. In the end, the difference from the simulation to the practical implementation was small and justifiable and the 16-QAM and 64-QAM cases were proven similar. This allowed the tests to pass to the second point.

3.5.2 Electrical Back-to-Back

In this second measuring point, the simulation of the receiver was proven to be imprecise. From the simulation of the receiver, a doubling of the EVM was expected. However, this was not the case seen in the practical experiments. From the first measuring point, an EVM of 1.1% was achieved at the output of the FPGA, so it was expected a final received EVM varying from 2% to about 2.4%, admitting some error margin. However, the practical results showed a different thing. The received EVM was 4.52%, which is two times higher than expected. These results were nowhere near the simulated ones, which indicates that some component or components were introducing a lot of distortion into the signal.

From the analysis of the Figure 3.27, a clear distortion that affects more the in-phase axis is visible. This asymmetrical distortion was not expected and may indicate some difference

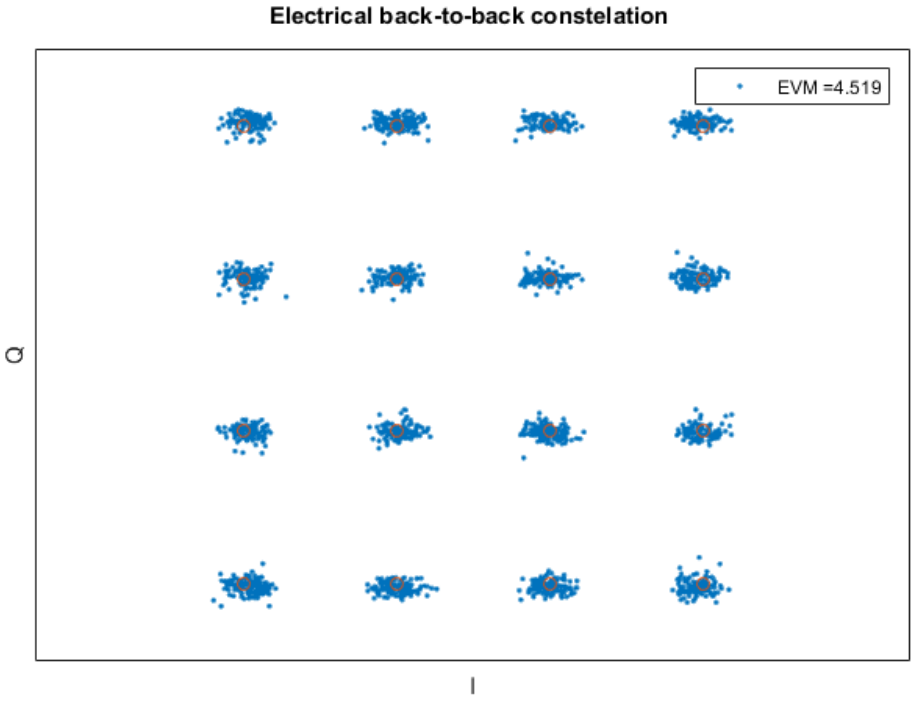


Figure 3.27: Electrical loopback with an 16-QAM constellation.

Table 3.3: EVM results obtained in electrical loopback for both 16- and 64-QAM cases.

EVM (%) 16-QAM	EVM (%) 64-QAM
4.519	4.1625
4.793	4.4251

in the processing between the in-phase and quadrature signals. However, the received signal is just divided into "in-phase" and "quadrature" signals in the receiver block and this block was simulated before being implemented. The fact that this behaviour is not visible in the simulation is intriguing and makes the discovery of the source of this distortion even harder.

Figure 3.28 shows the 64-QAM constellation that was obtained in electrical loopback. In it, the same asymmetrical distortion that was visible for the 16-QAM case is also present, which confirms the problem with the reception chain.

In Table 3.3, the final results for this measuring point are shown. In it, it is visible that the EVM results for the 64-QAM case are lower than the ones obtained for the 16-QAM. This was not expected since that in the first measuring point the EVM results for both constellations were similar. This inconsistency can be partially due to the high variation range presented in the results, which, as can be seen, can have variances of more than 0.2% in EVM. Other reason that might help explain the lower EVM for the 64-QAM case is the potential presence of errors. Once again, by looking at Figure 3.28, it is visible that the stretching in the "in-phase" direction of the constellation points might be causing some of those point to be interpreted as a different point, different from the original one. Because, this EVM does not

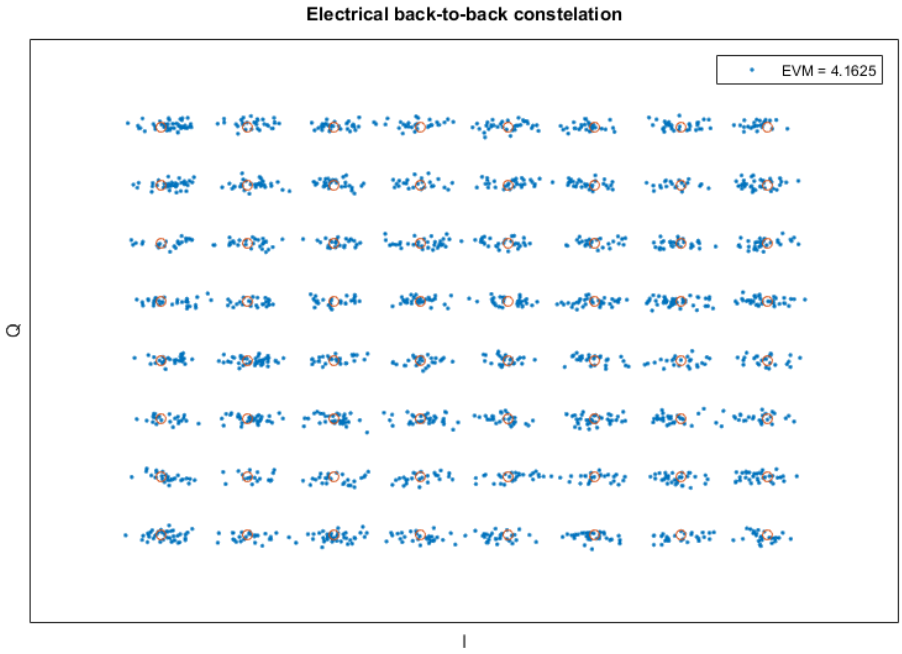


Figure 3.28: Electrical loopback with an 64-QAM constellation.

Table 3.4: EVM results obtained after optical transmission for both 16- and 64-QAM cases.

EVM (%) 16-QAM	EVM (%) 64-QAM
1.8021	1.4263
1.8060	1.4006

take into account the original data, this error would be interpreted as a normal point that is now closer to a different reference point. This might decrease the size of the error vector, which might cause a decrease of the obtained EVM.

3.5.3 Optical Transmission

As has been explained before, this measuring point was chosen to allowed for the determination of the performance of the optical link. In conjunction with the first measuring point, the data from both measurements can be analysed to reveal the total amount of degradation introduced in the signal only by the optical transmission.

The results obtained followed more or less the trend that has been observed in the first measuring point and once again the constellations were well defined, as can be seen in Figures 3.29 and 3.30, for the 16-QAM and 64-QAM case, respectively. However, the same problem found in the second measuring point is also present here, i.e., the EVM value for the 64-QAM case is steel significantly lower than the EVM value for the 16-QAM case, but in contrast with that measuring point, the stretching in the "in-phase" direction is not present and so it is less likely that some errors that might have occurred could be enough to justify at least part of

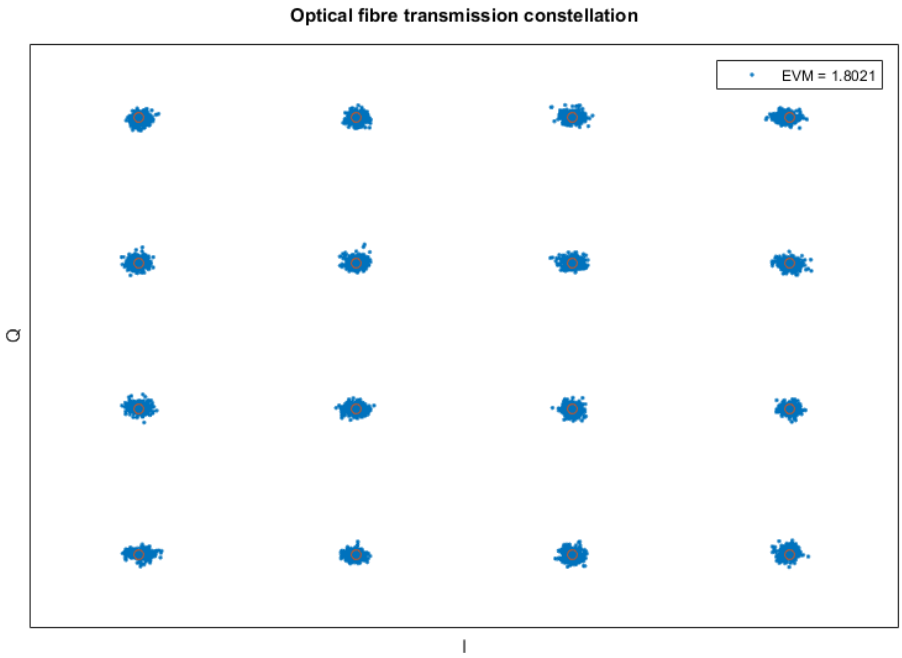


Figure 3.29: Optical output with an 16-QAM constellation measured in an oscilloscope.

Figure 3.30: Optical output with an 64-QAM constellation measured in an oscilloscope.

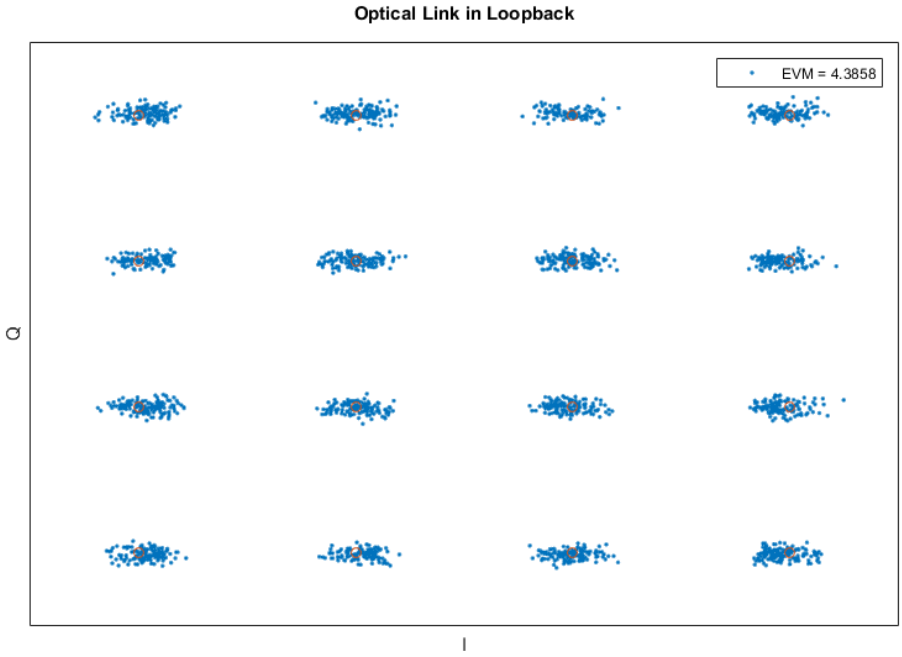


Figure 3.31: Final optical link 16-QAM constellation.

Table 3.5: Final EVM results.

EVM (%) 16-QAM	EVM (%) 64-QAM
4.3858	4.2726
4.3830	4.3845

this EVM difference. This difference also causes a problem in the determination of the value of the increase in EVM caused by the optical transmission. Analysing the 16-QAM case, an increase in EVM of about 0.65% was registered, however, when analysing the 64-QAM case, this increment lowers to about 0.24%.

Despite the problem in the determination of the exact value in that the optical transmission increases the EVM, both the value for the 16-QAM and for the 64-QAM case are still well bellow 2%, which are lower than the over 4% EVM obtained in the second measuring point. This fact might explain, in part, the results obtained in the fourth measuring point, but for now these results only gave confidence that the final link might work, and so the final implementation was done and the measuring of the fourth measurement point was started.

3.5.4 Point-to-Point Link with Optical Transmission

In the final measuring point, some of the behaviours and trends detected in the previous measurement points were detected again. Starting with the stretching of the constellation that was detected in the second measuring point, where the transmitter and receiver were directly connected. The same stretching is also present in the received constellations of this

point, as can be seen in Figures 3.31 and 3.32. However, the the EVM presented by the 16-QAM case is smaller than the one presented in the second measuring point. This was not expected due to the increase in the noise levels caused by the optical transmission. Even stranger is the fact that, unlike the 16-QAM case, the 64-QAM EVM presented here is more or less the same as it was in the second measuring point. This relative reduction of the EVM can be attributed to errors. The presence of errors can reduce the final EVM, however, it would increase the bit error rate.

The first justification that was developed was that in the second measuring point the receiver was being saturated due to too much power in the transmitter. However, after a remake of the second measuring point with an attenuator between the transmitter and receiver, the EVM did not decreased, in contrast, it increased the EVM, following the normal behaviour as if the receiver has not been saturated in the first place.

On the bright side, the remaking of the measurements revealed some hints into what might be causing the elongation. By mistake, the author of this work changed the place of the transmitter pair, i.e., the output of the FPGA is a differential output with a Tx^N and a Tx^P. These two cables would link to their respective connectors in the SFP testing board depicted in Figure 3.22. However, the author change this arrangement and where the N cable was supposed to be connected, the author connected the P cable and the same thing for where the P cable was supposed to be connected. This mistake caused a 90 degrees rotation in the elongation of the distortion present in the constellation, as can be seen in Figure 3.33. This rotation caused by the change of the cables' placement might indicate that the stretching is in fact caused by some error in the MGT's configuration. However, the author is not confident in this theory because the signal that comes from the MGT is just one, divided into 64 phases, and it is only divided into "in-phase" and "quadrature" signals already inside the receiver block. As this block was simulated and no signs of this elongation were detected, further research into this problem will be needed, perhaps a simulation based on actual received signals from the transmitter instead of just using the results of the transmitter simulation might reveal the cause of the elongation.

To conclude the analysis of the results, a final word on the overall good performance of the system must be written. In the end, the link was able to transmit information through the fibre and receive it again in the FPGA and the maximum EVM of the final transmission was less than 4.5% which is well bellow the limit of 8% imposed in the EVM for a 64-QAM transmission [34].

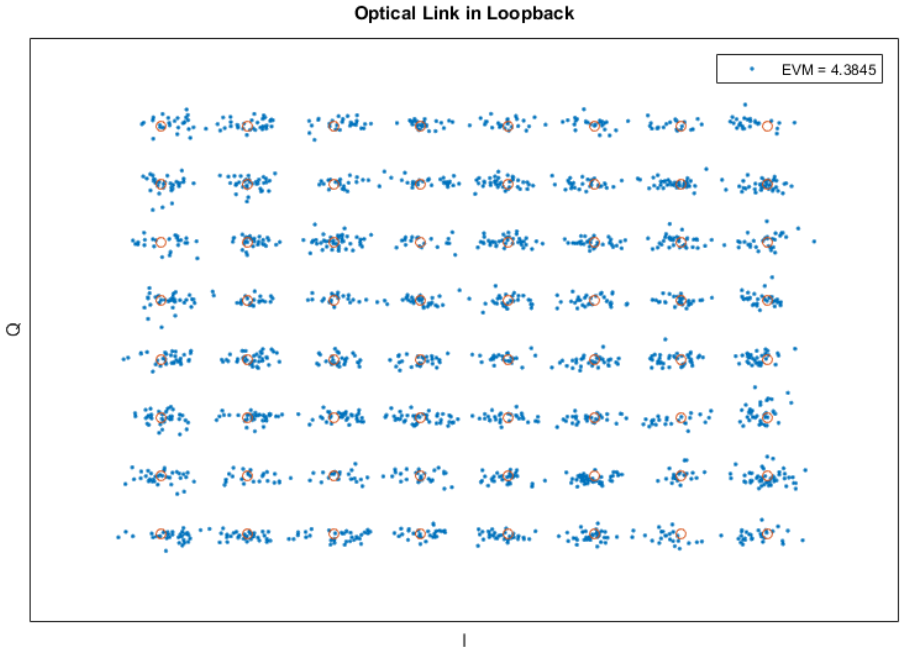


Figure 3.32: Final optical link 64-QAM constellation.

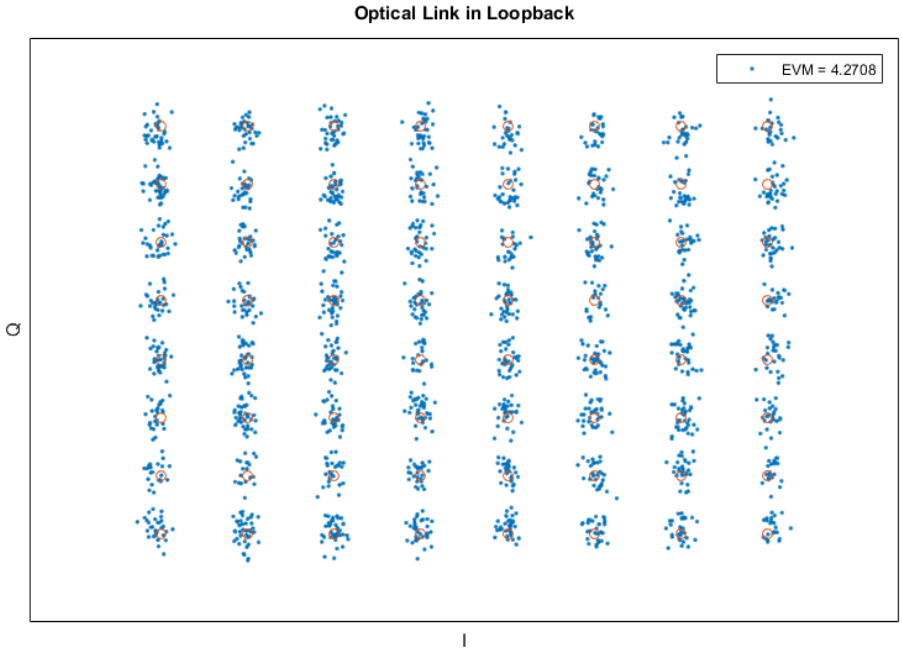


Figure 3.33: Inversion of the stretching present in the constellation.

Chapter 4

Optical Upconversion

4.1 Concept

The idea behind this part of the work was the development of a simple and scalable technique that could upconvert to mmWave range an ADT's signal. As was mentioned before, the conjunction of an ADT with optical fibre transmission has the potential to create a simple yet noise and distortion resilient way of transmitting data through the fibre. This concept was successfully demonstrated in the previous chapter, however, the signal frequency at the end of the fibre transmission was only 2 GHz, which, in that case was perfect for allowing the FPGA's receiver to acquire the signal, but it is not enough for dealing with the high frequency requirements for 5G, where the mmWave band is being pointed out as a solution to enable larger bandwidths. Despite current FPGAs manufacturers are presenting some MGTs capable of working at 58 Gbit/s [35], these devices were still not available in an FPGA kit to the general public at the time of writing this dissertation and so it is not yet possible to use an ADT to generate a digital signal at mmWave frequencies. A solution to this is the use of an external mixer cable of upconverting the digital RF signal from the ADT into this frequency band. However, the design of an RF mixer to this frequency is not very simple, requiring deep knowledge of RF theory and circuit design. And even if the goal is not the development of a new RF mixer, the ones available have a small range of frequencies that they can upconvert the signal to, when comparing to optical upconversion. Also, an optical upconverter is more simple and has advantages in terms of interconnection with the optical transmission. For these reasons the upconversion method used in this work will be optical.

The following sections will be dedicated to explaining the ADT architecture used for this part of the work followed be an in-depth discussion of the two optical upconversion techniques designed. Finally the last section of this chapter will be dedicated to the analysis of the results obtained.

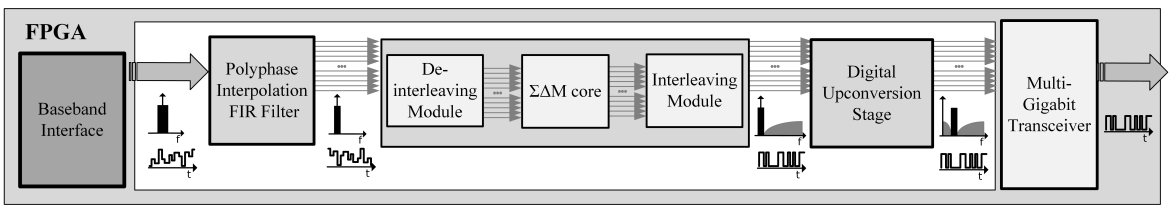


Figure 4.1: ADT architecture.

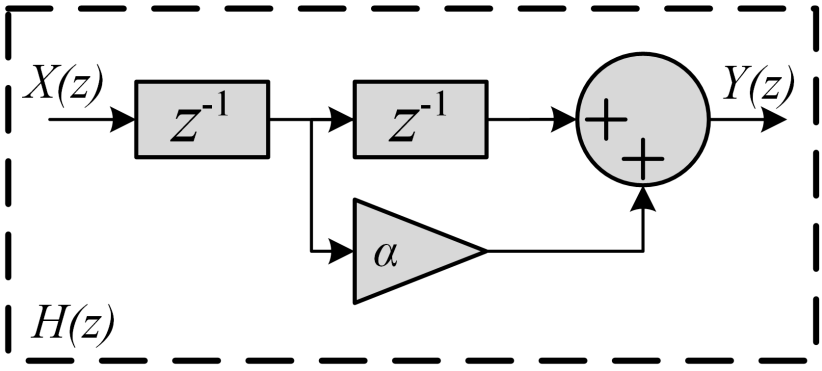


Figure 4.2: Delta sigma modulation core filter.

4.2 All-digital Transmitter

The ADT used in this part of the work was not the same as the one presented in the last chapter and its architecture was first introduced in [14]. However, most of the blocks were done using the same techniques. In this section some of the differences between the two architectures will be analysed. As the remaining parts that constitute the ADT are the same, the analysis of such blocks will be redirected to the last chapter, were the reader can find a detailed analysis of them.

The differences between the two architectures start right from the general topology. In contrast with the previous architecture, the ADT used for this part has the same topology as the one presented in Figure 1.4, in which the pulse modulator block is placed first and the upconverter is the last block of the ADT, a more detailed depiction of this architecture can be seen in Figure 4.1. This means that the ADT used here is a baseband-stage modulator due to the relative position of the pulse encoder in comparison with the upconverter. This type of modulator has the advantage that the upconversion block is much simpler when compared to the one used in the last chapter, however, this also means that this kind of modulator does not have the same carrier frequency flexibility and typically this frequency is bound to a quarter of the MGT working frequency.

Starting the analysis of the implementation of this ADT, the first difference in the blocks can be found right in the baseband interface. This block is the one responsible for receiving the data from the PC and then send it to the rest of the logic. In this implementation the use of a Random Access Memory (RAM) instead of a ROM means that data can be transmitted to the ADT in run time and there is no need for a different project to be created in order to change the transmitted data. This difference allowed for a faster testing of the implemented architecture.

After the signal is passed from the PC to the FPGA's RAM, the signals goes to a polyphase interpolation filter. In the case of this implementation and in contrast with the previous one, the filter used was a zero-order hold in a polyphase implementation. This type of filter was chosen due to its simplicity while providing the most important feature required for this block, upsampling the signal. In the end this filter was able to upsample the signal from its original sampling rate, 200 MHz, to the final equivalent sampling rate, 3.2 Gsps. The filter was replicated in order to upsample both the I and Q signals.

The next block, after the filter, is the de-interleaver. This block has the same architecture

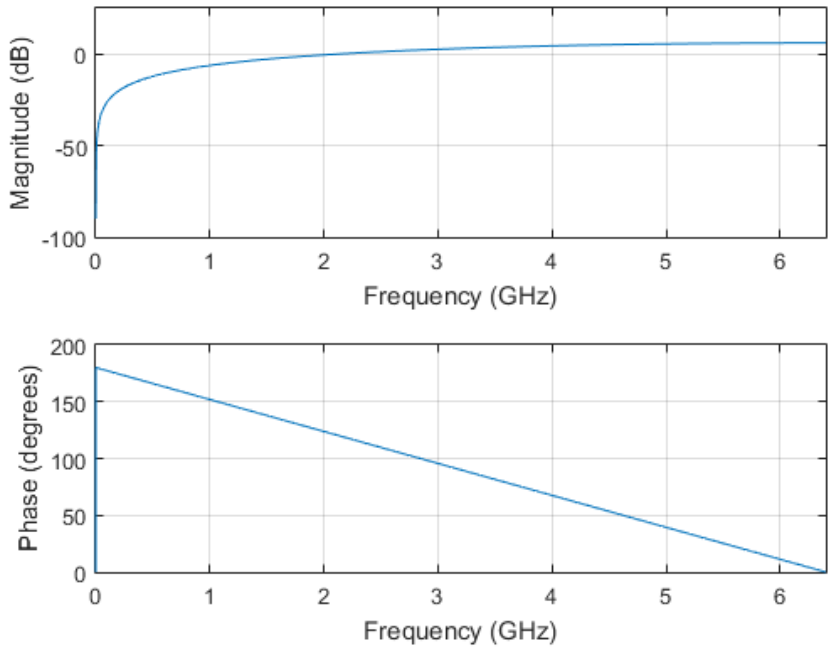


Figure 4.3: Frequency and phase response of the NTF.

---

as the one described in the previous chapter, subsubsection 3.2.1.3. However, due to the difference in the number of phases, this de-interleaver only has 16 phases and the k, value of contiguous samples is also 16. In the same way as the filter, this block was also replicated in order to be both in the I and Q signals' path.

With the 16 contiguous samples in each phase the signals are ready to enter the $\Delta\Sigma$M core. This block has the same topology as the one presented in subsubsection 3.2.1.4, however, this block is replicated in order to modulate both the I and Q signals. Besides the usual differences in the number of phases, from 64 to 16, in this case there is another difference which is the filter used in the loopback of the $\Delta\Sigma$M. From the topology presented in subsubsection 3.2.1.4, the STF was proven to be equal to one. Also in the same section the relation between the NTF and the filter $H(z)$ was determined by equation 3.4, where $NTF(z) = H(z) + 1$. With this equation in mind and knowing that the filter used here is depicted in Figure 4.2, which is a lower order filter than the one used in the previous implementation, the final NTF can be calculated to be:

$$NTF(z) = \left(\alpha z^{-1} + z^{-2}\right) + 1 = 1 + \alpha z^{-1} + z^{-2} \tag{4.1}$$

where $\alpha = -2cos(2\pi Fc/Fs)$. However, here $Fc = 0\ Hz$ because the type of modulator is no longer an RF-stage modulator, but is in fact a baseband-stage modulator. Due to this fact, $\alpha = -2cos(0) = -2$ and so the final NTF is:

$$NTF(z) = 1 - 2z^{-1} + z^{-2} \tag{4.2}$$

Having the NTF already calculated, the $freqz$ command from Matlab is used in order to confirm that the frequency response of the NTF have in fact a low-pass behaviour. That was

Table 4.1: Utilization values of the FPGA.

Resources	Utilization	Available	Utilization %
FF	10089	1075200	0.94
LUT	12378	537600	2.30
Memory LUT	2464	76800	3.21
I/O	12	832	1.44
BRAM	352	1728	20.37
BUFG	9	960	0.95
MMCM	1	16	6.25
GT	2	65	3.08

exactly what what was observed as can be seen in Figure 4.3, where is clear that the NTF has an attenuation near 0 Hz.

After the ΔΣM core, both I and Q signals enter the interleaver. This block is once again based on the same architecture as the one described in subsubsection 3.2.1.5. In there, it is explained the technique used to convert the k contiguous samples that come from the ΔΣM core and how to placed then, one sample per phase, in each of the 16 phases at the output of the interleaver.

Finally, after the interleaver, both the I and Q signals are ready to be upconverted. In the upconversion block two requirements have to be taken in consideration, first the constant envelope of the signal must not the changed and second both I and Q signals are needed to be combined into a single real signal in order to be transmitted by the MGT. The first of the requirements is fulfilled by choosing the carrier frequency into which the signal will be upconverted to as a quarter of the serializer frequency. The choice of this frequency falls into a specific case of the following equation:

$$e^{\frac{j2\pi nfc}{fs}} = cos\left(\frac{2\pi nfc}{fs}\right) + j \times sin\left(\frac{2\pi nfc}{fs}\right) \tag{4.3}$$

which, due to the fact that $fc = (1/4)fs$, collapses into:

$$e^{\frac{j\pi n}{2}} = cos\left(\frac{\pi n}{2}\right) + j \times sin\left(\frac{\pi n}{2}\right) \tag{4.4}$$

from this equation, it is possible to see that the quadrature signals will be multiplied by $cos(\pi n/2) = [1, 0, -1, 0]$, while the in-phase signals will be multiplied by $sin(\pi n/2) = [0, 1, 0, -1]$. Adding the two signals, results in a four component word, $[I, \overline{Q}, \overline{I}, Q]$, that will be serialized by the MGT. As can be seen, the final word consists only of 2 levels and combines both I and Q signals into a single real one, fulfilling both requirements which were previously defined.

For the implementation of this ADT, the FPGA kit used was the same as the one used in the previous chapter, the Xilinx VCU1283, and a table with the resources used can be seen in Table 4.1. With the ADT implemented, the implementation of the optical architectures could start.

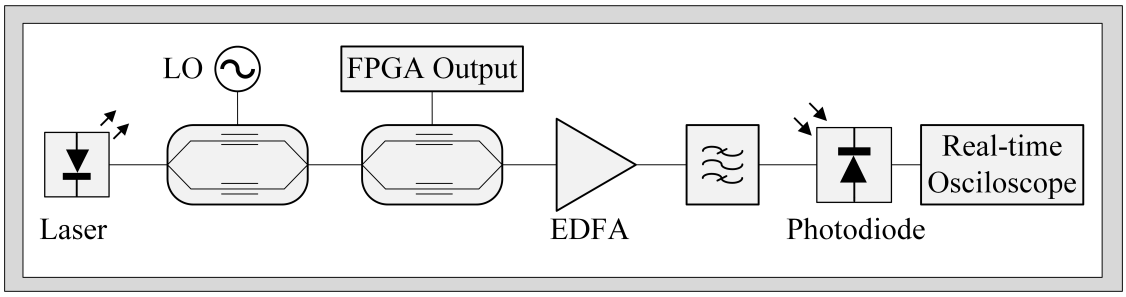


Figure 4.4: Dual carrier modulated optical upconversion architecture.

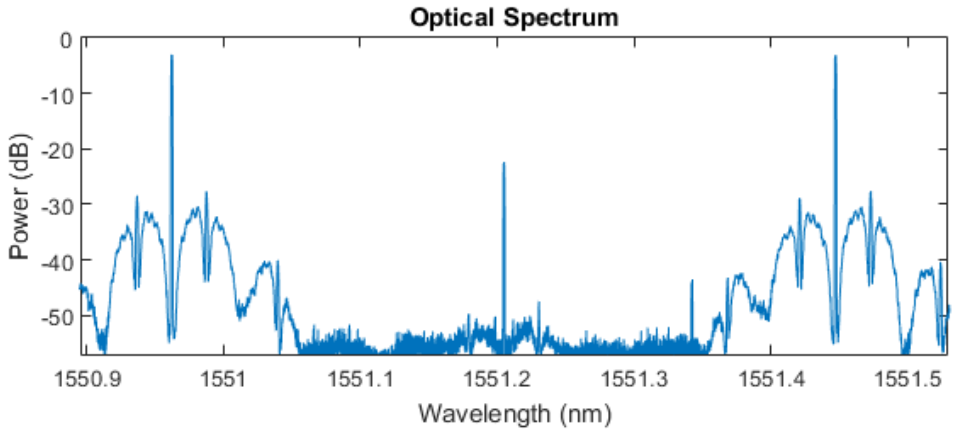


Figure 4.5: Optical spectrum of the dual carrier modulated optical upconversion architecture.

4.3 Optical Architecture

As it was mentioned in section 4.1, two different upconversion architectures were developed. Despite having similarities between them, the two architectures have slightly different characteristics that, in the end, change the type of applications in which they can be applied to.

4.3.1 Dual Carrier Modulated Optical Upconversion Architecture

The first architecture can be seen in Figure 4.4 and it is called dual carrier modulated optical upconversion. This architecture is composed of a laser, two dual-drive Mach Zehnders, a local oscillator, the FPGA with the implemented ADT, an EDFA, an optical filter, a photodiode and finally a real-time oscilloscope. The laser was set to 1551.2 nm with an output power of 13 dBm and then modulated by a tone in the first dual-drive Mach Zehnder. This frequency tone was varied in order to change the final upconversion frequency and so, the values of 15.1 GHz, 20 GHz and 30 GHz were chosen in order to demonstrate the flexibility of the proposed architecture. After the modulator the power presented by each carrier was -1 dBm when separated by 31.2 GHz and -5 dBm when separated by 60 GHz, the values of 31.2 GHz and 60 GHz reflect the fact that, at the modulation of the optical carrier with the RF tone, a replica of such tone appears at $Fcarrier + Ftone$ and another replica appears at $Fcarrier - Ftone$, which means that the two replicas will be separated by $2 \times Ftone$. Carrier

rejection was performed in order to suppress the original carrier, the valuer obtained was greater than 20 dB, in all tests with this topology. The second modulator is performing an on-off keying modulation in both tones with the signal that comes from the FPGA's ADT. A graphical representation of the spectrum at this point can be seen in Figure 4.5. In this figure the two main tones are clearly visible and, at their sides, the typical noise shaping pattern of the $\Delta\Sigma$M is also present. The third spike in the middle is the original optical carrier, this carrier was also modulated by the dual-drive Mach Zehnder, however, the modulated signal is bellow the noise floor of the optical analyser and so it is not visible in the figure. After the second modulator, the signal is amplified using an EDFA and then filtered using a band-pass filter with 200 GHz of bandwidth. Finally, the optical signal is converted to the electrical domain using a photodiode with proximally 100 GHz.

This first architecture has the disadvantage of not being suitable for long distance transmissions. This disadvantage comes from the fact that both tones are modulated, which means that at the photodiode for a good combination of both modulated signals, they should have the same phase, i.e., the modulated signals of the lower frequency tone should have the same phase as the ones in the upper frequency tone. Due to the chromatic dispersion, which is introduced in the signal during long distances transmissions, the phase of the modulated signals of both tones is not the same and so phase noise is introduced at the photodiode in the final electrical signal. This disadvantage can be suppressed by using just one of the modulated tones, this would result in a single sideband modulation. One way of achieving single sideband modulation is by using a filter that suppresses one of the modulated tones, however, this introduces complexity to the architecture as well as decreases the power available at the photodiode. Another way of achieving the same single sideband modulation is by using the same implementation as the one used in the second upconversion architecture, depicted in Figure 4.6.

4.3.2 Single Carrier Modulated Optical Upconversion Architecture

The second architecture is called single carrier modulated optical upconversion and it is composed of a laser, to dual-drive Mach Zehnders, two add-drop multiplexers, the FPGA with the implemented ADT, 20 km of single mode optical fibre, a photodiode, and a real-time oscilloscope. The laser was set to 1550,6 nm with an output power of 13 dBm. Then the signal from the laser was modulated in the fist Mach-Zehnder with a 28.4 GHz tone. After this modulation the signal was amplified in a EDFA in order to compensate the losses in both add-drop multiplexers. The first add-drop multiplexer was set in a demultiplexer configuration. Both the frequency of the local oscillator as well as the laser's wavelength were chosen so that in the demultiplexer this component presented in one of its outputs the lower tone and in the other output the higher tone. The tone with the highest wavelength was then modulated in the second Mach-Zehnder by the signal from the FPGA. Then the two signals were recombined by the second add-drop multiplexer. Both add-drop multiplexers had bandwidth equal to 100 GHz, this bandwidth is larger than what is necessary to contain the signal from the FPGA, however, these were the two add-drop multiplexers with the lowest bandwidth for this wavelength region present in the laboratory. The result signal from the multiplexer was then propagated through 20 km of standard single mode optical fibre before reaching the photodiode where the opto-electrical conversion of the signal was performed. Finally, the signal was sampled with a real-time oscilloscope and processed off-line.

As was mentioned before, this architecture is not affected by chromatic dispersion due to

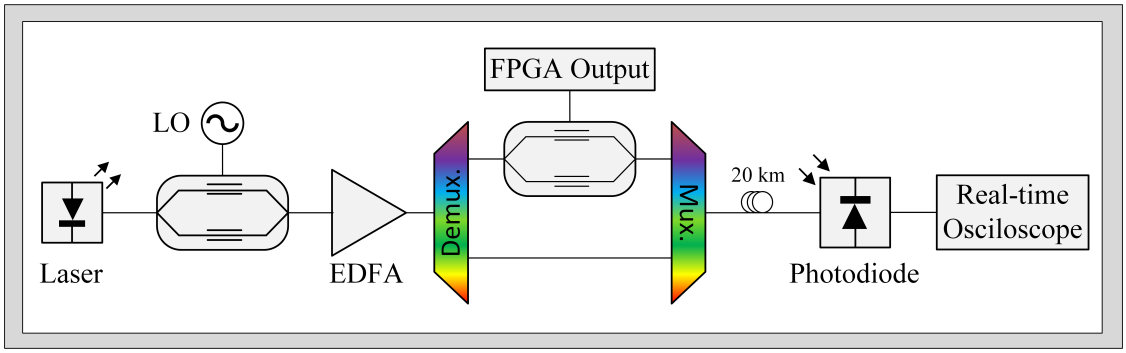


Figure 4.6: Single carrier modulated optical upconversion architecture.

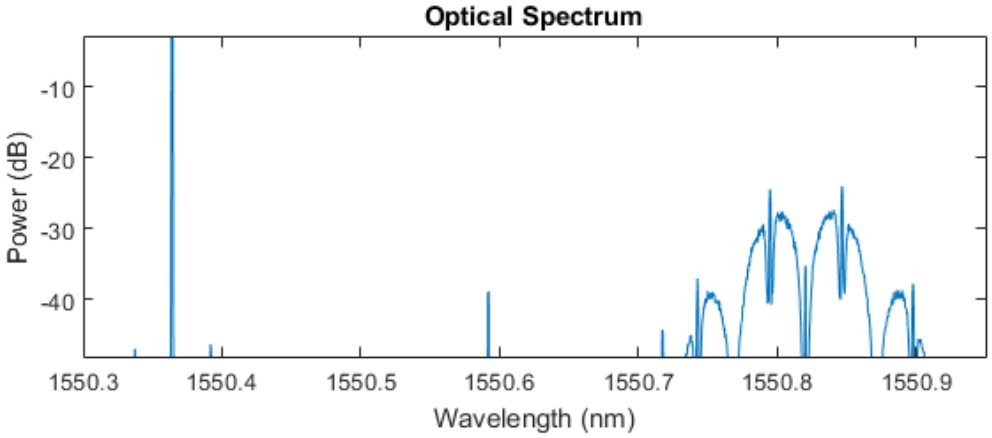


Figure 4.7: Optical spectrum of the single carrier optical upconversion architecture.

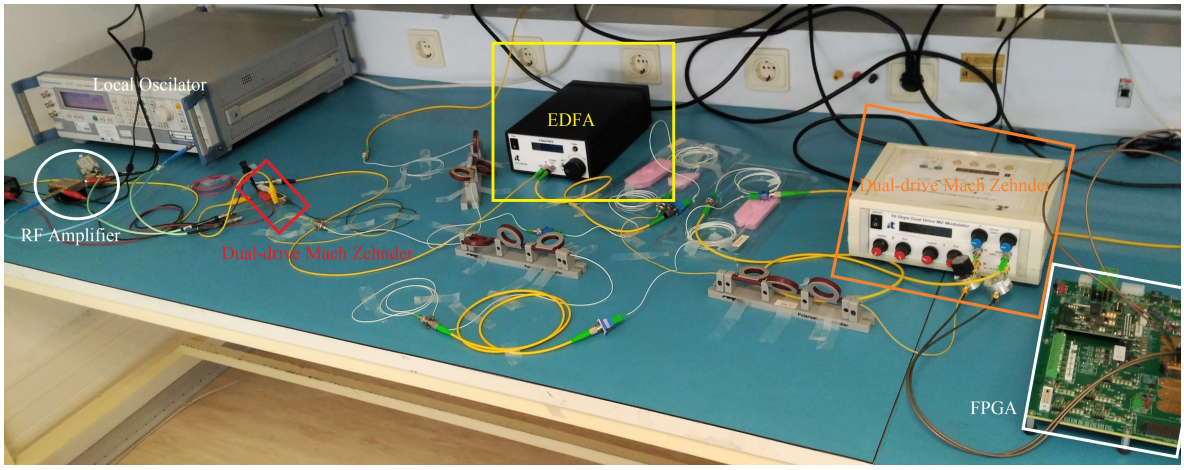


Figure 4.8: Experimental setup.

fact that it performs a single sideband optical upconversion. The spectrum after the second add-drop multiplexer is depicted in Figure 4.7, in it, it is visible the lower wavelength tone, in the left, and it is also visible the modulated signal, in the right.

Figure 4.8, represents the experimental setup of the second architecture. Starting from the left, it is visible the signal generator which provides the RF tone to the first modulator. However, due to the low power of its output signal, this tone is firstly amplified before going into the modulator, which is a dual-drive Mach Zehnder. The amplifier used can be seen right in front of the signal generator, with the white circle on top, while the first modulator is marked by the red square. The Laser is not visible in the picture, however, the yellow fibre that is visible coming from the stand behind is the one that comes from it. After this first modulator the signal enters the EDFA, which is marked by the yellow square. Next to the EDFA it is visible the two add-drop multiplexers. The one on the left is working as a de-multiplexer and the one on the right as a multiplexer. One of the outputs of the de-multiplexer goes directly to the multiplexer and the other goes to the second dual-drive Mach Zehnder. The second Mach Zehnder is marked by the orange square and it is connected to the FPGA, which is marked with an white square. The modulated signal goes to the multiplexer and joins the signal that came directly from the de-multiplexer. Finally, the signal goes to the photodiode, which is not represented in the figure, to be converted into the electrical domain. The first architecture's experimental implementation is not depicted in this dissertation due to the fact that most components are the same as the second one and also because it is simpler, which makes its deduction easy after seeing the second architecture's experimental implementation.

The measurements of the general performance of the ADT, and of the two architectures are presented in the next section, where there is also present a comparison of the electrical spectrum of both architectures.

4.4 Measurements

All measurements were performed using a real-time oscilloscope from Tecktronix, with the reference DPO77002SX. This oscilloscope was also used for the measurements done in section 3.5, which facilitated the measurement process.

The first measuring point was at the output of the FPGA. The measurements done here served not only to see the overall performance of the ADT, but also as a reference for comparison with the results after the optical upconversion. In Figures 4.9, 4.10 and 4.11 the change in EVM with the increase of the baud rate was tested. As expected the EVM suffered a degradation with the increase of the baud rate, with the best EVM being 1.22% at 20 Mbaud and the worst EVM being 2.27% at 100 Mbaud. This increase in EVM is caused by the decrease in energy of the symbol as the symbol rate increases. Despite the increase in EVM, its value at 100 Mbaud is still low enough for transmission of a 256-QAM [34], and so two more constellations were chosen to be tested at this baud rate, 64-QAM and 256-QAM.

The results of this experiment in conjunction with the previous 16-QAM constellation are shown in Figures 4.12, 4.13 and 4.14. This time, the EVM decreased with the change for higher modulations. Comparing the results for the 16-QAM case with the results for the 64-QAM, the decrease in EVM is not substantial and most of the difference can be attributed to the variance of the results, the remaining difference can be the cause of some errors, that jump from one constellation point to another, reducing the overall EVM. However, this reduction

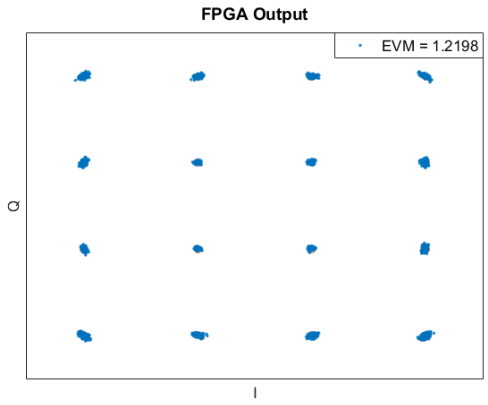


Figure 4.9: FPGA output constellation for 16-QAM with 20 Mbaud.

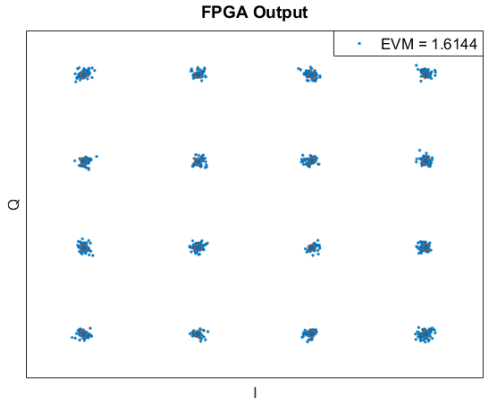


Figure 4.10: FPGA output constellation for 16-QAM with 50 Mbaud.

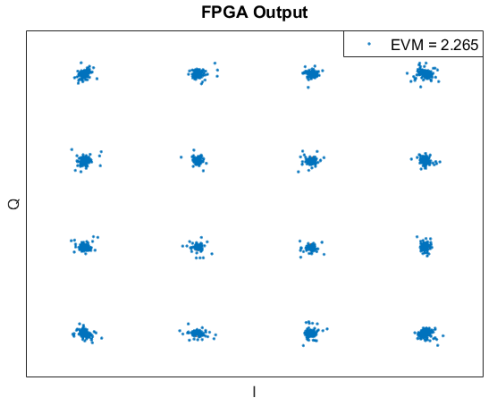


Figure 4.11: FPGA output constellation for 16-QAM with 100 Mbaud.

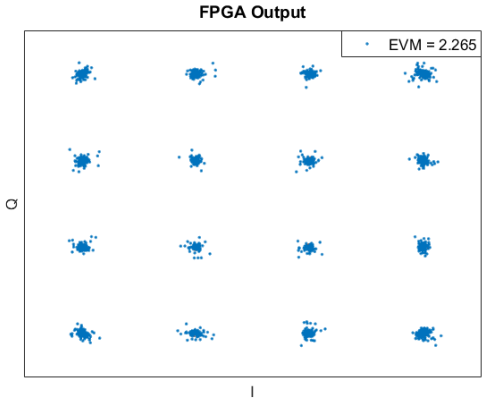


Figure 4.12: FPGA output constellation for 16-QAM with 100 Mbaud.

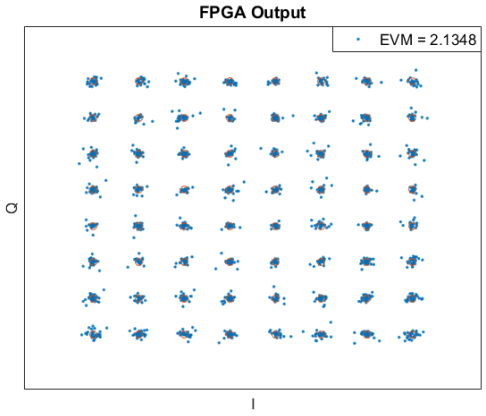


Figure 4.13: FPGA output constellation for 64-QAM with 100 Mbaud.

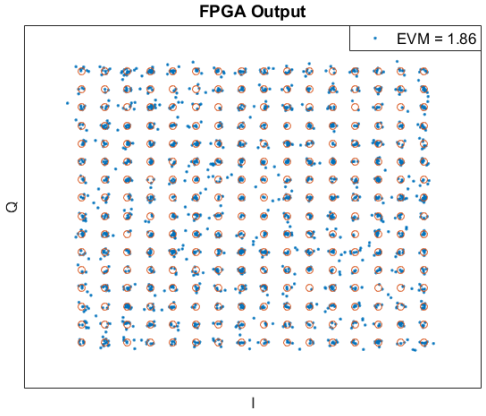


Figure 4.14: FPGA output constellation for 256-QAM with 100 Mbaud.

in EVM masks the increase in the bit error rate. This reduction in EVM caused by errors is going to have more impact as the number of points in the constellation increases. This is due to the fact that with the increase in the number of points in the constellation these points tend to be closer, which make the same error vector produce a symbol error in larger constellations but not in the smaller ones. From this, it was expected that this problem caused by errors in the retrieval of the constellation would be the biggest reason for the 256-QAM being the one with the lowest EVM, as when analysing Figure 4.14 it is visible that a large amount of points in the constellation can be interpreted as the wrong constellation point.

The results of the dual carrier modulated optical upconversion architecture can be seen in Figures 4.15, 4.16 and 4.17. When analysing the results, a pattern was discovered. The EVM was increasing with the rise of the carrier frequency. From a more careful analysis of the setup, two possible causes were found. First, the bit resolution of the oscilloscope used is lower at higher frequencies and its bandwidth which is just 70 GHz is already close to the 63.2 GHz carrier. This can cause an unwanted filtering effect of the signal. Second, it was also found that the local oscillator used presented an increase in phase noise with the increase in frequency, also contributing for a slight degradation of the constellation. Despite all these imperfections, the increase in EVM was kept under 2%, with the worst degradation being 1.87% when upconverting to 63.2 GHz. The remaining cases presented an increase in EVM of 1% for the upconversion to 27 GHz and an increase of 1.38% for the case of 43.2 GHz.

For the single carrier modulated optical upconversion architecture, depicted in Figure 4.6, the results are shown in Figures 4.18, 4.19 and 4.20. These results were taken with 20 km of optical transmission, however, the results without optical transmission were similar, presenting only a little decrease in EVM. Also, despite the results presented for this architecture only shown a single carrier upconversion frequency, this architecture is not bound to such frequency and theoretically the same carrier frequency agility displayed by the first architecture can be obtained also in this one. Changing the carrier frequency can be made in the same way as in the first architecture, i.e., by changing the frequency of the local oscillator. More frequencies were not tested due to time constraints.

Analysing the Figures 4.18, 4.19 and 4.20, it is possible to see the same pattern that was observed when comparing the different constellations without the optical upconversion. I.e., the measured EVM decreases when the constellation goes from a 16-QAM to a 256-QAM. As it was explained before, this decrease of the EVM is caused by errors in the reconstruction of the constellation, which makes one sample to be interpreted as a different point of the constellation. Moreover, the increased noise introduced by the optical upconversion magnifies this effect by increasing the probability of a symbol error. This increment gets more clear when comparing these results with the ones without upconversion. For the 16-QAM modulation the increase in EVM caused by the upconversion is 0.76%, when comparing the 64-QAM modulation this value is reduced to 0.44%, finally the comparison for the 256-QAM gives an increase of only 0.3%. However, the final EVM for the upconversion of the 16-QAM modulation presented by this optical upconversiom architecture is still better that the one presented by the first topology, while this topology presents an EVM of 3.02% at 60 GHz with 20 km of optical transmission, the first architecture presents an EVM of 4.13% at 63.2 GHz with just back-to-back transmission. The increase of 3.2 GHz in the carrier frequency is not responsible for the increase in EVM that can be seen when comparing the results of the first and second architecture, that is because when analysing the results for the first topology but choosing the replica at 56,8 GHz, the resulting EVM is almost identical.

Further proof of the better performance of the second architecture can be found when

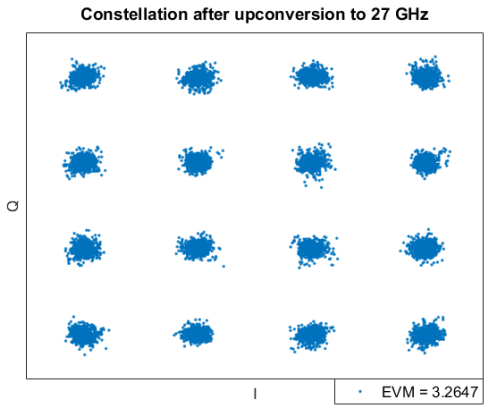


Figure 4.15: Constellation after the upconversion to 27 GHz for 16-QAM with 100 Mbaud (1^{st} architecture).

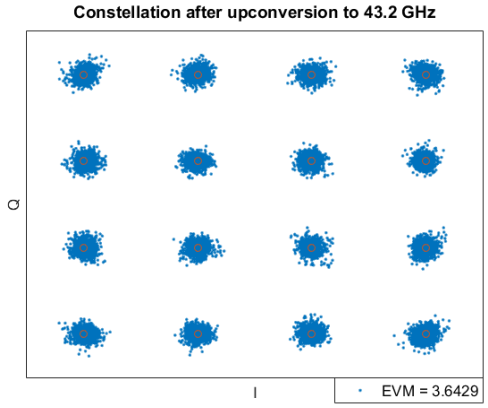


Figure 4.16: Constellation after the upconversion to 43.2 GHz for 16-QAM with 100 Mbaud (1^{st} architecture).

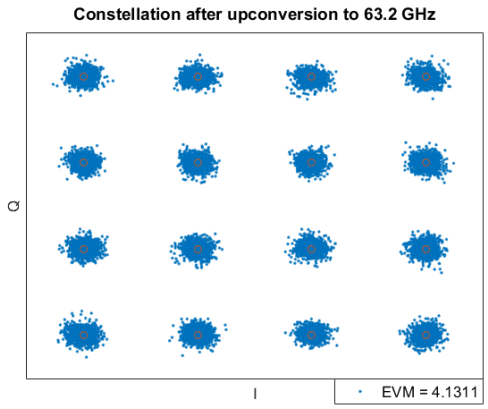


Figure 4.17: Constellation after the upconversion to 63.2 GHz for 16-QAM with 100 Mbaud (1^{st} architecture).

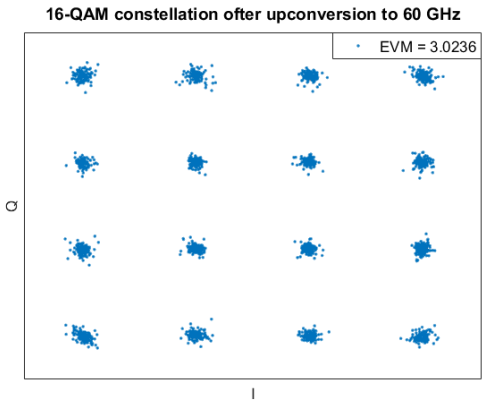


Figure 4.18: Constellation after upconversion to 60 GHz for 16-QAM with 100 Mbaud (2^{nd} architecture).

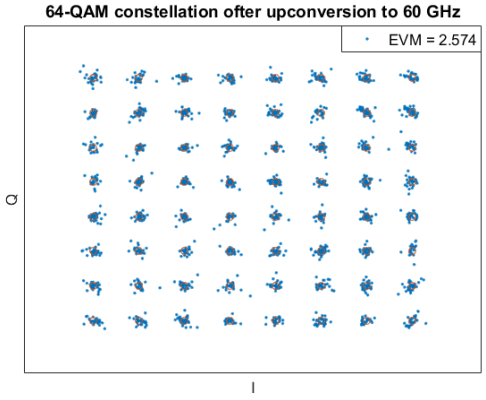


Figure 4.19: Constellation after upconversion to 60 GHz for 64-QAM with 100 Mbaud (2^{nd} architecture).

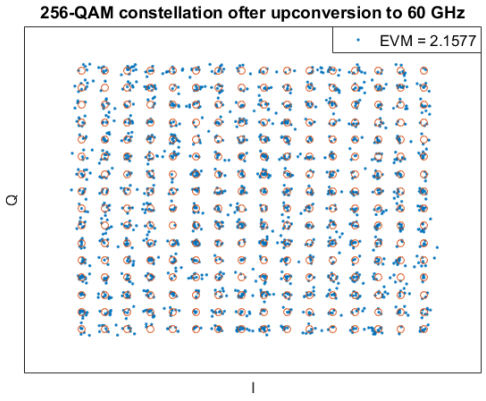


Figure 4.20: Constellation after upconversion to 60 GHz for 256-QAM with 100 Mbaud (2^{nd} architecture).

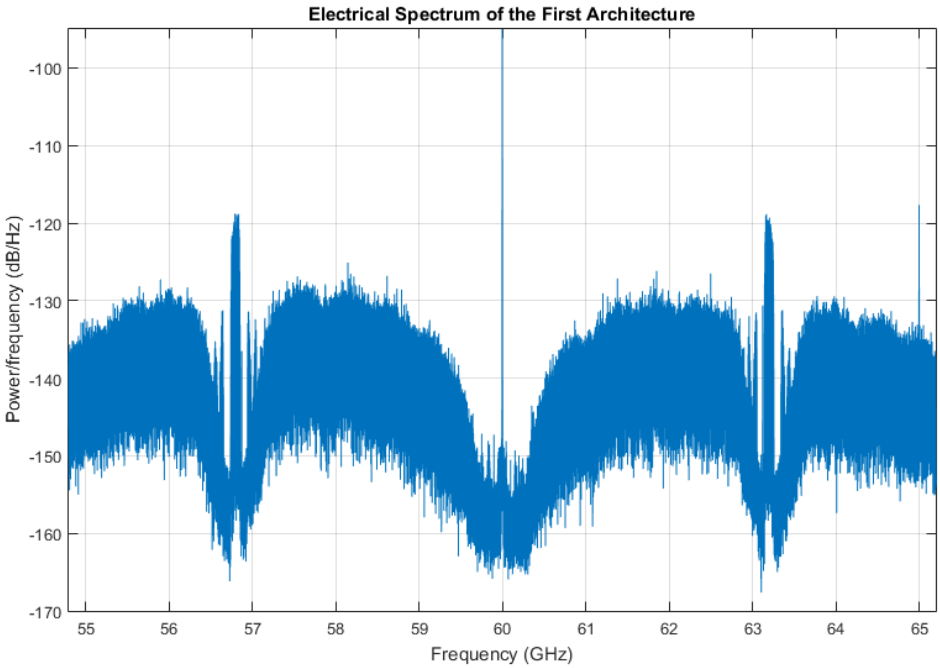


Figure 4.21: Final spectrum of the dual carrier modulated optical upconversion architecture.

comparing Figures 4.21 and 4.22. In Figure 4.21, a representation of the spectrum received from the first architecture at the oscilloscope can be seen. Figure 4.22 represents the same spectrum but received from the second architecture. A quick comparison between the two reveals a more clean spectrum for the second architecture. This difference in the two spectra will be reflected in the the obtained constellations.

Making a final comparison of the two architectures, it can be concluded that despite the first architecture being more easy to implement, the added complexity presented by the second architecture enables higher performance and larger transmission distances.

As a final remark about the decrease in EVM when passing from smaller constellations to larger ones is needed. This decrease in EVM is not an indicator of the improvement in the performance of the system caused only by the change in the type of modulation used. This only happens due to the inherent properties of the EVM calculation, which uses the closer reference constellation point to calculate the received vector. When error are present, the received vector is much shorter than it would otherwise be, which cause a decrease in the final EVM value. Furthermore, whenever this occurs, the bit error rate would no longer be zero, proving in fact that the performance of the system remains the same.

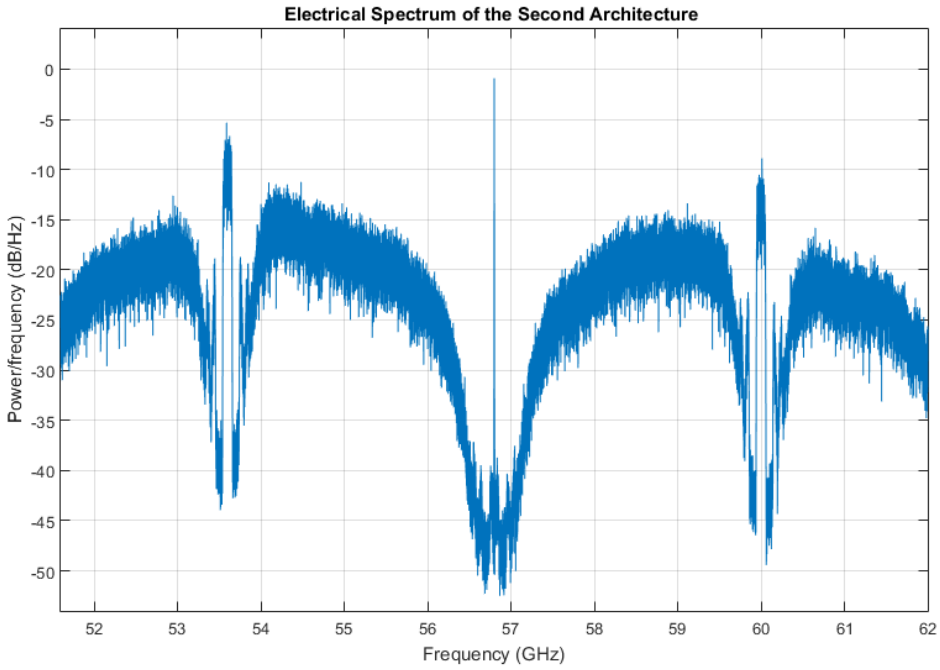


Figure 4.22: Final spectrum of the single carrier modulated optical upconversion architecture.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

The work done during this dissertation was focused on the development of solutions capable of being used in C-RAN scenarios. With this in mind, section 1.2 details the objectives of this work. The completion of such objectives resulted in:

- An all-digital point-to-point link capable of transmitting data through an optical fibre cable;
- Two distinct optical upconversion architectures capable of upconverting a digital signal into the mmWave frequency band.

For a more easy understanding of this dissertation, chapter 2 reviewed some important concepts. This included the concepts and state of the art of ADT, of $\Delta\Sigma$M and RoF.

In chapter 3, it is presented a description of the design and implementation process of the first ADT-based point-to-point optical link. The use of $\Delta\Sigma$M in the transmitter allowed for a simpler receiver, comprised only by a digital downconverter and a filter. This simplification was crucial to allow the integration of both the transmitter and the receiver in the same FPGA. In the end, the EVM measurements of the transmitter were close to the simulated ones and adding fibre transmission did not increase these values too much. These results proved the good behaviour of both the ADT and the fibre transmission. On the other hand, the measurements done to the receiver were not in complete agreement with the simulation and a horizontal stretching was present in the received constellation with and without fibre transmission. However, the final EVM results for the complete link were kept below 4.5%, which allows for the use of 64-QAM transmission. The maximum length of the presented setup was small, but it could be increased by a simple change of the SFP used. In the end, the objective of constructing a point-to-point link based on an ADT was achieved and its utilization in the implementation a fronthaul is a viable option, according to the experimental results.

Chapter 4 presents two different optical upconversion architectures. These were used to upconvert the ADT signal into the mmWave band. The first architecture, despite being simple does not provide chromatic dispersion resilience and so, the available transmission distance is small. On the other hand, the second architecture is more complex, but is not affected by chromatic dispersion. This allows for this architecture to be used when long distances

transmissions are needed. However, both implementations can be used in C-RAN scenarios. The use of the first implementation allows for a more simple and cost effective deployment of a mmWave upconversion, where the RRH is close to the base-station and the second one provides better performance and resilience to distortion for when the distance between those two elements is high.

5.2 Future Work

At the conclusion of this work several points for the improvement of the presented architectures were discovered. First, the filter used in subsection 3.2.1.1 might be improved to have a more steep slope in order to reduce the adjacent replicas that appears in the final transmitted signal. The improvement of this filter, despite not being critical, would reduce the distortion introduced in the signal, which could lead to an improvement in the overall performance of the transmitter and further reduction of the measured EVM.

Another point of future work will settle around the receiver. As was previously mentioned, the implemented receiver introduces a stretching in the constellation that was not present in the simulation. In order to find the cause of such imperfection more tests will be needed. As it was already referred in section 3.5, by changing the way the transceiver N and P cables connect to the N and P cables of the receiver, it is possible to change the orientation of such stretching. This might indicate that the stretching has something to do with the MGT. In order to have more information a phase shift of the signals prior to the receiver could reveal if the elongation is caused by some unwanted phase shift in the MGT.

Other tests would also be needed to be performed in both the point-to-point link and to the two optical upconversion architectures. These tests are bit error rate measurements which were not done due to time constraints. These tests would access with more precision the real performance of each system, while eliminating the problem that the EVM has when dealing with constellations with errors.

Finally, the last point of future work is the integration of the point-to-point link with real-time baseband modems.

Appendix A

Implementation on System Generator

In this Appendix the reader can find additional information about the implementation of the ADT that was previously describe in chapter 3. As most of the theoretical implementation was already explained in that chapter, this Appendix will focus more in the practical implementation that was done using System Generator. In accordance with chapter 3, the remaining of this Appendix will also be divided into two sections, one which will describe the implementation of the transmitter and another with the description of the receiver.

Transmitter

Figure A.1 is a logical representation of the implementation of the transmitter. In contrast with most of the other figures, this one is not a screen-shot of the System Generator implementation because the size of such implementation is too big to fit in a single figure. To overcame this problem, the top-level architecture is only shown in a logical format while the rest of the smaller blocks are depicted as they were implemented.

In the figure, it's visible on the left that the data is passed to the transmitter in the form of IQ data, then two interpolation FIR filters processed both I and Q data. An in depth description of these filters can be found in subsubsection 3.2.1.1. In Figure A.2 the polyphase implementation of such filters can be seen. On the top of the image is visible the input signal, which is then replicated and redirected to the 64 smaller FIR filters. The implementation of these smaller filters can be seen in Figure A.3.

After the filter, the signal which is now in a polyphase representation goes to the multipliers. In here, the signal is multiplied by a sine or cosine wave, one multiplies the I and the other the Q. The implementation of the multipliers can be seen in Figure A.4. Each phase of the signal is multiplied by a different phase of the sine or cosine signals. The sine and cosine signals are both generated by the DDS block. This block implements a polyphase direct digital syntheses, which is represented in Figure A.5. In the top conner a register saves the STEP value and only redirects it to the remaining blocks when the enable signal is '1'. Each of the remaining blocks implement two ROMs and its control logic. The control logic uses the STEP and the index of the block in order to calculate the index of the ROM to be read. The two ROMs are full with the values of a single period of a sine and cosine wave each. A representation of both the ROMs and the control logic can be seen in Figure A.6.

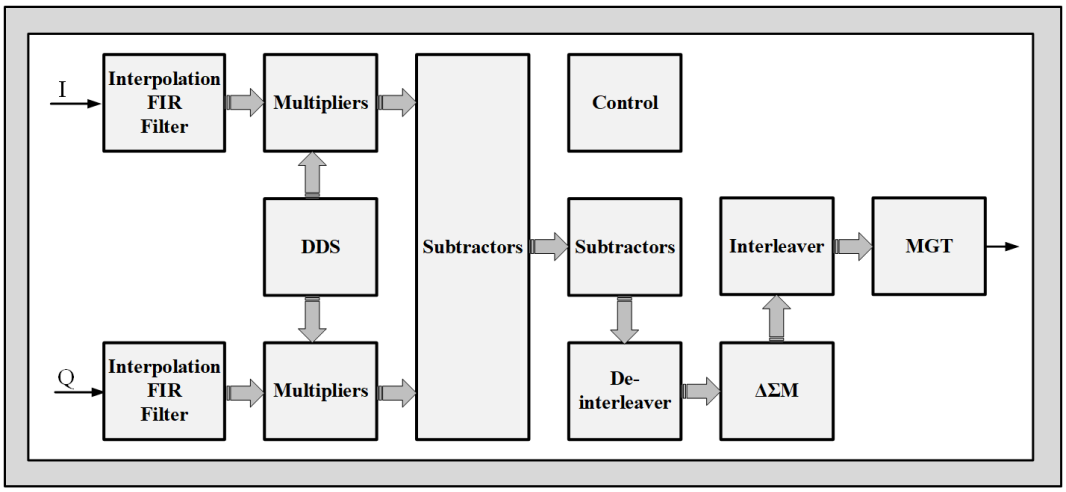


Figure A.1: Transmitter top-level architecture.

After the upconversion, the Q signal is subtracted from the I signal, resulting in a single real signal. The block that implements this subtraction has 64 subtracters and it's depicted in Figure A.7.

Before the signal enters the ΔΣM, a de-interleaving operation is needed. However, the implementation of such de-interleaver is already explained in subsubsection 3.2.1.3, moreover, the implementation with 64 phases is too big for a single figure and dividing it will result in unnecessary figures which would complicate the explanation. For those reason the 64 phase implementation will not be shown here.

With the de-interleaving operation done, the signal is ready to enter the ΔΣM, which is depicted in Figure A.8. This figure shows the polyphase implementation of the ΔΣM, where each smaller block is a ΔΣM core. As can be seen only the first core has its filter states initiated with the constant zero, than all other cores received its states from the core before. As can be seen in Figure A.9 these states are passed to the filter inside the ΔΣM core, which is depicted in Figure A.10. This filter is a fourth order filter, however, due to some coefficients being zero only five states are needed. These five states correspond to each delay introduced in the signals path by the FIR filter. In order to initiate these registers with the values that come from the previous ΔΣM core, a controller, depicted in Figure A.11, sends a value to the multiplexer in order to chose the correct input to be sent into the output. The value of the register "Constant8" is changed in order to change the controller's behaviour. I.e., if this value is 1, the controller gives the following output $[0, 1, 1, ...]$, if this value is changed to 2, the output of the controller changes to $[0, 1, 2, 2, ...]$. This behaviour allows for the filter to start its operation with the states from the previous ΔΣM core, while seamlessly passing to process the input samples. Finally, the remaining sub-block of the ΔΣM is the quantizer. This block can be seen in Figure A.12, where the incoming signal is slice in 3 different signals. The top signal only contains one bit and it's redirected directly to the output of the quantizer. The remaining to signals will result in the error of quantization. Because the original signal had 5 bits to its integer part, the reaming two signals are, from top to bottom, the lower four bits of the integer part and the rest of the bits are the decimal part. As the error is the difference between the original signal and the signal that goes to the output, the ROM is filled with the values of this subtraction and the four bits of the integer part are used as address. Then, as

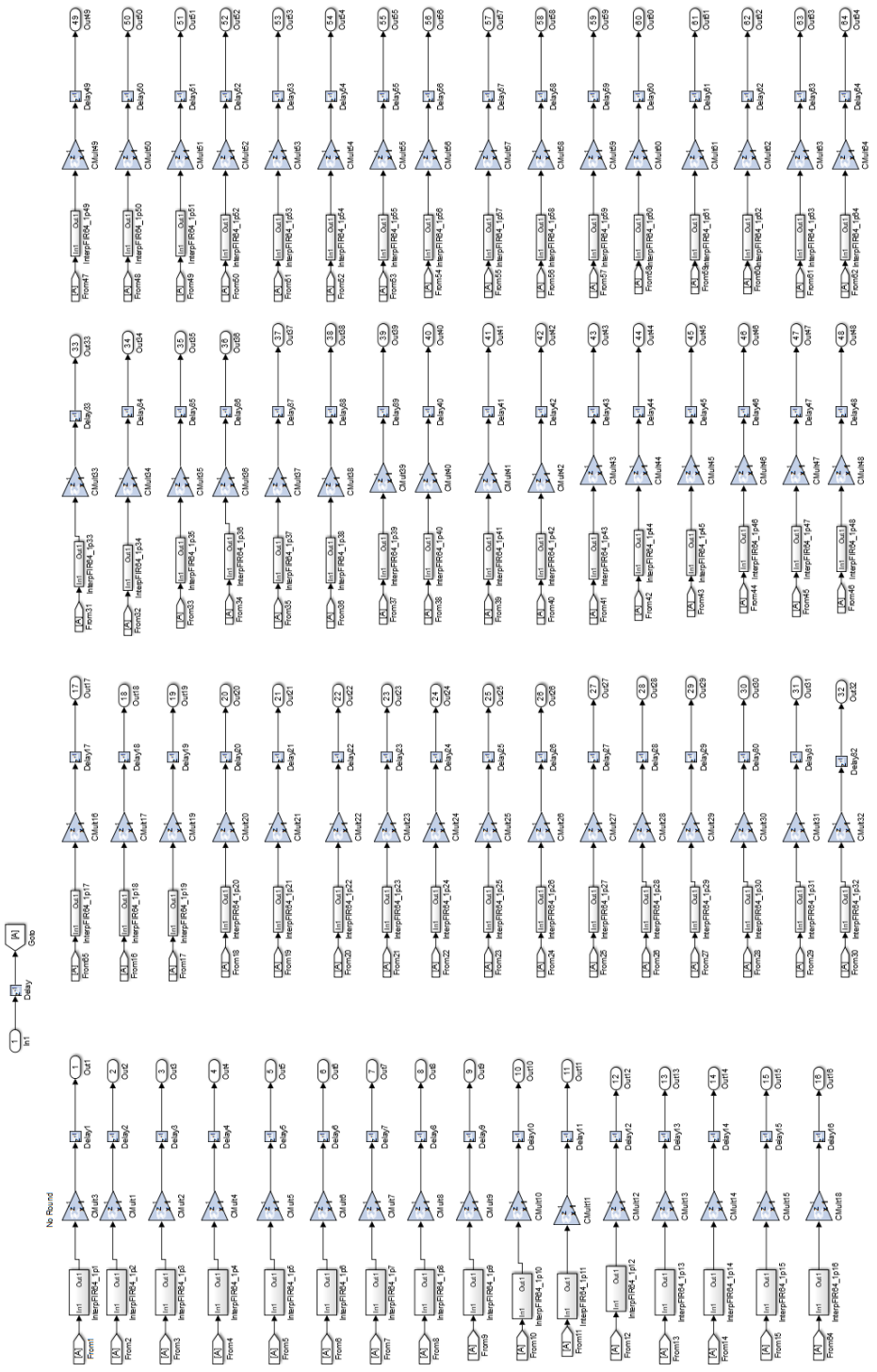


Figure A.2: Polyphase interpolation filter implementation.

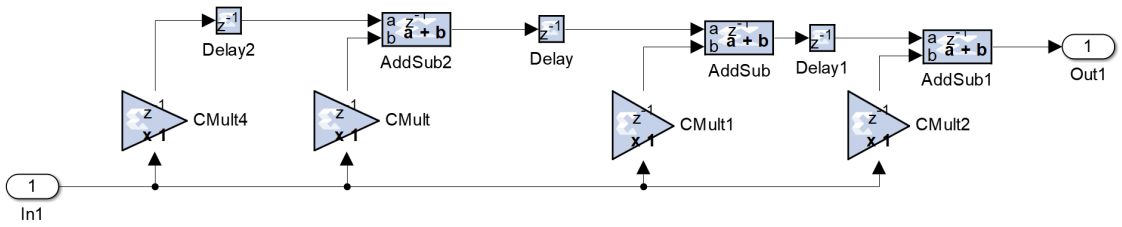


Figure A.3: FIR filter implementation.

---

the decimal part is not changed because the output has no decimal part, the value from the ROM is added to the decimal bits, resulting in the final error signal. The reader can also find a more theoretical explanation of the $\Delta\Sigma$M core in subsubsection 3.2.1.4.

With the conclusion of the $\Delta\Sigma$M, the signal goes to the interleaver. As was done for the de-interleaver, the interleaver block will also not be shown. However, the reader can find a detailed explanation of the working principle of this block in subsubsection 3.2.1.5.

The final block that the signal passes is the MGT, this block works as a serializer, passing the signal from the polyphase representation into a single phase one. The implemented MGT has an output bit rate of 8 Gbit/s.

Finally, the last block is the controller. This block can be seen in Figure A.13 and it is responsible for giving the enable signals for both the digital upconversion and de-interleaver and interleaver blocks.

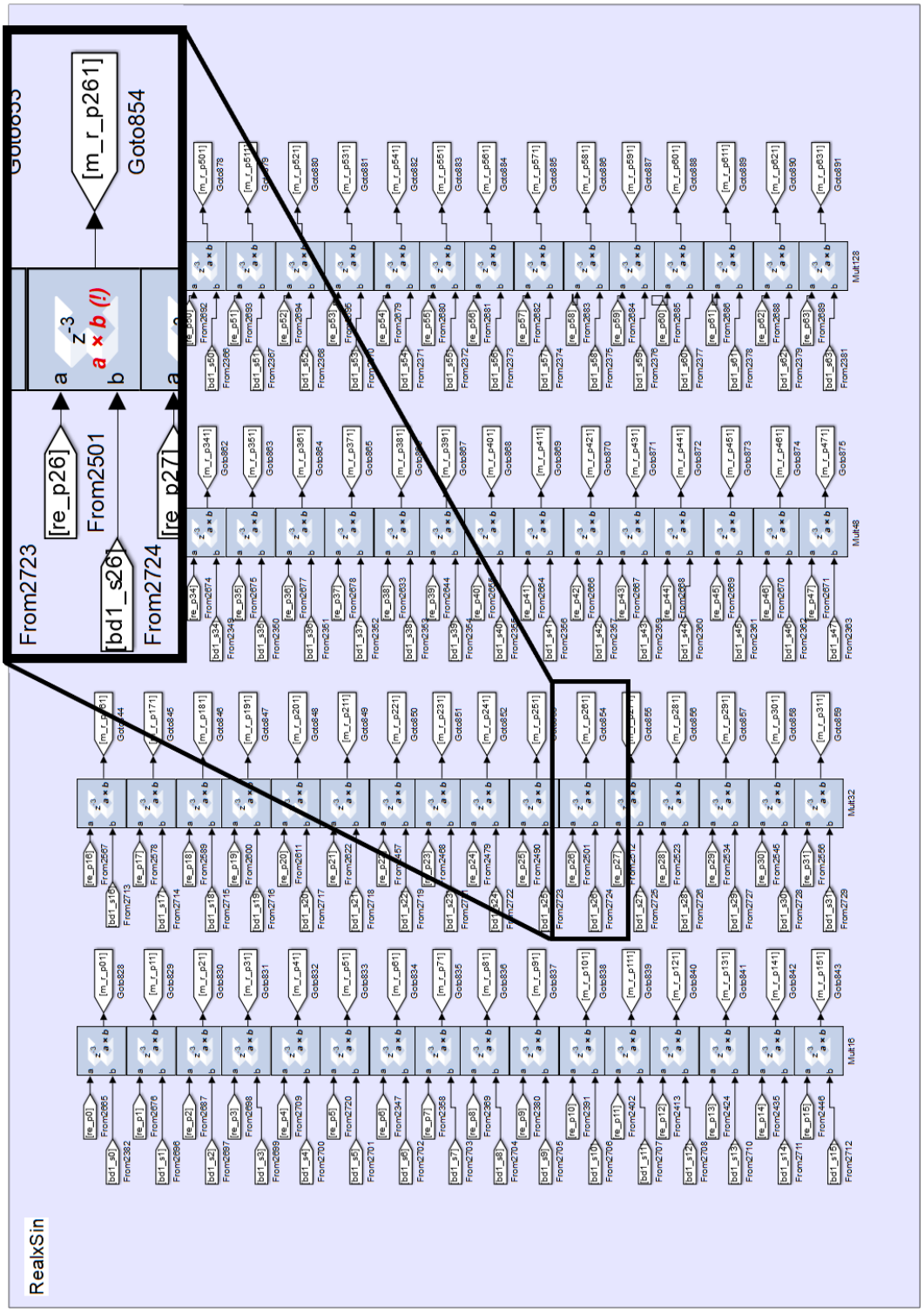


Figure A.4: Multipliers polyphase implementation.

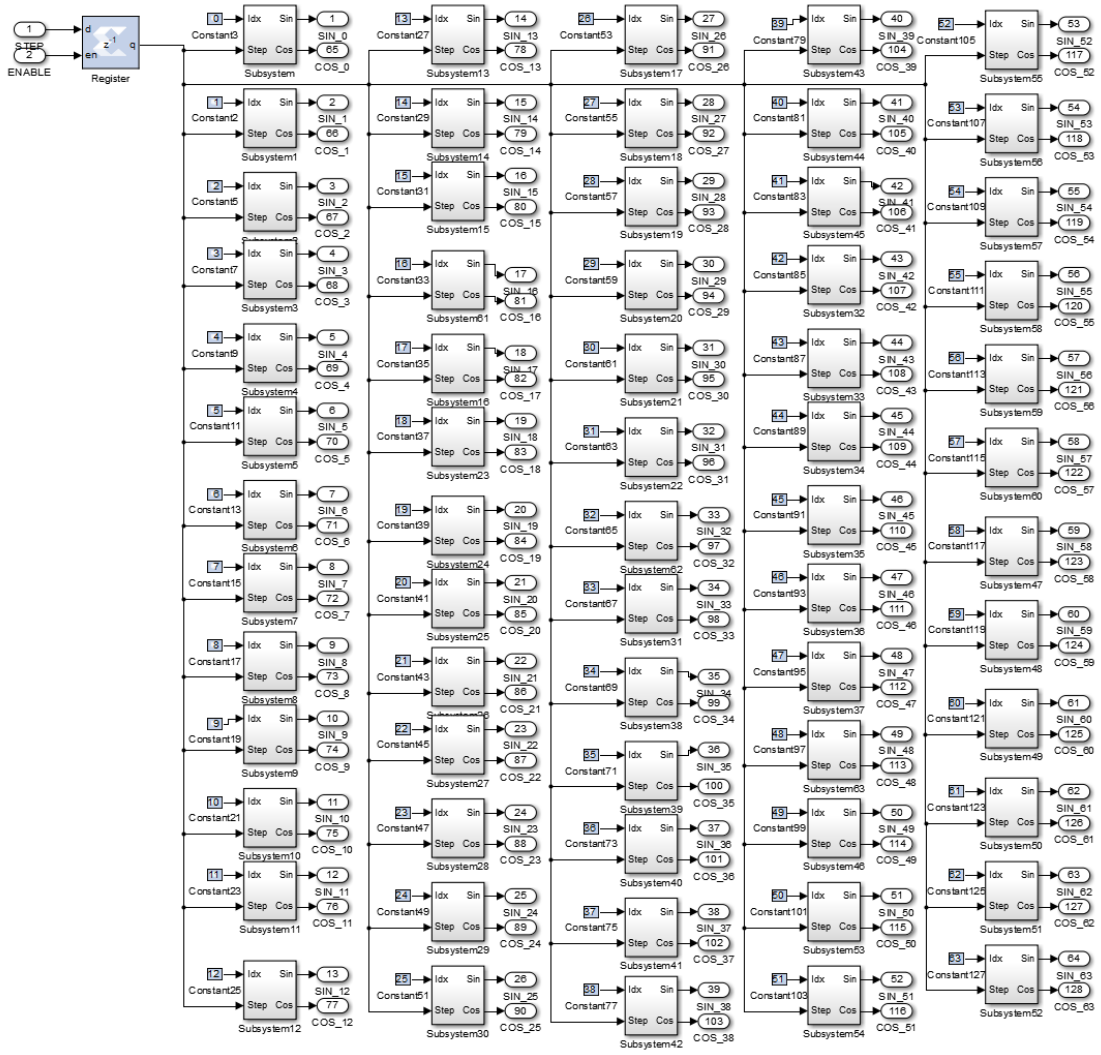


Figure A.5: Digital direct syntheses polyphase implementation.

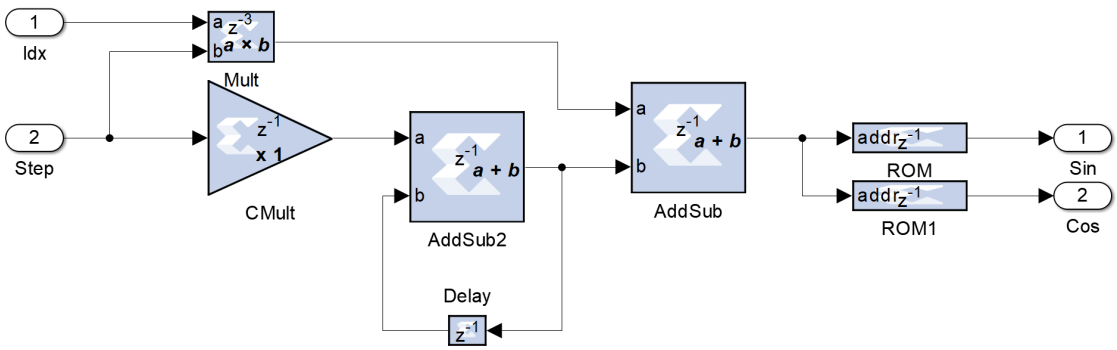


Figure A.6: Digital direct syntheses ROMs implementation.

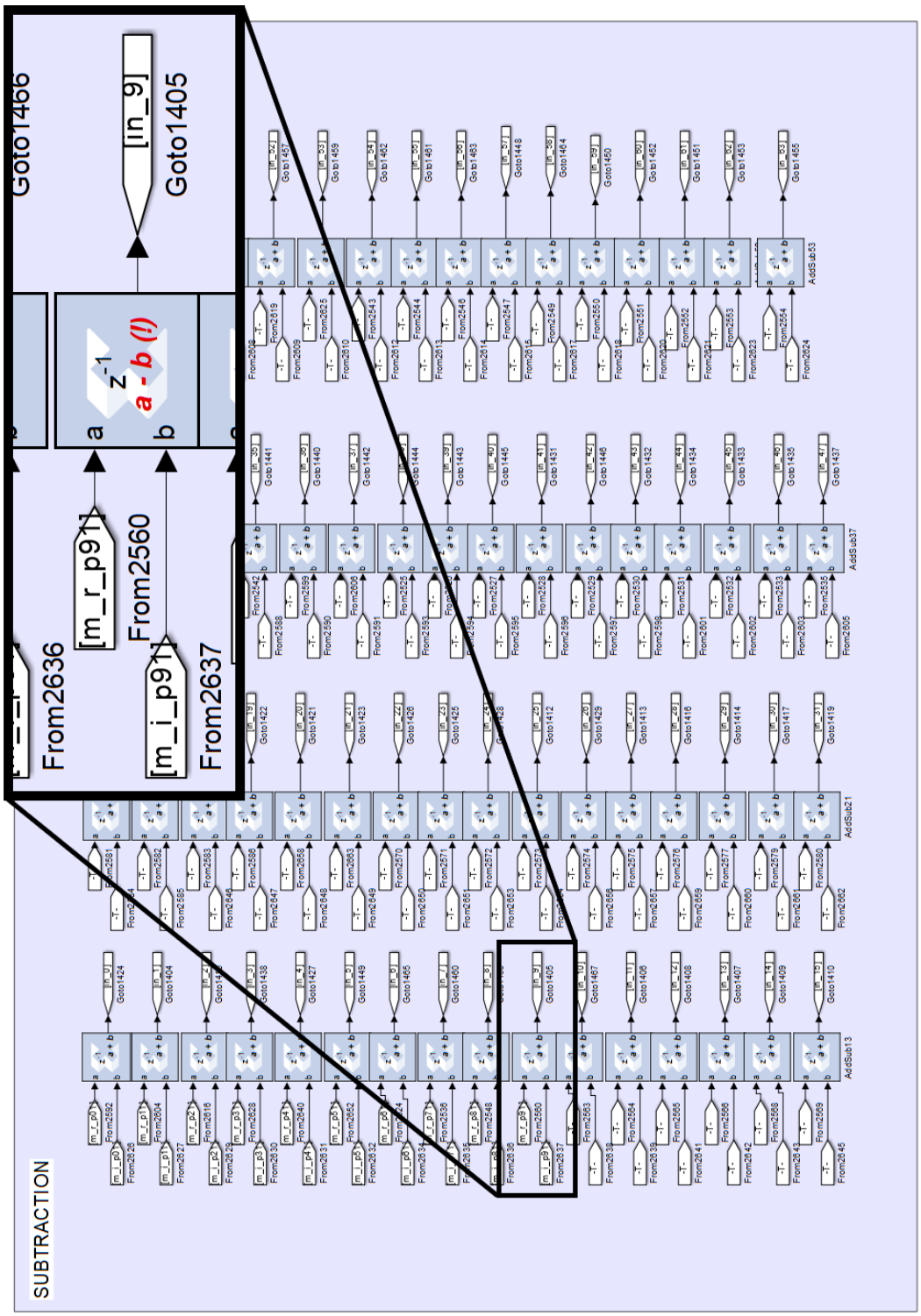


Figure A.7: Subtracters polyphase implementation.

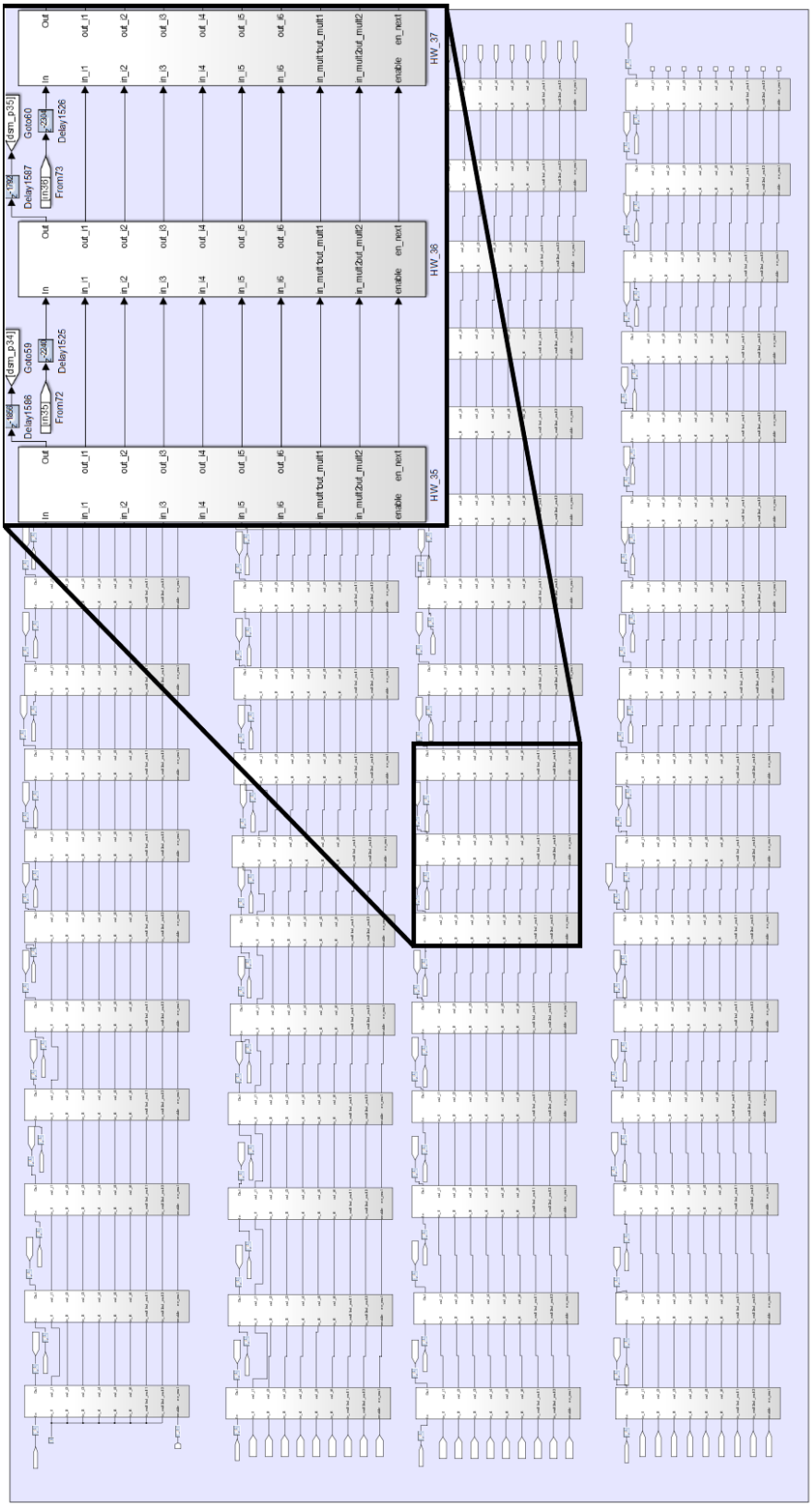


Figure A.8: DSM polyphase implementation.

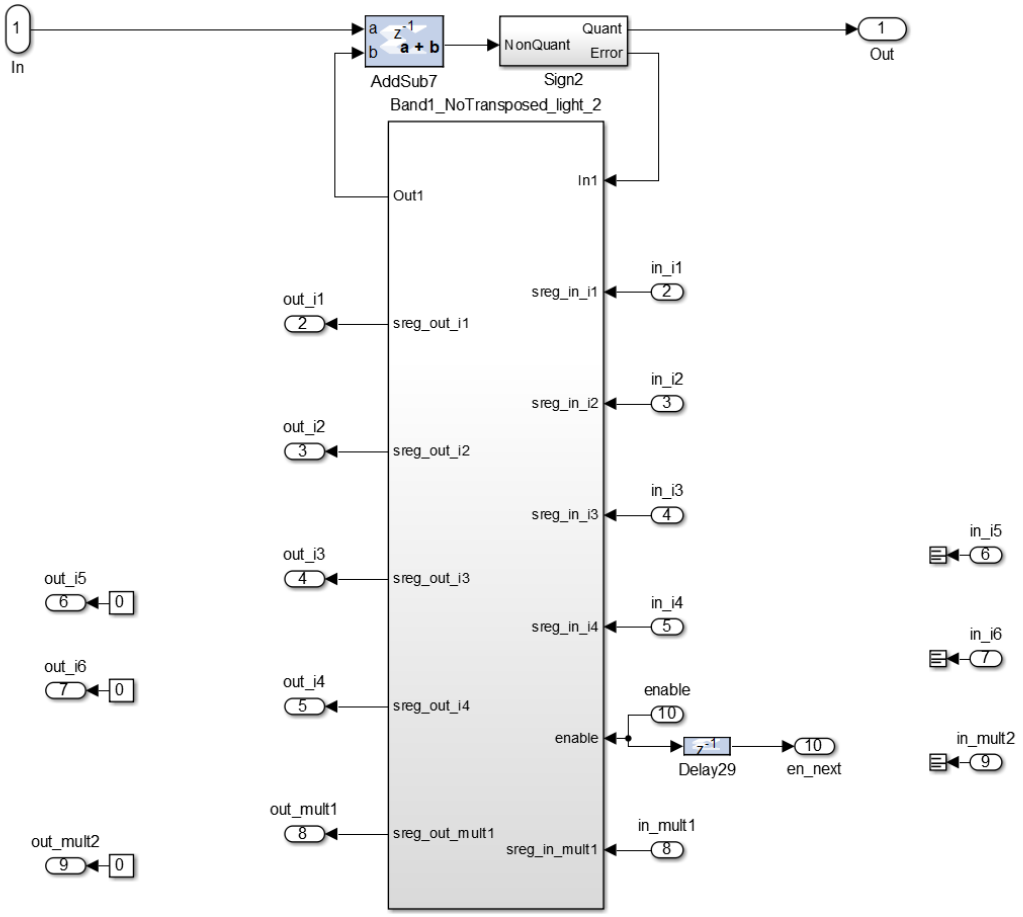


Figure A.9: DSM core implementation.

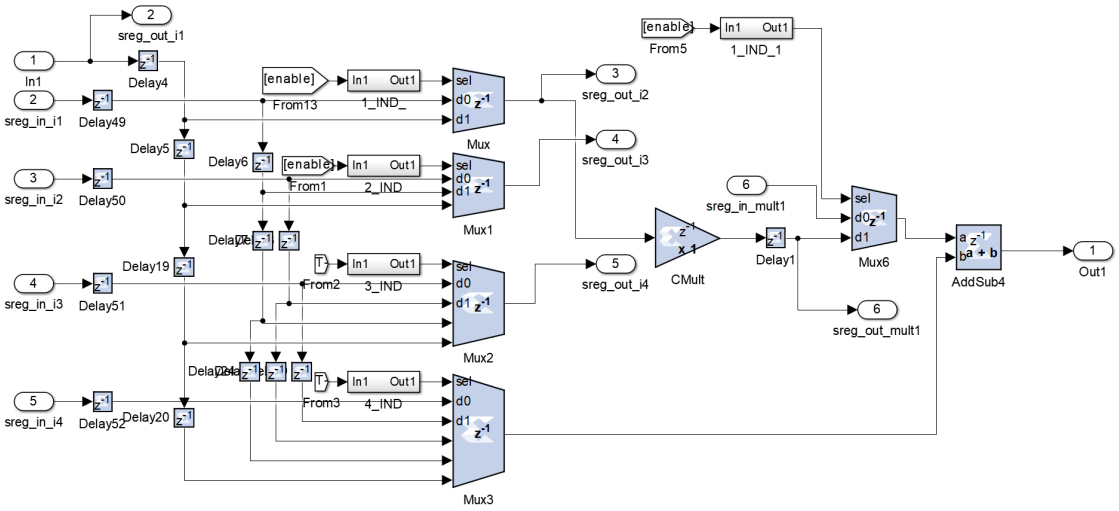


Figure A.10: DSM core filter implementation.

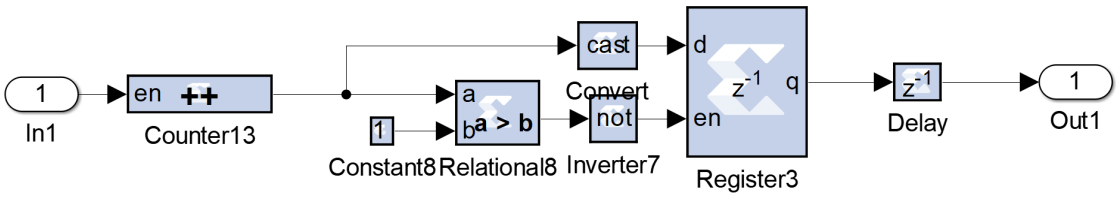


Figure A.11: Filter states initiation controller implementation.

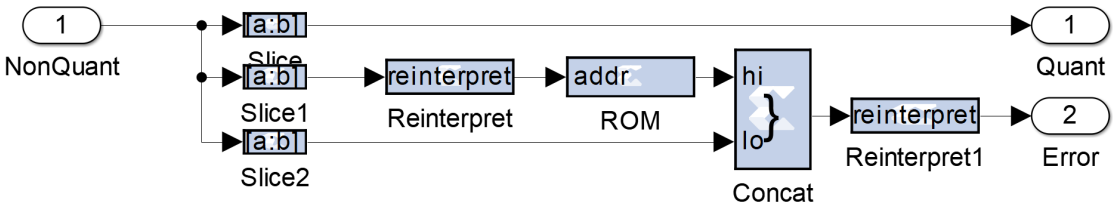


Figure A.12: DSM's quantizer implementation.

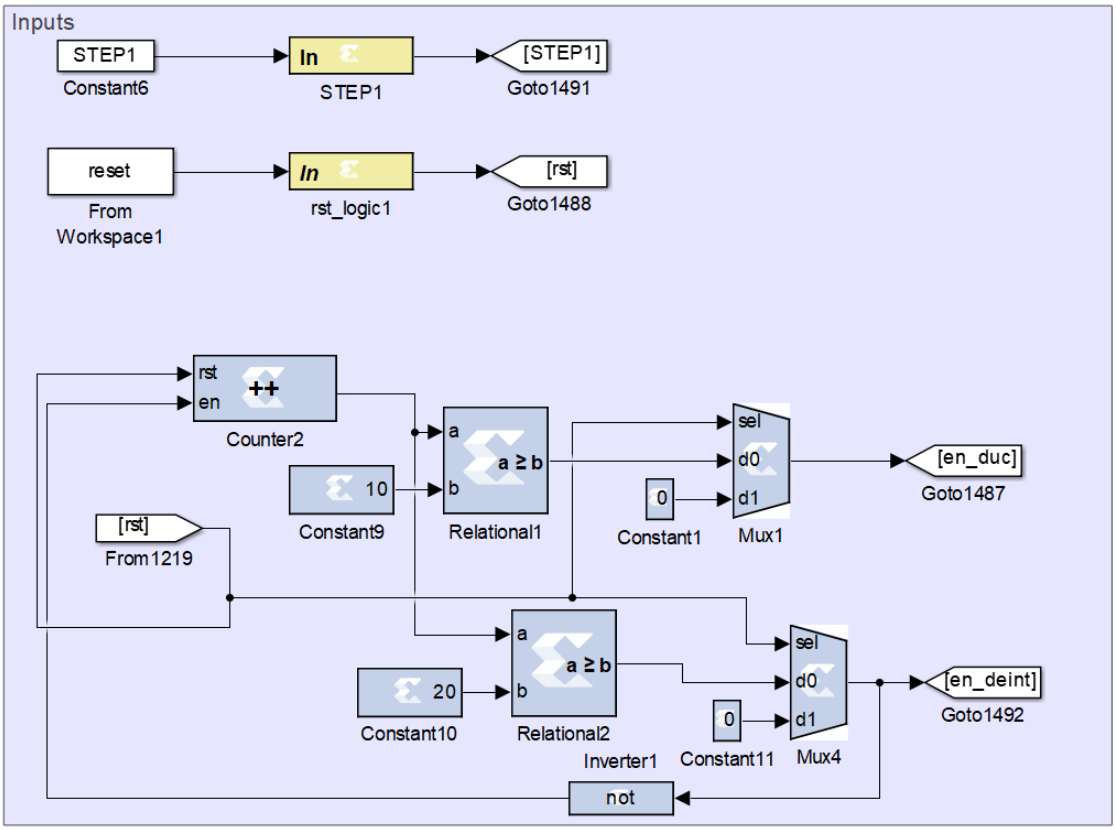


Figure A.13: Control implementation.

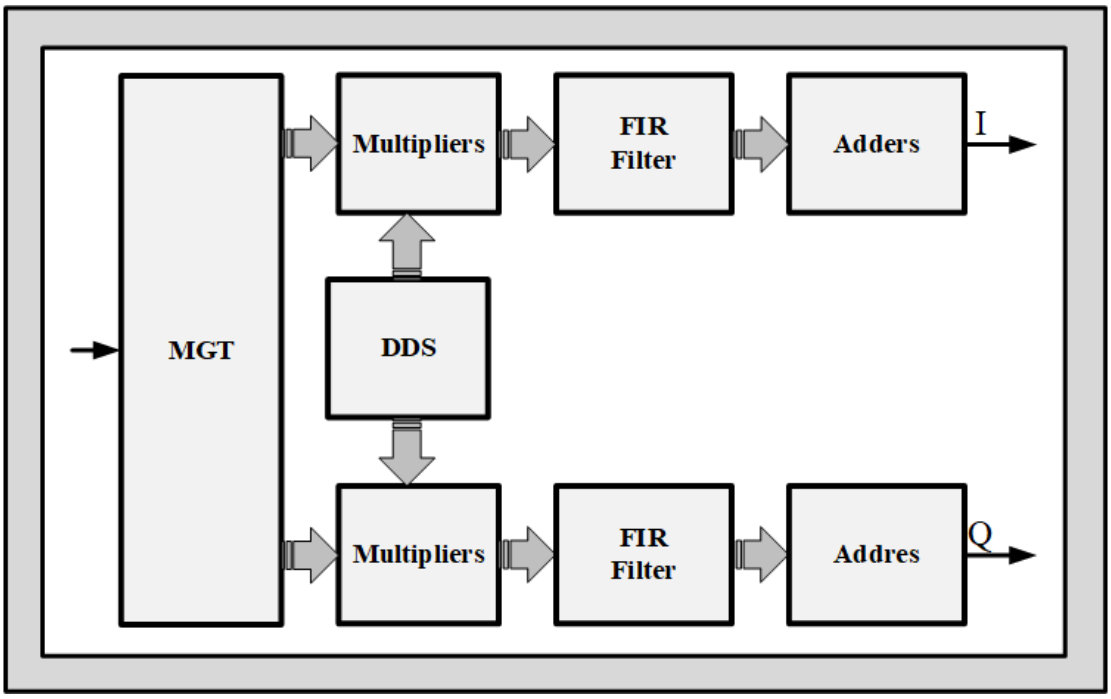


Figure A.14: Receiver top-level architecture.

Receiver

As it was the case for the transmitter, also in the receiver, the top-level architecture will only be shown in its logical form. In Figure A.14, a depiction of the receives architecture can be seen. The signal is sampled at 8 Gbit/s and then converted into a 64 phase signal in the MGT. After this the same implementation of the DDS present in the transmitter is now used for the downconversion. However, the multiplication block was changed and now the multiplication is done using multiplexers. The top-level architecture of this multiplication can be seen in Figure A.15, while in Figure A.16, the reader can see the implementation of on the multiplexers. After this downconversion the signal is filtered using a FIR filter. This filter is a decimation polyphase FIR filter and so it has 64 inputs and only one output. In the implementation this filter, which was explained theoretically in subsubsection 3.2.2.2, the smaller filters and the addition was separated. The filter implementation can be seen in Figure A.17, which presents the the clear division of the filter in FIR filter itself and the adders. The implementation of the polyphase FIR filter can be seen in Figure A.18, the smaller FIR filters are the same as the ones in Figure A.3 and so they are not shown here. Finally the implementation of the adders can be seen in Figure A.19, this block is the one responsible for the conversion of the signal back into a single phase representation.

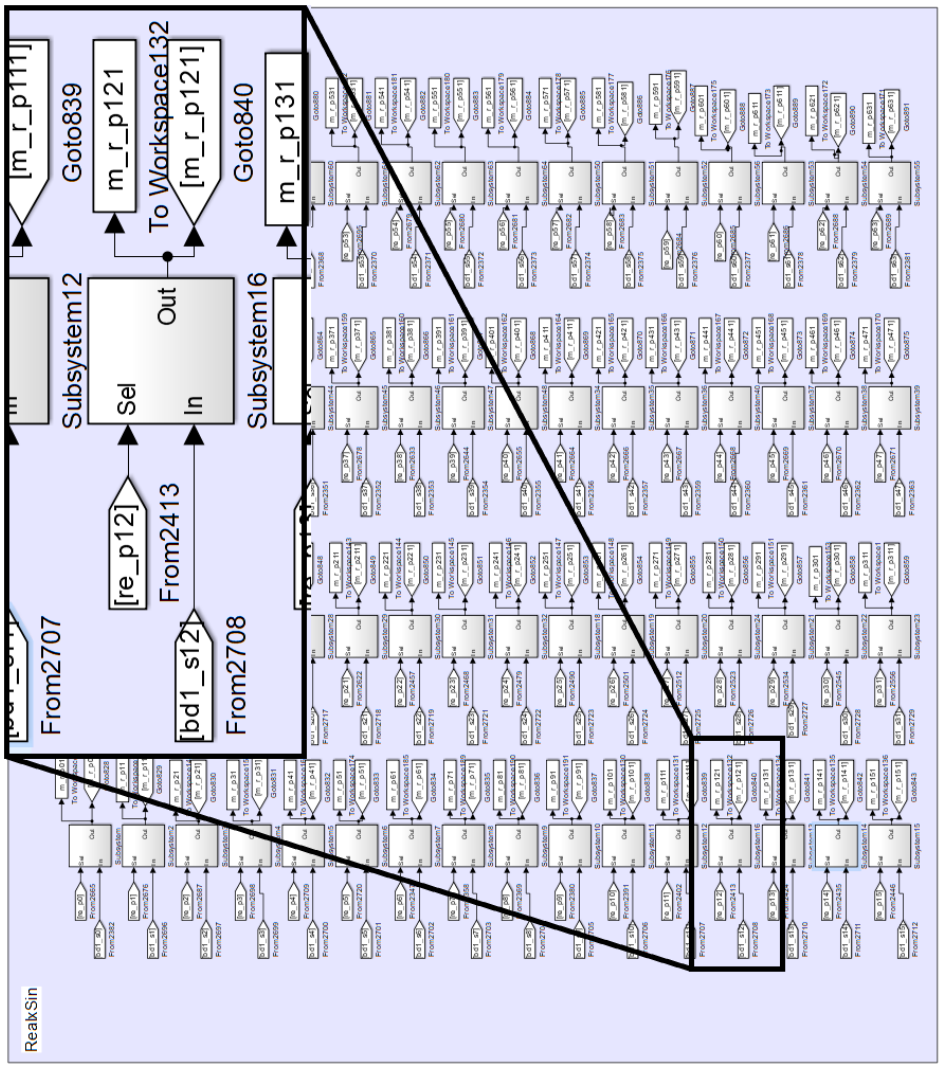


Figure A.15: Multiplication top-level architecture.

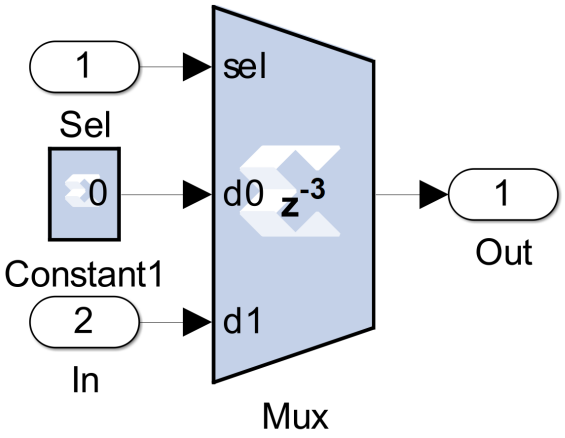


Figure A.16: Multiplication's multiplexer implementation.

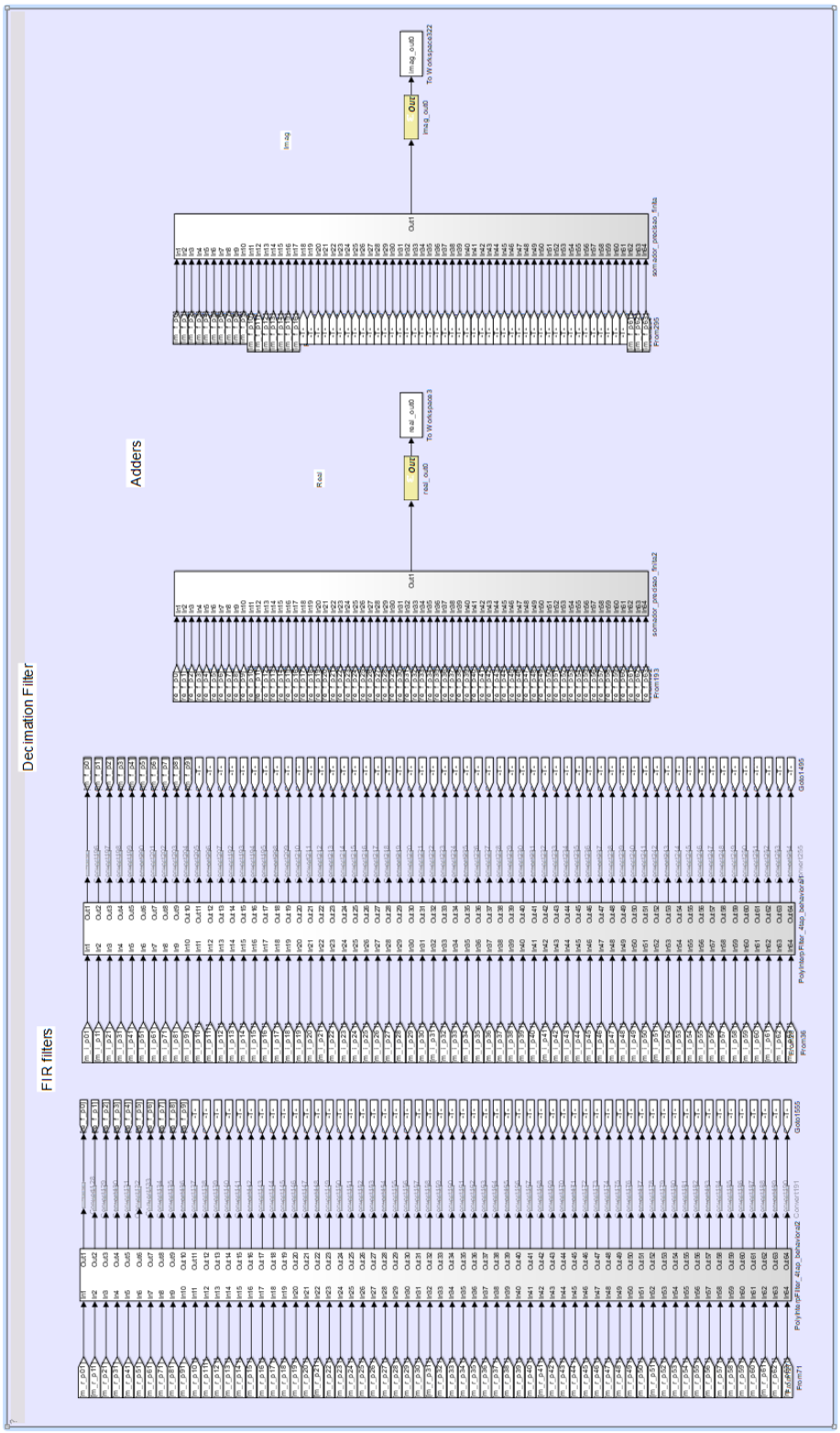


Figure A.17: Filter top-level architecture.

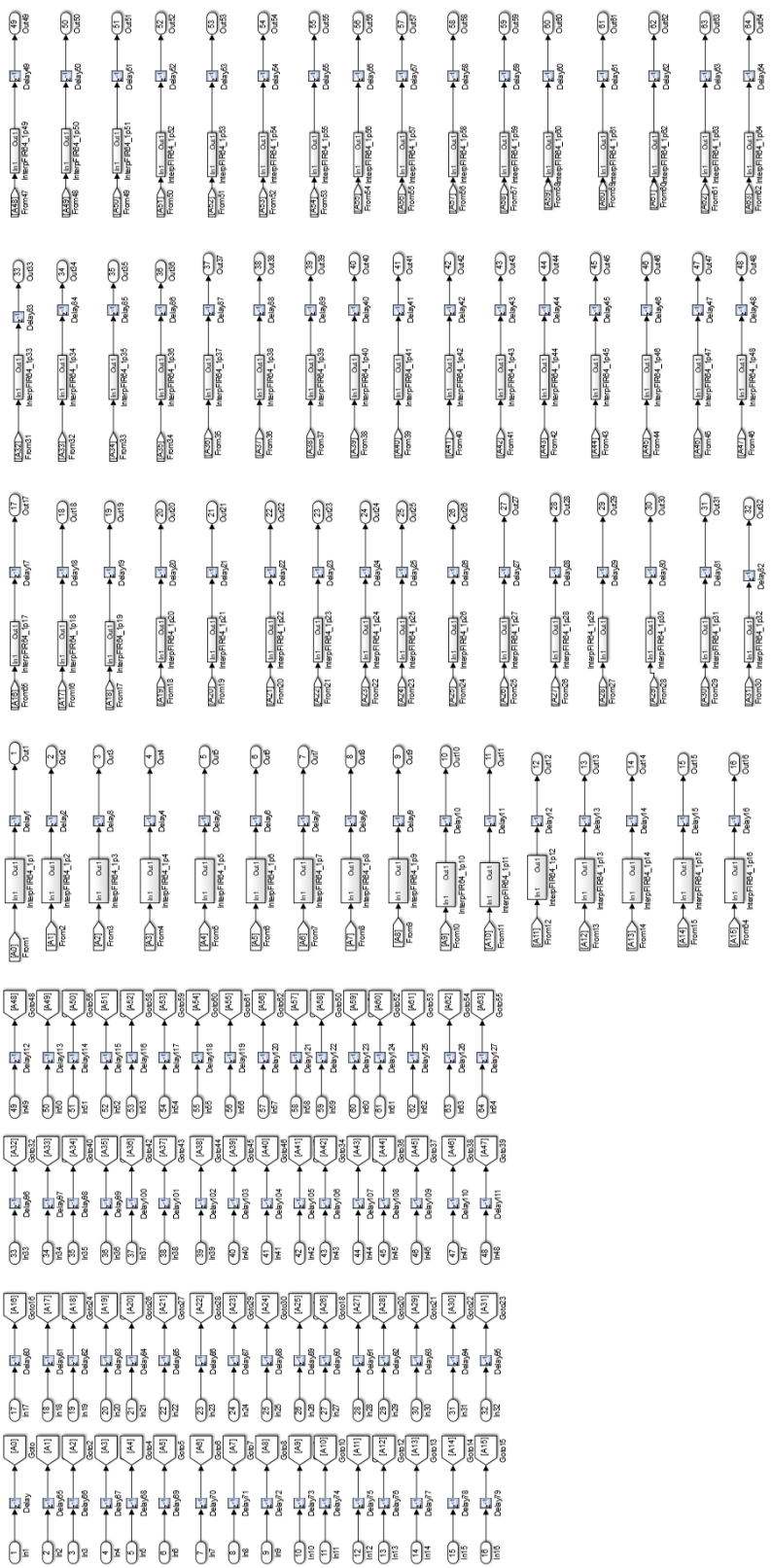


Figure A.18: Filter polyphase implementation.

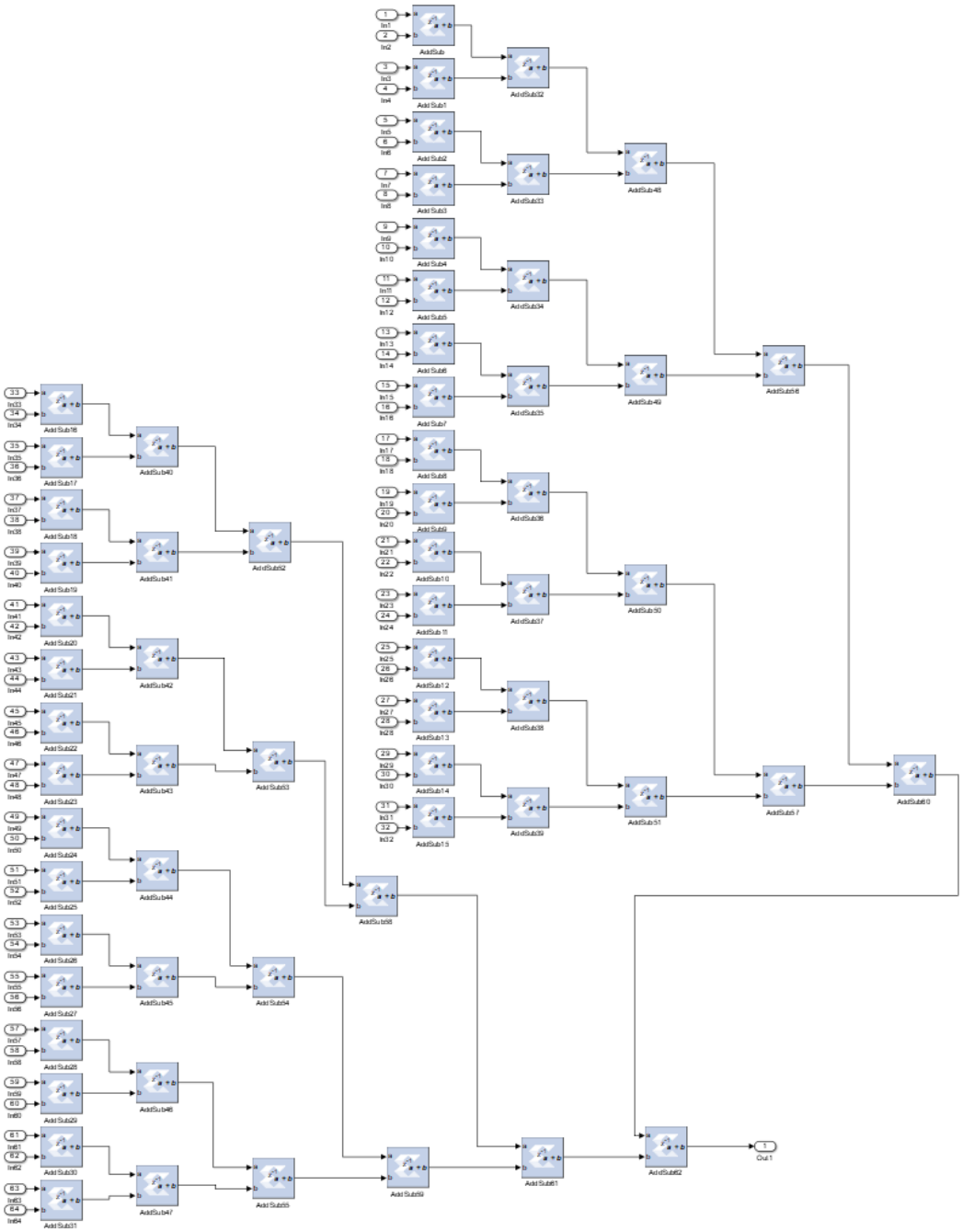


Figure A.19: Adders polyphase implementation.

Bibliography

[1] J. G. Andrews, S. Buzzi, W. Choi, S. V. Hanly, A. Lozano, A. C. K. Soong, and J. C. Zhang, "What Will 5G Be?", Selected Areas in Communications, IEEE Journal, vol. 32, n 6 , pp. 10651082, 2014.

[2] "Get ready for 5G", Nokia Networks, (2018). [Online]. Available: `https://networks.nokia.com/5g/get-ready`. [Accessed in 14^{th} of June 2018].

[3] Ofcom, "Update on 5G spectrum in the UK Statement", 2017. White Pap. [Online]. Available: `https://www.ofcom.org.uk/__data/assets/pdf_file/0021/97023/5G-update-08022017.pdf`. [Accessed in 18^{th} of June 2018]

[4] China Mobile, "C-RAN: the road towards green RAN", White Pap. ver 2.5, 2011.

[5] R. F. Cordeiro, A. S. R. Oliveira, and J. Vieira, "All-Digital Transmitter with RoF Remote Radio Head", IEEE MTT-S International Microwave Symposium (IMS), 2014.

[6] S. Hori, T. Yamase, M. Tanio, T. Kaneko, N. Tawa, K. Motoi, and K. Kunihiro, "A digital radio-over-fiber downlink system based on envelope delta-sigma modulation for multi-band/mode operation", IEEE MTT-S International Microwave Symposium (IMS), 2016.

[7] J. Mitola, "The software radio architecture", IEEE Communications Magazine, vol. 33, no. 5, pp. 26-38, May 1995.

[8] R. F. Cordeiro, A. Prata, A. S. R. Oliveira, J. M. N. Vieira, and N. B. Carvalho, "Agile All-Digital RF Transceiver Implemented in FPGA", IEEE Trans. Microw. Theory Techn., vol. 65, issue 11, 2017.

[9] R. F. Cordeiro, A. S. R. Oliveira, J. Vieira, and N. V. Silva, "Gigasample Time-Interleaved Delta-Sigma Modulator for FPGA-based All-Digital Transmitters", 17th Euromicro Conference on Digital System Design (DSD), pp. 222-227, 2014.

[10] D. C. Dinis, R. F. Cordeiro, F. Barradas and A. S. R. Oliveira, "Agile Single- and Dual-band All-Digital Transmitter based on a Pre-compensated Tunable Delta-Sigma Modulator", IEEE Trans. Microw. Theory Techn., pp. 1-11 , 2016.

[11] D. C. Dinis, R. F. Cordeiro, A. S. R. Oliveira, and J. Vieira, "Tunable delta-sigma modulator for agile all-digital transmitters". IEEE MTT-S International Microwave Symposium Digest, pp 1-4, 2016.

[12] D. C. Dinis, R. F. Cordeiro, A. S. R. Oliveira, J. Vieira, and T. O. Silva, "A Fully Parallel Architecture for Designing Frequency-Agile and Real-Time Reconfigurable FPGA-Based RF Digital Transmitters". IEEE Trans. Microw. Theory Techn., vol. 66, pp. 1489-1499, 2017.

[13] D. C. Dinis, A. S. R. Oliveira, J. Vieira, "All-digital transmitter based on cascaded delta-sigma modulators for relaxing the analog filtering requirements", IEEE MTT-S International Microwave Symposium Digest, pp 145-148, 2017.

[14] D. C. Dinis, R. F. Cordeiro, A. S. R. Oliveira, J. Vieira, and T.O. Silva, "Improving the performance of all-digital transmitter based on parallel delta-sigma modulators through propagation of state registers", Midwest Symposium on Circuits and Systems, pp. 1133-1137, 2017.

[15] M. Tanio, S. Hori, N. Tawa, T. Yamase, and K. Kunihiro, "An FPGA-based all-digital transmitter with 28-GHz Time Interleaved Delta-Sigma Modulation". IEEE MTT-S International Microwave Symposium (IMS), 2016.

[16] M. Tanio, S. Hori, N. Tawa, and K. Kunihiro, "An FPGA-based All-Digital Transmitter with 9.6-GHz 2nd order Time-Interleaved Delta-Sigma Modulation for 500-MHz bandwidth", IEEE MTT-S International Microwave Symposium (IMS), pp. 6-9, 2017.

[17] R. F. Cordeiro, "Novel Architectures for Flexible and Wideband All-digital Transmitters", Ph.D. Thesis, Universidade de Aveiro, Aveiro, 2017.

[18] N. V. Silva, A. S. R. Oliveira and N. B. Carvalho, "Evaluation of Pulse Modulators for All-Digital Agile Transmitters", IEEE MTT-S International Microwave Symposium Digest, 2012.

[19] R. F. Cordeiro, A. S. R. Oliveira, and J. Vieira, "Relaxing All-digital Transmitter Filtering Requirements Through Improved PWM Waveforms", IEEE MTT-S International Microwave Symposium (IMS), 2015.

[20] R. Schreier, and G. C. Temes ,"Understanding Delta-Sigma Data Converters", John Wiley and Sons, 2005.

[21] R. F. Cordeiro, A. S. R. Oliveira, J. Vieira, and T. O. Silva. "Wideband all-digital transmitter based on multicore DSM". in Proc. IEEE MTT-S Int. Microw. Symp., pp. 1-4. 2016.

[22] A. Frappe, A. Flament, A. Kaiser, B. Stefanelli, A. Cathelin, R. Daouphars, "Design techniques for very high speed digital delta-sigma modulators aimed at all-digital RE transmitters", 13th IEEE International Conference on Electronics, Circuits and Systems, pp. 1113-1116, 2006.

[23] H. Al-Raweshidy, and S. Komaki, "Radio Over Fiber Technologies for Mobile Communications Networks", Artech House, 2002.

[24] S. S. Pereira, A. Lourences-Riesgo, D. C. Dinis, A. S. R. Oliveira, J. N. Vieira, and P. Monteiro, "Millimetre-Wave Real-Time All-Digital Transmitter with Electro-Optical Upconversion", International Conference on Transparent Optical Networks, 2018.

[25] A. Lourences-Riesgo, S. S. Pereira, D. C. Dinis, J. N. Vieira, A. S. R. Oliveira, and P. Monteiro,"Real-Time FPGA-Based Delta-Sigma-Modulation Transmission for 60GHz Radio-over-Fiber Fronthaul", European Conference on Optical Communications, 2018.

[26] M. Swahn, "In-vehicle communications - is fibre optic cable set to replace copper?", EE-Times, 23^{th} of April 2009. [Online]. Available: `https://www.eetimes.com/document.asp?doc_id=1276577`. [Accessed in 17^{th} of May 2018].

[27] K. Greene, "Fiber Optics on a Plane - A new type of optical switch could help aerospace engineers replace heavy copper wires with fiber, making planes lighter.", MIT Technology Review, $25^{th} of September 2006$. [Online]. Available: `https://www.technologyreview.com/s/406560/fiber-optics-on-a-plane/`. [Accessed in 17^{th} of May 2018].

[28] "Tutotial Note #5 Modulation Schemes', ZHF Communication Thecnologies AG, 2018 [Online]. Available: `https://www.shf.de/wp-content/uploads/appnotes/shf_tutorial_note_modulation_schemes.pdf`. [Accessed in 4^{th} of June 2018].

[29] J. Renaudier, A. Carbo Meseguer, A. Ghazisaeidi, P. Tran, R. Rios Muller, R. Brenot, A. Verdier, F. Blache, K. Mekhazni, B. Duval, H. Debregeas, M. Achouche, A. Boutin, F. Morin, L. Letteron, N. Fontaine, Y. Frignac, and G. Charlet, "First 100-nm Continuous-Band WDM Transmission System with 115Tb/s Transport over 100km Using Novel Ultra-Wideband Semiconductor Optical Amplifiers", 2017 European Conference on Optical Communications (ECOC), 2017.

[30] "7 Series FPGAs GTX/GTH Transceivers User Guide (UG476)", Xilinx, 2016. [Online]. Available: `http://www.xilinx.com/legal.htm#tos` [Accessed in 27^{th} of July 2018].

[31] Lou Frenzel, "Understanding Error Vector Magnitude", 2013 [Online]. Available: `https://www.electronicdesign.com/engineering-essentials/understanding-error-vector-magnitude`. [Accessed in 26^{th} of July 2018].

[32] "10G/1G Dual Rate (10GBASE-SR and 1000BASE-SX) 400m Multimode Datacom SFP+ Optical Transceiver", Finisar, 2018. [Online]. Available: `https://www.finisar.com/optical-transceivers/ftlx8574d3bcv`. [Accessed in 6^{th} June 2018].

[33] "10GBASE-ER 40km SFP+ Optical Transceiver", Finisar, 2018. [Online]. Available: `https://www.finisar.com/optical-transceivers/ftlx1672d3bcl`. [Accessed 6^{th} June 2018].

[34] J. Wang, Z. Yu, K. Ying, J. Zhang, F. Lu, M. Xu, and G. Chang, "Delta-Sigma Modulation for Digital Mobile Fronthaul Enabling Carrier Aggregation of 32 4G-LTE / 30 5G-FBMC Signals in a Single-λ 10-Gb/s IM-DD Channel", Journal of Optical Communications and Networking, Vol. 9, Issue 2, pp. A233-A244 ,2017.

[35] "Virtex UltraScale+ 58G PAM4 Transceiver-Enabled FPGA", Xilinx, 2018. [Online]. Available: `https://www.xilinx.com/support/documentation/product-briefs/Virtex-ultrascale-plus-58g-product-brief.pdf`. [Accessed 19^{th} June 2018].