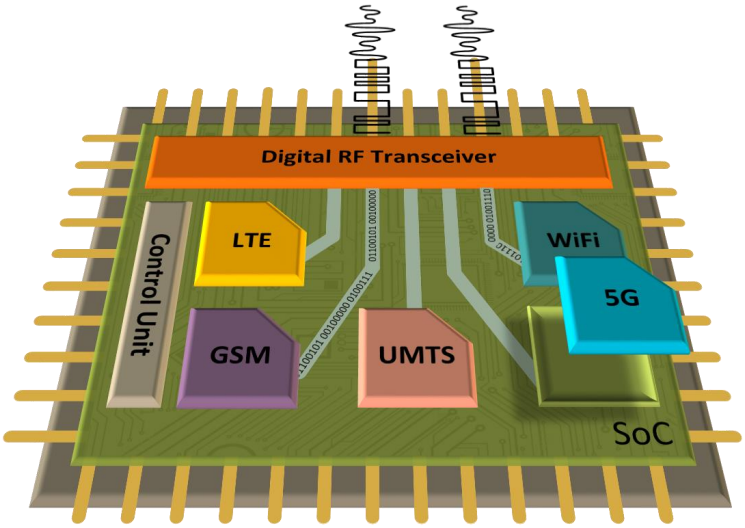
Universidade de Aveiro
Departamento de Electrónica, Telecomunicações e Informática
2018

Rui
Fiel Cordeiro

Novas Arquiteturas para Transmissores Digitais Flexíveis e de Banda Larga

Novel Architectures for Flexible and Wideband All-digital Transmitters



Rui
Fiel Cordeiro

Novas Arquiteturas para Transmissores Digitais Flexíveis e de Banda Larga

Novel Architectures for Flexible and Wideband All-digital Transmitters

Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Electrotécnica, realizada sob a orientação científica do Doutor Arnaldo Silva Rodrigues de Oliveira, Professor auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro e do Doutor José Manuel Neto Vieira, Professor auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

Apoio financeiro da FCT e do FSE no
âmbito do III Quadro Comunitário de Apoio.

o júri / the jury

presidente / president

Doutora Anabela Botelho Veloso
Professora Catedrática, Universidade de Aveiro

vogais / examiners committee

Doutor Christian Fager
Professor Associado, Chalmers University of Technology

Doutor Rui Ma
Investigador Sénior, Mitsubishi Electric Research Laboratories

Doutor Nelson José Valente da Silva
Investigador, Altice Labs

Doutor Pedro Miguel da Silva Cabral
Professor Auxiliar, Universidade de Aveiro

Doutor Arnaldo Silva Rodrigues de Oliveira (Orientador)
Professor Auxiliar, Universidade de Aveiro

agradecimentos / acknowledgements

O percurso deste Doutoramento foi cheio de altos e baixos e não teria sido o mesmo sem o apoio de várias pessoas que de uma forma ou de outra foram importantes para a realização deste trabalho. Por isto mesmo agredeço a todos aqueles que o tornaram possível.

Em primeiro lugar gostaria de agradecer aos meus orientadores Prof. Doutor Arnaldo Oliveira e Prof. Doutor José Neto Vieira que me proporcionaram a oportunidade de fazer o Doutoramento e que ao longo de vários anos me orientaram com o seu conhecimento e experiência para que o meu trabalho fosse o melhor possível.

Quero agradecer também a todos os meus colegas e amigos do Instituto de Telecomunicações a da Universidade de Aveiro sem os quais o meu percurso não só teria sido muito mais difícil, mas também muito menos interessante. Agradeço em especial ao Filipe Barradas, Ricardo Gonçalves, André Prata, Daniel Dinis, Nelson Silva, Diogo Ribeiro, Luís Cótimos Nunes, Ricardo Correia, João Santos, Daniel Belo e Tiago Varum que em muitas conversas, técnicas e não só, foram uma mostra de verdadeiro companheirismo e entreajuda.

Um agradecimento também ao Instituto de Telecomunicações, à sua direcção e aos seus funcionários, em particular ao grupo Radio Systems liderado pelo Prof. Doutor Nuno Borges, pelo suporte no meu percurso científico ao oferecer excecionais condições de trabalho e ao fomentar a exposição pública do meu trabalho.

O agradecimento também para a Fundação para a Ciência e Tecnologia (FCT), Universidade de Aveiro (UA) e ao Instituto de Telecomunicações (IT) pelo suporte financeiro oferecido no decorrer deste Doutoramento.

Quero também dar um agradecimento especial à Nádia que nos últimos anos tem tido a paciência para me suportar nos meus piores momentos, e cuja paciência tem sido um importante pilar de apoio na minha vida.

Finalmente, o maior agradecimento de todos vai para os meus pais, João e Amália, pelo seu incansável apoio e amor nos bons e acima de tudo nos maus momentos. Sem eles nunca teria chegado a este ponto da minha vida e acima de tudo não teria suportado as dificuldades com que me cruzei. É graças ao seu esforço e sacrifício que foi possível chegar aqui.

Palavras-chave

Transmissores RF Digitais, Rádio Definido por Software, Arquitecturas Reconfiguráveis, FPGA, Modulação Delta-Sigma, Modulação por Largura de Pulso.

Resumo

A próxima geração de comunicações sem fios (5G) exigirá taxas de transmissão mais elevadas, maior eficiência energética e uma melhor cobertura fazendo um uso mais eficiente do espectro de radiofrequência e adotando o uso de arquiteturas rádio mais flexíveis. Para cumprir tais requisitos, o desenvolvimento de novos dispositivos rádio será substancialmente mais complexo do que nas gerações anteriores. O futuro das comunicações rádio depende maioritariamente de dois fatores; o baixo consumo de potência e o uso inteligente dos recursos e tecnologias disponíveis. As abordagens convencionais para a camada física dos sistemas rádio não são as mais adequadas para lidar com a necessidade de dispositivos multi-banda e que usem múltiplos standards, por serem soluções ineficientes e demasiado caras para esse efeito.

Os transmissores rádio completamente digitais têm vindo a ser apresentados na literatura como uma solução inovadora e mais flexível para a implementação dos futuros sistemas de rádio. Os transmissores completamente digitais apresentam uma implementação da cadeia de processamento rádio, desde a banda-base até à conversão para RF, completamente constituída por lógica digital. Este conceito tira partido da vasta integração alcançada nas arquiteturas digitais, juntamente com a flexibilidade proveniente da digitalização das arquiteturas rádio que já se encontra em curso com a evolução dos rádios cognitivos e definidos por software. No entanto, devido a algumas limitações inerentes à tecnologia, este tipo de transmissores ainda não é amplamente utilizado na maioria dos sistemas.

Esta tese de doutoramento propõe e avalia novas arquiteturas para transmissores completamente digitais, bem como novas técnicas de processamento de sinal que possam beneficiar das tecnologias de implementação existentes (e.g. FPGAs) por forma a construir novos transmissores digitais de forma eficiente e flexível. O objetivo desta tese é reduzir as limitações atuais ainda presentes neste tipo de transmissores, nomeadamente as relacionadas com a eficiência, largura de banda, cancelamento de ruído e falta de flexibilidade. Na parte inicial desta tese é realizada a revisão do estado da arte das diversas topologias de transmissores digitais bem como as suas principais vantagens e limitações técnicas. É também feita uma análise comparativa das diversas técnicas apresentadas em termos da sua eficiência energética, flexibilidade, desempenho e custo.

De seguida, é apresentado o trabalho desenvolvido no contexto desta tese de doutoramento, seguindo-se uma discussão focada na resolução das atuais limitações deste tipo de transmissores. A primeira parte foca-se no uso de técnicas de processamento paralelo de sinal, por forma a suportar sinais de largura de banda mais elevada que os reportados no atual estado da arte.

O trabalho desenvolvido e publicado baseia-se no uso de arquiteturas implementadas em FPGA que contribuíram para um aumento da largura de banda num fator de aproximadamente dez vezes.
Outra das contribuições fundamentais desta tese consiste no aumento da eficiência do sistema através da melhoria da eficiência de codificação do sinal pulsado produzido. Com base no uso de múltiplos transmissores pulsados, é apresentado um esquema de combinação construtiva e destrutiva de sinais para a redução do ruído de quantização proveniente das técnicas de processamento de sinal pulsado usadas. Este trabalho resultou em duas importantes publicações que mostram que a melhoria da eficiência de codificação do sinal pode ser utilizada de forma a obter uma maior eficiência energética do transmissor.
Por último, são apresentadas diversas técnicas para a conversão dos sinais banda-base em sinais RF pulsados. As propostas apresentadas permitem o uso de uma arquitetura de hardware simplista, mas configurável por software, o que a torna bastante flexível. Com o uso desta arquitetura é possível alterar em pleno funcionamento a frequência central bem como a largura de banda e resposta do conversor pulsado.
O trabalho apresentado nesta tese demonstra alguns dos melhoramentos no estado da arte para transmissores rádio completamente digitais, baseando os resultados obtidos não apenas em simulações mas também na implementação e medidas realizadas sobre protótipos laboratoriais. O trabalho desenvolvido no âmbito desta tese contribuiu com avanços na implementação de transmissores ágeis, eficientes, com maior largura de banda e capazes de transmissão em múltiplas bandas com recurso a múltiplos protocolos, abrindo caminho para o desenvolvimento de novos rádios cognitivos e definidos por software.

Keywords All-Digital RF Transmitters, Software Defined Radio, Reconfigurable Architectures, FPGA, Delta-Sigma Modulation, Pulse Width Modulation.

Abstract

Next generation of wireless communication (5G) devices must achieve higher data rates, lower power consumption and better coverage by making a more efficient use of the RF spectrum and adopting highly flexible radio architectures. To meet these requirements, the development of new radio devices will be far more complex and challenging than their predecessors. The future of radio communications have a twofold evolution, being one the low power consumption and the other the adaptability and intelligent use of the available resources. Conventional approaches for the radio physical layer are not capable to cope with the new demand for multi-band, multi-standard radio signals and present an inefficient and expensive solution for simultaneous transmission of multiple and heterogeneous radio signals.

Digital radio transmitters have been presented as a solution for a newer and more flexible architecture for future radios. All-digital transmitters use a completely digital implementation of the entire radio datapath from the baseband processing to the digital RF up-conversion. This concept benefits from the use of highly integrated hardware together with a strong radio digitalization, motivated by the flexibility and high performance from cognitive and software defined radio. However, such devices are still far from a massive deployment in most of communication scenarios due to some limiting factors that hinder their use.

This PhD thesis aims to the development of novel radio architectures and ideas based on all-digital transmitters capable of improving the adaptability and use intelligently the available resources for software defined and cognitive radio systems. The focus of this thesis is on the improvement of some of the common limitations for all-digital transmitters such as power efficiency, bandwidth, noise-shaping and flexibility while using efficient and adaptable digital architectures.

In the initial part of the thesis a review of the state-of-the-art is presented showing the most common digital transmitter architectures as well as their major benefits and key limitations. A comparative analysis of such architectures is made considering their power and spectral efficiency, flexibility, performance and cost.

Following this initial analysis, the work developed on the course of this PhD is presented and discussed. The initial focus is on the improvement of all-digital transmitters bandwidth trough the study and use of parallel processing techniques capable of greatly improve common bandwidth values presented in the state-of-the-art. The presented work has resulted in several publications where FPGA-based architectures use parallel digital processing techniques to improve the system's bandwidth by a factor higher than 10.

Other fundamental contribution of this thesis is focused on the pulsed-transmitters coding efficiency. In this section of the thesis, a method is presented showing the reduction of the quantization noise created by low amplitude resolution digital transmitters using multiple combined pulsed-transmitters to cancel the noise in specific frequencies. This work has resulted in two main publications that showed how to increase the coding efficiency of the pulse-transmitters as well as the overall efficiency of the transmission system.

Lastly, new-noise shaping methods are presented in order to develop new and more flexible architectures for all-digital transmitters. The methods presented use new quantization processes that allow for the shaping of the quantization noise produced in pulsed-transmitters while using very simple and adaptable architectures. With these new techniques, it is possible to adjust the noise frequency distribution and deliberately change the noise shape in order to change some of the transmitter's characteristics such as central frequency or bandwidth.

The work presented on this thesis has shown promising improvements to the all-digital transmitters' state-of-the-art, either in simulations and laboratory prototype measurements. It has contributed to advance the state-of-the-art in agile and power efficient all-digital RF transmitters with multi-mode and multi-channel capabilities and the improvement of the transceiver's bandwidth enabling the development of true software defined and cognitive radio systems.

Contents

List of Figures

Abbreviations

ADT	All-Digital Transmitter
ASIC	Application Specific Integrated Circuit
BB	Baseband
BP	Band-pass
BRAM	Block RAM
BW	Bandwidth
CE	Coding Efficiency
CR	Cognitive Radio
DAC	Digital-to-Analog Converter
DSM	Delta-Sigma Modulation
DSP	Digital Signal Processor
DUC	Digital Up-Convertion
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
HW	Hardware
I	In-Phase Signal Component
IF	Intermediate Frequency
LO	Local Oscillator
LP	Low-pass
LUT	Look-Up Table
MGT	Multi-Gigabit Transceiver
MIMO	Multiple-Input Multiple-Output
MUX	Multiplexer
NCO	Numerically Controlled Oscillator
NTF	Noise Transfer Function
OSR	Oversampling Ratio
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PWM	Pulse-Width Modulation
Q	Quatdrature Signal Component
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying

RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-Only Memory
SDR	Software Defined Radio
SISO	Single-Input Single-Output
SMPA	Switched-mode Power Amplifier
SNR	Signal-to-Noise Ratio
SoC	System on Chip
SQNR	Signal-to-Quantization Noise Ratio
SSB	Single-Side Band
STF	Signal Transfer Function
TIDS	Time-Interleaved Delta Sigma
VSA	Vector Signal Analyzer

Chapter 1

Introduction

1.1 Background and Motivation

In the last decades wireless communications have witnessed a remarkable growth in terms of access points, mobile terminals and throughput to drive the demanding multimedia services and constant connectivity requirements. This has led to successive generations of mobile cellular standards from the highly successful 2G networks (GSM), going through the 3G (HSPA), up to the current 4G (LTE).

Next generation (5G) wireless communications will deliver gigabit per second data rates, with both base-stations and mobile devices capable of operating at a vast range of frequencies and using considerably wider bandwidths [ABC+14]. The cooperation between access-points and network terminals using different heterogeneous technologies will be necessary to support the needed flexibility and spectral efficiency for 5G networks. Therefore, 5G radios must efficiently answer to the new communication challenges and at the same time be capable of incorporate previous standards. An increasing use of new wireless standards with different frequencies, diverse coding and modulation schemes and targeting different applications is also taking place. In scenarios of this nature, highly flexible, power efficient and wideband radio transceivers are required to adapt themselves to the communication environment changes. In fact, for such approach, the physical layer of the radio must be able to support the simultaneous transmission of multi-band, multi-rate and multi-standard signals, which is unpractical or inefficient with conventional radio architectures [BBS+12].

Furthermore, there will be an increasing trend to digitalization motivated by the flexibility and high performance allowed by the cognitive radio (CR) and software defined radio (SDR) approaches, where mixed-signal and all digital systems will have a substantial importance in the design of radio and telecommunication systems. Radio architectures for SDR and CR rely on an highly adaptive radio transceiver with a strong foundation on digital signal processing, which will push further the radio transceiver to its digitalization and closer to the Mitola proposal (see Figure 1.1) [Mit93]. Under the SDR concept, most of the radio specification

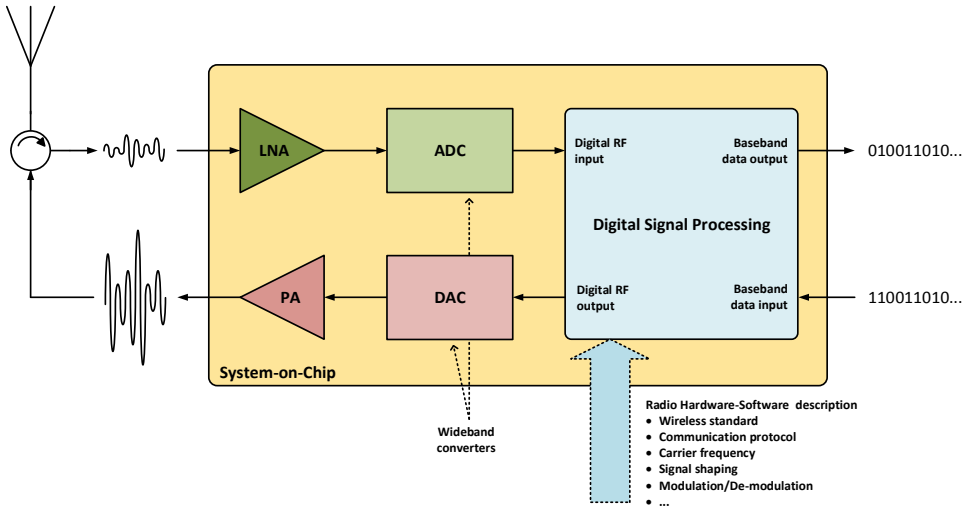


Figure 1.1: Ideal SDR system based on digital signal processing.

would be described as software and/or reconfigurable hardware, the radio functionality could be easily improved, extended or completely changed without any change to the physical hardware. Moving the software and the signal generation closer to the antenna and removing most of the conventional RF hardware from the path would be a improvement for both the mobile terminal and the base-station viewpoints. The mobile terminals, and consequently the users, could benefit from increased coverage and more flexible services with increased personalization and choices, especially due to the improved product evolution that SDR could facilitate. On the other side, base-stations could profit of faster development and time-to-market of the communication standards at a reduced cost. This would eventually lead to faster introduction of new services into the network.

Furthermore, the radio digitalization allows for the massive miniaturization of the radio hardware, since digital logic blocks continue to shrink with technology evolution following Moore's Law, which barely happens with the analog components. While decrease the area in analog circuits is usually an option, more often than not, shrinking the analog circuit leads poorer components tolerances [BBS+12]. This will eventually decrease the analog circuit performance or render it unpractical for certain radio applications. On the other hand, nowadays most of systems use a large amount of analog circuits, but also have a significant digital component (usually for the baseband processing). While mixing analog and digital circuits on a single chip is possible, it is usually troublesome and requires a set of implementation compromises that decrease both the digital and the analog circuit performances.

To sum up, it is still necessary to find the appropriate technology and radio architecture that will be capable to cope with the next generation of wireless communications challenges, specifically multi-band and multi-standard operation, and at the same time allow a shrink in size of the radio transceivers while maintaining its performance.

A definitive solution was not yet proposed, however a promising approach for the radio transmitter is the use of completely digital pulsed transmitters also called all-digital transmitters (ADT). Some flexible digital radio transceiver architectures were already presented as a solution to use under the SDR proposal [Mit93]. The use of radio signals completely described by software and a transceiver capable of changing its transmitter and receiver capabilities using digital signal processing will make the SDR concept a reality. Such concept has inherent high flexibility and it is an important step towards the development of a highly flexible radio. The last developments on this field include novel all-digital transmitter architectures where the radio datapath is digital from the baseband (BB) up to the radio frequency (RF) stage. Such concept has inherent high flexibility and it is an important step towards the development of SDR-based transmitters for next generation communication systems.

All-digital transmitters are characterized for the complete generation of RF signals with digital architectures [EHG13]. While many techniques can be used, most of presented architectures use pulse-width modulation (PWM) or delta-sigma modulation (DSM) to modulate RF signals into 2-level signals [KHM$^+$01, Sch02, JS06, NL08, CSV11]. Together with noise cancellation techniques, this allows for the direct use of these signals as a transmitter output. This class of transmitters, named pulsed-based transmitters, not only allows for a completely digital architecture but is also inherently immune to components nonlinearities, which can compromise performance in analog transmitter architectures [BBS$^+$12]. At the same time, switch-mode power amplifiers (PA) and other CMOS PA solutions are gaining increasing importance due to their high integration level and power efficiency [OJA$^+$11, SC11, NFDR12, EH13]. The computation power in common CMOS processes allows the design and production of intricate transmitter designs using completely digital or mixed-mode integrated approaches. The exploration of these new designs will eventually bring cheaper and more efficient alternatives to the classic homodyne and heterodyne radio transceivers.

However, implementing such radio for a real world communications scenario is a challenging task, where a few key limitations still prevent a wider adoption of this concept. Some of these limitations constrain the transmitter coding efficiency, achievable signal bandwidth, transceiver flexibility for multi-carrier systems, maximum carrier frequency, spectral purity or transmitted signal quality. All of these issues still need to be, either partially or fully, addressed so that the use of all-digital transmitters becomes a more widely adopted solution.

In conclusion, all-digital transmitters show the necessary adaptability for highly dense and heterogeneous wireless networks while providing exceptionally integrated architecture for the radio transceiver. However, these architectures are still subject to some performance issues that restraint their use when compared to conventional radio architectures. This thesis will focus on the improvement and proposal of digital and mixed-mode architectures capable to cope with the presented issues.

1.2 Hypothesis

In the scope of this PhD, this thesis supports the following hypothesis:

New all-digital transmitter architectures can be designed and implemented to improve the typical figures of merit in terms of bandwidth, spectral purity and flexibility while using highly integrated digital hardware.

1.3 Thesis Main Objectives

The purpose of this thesis is to study and design digital hardware architectures for efficient and spectrum flexible all-digital transmitters. The novelty consists in the use of digital processing techniques to optimize the transmitted waveforms. Between them, signal shaping, up-conversion, noise cancellation techniques and new hardware architectures are to be implemented to achieve a more flexible and efficient transmitter. Partial runtime reconfiguration of the system and the on-line capability to design optimized waveforms for custom modulations will allow a higher degree of flexibility compared to common transmitter architectures. The use of pulse-shaped transmitters has the potential benefit of a higher PA efficiency due to the constant envelop signal. With the improvement of the transmitter spectral efficiency the overall power efficiency of the system is enhanced. The hardware architectures should rely on agile and high performance all-digital transmitters, using advanced signal shaping techniques for enhanced multichannel operation as well as improved bandwidth, efficiency and noise reduction. This work will also focus on reducing the reconfiguration times and improvement of the reactivity of CR and SDR transceivers, and also tight integration of signal shaping and up-conversion techniques with FPGA-based baseband processing engines for high throughput and low latency. If possible the complete FPGA integration of the flexible transmitter should be enforced since it allows a greater degree of flexibility for the use with multiple baseband protocols in already implemented wireless communications systems. On this matter, the objectives defined for the thesis are the following:

- Study of the state-of-the-art all-digital transmitter architectures advantages and limitations. The study will focus on power efficiency, signal bandwidth, maximum carrier frequency, transmitter flexibility, signal-to-noise ratio, spectral purity and hardware integration.

- Advanced digital signal shaping techniques and corresponding implementation circuits that allow a full FPGA-based processing of high bandwidth signals.

- New noise cancellation models and its efficient implementation in reconfigurable hardware enabling the RF signal transmission with improved power efficiency and lower filtering requirements without sacrificing the adaptability.

- Novel baseband to RF up-conversion techniques and corresponding fully integrated FPGA-based realization circuits that allow the use of flexible hardware modules for configurable and simultaneous multichannel and multi-standard operation.

1.4 Main Contributions

During the course of this thesis the publications presented, with new methods and architectures, had contributed to the state-of-art for the all-digital transmitters. For a better understanding of the work here presented, the most significant contributions from the author are appended to this thesis as a support material. The following papers were published accordingly to the following themes:

On the improvement of all-digital transmitters bandwidth:

- **Gigasample Time-Interleaved Delta-Sigma Modulator for FPGA-based All-Digital Transmitters** (*Appendix C*)

  R. F. Cordeiro, Arnaldo S. R. Oliveira, José Vieira, Nelson V. Silva in *2014 17th Euromicro Conference on Digital System Design (DSD)*

  DOI: 10.1109/DSD.2014.70

- **Wideband All-digital Transmitter Based on Multicore DSM** (*Appendix D*)

  R. F. Cordeiro, Arnaldo S. R. Oliveira, José Vieira, and Tomás Oliveira e Silva in *2016 IEEE MTT-S International Microwave Symposium (IMS)*

  DOI: 10.1109/MWSYM.2016.7540117

System integration and flexible architectures:

- **All-Digital Transmitter with RoF Remote Radio Head** (*Appendix A*)

  R. F. Cordeiro, Arnaldo S. R. Oliveira, and José Vieira in *2014 IEEE MTT-S International Microwave Symposium (IMS)*

  DOI: 10.1109/MWSYM.2014.6848470

- **Agile All-Digital RF Transceiver Implemented in FPGA** (*Appendix B*)

  R. F. Cordeiro, André Prata, Arnaldo S. R. Oliveira, J. M. N. Vieira, and Nuno Borges Carvalho in *IEEE Transactions on Microwave Theory and Techniques (Volume: 65, Issue: 11, Nov. 2017))*

  DOI: 10.1109/TMTT.2017.2689739

- **Tunable delta-sigma modulator for agile all-digital transmitters**

  Daniel C. Dinis, R. F. Cordeiro, Arnaldo S. R. Oliveira, and José Vieira in *2016 IEEE MTT-S International Microwave Symposium (IMS)*

  DOI: 10.1109/MWSYM.2016.7540148

- **Agile Single- and Dual-Band All-Digital Transmitter Based on a Precompensated Tunable Delta–Sigma Modulator**

  Daniel C. Dinis, R. F. Cordeiro, Filipe M. Barradas, Arnaldo S. R. Oliveira, and José Vieira in *IEEE Transactions on Microwave Theory and Techniques (Volume: 64, Issue: 12, Dec. 2016)*

  DOI: 10.1109/TMTT.2016.2622696

- **A Fully Parallel Architecture for Designing Frequency-Agile and Real-Time Reconfigurable FPGA-based RF Digital Transmitters**

  Daniel C. Dinis, R. F. Cordeiro, André Prata, Arnaldo S. R. Oliveira, José Vieira, and Tomás Oliveira e Silva in *IEEE Transactions on Microwave Theory and Techniques (accepted for publication)*

Transmitter coding efficiency and spectral purity:

- **All-digital Transmitter with Mixed-domain Combination Filter** (*Appendix E*)

  R. F. Cordeiro, Arnaldo S. R. Oliveira, and José Vieira in *IEEE Transactions on Circuits and Systems II: Express Briefs (Volume: 63, Issue: 1, Jan. 2016)*

  DOI: 10.1109/TCSII.2015.2483198

- **A Broadband Almost-Digital RF Transmitter With an Efficient Power Amplifier**

  Wonhoon Jang, R. F. Cordeiro, Arnaldo Oliveira, and Nuno Borges Carvalho in *IEEE Transactions on Microwave Theory and Techniques (Volume: 64, Issue: 5, May 2016)*

  DOI: 10.1109/TMTT.2016.2549532

New noise shaping techniques for pulse converters:

- **Relaxing All-digital Transmitter Filtering Requirements Through Improved PWM Waveforms** (*Appendix F*)

  R. F. Cordeiro, Arnaldo S. R. Oliveira, and José Vieira in *2015 IEEE MTT-S International Microwave Symposium (IMS)*

  DOI: 10.1109/MWSYM.2015.7166799

Other related themes:

- **FPGA-based all-digital transmitters**

  R. F. Cordeiro, Arnaldo S. R. Oliveira and José Vieira in *2015 25th International Conference on Field Programmable Logic and Applications (FPL)*

  DOI: 10.1109/FPL.2015.7293995

- **All-digital transceivers - Recent advances and trends**

  André Prata, R. F. Cordeiro, Daniel C. Dinis, Arnaldo S. R. Oliveira, José Vieira and Nuno B. Carvalho in *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*

  DOI: 10.1109/ICECS.2016.7841175

1.5 Organization

This thesis is divided into four chapters. First in Chapter I, this introduction presents the background and the motivation for this thesis as well as its main objectives.

Chapter II is dedicated to the digital transmitters state-of-the-art with particular focus on recent transmitter architectures already presented in the literature and the limitations in current state-of-the-art.

Chapter III disserts about the proposed architectures realized during the course of this PhD thesis. The achivements presented focus on the improvement of the ADT's bandwidth, new noise cancelation methods and novel baseband to RF digital up-convertion techniques.

Finally, chapter IV draws a conclusion on the work presented in this thesis as well as its impact on the state-of-the-art for all-digital transmitters.

Additionally, in the end of this document a series of appendixes is presented. The appendixes are the author published papers that are relevant for the specific topics explored during the thesis. These papers are referenced through out this document and can be used as a more detailed reference for a specific topic.

Chapter 2

State-of-the-Art

2.1 Introduction

Research on flexible and agile radio transceivers based on Software-Defined Radio (SDR) is increasingly important due to the unparalleled proliferation of new wireless standards operating at different frequencies, using diverse coding, multiple modulation schemes and targeted to different ends. Different applications, costs and available technologies have helped the proliferation of diverse radio architectures.

Although the concept of SDR was idealized as mainly digital signal processing and direct RF conversion using ADCs and DACs, usually such a simplistic architecture is unachievable. This is because high carrier frequencies or large bandwidth signals are often unrealizable using direct signal conversion without any type of analog mixing, or such architectures are simply to expensive due to the need for high speed data converters and high dynamic range.

In this sense, SDR transmitters often have a multiple hardware architectures that, despite not being the ideal SDR system are still used into the so called software-defined radios. In this chapter a general overview of some potential transmitter architectures is made with a discussion of their advantages, limitations and their possible applications, with particular focus on RF pulsed transmitters.

2.2 Classical RF Single-band Transmitter

A vast number of the traditional transmitter architectures that have been implemented over the last few decades are based on either the homodyne or heterodyne transmitters. In these architectures, a local oscillator (LO) generates the RF carrier, which is mixed with the baseband/IF signal using an analog mixer or, in the case of the heterodyne transmitter, uses multiple mixing stages to shift the signal to the desired carrier frequency. Most of modern radio transmitters usually employ complex in-phase (I) and quadrature phase (Q) signals at baseband and up-convert the signal to RF using analog complex mixers.

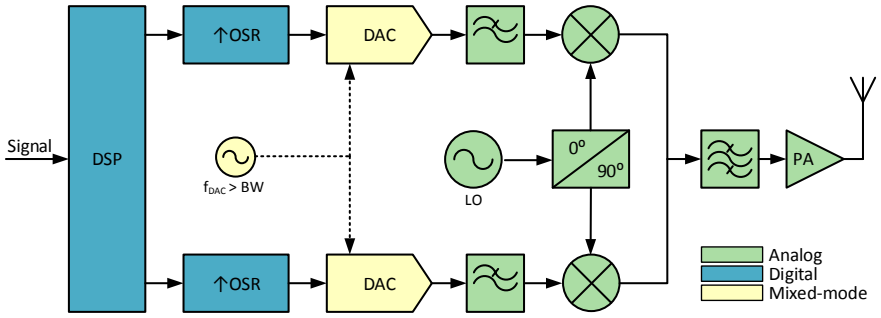


Figure 2.1: Homodyne transmitter system architecture with analog signal mixing.

The transmitter architecture in Figure 2.1 represents a homodyne zero-IF architecture. This particular architecture can be very versatile for SDR as long as the LO is capable to generate the appropriate carrier waves for in-phase and quadrature signals with adequate signal quality.

The digital baseband signal is converted to the analog domain using two DACs for the real (I) and imaginary (Q) components. After this, all the processing is analog RF. The DAC output signal is usually a non-return-to-zero reconstructed signal so there is the need to use low-pass filters to remove unwanted DAC image replicas resulting from the sampling operation. Typically these signals have only a few hundreds of MHz or less, which makes the data converters less expensive since their sampling frequency is quite low. The complex IQ mixer is used to up-convert the baseband signal up to the LO frequency in a single band up-conversion. A bandpass filter is added before the PA to remove the mixing harmonics.

While highly popular in the industry, homodyne and heterodyne transmitter architectures have a set of limitations that prevent their use in more complex or flexible systems such as multi-carrier or multi-band scenarios. In fact, these type of transmitters can not be naturally expanded to multi-carrier scenarios without the replication of the entire radio hardware. This comes at an additional cost of area for the radio transceiver that is usually large, since analog RF circuits can't be miniaturized as easily as digital circuits [BBS+12].

Other common problem for RF analog circuits is the existence of nonlinearities in the system. In fact, both the mixer and the PA are highly prone to non-linear behavior because of their analog components. Apart from suffering from nonlinearity issues, there are IQ gain and phase mismatches and LO phase noise and spurs. All these problems lead to the degradation of the signal quality at the transmitter output. In more complex architectures, with multi-carrier radio systems, there is also the interference between channels in both transmission and reception that becomes more severe for reduced area circuits [BBS+12].

For these reasons, the classic RF transmitter architectures are not suitable for efficient implementations of simultaneous multi-band, multi-carrier transmitter systems.

2.3 RF DACs

Since the analog RF mixing is one of the main sources of noise and nonlinearities in the transmitter chain, a straightforward solution is to remove the analog mixer. A possible solution would be to use direct digital to RF conversion instead of common homodyne or heterodyne architectures. This has led to the development of the RF DACs, in which the RF transmitter chains is digitally implemented in a single device and the DAC directly converts the digital RF signal to the analog domain [BCW+11]. A big advantage of the use of RF DACs is the fact that the transmitter can be implemented in a digital device, which can be reconfigurable and benefit from the shrinking in size of digital logic. This allows for the simpler design and production of multi-band and multi-mode transmitters and reconfigurable radios.

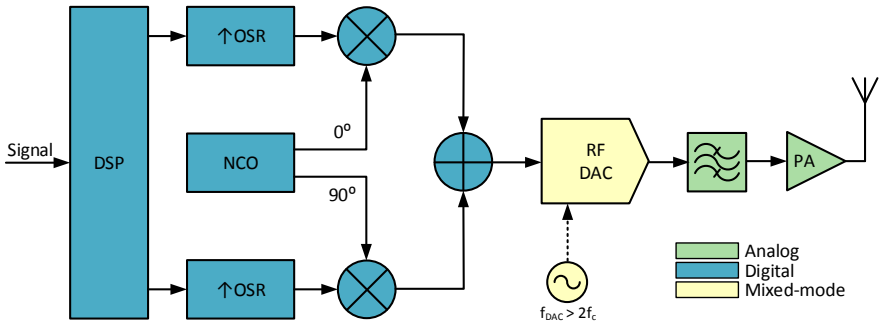


Figure 2.2: RF DAC transmitter system architecture.

The transmitter architecture presented in Figure 2.2 presents a RF DAC based radio transmitter. The complex signal components, I and Q are oversampled to a high oversampling ratio (OSR) to allow for direct digital up-conversion using a digital multiplier as mixer. The carrier wave can be generated using a numerically controlled oscillator (NCO). After combining the I and Q up-converted signals, the digital signal at the input of the DAC is a digital representation of the RF signal. Since RF DACs use direct digital up-conversion, the sampling frequency of the output DAC must be at least two times higher than the carrier frequency to respect the Nyquist sampling criterion. In fact, RF DACs have no fundamental difference from conventional DAC with exception of their very wide bandwidth [BMK+11].

However, there are some challenges in obtaining the required spectral purity at RF frequencies. RF DACs suffer several problems that are common to conventional DAC but become more evident when working at higher sampling frequencies and this may limit its application in radio systems. The major problems rely on frequency-dependent amplitude distortion and nonlinearity spurs. At close-to-Nyquist frequencies, the nonlinear effects become more evident and unwanted harmonic emissions or intermodulation products may occur [Mal07].

The DAC is essentially digital in its structure since the output is achieved by switching

weighted voltages, currents or impedances. For close to Nyquist frequencies, the output signal transitions between DAC amplitude limits are very frequent due to the oscillatory nature of the carrier wave. This means a significant part of the DAC hardware is constantly switching, which will increase its power consumption with the increase of the carrier frequency. To overcome the power and area cost of RF DAC it is possible to decrease the DAC resolution but this will make even more prominent the nonlinear spurs emissions.

Because the above mentioned reasons and the fact that most commercial RF DACs with more than 3GHz sampling frequency are yet too expensive, the use of the RF DAC is usually limited to bands under GHz for most of the applications or only used for expensive systems.

2.4 Pulsed Transmitters

In recent years, the proliferation of mobile communications networks has created a major concern in the development of new flexible radios, capable of adapting to different communication scenarios while maintaining high power efficiency. In this regard, the use of pulse-modulated signals using Pulse Width Modulation (PWM) or Delta-Sigma Modulation (DSM) associated with Switched-Mode Power Amplification (SMPA) is thought to be a promising approach for RF transmitters in SDR. Pulsed transmitters can in fact be seen as a subset of RF DACs, since they allow the output of RF signals directly from digital hardware. In other words, pulsed transmitters are 1-bit RF DACs.

Pulsed-modulation radios use the full digitalization of the radio system that poses an important step towards the complete software description of radio signals proposed in SDR. The use of digital signal processing techniques and the radio integration into a single digital chip will lead to highly flexible telecommunication systems, which will be fundamental for the next generation of wireless networks. On the other hand, in pulse-modulated transmitters, the transistor performing the power amplification behaves as a switch, dissipating less power and therefore a more efficient power conversion can be reached. Furthermore, pulse-modulation can use 2-level signals that allow power amplification with reduced in-band signal distortion resulting in a transmitter with a high in-band linearity [EHG09, EKR+11].

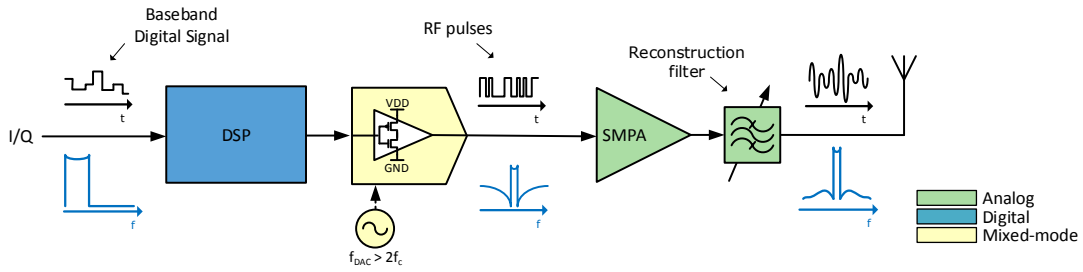


Figure 2.3: Pulsed transmitter system architecture concept.

Figure 2.3 shows the basic concept architecture for pulsed transmitters. The input signal is processed in the digital domain for either the baseband and the RF stages. The pulsed digital RF is converted to the analog domain using a high speed digital buffer and the signal is posteriorly amplified using a 2-level SMPA. An output reconstruction filter is necessary to remove the quantization noise from the pulsed signal. This filter can be made tunable to allow for different carrier frequencies.

2.4.1 Pulsed Transmitter Architectures

Recent advances involving pulsed RF transmitters include the development of novel all-digital architectures where the radio datapath is digital from the baseband up to the RF stage. These transmitters use digital representations of the RF signal and perform a 2-level quantization directly at RF rates. The conversion from multiple bit digital representation to a 2-level binary signal is usually done by means of DSM or PWM schemes. State-of-the-art pulsed transmitters presented in the literature fall within this principle, with amplitude and phase modulation of the RF carrier using band-pass DSM [JS08, JS06], PWM [OAE+12, PJ12, OJA+11, NL08], low-pass DSM with digital up-conversion [FFS+08, JS07] or hybrid DSM-PWM architectures [MHH+14].

Band-pass ADT architectures, as shown in Figure 2.4, were originally presented using band-pass DSM modulation to transmit the signal centered at RF frequencies. By using a DSM transfer function with a zero centered at the carrier frequency the quantization noise is removed from that frequency so that a signal can be transmitted in that band. Prior to the DSM stage, the signal must be up-converted digitally to the carrier frequency, hence the sampling frequency might be rather high (considering for example GHz communications). In fact the clock must be at least two times the carrier frequency, which establishes a very high sampling clock for the digital hardware.

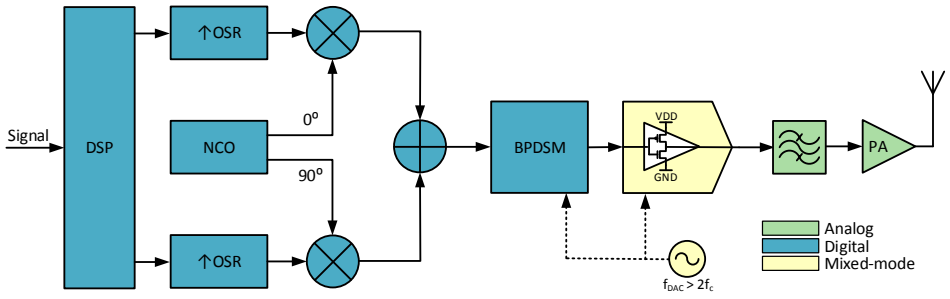


Figure 2.4: Band-pass DSM-based all-digital transmitter.

To allow for several GHz clock frequencies, typically pulsed-transmitters or all-digital transmitters (ADT) are implemented using Application-Specific Integrated Circuit (ASIC) technology. While this approach often offers a better frequency performance, alternatively a

low-pass DSM can be used in order to quantize the signal into a 2-level signal before the frequency shift to RF. The main advantage of splitting the digital transmitter in a low-pass baseband modulation and up-conversion stage is to reduce the high frequency clock requirements for the circuit logic. This away, by performing a digital up-conversion separately on the 2-level signal, it is possible to use lower clock frequency logic for most of the digital transmitter design as in Figure 2.5. Only the digital mixer at the up-conversion has to work at two times (or four times for simultaneous amplitude and phase modulation) the RF carrier. This architecture consents the implementation of a radio system with a more flexible technology, such as FPGA, for common wireless communications standards [GHA+10b, Gha10a, SADERH08, HHNG08].

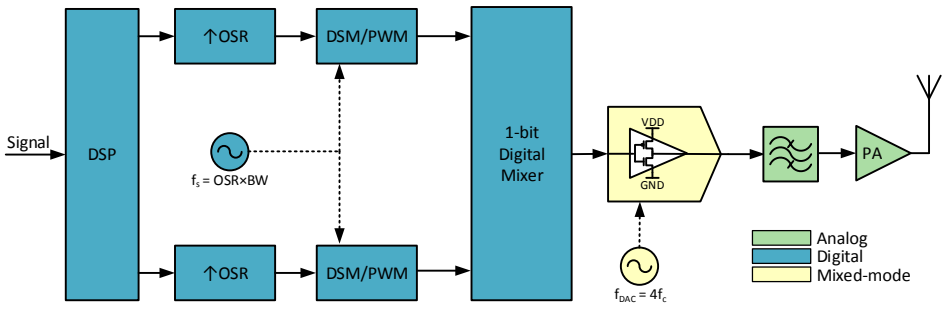


Figure 2.5: Low-pass DSM/PWM based all-digital transmitter system architecture.

While DSM applies noise shaping, which reduces the quantization noise near the carrier, it does not allow large bandwidths due to logic clock frequency limitation [EHG11]. On the other hand, with PWM logic is fairly easier to design and implement at higher rates with higher oversampling ratio (OSR), but introduces high power harmonic noise near the carrier frequency. Although, in both situations a high quality factor filter is needed to attenuate the out-of-band quantization noise, usually PWM quantization noise has higher power levels near the carrier signal.

2.4.2 Oversampling Pulsed Converters

Pulsed transmitters are usually based in pulse shaping techniques that convert a continuous signal to a pulsed oversampled version of the signal. While many techniques can be used for all-digital transmitters, the most efficient and used techniques are DSM and PWM. This section will explain the advantages and the main limitations considering all-digital radio transmitter applications.

Pulse Width Modulation

Pulse width modulation is a well known technique used for decades in control and audio applications. The conventional approach for the PWM converter is to compare a reference

signal (usually a sawtooth or triangle wave) with the input signal as shown in Figure 2.6. The comparison result will be a 2-level square wave with value +1 if the signal is higher than the reference signal and -1 in the opposite case.

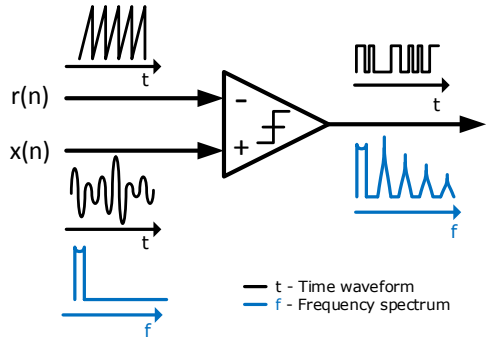


Figure 2.6: Pulse width modulation.

When using digital PWM, the input signal is typically an oversampling version of the original signal, since for a uniform sampling PWM the minimum duty cycle is set by this sampling frequency. The higher the sampling frequency, the shortest will be this minimum pulse duration that allows for a better representation of the signal. For RF signals working at GHz speeds, it may be challenging to have a comparator working at those frequencies. In such situations, polyphase implementations can be used, which reduces the clock rate demand but increases by the same factor the necessary digital logic.

Figure 2.7 shows the PWM-based ADT spectrum of a RF signal with a 1 GHz carrier. As it can be seen in the figure, PWM generates high peaks of quantization noise around the carrier frequency that limit the maximum achievable bandwidth. The PWM noise comes from the fact that the signal is quantized into a 2-level signal. This means that part of the energy of the transmitted signal is spent in quantization noise and PWM harmonic distortion, therefore this decreases the spectral and power efficiency of the transmitter.

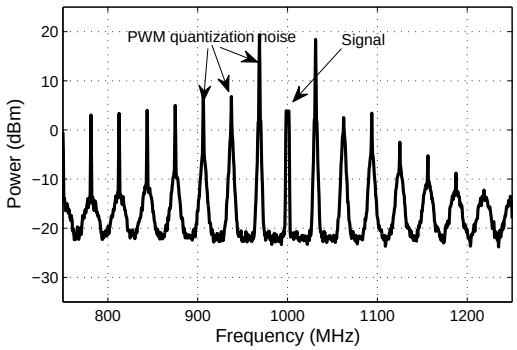
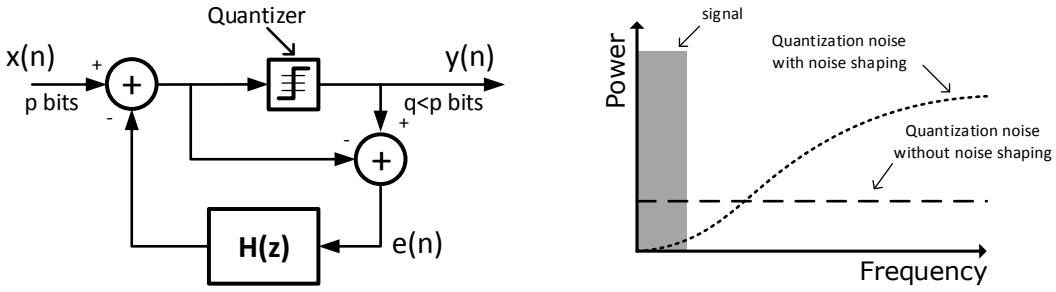


Figure 2.7: PWM-based transmitter spectrum.

Although PWM is highly popular for low frequency applications, in RF scenarios PWM-based transmitter have a set of drawbacks that limit its usability. In most cases PWM signals present a very low bandwidth or low SNR due to the quantization noise of the finite resolution PWM. Even with natural sampling PWM, where the time resolution is ideally infinite (without quantization) there are PWM harmonics limiting the available bandwidth [SS03]. There are however some techniques that can be applied to the PWM conversion that allow for the improvement of the SNR or to diminish the high power harmonic distortion peaks.



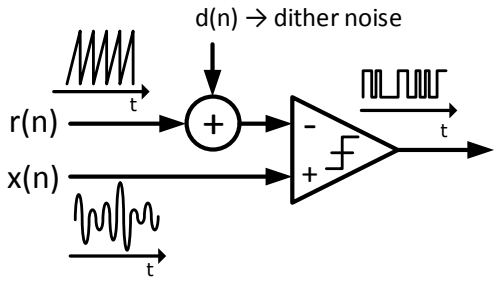
(a) Noise shaping model.

(b) Noise shaping spectrum illustration.

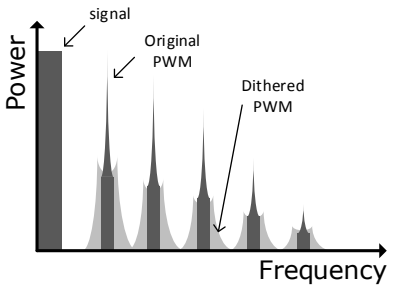
Figure 2.8: Noise shaping model from p to q bits.

Noise shaping is a technique that allows to quantize a signal to lesser amplitude levels without reducing its SNR over a given bandwidth and considering an oversampled signal. In a general form, noise shaping can be described as the model in Figure 2.8a. At the input the signal $x(n)$ is coded with p bits, after quantization the output signal is coded with q bits where $q < p$. Although this quantization process adds noise to the signal, if the filter $H(z)$ is properly chosen it is possible to filter the quantization noise so that it won't affect the signal. Since PWM is itself a quantization process, applying a noise shaping process allows a better SNR performance for the same number of PWM levels.

Other improvement to the PWM conversion is the use of dithering. PWM creates high power harmonic peaks in unwanted frequencies in the spectrum. This is undesirable for radio transmitters since it interferes with other communication channels, hence this noise must be filtered. However, it is very difficult to effectively filter the PWM harmonics since, the closer the harmonics are to the signal, the higher is their power, as shown in Figure 2.7. Dithering adds random noise to the PWM waveform so that its harmonics noise energy is spread in frequency. This is done be adding a noise source in either the signal or reference wave path before the comparison and quantization as shown in Figure 2.9a. With the added noise, the reference wave transition become non-deterministic as well as the PWM period. Without a deterministic period, the PWM spectrum will not have high energy peaks at frequencies corresponding to this transition, but instead this energy is spread around these frequencies.



(a) PWM dithering model.

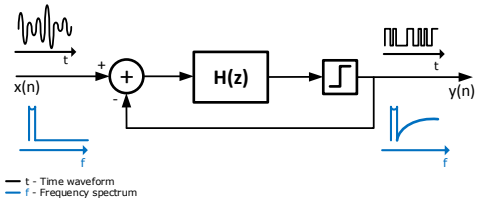


(b) PWM spectrum illustration using dithering.

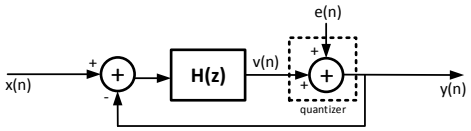
Figure 2.9: PWM dithering using random noise source.

Delta-Sigma Modulation

Delta sigma modulation is a well know signal encoding method that allows to trade amplitude resolution for time resolution of a signal without compromising the in-band signal quality. DSM is a very popular method widely used in audio, control and even radio communication applications. The functional concept of the DSM is to use an error feedback to reduce the quantization noise added to the signal by the quantizer in a specified bandwidth. This bandwidth and the error attenuation is defined by the loop filter, $H(z)$, which imposes the limitation for the maximum signal bandwidth for a given SNR. This principle of operation falls into the noise shaping concept previously presented.



(a) Delta-Sigma modulator.



(b) Linear model approximation.

Figure 2.10: Delta-Sigma modulation.

The Delta-Sigma modulation is a nonlinear system, due to the quantizer effect, as well as a dynamic one, due to the memory in the filter H(z), which makes its analysis a difficult mathematical task. However, a qualitative behavior can be extracted from a simpler linear model [ST05] as presented in Figure 2.10b. This model assumes that there are two different inputs in the system, the signal to be modulated, $x(n)$, and the quantization error added by the output quantizer, $e(n)$. Using this model, where the quantizer is reduced to a linear addition of noise, one can find the output $y(n)$ transfer function depending on these two inputs. Consider the Z-transform of $x(n)$, $e(n)$, $y(n)$ and $v(n)$ to be respectively $X(z)$, $E(z)$,

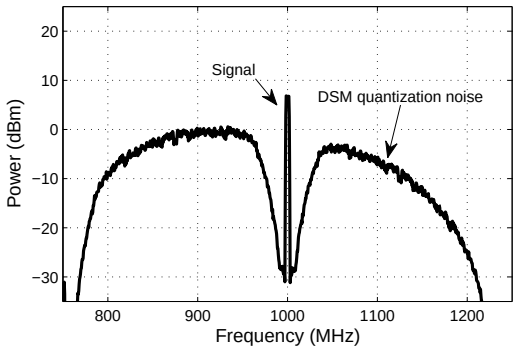


Figure 2.11: DSM-based transmitter spectrum.

$Y(z)$ and $V(z)$. The DSM output is given by equation (2.1);

$$\begin{aligned} Y(z) &= V(z) + E(z) \\ &= H(z)[X(z) - Y(z)] + E(z) \\ &= \underbrace{\frac{H(z)}{1+H(z)}}_{STF(z)} X(z) + \underbrace{\frac{1}{1+H(z)}}_{NTF(z)} E(z) \end{aligned} \tag{2.1}$$

Replacing the filter $H(z)$, with a delayed integrator the output is as shown in (2.3).

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.2}$$

$$Y(z) = \underbrace{z^{-1}}_{STF(z)} X(z) + \underbrace{1 - z^{-1}}_{NTF(z)} E(z) \tag{2.3}$$

Where the Noise Transfer Function, $NTF(z) = 1 - z^{-1}$, is a high-pass filter and the Signal Transfer Function, $STF(z) = z^{-1}$, is a delay. In this example, with a first order DSM loop filter, the signal is delayed for a sample while the quantizer noise is filtered to higher frequencies.

The function $H(z)$ can however have a higher order to improve in-band noise rejection and provide higher signal quality also refered as Signal to Quantization Noise Ratio (SQNR). Higher order modulators provide considerably higher SQNR improving their in-band noise rejection. Using higher order modulators, the DSM NTF will also be a higher order filter and therefore be capable of a greater attenuation for the quantization noise. Figure 2.12 shows the different spectral noise shaping for low-pass DSM up to the third order. It is clear that the second and third order modulators have better noise rejection in the low-pass signal band.

As shown on Figure 2.12 higher order modulations are preferable for most of applications (including RF transmitters) since they provide better SNR. However, they are well known for

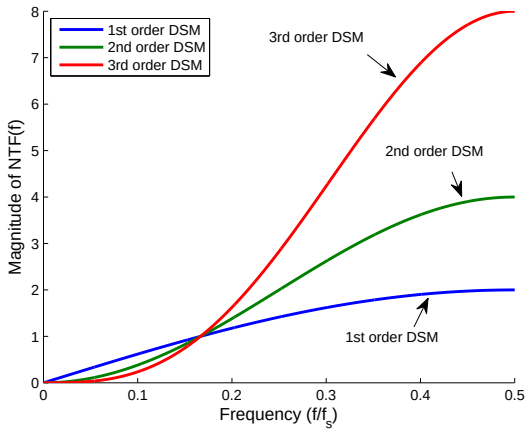


Figure 2.12: DSM NTF frequency response magnitude.

stability problems and usually require more complex hardware implementations. Additionally, for RF transmitters other considerations should be done considering its bandwidth and spectral efficiency. These considerations will be further explored in the next sub-sections of this document.

2.4.3 Limitations of Pulsed Transmitters

With a better understanding of the common topologies for pulsed transmitters, it is important to understand the main limitations that these systems still have and the origin of those limitations. The following section documents important digital transmitter characteristics and the main limitations still needed to be addressed for these systems to be considered as a viable alternative for RF transmission.

Efficiency and Spectral Purity

ADTs use the RF pulsed signals in order to take advantage of efficient switching-mode amplification and digital signal processing techniques to achieve a more efficient transmission. However, there are still a number of key limitations preventing the widespread use of all-digital transmitters. In theory, SMPA can reach 100% efficiency, however the transmitter efficiency also depends on the coding efficiency of the transmitted signal [JS06]. Coding efficiency (CE) can be defined as the transmitted signal power over the total transmitted power as shown in equation (2.4).

$$CE = \frac{P_{signal}}{P_{total}} \tag{2.4}$$

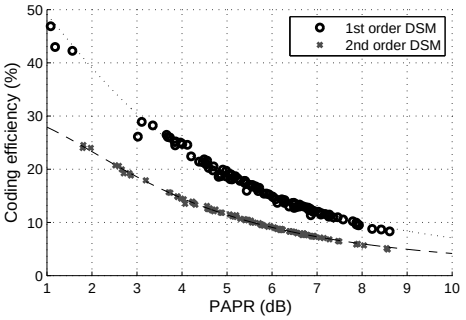
In this sense, the transmitter power efficiency depends on the product of the coding efficiency and the power amplifier (PA) efficiency [GHA+10b], as in equation (2.5).

$$\eta_{T_x} = CE \times \eta_{PA} \tag{2.5}$$

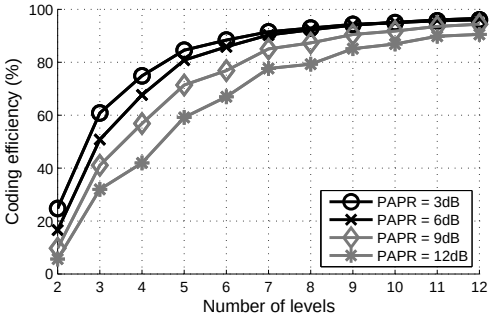
The CE is considered in many papers as one of the transmitters fundamental characteristics. However, the CE value is signal dependent and the transmitter coding efficiency cannot be defined, calculated or measured without considering a specific signal.

Coding efficiency gives an understanding of the transmitter unwanted emissions and overall RF signal purity. This is a critical value since pulsed transmitters output signal has a significant amount of unwanted spurious. Due to their lack of amplitude resolution (usually 2 or 3-level signals), pulsed transmitters add a significant amount of harmonic noise. Although the distribution and total amount of the quantization noise depends on the used modulation, the value is not negligible and should be considered for the pulsed transmitters efficiency.

In summary, the CE of the output signal in an ADT depends on the characteristics of the input signal and the modulation used. For example, the coding efficiency of DSM varies with the input signal's peak-to-average power ratio (PAPR). Additionally, higher orders of modulation will further decrease the coding efficiency of the transmitter. Figure 2.13a shows a representative graph of coding efficiency measurements for an all-digital transmitter with both first and second order modulators for different PAPR signals. Figure 2.13b shows the coding efficiency variation of different PAPR signals for a growing number of output levels. It is perceptible that for common wireless communication standards with PAPR varying from 3 dB up to 12 dB the coding efficiency is considerably low, especially for higher order modulators.



(a) Coding efficiency on low pass DSM-based ADT with 2 levels.



(b) Coding efficiency variation with the number of output levels.

Figure 2.13: Coding efficiency measurements for DSM-based pulsed transmitters.

The number of output levels influences the maximum achievable CE since it defines the total quantization noise in a certain signal. If DSM is used with more two levels, the quantization noise of the signal conversion can be decreased. Considering this, the number of levels not only influences the SNR, it also influences the coding efficiency of the DSM.

It is reasonable to assume that most of the noise in a digital transmitter comes from the

quantization noise of pulsed modulations. The low resolution signals can not reproduce the original signals without some error due to the limited number of amplitude levels.

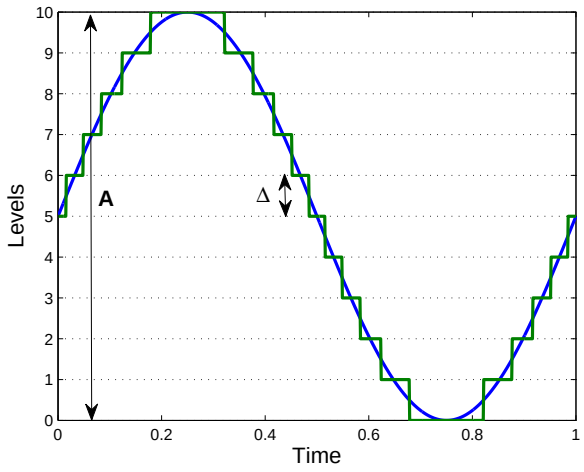


Figure 2.14: Example of a quantization of a sinusoidal wave. In blue, the high resolution wave has no quantization error, while the approximation, in green, has a significant amount of added noise due to the limited number of levels.

Let the blue signal in Figure 2.14 be the baseband signal to convert in a pulsed representation, or in other words, the signal to be quantized. The signal maximum peak to peak amplitude is the value A, and the number of quantization levels is N. Assuming this, the amplitude difference between two levels is the value $\Delta = A/(N-1)$ as shown in Figure 2.14.

Assuming a sinusoidal wave as in the plot above, the average power of the signal will be given by equation (2.6).

$$P_s = \frac{1}{T}\int_0^T \left(\frac{A}{2}\sin\left(2\pi\frac{t}{T}\right)\right)^2 dt = \frac{A^2}{8} \tag{2.6}$$

For different waveforms, the RMS power will depend on the characteristics of the signal, which might have amplitude distributions that are very different from a sinusoidal wave. In fact, different PAPR signals will have different amplitude distributions that, for the same amplitude A, have a smaller average power. It is impossible to take into account every type of amplitude distributions for the signals, but one can use the relation between the peak power and the average power of the signal that is given by its PAPR as in (2.7).

$$P_{avg} = \frac{P_{peak}}{PAPR} \tag{2.7}$$

Considering this and the maximum amplitude A, the power variation with the PAPR is given by (2.8).

$$P_s = \frac{A^2}{8PAPR} \tag{2.8}$$

On the other hand, the maximum error for any given level will be $\Delta/2$. Considering this, the error value will be distributed between $-\Delta/2$ and $\Delta/2$. Again, the error amplitude distribution is not necessarily uniform and can depend, up to some degree, on the signal amplitude distribution as well as the quantization levels distribution. For simplicity reasons however, as an approximation, the distribution of the error amplitude is considered uniform. The quantization error power will be:

$$P_e = \left(\sqrt{\frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} x^2 dx}\right)^2 = \frac{\Delta^2}{12} = \frac{A^2}{12(N-1)^2} \tag{2.9}$$

Considering now the coding efficiency from equation (2.4), the coding efficiency of a signal depending on its quantization levels is given by equation (2.10)

$$CE = \frac{P_s}{P_s + P_e} = \frac{\frac{A^2}{8PAPR}}{\frac{A^2}{8PAPR} + \frac{A^2}{12N^2}} = \frac{\frac{1}{8PAPR}}{\frac{1}{8PAPR} + \frac{1}{12N^2}} \tag{2.10}$$

Finally the coding efficiency variation for different PAPR signals, depending on the number of quantization levels is shown in Figure 2.15. It is evident that the PAPR of a signal has a great impact on the CE efficiency of the transmitter especially for lower number of quantization levels.

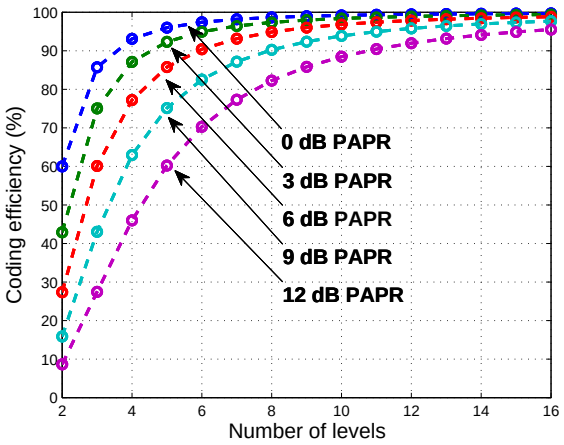


Figure 2.15: Expected coding efficiency variation depending on the number of output levels for different PAPR signals.

Notice that the plotted graphic is merely an indication of expected CE values for certain signal and quantization characteristics. While the approximations made are valid to understand the CE behavior, they might not indicate the true obtained value for those specific conditions since some assumptions might not apply. For example, the assumption that the quantization noise is uniformly distributed in the amplitude is not necessarily true for DSM and PWM modulations. Nonetheless, from equation (2.10) and Figure 2.15 it is possible to

understand the CE trend with the number of levels, as well as the rough estimation of the necessary signal levels to achieve a certain coding efficiency.

The low coding efficiency verified for a 2-level signal is linked to the existent quantization noise common to most pulsed RF transmitters (as shown in the spectra in Figure 2.7 and 2.11). The improvement of coding efficiency is essential for the successful adoption of pulsed transmitters as a competitive solution and therefore has received a considerable attention in the literature [HMFP13, MHFP12, MHL+13]. Most of known methods improve the coding efficiency using some form of quantization noise cancellation at the transmitter output. Partial noise cancellation was used to generate RF outputs that have higher coding efficiency at the trade of lower PA efficiency [SOC13, GEN+12, CSV11, CHV13]. Although with lower drain efficiency, these systems establish an optimal point between coding efficiency and drain efficiency, which improves the overall system efficiency. Other possibility is the use of multiple pulse encoders to have a n-level output signal, this improves coding efficiency with growing number of quantization levels but starts to behave as conventional RF DAC with all its inherent problems.

Signal to Noise Ratio

While the coding efficiency refers to the out of band noise, there is also quantization noise from the pulsed modulation that falls within the signal's band. The in-band noise from the quantization error will decrease the transmitter's signal quality, or in other words its SNR. Besides a low amplitude resolution, pulsed digital transmitters usually have a finite time resolution, which means that the signal is, not only quantized in amplitude, but also discretized in time. Both the amplitude quantization and the time discretization, i.e. sampling, introduce quantization noise that falls within the signal's band.

The signal to noise ratio of a signal is given by the ratio between the signal power and the noise power as in equation (2.11).

$$SNR = \frac{P_s}{P_n} \tag{2.11}$$

To evaluate a DAC performance when using low resolution signal converters, instead of using the SNR, the metric used is often the Signal to Quantization Noise Ratio (SQNR). Similar to the SNR, the SQNR is a ratio of power, but it is assumed that the noise power P_n is the quantization noise that comes from the pulse modulation or similar quantization processes without considering other external noise sources.

The PWM frequency behavior and its SQNR is already a well known subject [CVS10,SS03] and it may vary depending on the type of PWM used. For the purposes of this work, considering the application of PWM in all-digital transmitters with a digital implementation, the PWM type considered uses uniform sampling [SS03]. A general form for the SQNR of this PWM topology signal can be given by the equation in (2.12).

$$SNR_{PWM}(dB) = 20\log_{10}(M) + 1.76 + 10\log_{10}(OSR) \tag{2.12}$$

where M is the number of time steps (number of pulse width levels) in the PWM waveform and OSR is the oversampling ratio of the input signal. The actual signal of interest occupies a smaller bandwidth, BW, which is less than the Nyquist bandwidth. If filtering is used to filter out noise components outside the bandwidth BW, then a factor (called process gain) relative to the OSR must be included in the equation to account for the resulting increase in SNR. Figure 2.16 shows the PWM SQNR with variation of the OSR and the number of time steps (M). The dashed line represents the particular case where the number of PWM levels grows with the same pace as the OSR, which portrays the case where the sampling frequency is increased.

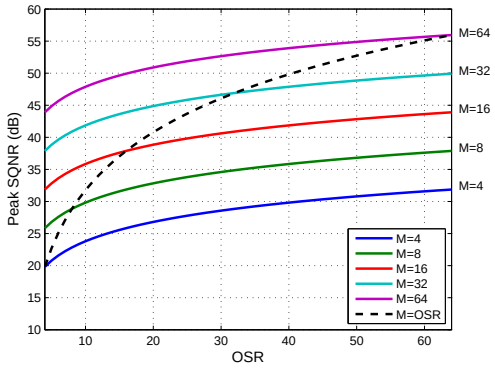


Figure 2.16: PWM with M possible pulse widths maximum SQNR depending on OSR.

DSM uses noise shaping to reduce the quantization noise in the signal's band. In DSM the reduction of in-band noise can be achieved by increasing its internal filter order. Additionally, the increase of the OSR also improves the achievable SNR. Accordingly to [ST05], for a Lth order delta-sigma modulator, the SQNR can be described accordingly to equation (2.13).

$$SNR_{DSM} = \frac{1}{\sqrt{8}}\sqrt{6\pi}\frac{\sqrt{(2L+1)!}}{L!}\left(\frac{OSR}{2\pi}\right)^{\frac{2L+1}{2}} \tag{2.13}$$

Converting to dB units and simplifying it, equation (2.13) becomes (2.14).

$$SNR_{DSM}(dB) = 3.01 \times \log_2(OSR) \times (2L+1) - 9.36L - 2.76 \tag{2.14}$$

Figure 2.17 shows the SQNR variation with OSR for DSM modulators from the first to the seventh order.

Comparing DSM with PWM, the maximum achievable SQNR values are quite different for the same value of OSR. This is due to the noise shaping behavior of the DSM that removes the in-band quantization noise. However, it must be stated that the hardware implementation

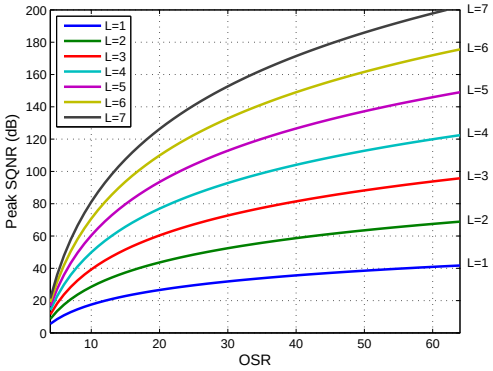


Figure 2.17: DSM maximum SQNR for a Lth order modulator depending on OSR.

of PWM is much simpler than the DSM and typically allows for higher OSR values.

It is clear that for DSM there is a big advantage in using higher order modulators, however these modulators have problems that might limit these gains. As seen in the previous sections, higher order DSM loops have a lower coding efficiency, which is not desirable for a RF transmitter since a lot of power is lost into noise. This happens due to the higher NTF gain for frequencies outside the signal's band. This higher gain, however, is necessary to achieve the desired noise rejection in the loop filter that improves the SNR. Besides the lower coding efficiency, the high NTF gain also causes instability in the DSM feedback loop. This causes stability problems for DSM of higher orders [Sch93].

Other problem, is the lower bandwidth in higher order modulators. While there seems to be no relationship between the order of the DSM and its bandwidth for a fixed OSR, the hardware implementation of higher order modulators is usually much more complex than a simple first order modulator. Its hardware implementation often has high critical path time delay that decrease the maximum clock frequency for that specific implementation hence reducing either the BW or the OSR and therefore degrading the SNR.

Bandwidth

An important feature of any radio transmitter is its bandwidth, which is directly related to the capacity of the transmitter to send information at certain data-rate. The quantization noise not only diminishes the signal coding efficiency and SNR but also limits the transmitter's effective available bandwidth. Due to the need for oversampling, usually pulsed transmitters have a very narrow bandwidth compared to their sampling frequency. In digital hardware implementations, switching logic has frequency limits that bound the achievable sampling frequency, f_s, to a maximum value depending on the technology used, inflicting either a maximum OSR or a maximum signal bandwidth (BW). The OSR depends on the BW of the signal to be transmitted with a relation as shown in equation (2.15). For a fixed sampling

frequency, a signal with higher BW decreases the OSR of the modulation and vice-versa.

$$OSR = \frac{f_s}{2BW} \tag{2.15}$$

In most cases, this means that all-digital transmitters have a BW limited to a few units of MHz for FPGA designs and less than 50 MHz for ASIC. Most of pulsed-RF transmitters achieve higher OSR optimizing the digital design for a higher frequency [CRJZ11]. In oversampling pulsed conversions such as PWM or DSM, the achievable BW and SNR are tightly connected and improving one often degrades the other. In both PWM and DSM the sampling frequency, f_s, is generally enforced by the maximum logic hardware frequency that is fixed. On the other hand, for oversampling pulsed converters, the OSR is directly connected to the achievable SNR, where the higher the OSR offers a better quality signal. Increasing the modulator bandwidth without increasing the OSR will always decrease the modulated signal SNR. This reduces the bandwidth problem to a sampling frequency maximization problem.

In digital designs, an alternative to reach a higher sampling frequency is the use of parallel processing followed by dedicated high-speed logic only for the digital up-conversion stage [EHG11, HHGP13, COVS13]. These techniques are often called polyphase implementations since the converter processes multiple signal phases in parallel at each clock period. While with PWM a parallel architecture is a trivial concept to understand (see Figure 3.5), DSM is not so easy to parallelize since it relies on feedback signals.

Parallel architectures make possible the design of considerable higher bandwidth transmitters working at reduced logic frequencies for most of the design and the competitive integration with lower-cost technologies, however it relies on the use of dedicated high speed logic at the output to guarantee the data throughput.

Carrier Frequency Flexibility

The functionality and flexibility of the transmitter is also of great importance since the purpose of a digital transmitter is to easily adapt the radio to its environment and user demands. Carrier frequency flexibility means a single digital chip can be a wideband radio for multiple channels and standards. A considerable advantage of RF DACs and pulse transmitters is the possibility for multi-band and multi-carrier transmission, which is impracticable in conventional RF transmitter architectures without hardware replication.

In fact, some works in the literature present all-digital transmitters with fine tuning capability and simultaneous multi-band operation, capable of simultaneously transmit different communication standards on different carriers. In [SOBC13, SOGC12] two different signals at different carriers are independently generated one from the other and then at the output they are multiplexed in time. The operation is performed digitally at the input of a high speed serializer by interleaving two signals. While, this allows a multi-carrier transmission, it needs to have a two times higher sampling frequency at the output of the transmitter. For

higher carrier frequencies (as an example the 2.4GHz band) this is impracticable since the necessary sampling rate is much higher. Other limitation is the fact that each one of the different signals must not have any spectral component at each other's signal carrier frequency. This is hard to obtain using pulsed transmitters since they create harmonic distortion with an infinite spectrum. However, this is achieved by using DSM and forcing its loop filter zeros at all the carrier frequencies as shown in Figure 2.18.

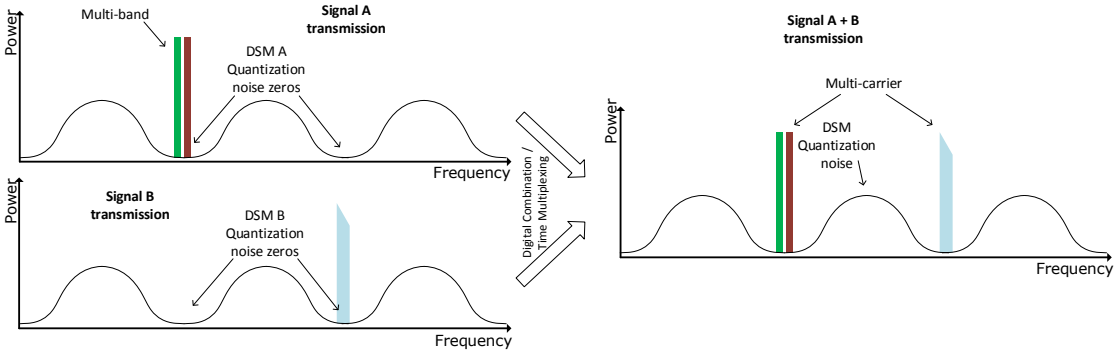


Figure 2.18: Concurrent multi-band and multi-carrier ADT concept based on DSM.

Other multi-carrier and multi-band approaches use band-pass DSM to design a transmitter with multiple independent pass-bands [MFK17]. Concurrent multi-band DSM was used in [CMST15] and [CMS+15] to achieve a compact and flexible multi-band transmitter implementation for LTE-Advanced. In this paper the authors use a single transmitter capable of simultaneous transmission at 856 MHz and 1450 MHz channels with 20 MHz bandwidth each. In [MTKS13] and [KI10] the authors use a similar concept of concurrent multi-band DSM to design a dual-band transmitter. Combining two band-pass DSM and properly adjusting their NTF the band-pass center frequencies can be independently adjusted.

Although, the use of concurrent multi-band DSM allows for the design of multi-band transmitters for any given frequency band, none of these transmitters allows the dynamic change of the central frequencies of the transmitter. This binds the transmitters to the fixed and unchangeable set of frequency bands.

Summary

While some pulsed transmitter and all-digital topologies seemed promising, the previous sections of this document showed and explained some of their limitations. This thesis focus on improving the capabilities of all-digital transmitter by addressing some of the above stated limitations. The following thesis chapter presents several hardware architectures, as well as processing method proposals, for the improvement of the state-of-the-art characteristics of all-digital transmitters. The different sections in chapter III target the different limitations presented for the state-of-the-art in chapter II.

Chapter 3

Novel Architectures for All-digital Transmitters

Outline

This chapter provides a description of the main developments that resulted from this PhD. The aim of this chapter is to provide both the background and implementation details of the developed solutions for pulsed all-digital transmitters.

The sections of this chapter are divided into four main themes regarding the achievements obtained in the following order: The first section presents efficient architectures of ADTs focusing on FPGA hardware implementations. The second section is focused on the improvement of the bandwidth through the use of parallel architectures. The third section shows different hardware architectures to improve the coding efficiency and overall power efficiency of ADTs. And finally, the fourth and last section demonstrates the use of two different techniques to improve the overall flexibility of pulsed transmitters systems.

Each one of these sections points to one or more append published papers that explore further details about the conceived architectures, hardware implementations and explore the achieved results.

3.1 All-digital Transmitter Architectures and Applications

In this section the main features of the used ADT architecture are shown and explained. The presented architectures were, in a general form, the basic concept for the most of this PhD thesis achievements. This section gives an overall explanation of the functionality for the main hardware blocks in the FPGA-based ADT architectures proposed in this document. Focusing on the practical implementation of digital transmitters, this section introduces several of the used hardware solutions to devise the necessary building blocks of the proposed ADT architectures.

3.1.1 All-digital Transmitter FPGA Implementation

In the previous chapter, a series of ADT topologies and architectures were presented and detailed. The functional differences of these topologies were presented, however no specific details about their hardware architecture and implementation were discussed. This section will take a deeper look into the hardware architecture as well as the platform used during the experimental phase of this thesis.

The design and development of ADTs is not limited to the use of adequate and flexible topologies, but also relies on their efficient hardware implementation. On the other hand, the real-time processing of wireless standard signals dictates the need of powerful digital signal processing techniques and circuits capable of coping with the high bandwidth demand. Additionally, due to the flexible nature of the ADTs, different forms of specialized hardware might be necessary to cope with the demands of the multiplicity of wireless standards and signals to be used.

For the reasons described above, most of ADT architectures presented in the literature use some type of configurable hardware instead of industry standard approaches, being the most common platforms based on ASIC, FPGA, DSP or other application specific circuit combination. The choice of the hardware platform is highly influenced by the communication scenario, in which the ADT is used, communication standards, performance needs and cost.

However, for the purposes of this thesis, FPGAs were found to be the better solution for the development of new architectures for flexible and wideband ADT, since modern FPGAs provide a good compromise between processing power, clock frequency and circuitry integration. Current FPGAs on the market already have the equivalent capacity of millions of digital gates allied to a set of dedicated hardware blocks such as block RAM memory, DSPs, embedded processors and high frequency digital transceivers. These building blocks, together with FPGAs reconfiguration ability make this integrated circuit a valuable candidate as an hardware platform for the implementation of ADT as well as SDR systems.

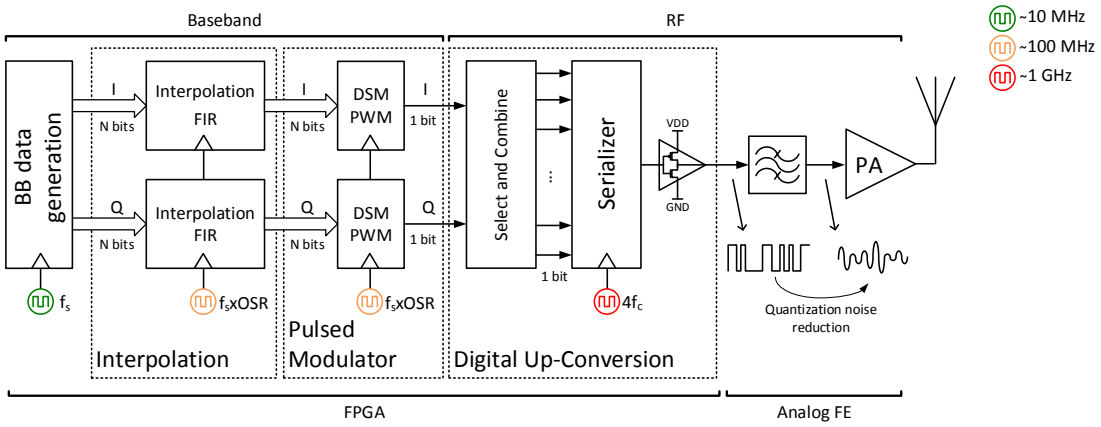


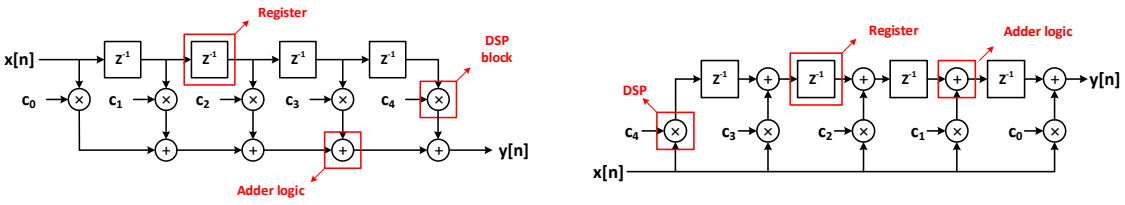
Figure 3.1: Low-pass DSM/PWM based all-digital transmitter architecture

The low-pass DSM or PWM based all-digital transmitter architecture is shown in detail in Figure 3.1. As shown in the previous chapter, this architecture can be divided in 3 main functional blocks; the interpolation stage, the pulsed modulator and the digital up-conversion.

3.1.2 Interpolation Stage

The function of the interpolation stage is to improve the OSR of the baseband signal for the pulsed modulator. As noted on Figure 3.1, the typical baseband signal sampling frequency is around the tens of MHz, depending on the standard and signal bandwidth. While these sampling rates are usually sufficient for most wireless signals, its oversampling ratio is too low to be directly converted with a pulsed modulator. As shown in Figures 2.16 and 2.17, pulse modulation requires an OSR typically larger than 10 in order to convert the signal with an acceptable value of SQNR. A good ADT architecture should consider an interpolation stage to up-sample the input baseband signal from the tens of MHz to the hundreds of MHz in order to guarantee the pulsed signal quality. The increase of the sampling frequency would be beneficial, however the hardware complexity of the pulse modulator circuit, as well as the interpolation filter itself, can limit the maximum hardware frequency achievable.

For this work, the interpolation filter type used is a finite impulse response (FIR). The FPGA implementation of FIR filters is possible through the use of dedicated DSPs together with conventional logic gates. While there are several FIR structure options, for a resource efficient hardware application, the most common structures used are the direct form (Figure 3.2a) or the transpose form (Figure 3.2b) for pipeline optimization. Both these structures allow to have the desired impulse response excluding the delay that is imposed by the type of pipeline strategy used.



(a) FIR direct form.

(b) FIR transpose form.

Figure 3.2: FIR filter forms with different hardware implementations.

Modern FPGAs already include an impressive set of tools to support a variety of hardware implementations. For the work presented in this thesis, the design, optimization and application of the FIR filter coefficients was done using a variety of MATLAB functions to find the most suitable impulse response for each case. However, for the hardware construction of the single-phase FIR filters, the Xilinx FIR compiler tool was used for a faster FPGA integration.

This tool allows for the translation of the filter coefficients to the necessary FPGA-based FIR hardware implementation.

3.1.3 Pulsed Modulator

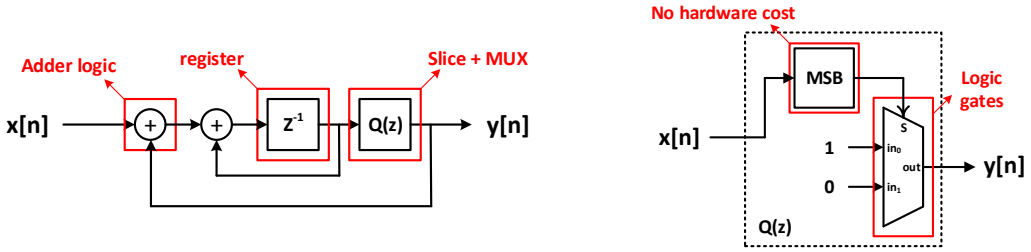
The pulse modulator can be considered the core of the ADTs architecture since it establishes a significant part of the system characteristics. The main purpose of the pulsed modulator is, as previously stated in chapter 2, to convert the high amplitude resolution signals into lower amplitude resolution or even pulsed signals without significant loss of signal to noise ratio in the signal's bandwidth.

In order to properly convert the input signal, several techniques were already discussed, as well as their advantages and drawbacks. During the development of the hardware architectures used for this thesis, the main focus was on Delta-Sigma (DSM) and Pulse-width (PWM) modulations. For both approaches, the focus was on the enhancement of signal quality and bandwidth from current state-of-the-art ADTs. This was done introducing new and optimized pulse modulator topologies that could be efficiently implemented in common digital hardware blocks.

The following paragraphs focus on the hardware implementation strategies used for DSM and PWM that were used through out the work developed during this thesis.

Delta-Sigma Modulator

The basic structure of the 1^{st} order DSM is shown on Figure 3.3. This structure has two feedback loops, one on the integrator shaping filter, and one from the output to the input signal. The adders from these loops were implemented using generic FPGA logic gates. While modern FPGAs allow for the use of dedicated DSPs for math operations, in this particular case this would lead to larger critical path.



(a) Top-level DSM hardware architecture. (b) 2-level quantizer (Q(z)) detailed hardware.

Figure 3.3: First order DSM hardware architecture example.

Due to the need of the adders inside a feedback loop, the use of pipelined DSPs must be avoided because it changes the internal loop delay, which modifies the DSM internal state

progression leading to unstable and unpredictable behavior. Even more, for FPGAs conjugating conventional logic gates with DSPs (without pipeline) would lead to higher routing delays between blocks decreasing the achievable sampling frequency.

Inside the feedback loop, the number of adder's bits is other major concern for the hardware implementation of the internal logic of the DSM. It is reasonable to assume that higher bit words on a digital DSM leads to a more precise operation, hence less error at the output. However, higher bit resolution for the adders will also increase the amount of logic levels in the propagation delay for the critical path. Figure 3.4 shows the progression of the number of logic levels for an adder block depending on the number of bits of the input words. The example values are from a Xilinx Kintex 7 FPGA (XC7K325T) with an adder implemented on FPGA logic fabric.

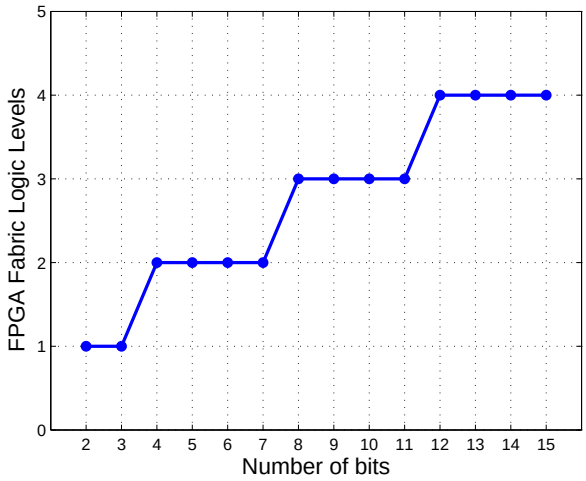


Figure 3.4: Logic levels growth with the increase of the number of bits for the internal adder block in the DSM logic.

It should be noted that a SNR limitation already exists from the DSM output due to the signal quantization to a pulsed signal. Figure 2.17 in the previous chapter shows the SNR variation accordingly to the oversampling ratio (OSR) and DSM order (L). Using this figure, and considering typical DSM cases, with OSR varying from 20 to 40 for first and second order modulators the target peak SQNR is between 30 dB and 60 dB. If we consider now the SNR of a digital signal with n bits as in equation (3.1), it is possible to calculate the number of bits necessary to be within that SNR.

$$SNR_n = 20log_{10}(2^n) \quad \Rightarrow \quad n = \frac{SNR_n}{20log_{10}(2)} \tag{3.1}$$

For 30 dB the necessary word length is 4.98 bits, and for 60 dB it is 9.96 bits. So, to keep the internal signals within the SNR limits 10 bits for the internal logic would be sufficient. Crossing this information with the graph from Figure 3.4 we can use up to 11 bits with

the same number of logic levels in the logic datapath. In this sense, it is possible to use additional bits without any additional penalty in the maximum sampling frequency. For other applications, where the bandwidth is more critical than the SNR, an approach with less bits can be used. For example if 30 dB is the target, 5 to 7 bits should be sufficient and it reduces the number of logic levels for the adders, improving its maximum sampling frequency.

Due to its simplicity, usually the quantizer is not viewed as a critical part for the hardware implementation. However, since it is inside the DSM loop, any optimization in the used logic will benefit the overall DSM bandwidth. To implement the quantizer, the multi-bit word at its input is reduced to a single bit through a slice operation. Using a 2's complement word, the most significant bit has the information if the signal is positive ('0') or negative ('1'). From this bit the output of the DSM can be directly obtained with a bit inverter. Additionally, the most significant bit can be used as a selection bit in a multiplexer for the DSM feedback as in Figure 3.3b. The advantage of using a multiplexer is that the feedback can be defined without any multiplier gain or multiply block that relies on DSPs or LUTs.

For the development and simulation of the DSM architectures used in this thesis it was used a Xilinx tool called System Generator that allows to integrate the developed FPGA hardware into Matlab's Simulink. The advantage of this tool was to quickly simulate and understand the impacts of the hardware choices made.

Pulse-Width Modulator

As presented in chapter 2, PWM works by comparing the input signal with a predetermined reference signal. As it is presented in Figure 2.6 this relies on the use of a comparator. If we consider the necessary number of PWM levels and OSR to obtain a good SNR value (see Figure 2.16) the sampling rate of that comparator would be out of the reach for generic FPGA logic fabric. Considering this, the use of a direct comparator in FPGAs is out of the question for wireless communication signals.

An alternative approach is to use a look-up table (LUT) with the PWM words for each input signal level and use a parallel-in, serial-out (PISO) block to serialize the PWM in time [SOC13] as shown in Figure 3.5. Using a LUT, the input binary word (2's complement) of the PWM is converted to a different coded word where the number of '1' bits is proportional to the value at the input. Using this method, one can encode and save the possible output states of the PWM into a memory with all the possible output states as a LUT.

To implement this PWM conversion in an FPGA the PWM LUT can be implemented using a block RAM memory primitive, that will be accessed as a ROM by the input signal. Mapping the samples in the memory in the correct way guarantees that a direct access by the input most significant bits can be used to address the PWM LUT memory, i.e. the less significant bits are considered as a don't care for the LUT address. This is illustrated in Figure 3.6, for simplicity reasons it is considered a 4 bits input signal (varying from 0 to 15).

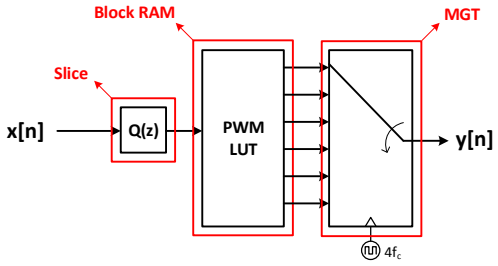


Figure 3.5: Pulse width modulation using LUT with coded PWM words.

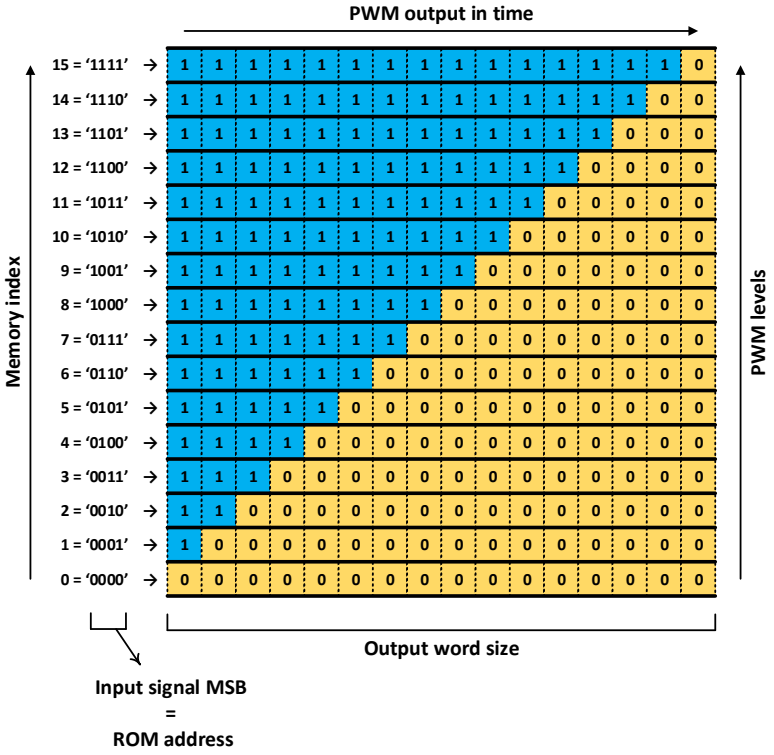


Figure 3.6: Example of PWM LUT memory with 16 levels.

For every binary input between '0000' and '1111', there is a coded PWM output with the equivalent duty cycle defined and store in the memory. For example, if we want the PWM output of the value 2 = '0010', we index the ROM with that value. From the memory in the index position 2, the PWM output is '1100000000000000', that is equivalent to a rectangular wave with duty cycle equal to $\frac{2}{16}$ of PWM wave period.

Note that the memory is accessed at the sample rate of the input signal assuming that the baseband signal has a certain OSR defined by the interpolation stage. At the output of the PWM LUT, the hardware clock has the same rate as the input since the PWM output word

is accessed one entire PWM period at a time (as a parallel word). The PWM word can be serialized in the correct order to create the desired PWM wave at the transmitter's output.

3.1.4 Digital Up-Conversion

To up-convert the baseband signal to the desired carrier frequency, a digital up-conversion scheme as shown in Figure 3.7 can be implemented.

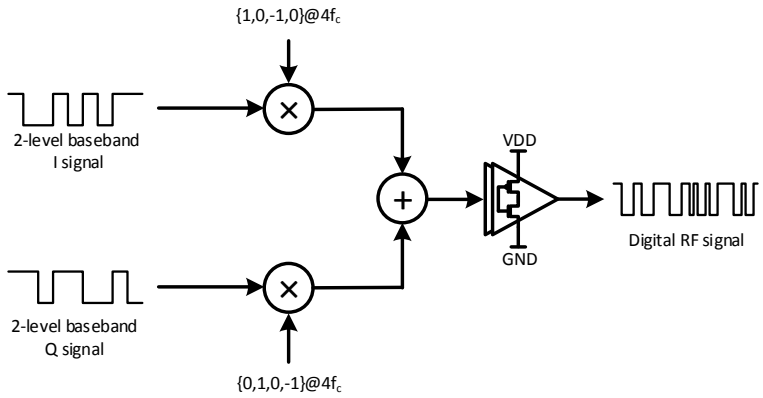


Figure 3.7: Digital up-conversion using a digital carrier wave to maintain a 2-level RF signal.

As opposed to the analog mixers, the digital up-converters shift the baseband signal using low resolution digital signals for both the baseband signal and the carrier local oscillator (LO). The carrier wave can be simplified to a sequence of three different values, -1, 0 and +1. Doing this, allows to have two quadrature carrier waves only using sequences of 4 samples, [1,0,-1,0] and [0,1,0,-1], with the sampling frequency equal to four times the carrier frequency f_c. To better understand this, Figure 3.8 shows a temporal diagram example of the waves used in the digital up-conversion scheme shown in Figure 3.7.

Figure 3.8 shows the in-phase (I) pulsed signal multiplied by a digital waveform that is either 1, 0 or -1, as well as the quadrature (Q) pulsed signal multiplied by the same waveform 90 degrees phase shifted. After that, the waves are summed resulting in a 2-level signal that will have the desired center frequency at f_c as well as odd harmonics of f_c due to the use of a square carrier wave. The undesirable harmonics are removed by the output RF reconstruction filter as depicted in Figure 3.1.

Most of ADTs in the literature are usually implemented using ASICs since this technology allows higher output clock rates. This is fundamental since the digital up-conversion stage in the ADT architecture shown in Figure 3.1 must be operated at 4 times the RF carrier frequency, which is challenging for synchronous digital logic. The presented scheme relies on the use of two multipliers as well as an hardware adder at very high clock frequencies. However, common FPGA logic fabric or integrated DSP slices are not capable to cope with these clock rates since they are limited to a few hundreds of MHz.

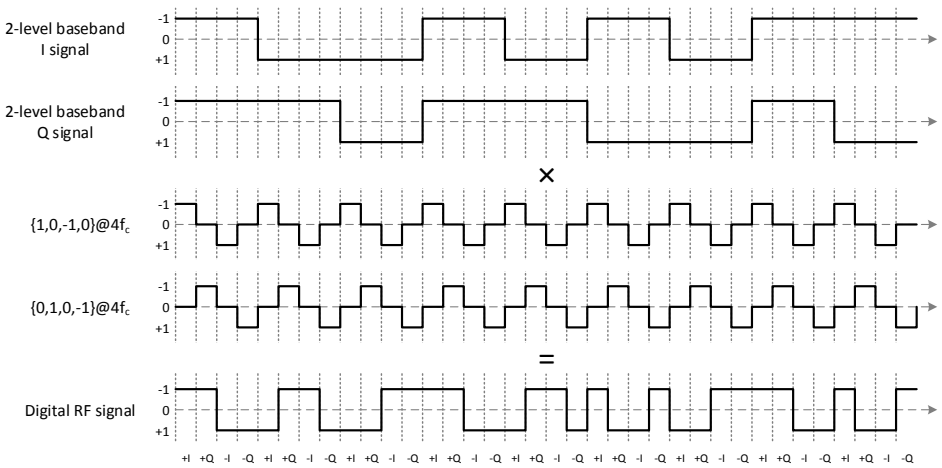


Figure 3.8: Input and output waves as presented in Figure 3.7. The first pair of waves represents the I and Q components of the 2-level baseband signal. The second pair of waves is the carrier quadrature waves sampled at $4f_c$ reduced to only 3 amplitude levels. The last wave is the modulated RF output at f_c.

To override this limitation a different DUC technique can be used. Looking closely to the timing diagram presented in Figure 3.8, it is possible to realize that the RF output can be obtained as a direct result of the I and Q input signals. The RF sequence at the output can be directly extrapolated from the input I and Q signals such that the output is the sequence $[..., +I_n, +Q_n, -I_n, -Q_n, +I_{n+1}, +Q_{n+1}, -I_{n+1}, -Q_{n+1}, ...]$. This repeated sequence allows to use a hardware optimization for the DUC circuit such that it decreases the complexity of the high speed digital logic. Instead of multipliers and adders, the circuit is reduced to a multiplexer switch that changes between the I, Q signals and their negated versions at a sampling rate of $4f_c$. Figure 3.9 shows this hardware concept change, that allows for the use of different logic building blocks. Using this concept, the high frequency clock part of the circuit is reduced to a high speed multiplexer that converts the I, Q, $-I$ and $-Q$ parallel inputs to the desired output sequence as sohwn on Figure 3.8.

On modern FPGAs, the core logic fabric is usually usable up to a few hundreds of MHz. Hardware complexity and generic routing of the signals don't usually allow for the adoption of FPGAs at RF frequencies, being its use many times limited to baseband processing. However, more recent FPGA chipsets have specialized hardware for very high speed serialization of parallel signals. This is usually used in high-speed point-to-point communication systems, using either coaxial cable or optical fiber as a transport method of a 2-level signal. In the context of this thesis, the Multi-Gigabit Transceivers (MGT) were used to created a direct output of a pulsed digital signals at high bit-rates (up to 6.0, 16.3 or 28.05 Gb/s depending on the hardware version).

In this thesis, the MGT were used to achieve the digital up-conversion as presented in

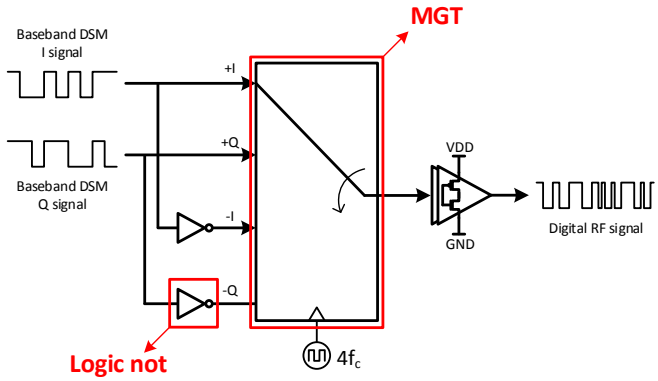


Figure 3.9: Digital up-conversion using high speed multiplexing of the baseband signals with a serializer.

Figure 3.9. The IQ signal sequence, as shown on Figure 3.8, is calculated in parallel at a lower frequency for multiple time steps. These signals are used as parallel inputs of the MGT serializer. At higher frequency, $4 \times f_c$, the 2-level serializer output is the expected RF signal up-converted to the carrier frequency f_c. This allows to convert the high frequency signal directly from a single FPGA, which allows for the full integration of an ADT on a single chip.

Summary

The use of the above mentioned techniques allowed for the implementation of agile and fully integrated ADT into a single FPGA. These techniques were used in all implementations presented in this thesis. Examples of their use are in the appended papers A and B.

In the appended paper A new radio-over-fiber system that uses an ADT architecture is presented. In this paper the advantages of the FPGA high integration are shown, using an ADT to implement a flexible centralized digital radio, able to perform the baseband processing and transmission over an optical fiber of RF signals. As a result, it enables a very simple remote radio head comprised only by an amplifying stage, a bandpass filter and an antenna. The digital signal at RF is transmitted over fiber using a simple on-off optical modulation, reducing the limitations of conventional analog radio-over-fiber systems, but maintaining the advantages of a reduced complexity transmitter radio head.

In the appended paper B the ADT architecture is merged with a fully digital receiver architecture to implement a new all-digital transceiver integrated into a FPGA chip. Both the RF receiver and transmitter were entirely implemented using a digital datapath from the baseband up the RF stage without the use of conventional analog-to-digital converter (ADC), digital-to-analog converter (DAC) or analog mixer. The digital transmitter uses delta-sigma modulation and digital up-conversion to produce a 2-level RF output signal. The receiver uses a high-speed comparator and PWM to convert the RF signal into a single bit data stream,

which is digitally filtered and then down-converted. Both the transmitter and the receiver are agile with flexible carrier frequency, bandwidth and modulation capabilities. The results show the feasibility of this approach as a more flexible alternative to common radio architectures as well as the potential of integrating of a fully digital radio into a single digital logic chip.

3.2 Parallel Signal Shaping Techniques

In this section the main focus is on the development of new signal shaping techniques and their implementation architectures with the purpose of improving the modulators sampling frequency. Therefore, this will improve some of the digital transmitter figures-of-merit, particularly the signal bandwidth.

The bandwidth is a fundamental figure-of-merit for any RF transmitter. In ADTs, the bandwidth still is one of the main limitations that constrains the use of this type of transmitters on a larger set of applications.

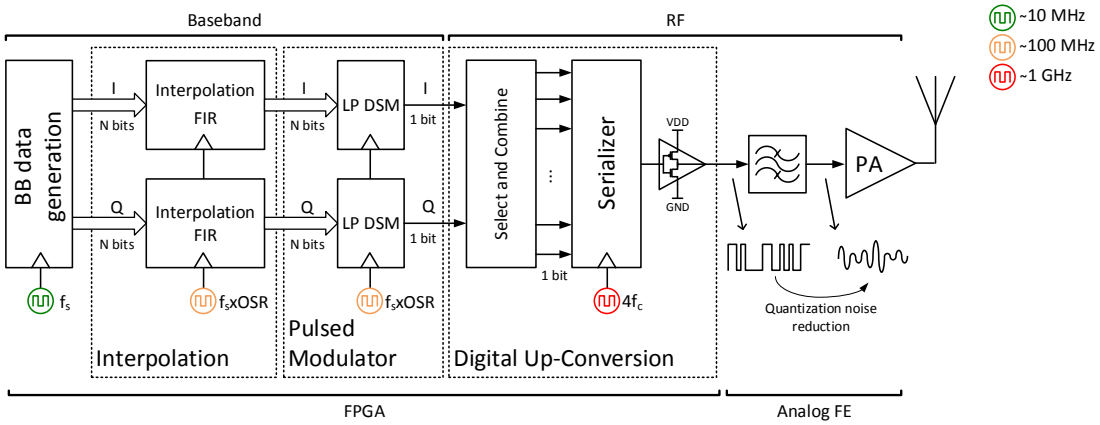


Figure 3.10: Low-pass DSM-based all-digital transmitter using a single path approach.

A DSM-based pulsed transmitter architecture is shown in Figure 3.10, where low-pass DSM is used to convert its input to a 2-level signal before digital up-conversion. This type of architecture allows the entire digital processing of the signal at the baseband level, enabling the use of lower clock frequencies for most of the digital hardware design. In fact, only a high speed output serializer transceiver has a clock at high frequency rates, particularly four times the carrier frequency when using quadrature modulated signals. This is a well suited architecture for all-digital transmitters, particularly those implemented using FPGA devices. Such architecture takes advantage that most of the datapath can be implemented with lower clock frequencies, in the range of the hundreds of MHz. Additionally, modern FPGAs have dedicated high speed hardware that can be used to achieve the necessary high bit-rates for RF signals.

However, in this architecture as presented in Figure 3.10, the low-pass DSM uses slower clocks in the MHz range, which comes at the cost of a reduced signal bandwidth. Considering the necessary OSR for pulsed modulators and the low order DSM, most of these modulators are limited to small bandwidth signals. In fact, as presented in Chapter 2, state-of-the-art figures-of-merit for ADT bandwidth are usually no more than 10 MHz, which is quite limited for modern radio standards.

Since the signal bandwidth is mainly limited by the modulator sampling frequency, parallel modulator architectures are often used to improve the bandwidth as shown in Figure 3.11. By increasing the number of parallel inputs and outputs of a particularly modulator, the transmission system can be converted from a single-input single-output (SISO) system to a multiple-input multiple-output (MIMO) system. With this conversion it is possible to increase the data rate without increasing the clock frequency of the hardware, effectively improving the transmitter's bandwidth.

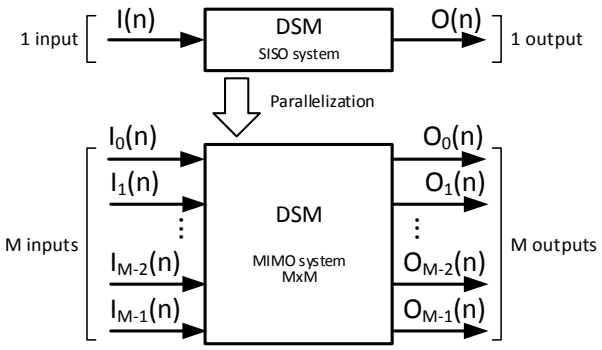


Figure 3.11: Concept of parallelization of a processing system by transforming a SISO system into a MIMO system.

3.2.1 Time-Interleaved Delta-Sigma Modulator for All-Digital Transmitters

Proposal

In the appended paper C, a Time-Interleaved Delta Sigma (TIDS) approach for ADT is proposed and analyzed in terms of frequency performance. In this approach, two modulators, a first and second order DSM, are decomposed into time-interleaved equivalents. This is done with a polyphase decomposition of the internal filter of the DSM, particularly the integrator, A(z), as shown in the example in Figure 3.12. Low order modulators were used since they provide better coding efficiency, as shown in chapter 2, and usually have simpler hardware architectures favoring higher sampling frequencies.

The DSM internal filter loop $H(z)$, can be decomposed into its M×M polyphase equivalent. $\overline{H}(z)$ is a set of different transfer functions $\overline{P}_{ij}$ such that each parallel output, O_i, depends on the input I_j as shown in equation (3.2). The transfer functions $\overline{P}(z)_{ij}$ are given through the polyphase decomposition of the original $H(z)$ [Vai93]. Re-arranging the new transfer functions into the matrix form, $\overline{H}(z)$ has the form as shown in (3.3).

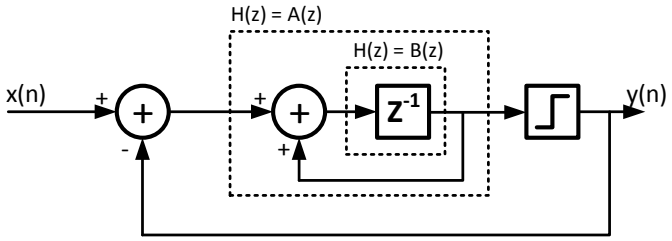


Figure 3.12: Illustrative first order DSM with and integrator as loop filter.

$$O_i(z) = \sum_{j=1}^{M} \overline{H}_{ij}(z) I_j(z) \tag{3.2}$$

$$\overline{H}(z) = \begin{bmatrix} \overline{P}_{1,1}(z) & \overline{P}_{1,2}(z) & \cdots & \overline{P}_{1,M}(z) \\ \overline{P}_{2,1}(z) & \overline{P}_{2,2}(z) & \cdots & \overline{P}_{2,M}(z) \\ \vdots & \vdots & \ddots & \vdots \\ \overline{P}_{M,1}(z) & \overline{P}_{M,2}(z) & \cdots & \overline{P}_{M,M}(z) \end{bmatrix} \tag{3.3}$$

However, the polyphase decomposition changes depending on the function $H(z)$ and there are multiple approaches when using a DSM loop filter. In fact, most of the times this decomposition is done to the loop integrator, which might not be the optimum solution. In the appended paper C two different approaches were used, decomposed the integrator, $A(z)$, and just the delay in the integrator, $B(z)$. As expected, the polyphase decomposition matrices are different depending on the chosen $H(z)$, which results in different hardware implementations as shown in (3.2) and (3.5).

$$A(z) = \begin{bmatrix} \frac{z^{-1}}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} \end{bmatrix} \tag{3.4}$$

$$B(z) = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ z^{-1} & 0 & 0 & 0 \end{bmatrix} \tag{3.5}$$

Matrices (3.4) and (3.5) give the relationship between the input and the output phases such that an output phase is equal to the sum of all the terms of a column each one multiplied by respective the input in each row [Vai93]. Comparing the two approaches some differences are observable from the matrices. In the integrator ($A(z)$ in Figure 3.12), each output depends on multiple inputs multiplied by a different $\overline{P}_{ij}$. In the delay ($B(z)$ in Figure 3.12) approach, most of these partial transfer functions $\overline{P}_{ij}$ are zero, in this case, each output depends on only one of the inputs. This way, the hardware complexity remains reduced since no additional adders are needed to sum the multiple contributions of each input.

The different hardware implementations, that result from both of these approaches, create very different critical paths delays that have a significant difference for the achievable sampling frequency. In paper C, the two decomposition solutions were implemented in a FPGA circuit and an analysis of the maximum clock frequency was made for both the first and second order modulator. For each architecture, the maximum achievable frequency was found for different number of parallel paths from 2 up to 16. The equivalent sampling frequency, f_s is defined as the circuit clock frequency f_{clk} times the number of parallel paths M. For each different polyphase DSM implementation mapping, place and routing routines were used to maximize the hardware clock frequency in the used FPGA device.

Results

The optimization results are shown in Figures 3.13 and 3.14, which display respectively the equivalent sampling frequency and the number of logic levels variation with the number of parallel paths.

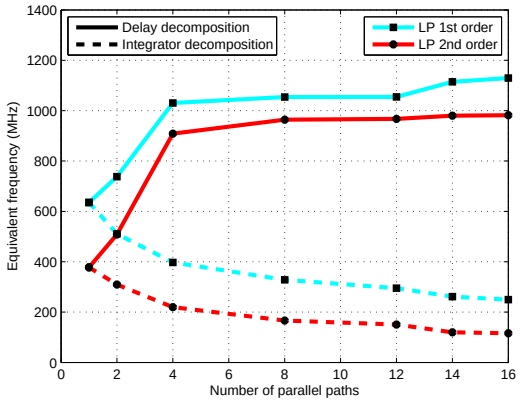


Figure 3.13: Maximum equivalent frequency for the modulator depending on the number of parallel paths.

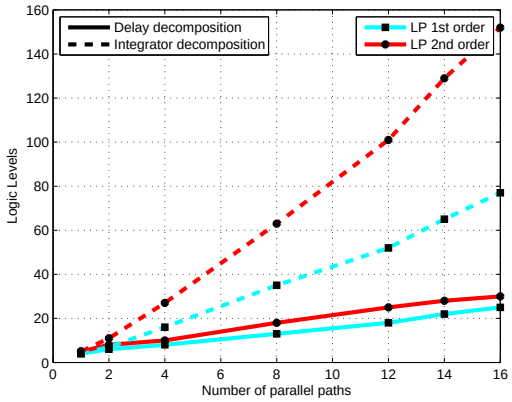


Figure 3.14: Number of logic levels in the critical path depending on the number of parallel paths.

In previous publications, TIDS approaches [EHG11] have been presented with substantial improvement in terms of sampling frequency, however, once you consider the real gains for a specific technology most of these gains disappear or are marginal. Figure 3.13 show that not only the gains are not linear with the number of paths but also that they might not even exist.

For the integrator decomposition, with the growth of parallel paths, the equivalent sampling frequency decreases as can be seen in the dashed line plots in Figure 3.13. This is explained by the growing number of logic levels added to the critical path due to the use of multiple inputs combined for each of the parallel outputs shown in Figure 3.14. Note that these tests consider a specific technology, FPGAs, but can be used without loss of generality.

Independently from the technology, more adder stages must be added to combine the multiple inputs. So, even for different digital logic technologies, the same behavior will occur, just with different frequency values.

Using the delay composition however, there are some gains in terms of equivalent sampling frequency as shown by the solid plot of Figure 3.13. The use of only one input for each output allows this approach to grow in number of parallel paths without additional adder levels. This has resulted in smaller delays in the critical path allowing the polyphase decomposition to have higher frequency gains. However, these gains do not keep expanding with the growing number of parallel paths. In fact, the maximum sampling frequency saturates near 1 Gsps. This happens because even with delay decomposition, there is still a growth in the number of logic levels in the critical path.

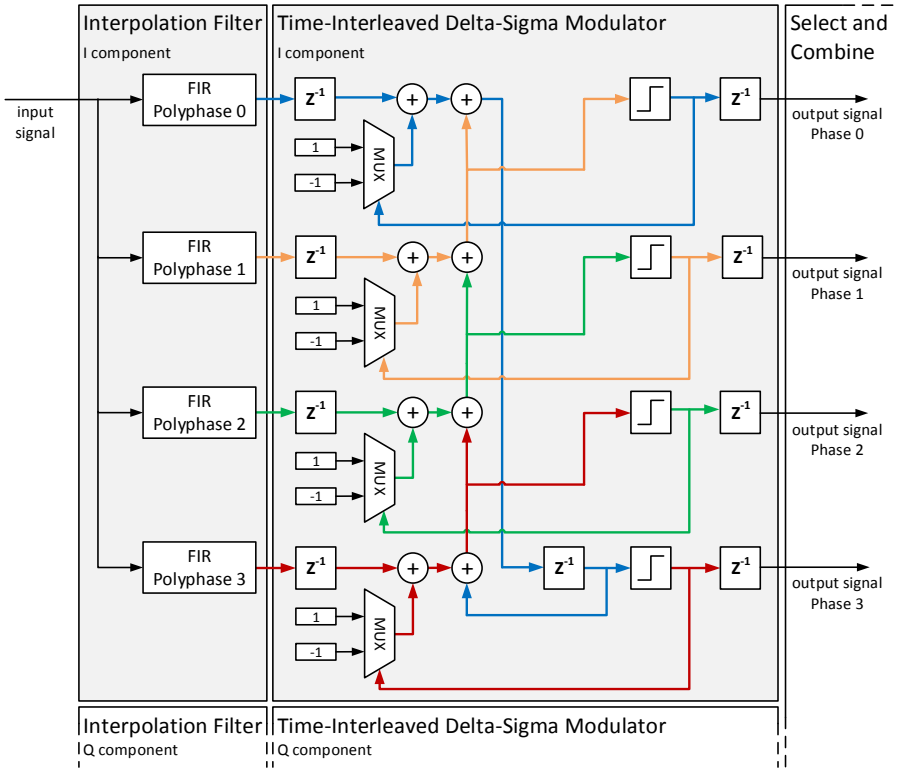


Figure 3.15: Developed TIDS architecture using a first order low-pass DSM with the topology presented in Figure 3.12. In this architecture the polyphase decomposition was made using the delay decomposition as presented in equation (3.5)

Due to the existence of the feedback loop in DSM, the polyphase is never a truly parallel approach from the hardware point of view. Looking to the hardware implementation of the delay decomposition for a first order DSM, in Figure 3.15, we can analyze the precedence relationships between the different input and output phases of the the TIDS. Although multiple output are computed in one clock period, these outputs have a relationship between them.

In fact, the output phase 0 depends on the output phase 1, the output phase depends on the output phase 2 and so on. This dependency is only broken at the last output phase that depends on the previous sample from initial phase 0. This means that although all the phases are computed in a clock cycle, each one of them needs to wait for the signal propagation of the previous phase, increasing the digital path delay.

Nonetheless, with the use of delay decomposition it was shown a minimization of the number of logic levels growth and frequency gains from the polyphase decomposition were achieved for the TIDS. In the appended paper C this resulted in FPGA-based modulator capable of achieving more than 1 Gsps of sampling frequency for DSM as shown in Figure 3.13.

3.2.2 Multiple Parallel Delta-Sigma Modulation for All-Digital Transmitters

The delay propagation limitation of the digital hardware does not allow the massive scalability of the TIDS to further increase the DSM processing speed. Even using improvements to the polyphase decomposition, the modulator sampling frequency still remains the bottleneck of the processing power for ADT, limiting both SNR and bandwidth.

To guarantee the scalability of parallel architectures, ideally, all the signal parallel phases should be independent between each other. This can be achieved be guaranteeing that the output phases do not depend on each other, or at least depend with a delay that allows to add a register between those phases to break the delay propagation.

Proposal

Considering this, an alternative parallel modulator approach is proposed by processing multiple time slots of the input signal independently. While in the TIDS approach, each parallel hardware block processes one of the phases of the signal, it is possible to process a block of contiguous samples correspondent to a contiguous time slot.

The proposed architecture is based on a truly parallel system using multiple DSM cores working separately. Each one of these cores processes independently one contiguous time frame of input signal. Using K single path DSM cores, with different time frames of the input signal, will allow to process a signal with sampling frequency f_s with a hardware clock frequency f_{clk} that is K times lower, or in other words $f_{clk} = f_s/K$. This concept allows for the processing of multiple signal time frames at a clock rate that is $f_{clk} = f_s/K$. Using K DSM cores, the resulting processing rate will be equivalent to a higher sampling frequency of $f_s = K \times f_{clk}$

The proposed parallel concept is explained in Figure 3.16. Consider the input signal presented in this figure to be divided into multiple non-overlapping time segments (orange, green and blue sections on Figure 3.16). Each one of these segments has a fixed length in time corresponding to a segment of N samples and can be processed in parallel in a different

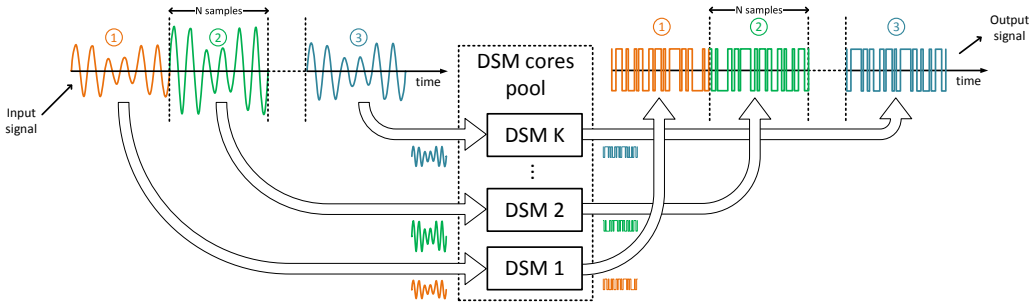


Figure 3.16: Multiple DSM core architecture proposed for increased sampling frequency modulators. Each DSM core independently processes a different time frame of the high f_s input signal.

DSM core. However, DSM cannot be directly converted into multiple parallel and independent modulators with the same output as a single path. Since a feedback loop exists, the past states of the modulator influence the current output signal of the modulator. Even more, DSM uses either integrator or delayed integrator filters depending on the used DSM topology, which by definition have an infinite memory where all the previous integrator states equally contribute for the current integrator state and therefore to the DSM output.

While all the previous states have influence in the integrators of the loop filter, the DSM output converges to the input signal in the signal bandwidth (assuming a proper OSR). Filtering the DSM output signal and comparing it with the input signal allows for the verification that the error between them tends to be minimized over time. In Figure 3.17, an example of the input signal, the filtered DSM output and the error between them is shown. In the image, the filtered output signal eventually converges to the input signal with a negligible error.

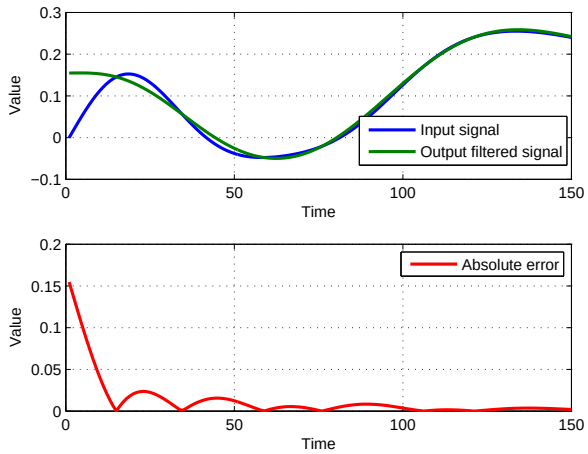


Figure 3.17: Initial response of a Delta-Sigma modulator to a continuous input signal over 150 time steps. Top: Comparison between DSM input and its low-pass filtered output. Bottom: Absolute error value between the input signal and its low-pass filtered output.

It is important to understand that the initial error happens because the initial internal state of the modulator does not consider past states since at the begging of the simulation they are inexistent. Although the modulator has an infinite memory, the error behaves as a decaying memory system, which means that after a certain amount of time the initial state error is negligible.

It is not trivial to find the necessary time or number of samples necessary for the output to converge to the input. This depends on several factors related to both the modulator order and the signal characteristics. Since most of the times we can not predict all the characteristics of the input signal, it is impossible to find a convergence time depending on the signal. However, the modulator order influence is clearer. Higher order DSM have more integrators in the feedback loop, which increases the memory effect and the convergence time. Nonetheless, given enough time the error will eventually be minimized as shown in the example in Figure 3.17.

Using the concept presented in Figure 3.16, in every N samples there would be a transition between time segments that generates an error as presented in Figure 3.17. Understanding the behavior of this error is fundamental to chose an appropriate value for the time segment length N. To find the appropriate block size in terms of samples, the DSM outputs of a single path DSM (SISO DSM) were compared with the same signal being processed in time segments of size N (MIMO DSM). The signals are compared after filtering the DSM noise of the output signals using the same low-pass filter. The signal degradation in terms of signal-to-noise ratio (SNR) is analyzed to compare how much does the MIMO DSM approach deteriorates the signal with reference to the single path method (SISO DSM).

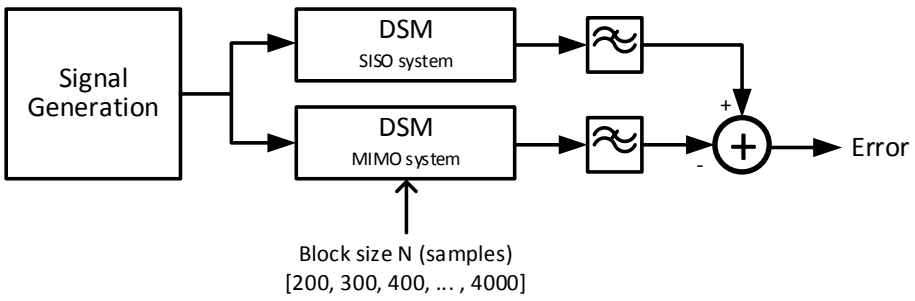


Figure 3.18: SNR degradation simulation between SISO and MIMO DSM.

The simulation method used is shown in Figure 3.18, where the SNR degradation is extracted from the error value achieved from the difference between SISO and MIMO DSM architectures. A set of multiple simulations were made using random multi-tone signals with different PAPR values varying between 3 and 12 dB for a first order and second order DSM. The block size N varies between 200 and 4000 samples with a step of 100 samples between

simulations. The black circles and crosses presented on Figure 3.19 represent each one of the simulation runs with a random input signal for the first and second order DSM respectively. The blue and green lines are the mean value for a certain N value, also for first and second order modulations respectively. Simulation results are shown in Figure 3.19 for the variation of the SNR degradation with the block size N in number of samples.

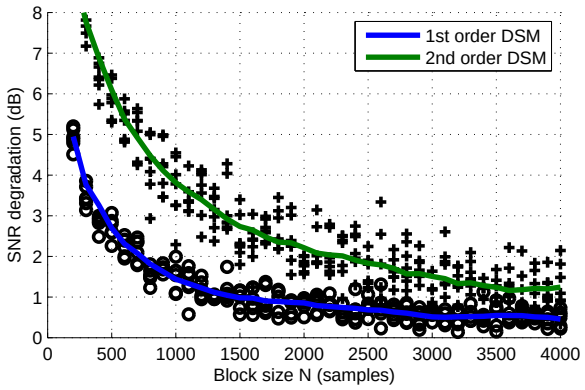


Figure 3.19: SNR degradation between a single path DSM and the proposed multiple core DSM approach. The simulation was run using a set of random signals with PAPR values between 3 dB and 12 dB and bandwidths from 5 MHz to 100 MHz.

It is possible to see, as expected, that the order of the modulator affects the SNR degradation because it changes the amount of memory in the modulation. The second order modulator has a higher signal degradation when compared to the first order modulator because its topology has more integrators hence more memory. This way a second order modulator takes more time to respond to a signal block change, needing more samples to stabilize. The block size N chosen will depend on the desired SNR and will untimely be a crucial factor for the hardware implementation of this concept.

This new modulation concept, as shown in Figure 3.16, was proposed on the appended paper D to improve the transmitter's DSM sampling frequency in order to enhance the achievable signal bandwidth of ADT systems. The proposed architecture is based on a truly parallel system using multiple DSM cores working separately. In particular, the paper D uses 16 parallel paths as shown in block diagram in Figure 3.20. The proposed system architecture uses a polyphase interpolation filter with 16 phases to achieve a higher sampling frequency for the baseband signal. The polyphase interpolation filter generates 16 different phases for the signal, which has a different sample distribution in time from the 16 time segments of the DSM cores. A shift in the organization of the produced samples is necessary. To achieve this a de-interleave block is used such that its parallel inputs, $I_k(n)$, and outputs $O_k(n)$ are related to the polyphase filter phases, $P_k(n)$ accordingly to equations (3.6) and (3.7).

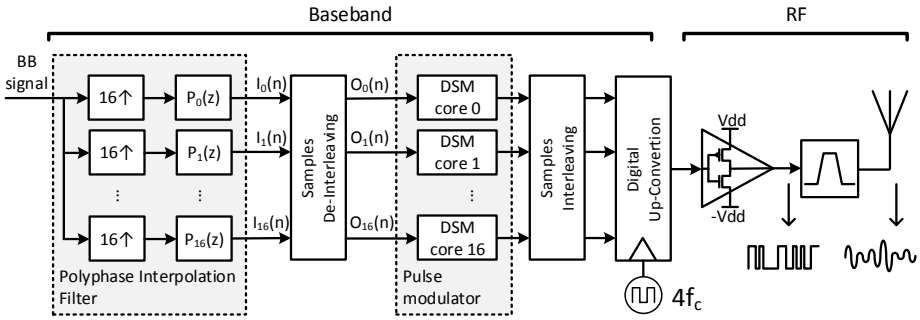


Figure 3.20: Proposed architecture for the wideband all-digital transmitter based on multiple DSM cores.

$$
\begin{aligned}
I_0(n) &= [\quad P_0(0) \quad P_0(1) \quad P_0(2) \quad \cdots \quad P_0(N)] \\
I_1(n) &= [\quad P_1(0) \quad P_1(1) \quad P_1(2) \quad \cdots \quad P_1(N)] \\
I_2(n) &= [\quad P_2(0) \quad P_2(1) \quad P_2(2) \quad \cdots \quad P_2(N)] \\
&\qquad\qquad\qquad\qquad\qquad\qquad \ddots \\
I_{16}(n) &= [\quad P_{16}(0) \quad P_{16}(1) \quad P_{16}(2) \quad \cdots \quad P_{16}(N)]
\end{aligned} \tag{3.6}
$$

$$
\begin{aligned}
O_0(n) &= [P_0(n) \quad P_1(n) \quad \cdots \quad P_{16}(n)] \\
O_1(n) &= [P_0(n{+}N) \quad P_1(n{+}N) \quad \cdots \quad P_{16}(n{+}N)] \\
O_2(n) &= [P_0(n{+}2N) \quad P_1(n{+}2N) \quad \cdots \quad P_{16}(n{+}2N)] \\
&\qquad\qquad\qquad\qquad \ddots \\
O_{16}(n) &= [P_0(n{+}16N) \quad P_1(n{+}16N) \quad \cdots \quad P_{16}(n{+}16N)]
\end{aligned} \tag{3.7}
$$

By changing the interpolated signal sample order accordingly, each one of the independent DSM cores can process a portion of the baseband signal corresponding to a contiguous time block $O_k(n)$. Although the processing is done at a lower clock frequency, it is equivalent to the higher sampling frequency imposed by the polyphase filter. In this particular paper the equivalent sampling is increased up to 3.2 Gsps. After the re-arranged samples are processed in the DSM cores, an interleaving block re-organizes the samples to their original representation as a polyphase signal. However, this is now a set 2-level signals that are a DSM representation of the interpolated baseband signal at 3.2 Gsps. The 16 phases 2-level samples are up-converted using the serializer technique as already explained in this chapter. At the output of the serializer a signal sampled at 3.2 Gsps is obtained.

Results

The improvement on the sampling speed at the DSM stage allowed for the increase of the achievable bandwidth of the modulation with an acceptable SNR. In Figure 3.21 three different transmitted signals are shown using the proposed modulation concept, the increasing bandwidth illustrates the high bandwidth variation allow by this transmitter. The measured signal spectra goes up to a bandwidth of 122 MHz proving that this system is able to cope with large bandwidths.

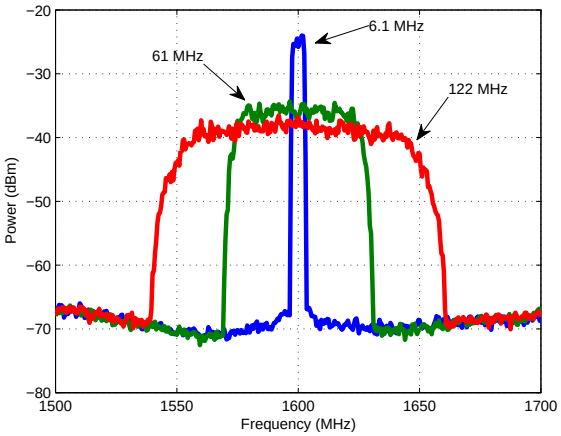


Figure 3.21: Spectra capture of the transmitted signals. The signals are a 6.1 MHz, 61 MHz and 122 MHz 64-QAM for colors blue, green and red respectively.

Additionally, Figures 3.22 and 3.23 show respectively the SNR and EVM measurements for the proposed architecture. Note that up to 122 MHz bandwidth the SNR achieved is always superior to 30 dB allowing for the transmission of high order modulations (an example is the 64-QAM signal shown in Figures 3.22 and 3.23) at high data rates.

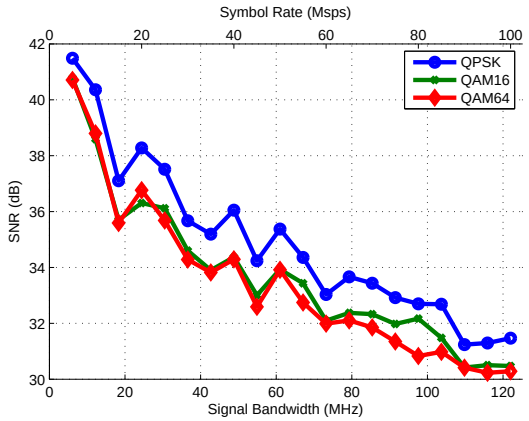


Figure 3.22: SNR measurement for a bandwidth sweep from 6.1 MHz to 122 MHz with a carrier frequency of 1.6GHz.

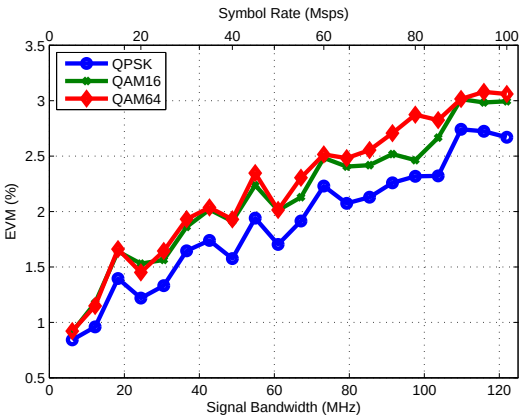


Figure 3.23: EVM measurement for a bandwidth sweep from 6.1 MHz to 122 MHz with a carrier frequency of 1.6GHz.

The decrease in terms of signal power as the bandwidth increases is due to the fixed energy available by the two-level transceiver. The transceiver output signal has a constant energy independently of the signal bandwidth, hence for larger bandwidth signals the energy per Hz is reduced due to the spread trough the larger frequency band of the signal. At the time of this paper publication, this architecture had the highest achievable signal bandwidth for ADT radios. In fact, this architecture allowed the improvement of the state-of-the-art bandwidth from less than 20 MHz to more than 120 MHz.

The system uses a set of parallel DSM cores that are independent between each other but allow for the linear scaling of the hardware improving the sampling frequency of the transmitter modulator. Contrary to other parallel architectures such as TIDS, the proposed method is considerably immune to the complexity of the modulator.

Summary

As the bandwidth is a fundamental figure-of-merit for any transmitter, it was shown in this thesis section that a mixture of signal processing techniques and the clever use of hardware architecture optimizations allows for a significant increase of the transmitter bandwidth. In the previous section two different concepts for parallel DSM architectures were shown both with the purpose of the sampling frequency improvement. Both these architectures have taken advantage of the hardware replication and parallelization of digital circuitry, proving one of the best advantages of digital hardware integration, its scalability. The resulting achievements and conclusions led to an improvement of state-of-the-art figures of merit and were published by the author in the appended papers C and D.

3.3 Enhanced Coding Efficiency Architectures

The focus in this section is on the reduction of the quantization noise created by the digital transmitters. Most architectures rely on the use of low resolution output signals using a direct output from digital hardware without the need of conventional DACs. However, the use of low resolution signals creates a significant amount of out of band harmonic distortion degrading other frequency bands. This section focus on the reduction of this harmonic noise while avoiding narrow band filters or adding in-band distortion.

As previously stated in chapter 2, all-digital transmitters have much more efficient signals at the power amplifier using constant or quasi-constant envelope signals. For the particular case of 2-level signals, it can be amplified using saturated transistors in switch-mode power amplifiers, which ideally would reach 100% power efficiency. However, using highly quantized signals, a substantial amount of the signal is quantization noise. Even though, well taught modulations allow for a significant decrease of the noise within the signal's frequency band, quantization noise in the adjacent bands will always be created trough quantization. For quantized signals, especially using pulsed modulations such as DSM, PWM or PPM, there is a direct relationship between the number output levels and the amount of quantization noise in the signal. In fact, less quantization levels, M, creates more quantization noise added to the signal. This relationship between the quantization noise and the number of levels M follows the known Signal to Quantization Noise Ratio (SQNR), as shown in equation (3.8).

$$SQNR = 20log10(M) \tag{3.8}$$

Although in pulsed modulations, the in-band SQNR can be improved with higher OSR and the clever filtering of the added quantization noise, this noise still remains a part of the transmitted signal as seen in Figure 3.24.

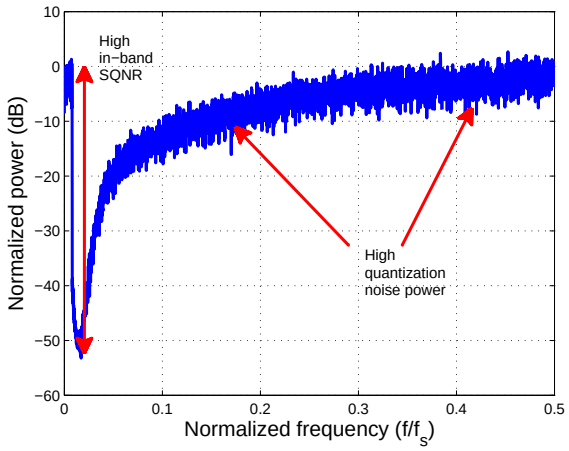


Figure 3.24: Delta-sigma quantized signal spectrum with the signal separated from the higher frequency quantization noise.

Since a significant portion of the signal is quantization noise, a large amount of the power spent for transmission and amplification will be unnecessary and useless. Even more, this quantization noise usually falls in the adjacent frequency bands interfering with other signals. Accordingly to [JS06] this will reduce the overall transmitter efficiency since although a more efficient signal is being used in the PA, a large portion of it is unwanted harmonic noise that should be considered in the overall efficiency. This efficiency can be calculated through the ratio between the total transmitted power and the useful in-band signal power. This is defined as the signal or transmitter coding efficiency (CE) as previously seen in (2.4).

Analog output filters can be used to improve the signal coding efficiency but this comes at a cost. One of the problems is the fact that the narrow-band filter at the transmitter output binds the transmitter to its bandwidth losing some carrier frequency flexibility. On the other side, filtering the signal will destroy the constant envelope that allows efficient SMPAs to be used.

3.3.1 All-digital Transmitter with Mixed-domain Combination Filter

Proposal

To improve the CE in ADT, a new signal combination technique was presented in the appended paper E. This section describes the method proposed to create a digitally controllable filtering of the transmitter's output signal. This method significantly decreases the ADT output quantization noise through a signal combination process, improving its CE as well as its flexibility by relaxing the output filter quality factor requirements.

Multi-level digital transmitters were already used in the great majority of RF-DAC systems. However, in the context of this thesis, only the multi-level digital transmitters that are based in pulsed signal representation are explored. The main concept for these architectures is that the multi-level can be achieved by combining several 2-level outputs as shown on Figure 3.25.

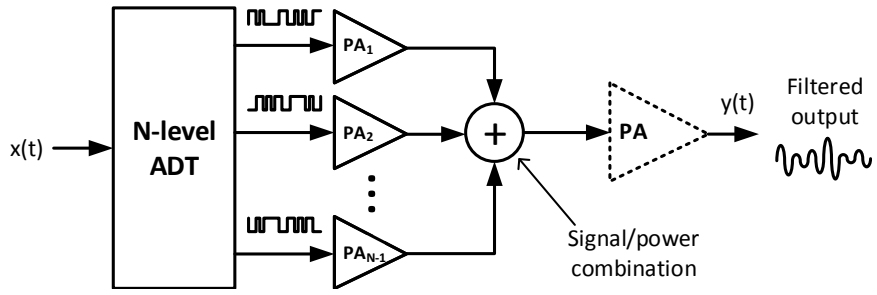


Figure 3.25: Multi-level ADT concept based on the combination of multiple pulsed signals.

These architectures allow to have an output filtered signal, with high CE, while maintaining an amplification stage that uses mainly SMPA. A second PA stage can be used after signal combining. However, after combination, the signal is not a pulsed signal and a SMPA can

no longer be used. A mixed amplification architecture can be used by applying amplification schemes that are highly efficient using small back-off (up to 6 dB) amplifiers. Using this type of mixed architecture one can take benefit of the best of both worlds using high CE signals with low envelope variation as in [EH13] and [JCOC16].

Many multi-level digital transmitters were already presented in previous papers and even commercial products. Most of them are labeled as RF DACs since they are in fact common DAC architectures that work at very high speeds allowing for the direct conversion of RF signals. Similar to the proposed method, RF DACs combine multiple digital outputs in order to have a multi-level signal with higher coding efficiency while maintaining a very integrated architecture. However, there are some challenges in obtaining the required spectral purity at RF frequencies using RF DACs. The major problems rely on frequency-dependent amplitude distortion and nonlinearity spurs [Mal07]. At close-to-Nyquist frequencies, the nonlinear effects become more evident and unwanted harmonic emissions or intermodulation products may occur. Essentially these problems come from the fact that combined signal power levels must be strictly equal and well synchronized to ensure that the RF DAC has a linear response. This issue becomes very difficult to tackle for large bandwidths, which is problematic considering that these signals are modulated at GHz frequencies.

The proposed method in appended paper E uses multiple ADTs combined to compose a constructive combination of signals within the signal bandwidth and a destructive combination in the adjacent side bands. The proposed architecture for this combination method is shown in Figure 3.26. The main difference from other multi-level digital transmitters is that the output signal is not constructed as a multi-level modulated signal strictly speaking, but as a filtering of the original 2-level DSM modulated signal trough signal interference.

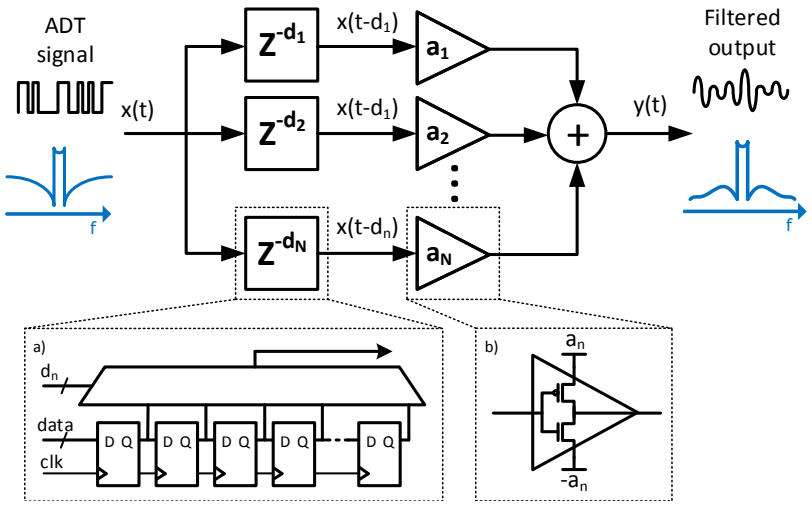


Figure 3.26: Simplified structure of a combination filter as proposed in appended paper E. Each branch has a specific time delay d_n and signal gain a_n.

The original 2-level RF signal is copied to multiple parallel paths, each one connecting to an independent adjustable delay. After the delay, each one of the delayed signals connects to a variable gain stage. By adjusting the variable delays d_n, the gain coefficients a_n and combining these multiple outputs with the adequate weighting, it is possible to cancel the power in particular frequencies of the transmitted signal. Using this technique, filtering stop bands can be targeted at the quantization noise frequency bands. The degree of attenuation depends on the filtering frequency response, which is tightly connected to the number of branches used. Having more branches results in a higher order filtering, however this might not be practical since it relies on the use of a large number of delayed signal paths resulting in higher hardware complexity.

As other multi-level transmitters, this technique has a CE that depends on the number of levels N. From the approximated curve already shown in (2.10) and the Figure 2.15, most of the signals already present a CE superior to 90% after 10 amplitude levels. The proposed filtering method was simulated using as an input a RF 2-level signal from an all-digital transmitter using delta-sigma modulation. In the simulation, the ADT signal was replicated through a variable number of branches adjusting the delays to filter out the quantization error. The number of levels N is related to the number of branches as $N-1$, simulating a number of branches between 1 and 15. Multiple signals with different PAPR values were simulated, particularly signals with 3 dB, 6 dB, 9 dB and 12 dB PAPR. All the signals are real QAM signals with different modulation orders.

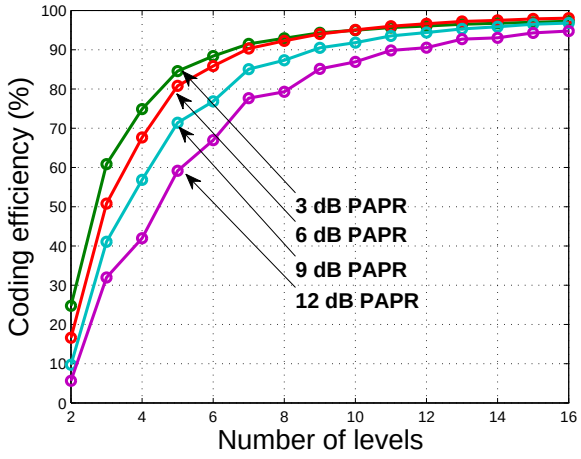


Figure 3.27: Simulation of the coding efficiency variation depending on the number of output levels for different PAPR signals using the structure in Figure 3.25.

From a comparison between Figures 2.15 and 3.27 it is possible to observe the same tendency for both the system simulation and theoretical multilevel transmitter coding efficiency. While the lower resolution results are slightly inferior to the theoretical values, for higher number of levels the values quickly converge.

The filtering structure presented in Figure 3.26 can be used to approximate any desired frequency response within an error margin as small as wanted. The process of combining multiple delayed signals changes the frequency response of the transmitter as in a finite impulse response filter. The frequency response of the proposed filtering architecture, in Figure 3.26, can be treated as a finite impulse response combination filter. The filtering time domain response is defined in (3.9), as well as its Fourier transform in (3.10). The term $H(f)$ is the frequency response of the filter, as generated by the interference between the signals. By adjusting the delays, d_n, and the gains, g_n, in the structure in 3.26, the frequency response can be adjusted to remove the DSM quantization noise from the output signal.

$$y(t) = \sum_{n=1}^{N} a_n x(t - d_n) \tag{3.9}$$

$$Y(f) = \underbrace{\Big(\sum_{n=1}^{N} a_n e^{-j2\pi f d_n} \Big)}_{H(f)} X(f) \tag{3.10}$$

Combining multiple RF signals can be challenging since minor non-ideal properties in the circuit components can introduce problematic errors, especial with signals in the GHz order. On the other hand, it is very difficult to guarantee uniform time delays and gains for a large bandwidth, which is problematic while using pulsed modulator signals. Depending on the OSR, most of the transmitted signal frequency spectrum is noise. When transmitting tens of MHz of signal bandwidth, the total modulator frequency spectrum can easily reach more than 1 GHz of frequency span, most of which has to be filtered. The large frequency spectrum of the transmitter creates a lot of unwanted harmonic content. To filter all this harmonics with the structure presented in Figure 3.26, it is essential that the delays d_n and gains a_n remain constant over a larger frequency band. An example of this is presented in Figure 3.28 where a captured ADT frequency spectrum is shown in a blue color plot. The same figure shows the ideal filter to apply to the signal, in red dashed line, in order to remove the quantization noise.

One of the main advantages of the use of ADTs, is the fact that digital signal processing can be applied to the RF signal directly in the digital domain avoiding the non-ideal behavior of analog components. By nature, digital circuitry is much more immune to components mismatches and non ideal behaviors [BBS+12]. Using 2-level signals, the gain stage can be simplified to a digital buffer with reconfigurable output voltage as displayed in Figure 3.26 b). Digital shift registers were used to define the path delay of the signal as in Figure 3.26 a). This allows to have uniform delays between all the combination paths and constant time delays for the entire bandwidth. The delays are fixed step delays, in which $d_n = k_n d_0$ with d_0 being the output sampling period ($d_0 = 1/f_s$). This means that using this delay, the frequency

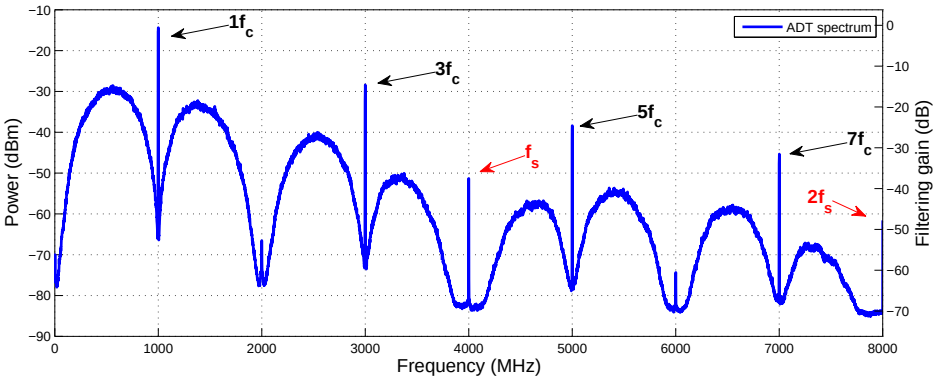
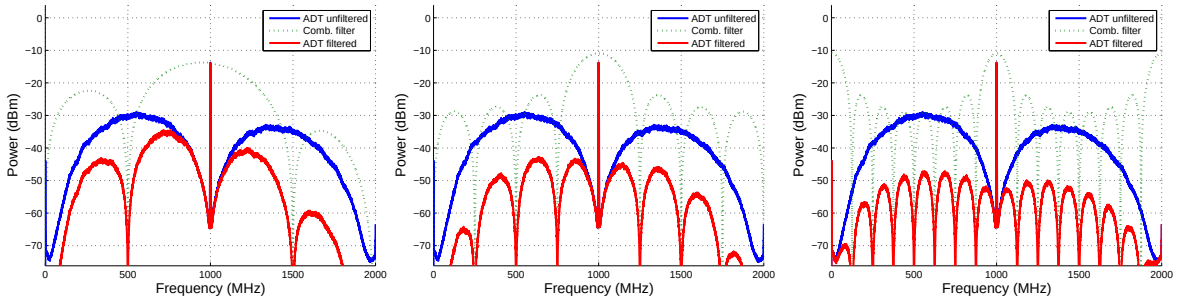


Figure 3.28: ADT spectra for a frequency span of 8 GHz together with the ideal filtering to remove all the quantization noise.

response of the combination filter presented in Figure 3.26 can only be projected between 0 and $f_s/2$ Hz, since it is limited by the sampling frequency at the output of the ADT.

In Figure 3.28, the green dotted frequency response, is one example of the type of filtering achieved by the proposed method. Looking to it in more detail, it is possible to observe that the expected frequency response of this method is very different from the ideal filtering, due to reduced number of branches, 8 in the example figure, but can be used to obtain similar results. This filtering method uses some optimizations were used in order to maintain a reduced complexity for the final transmitter architecture. Besides the passing band in f_c, other passing bands are used in order to improve the attenuation of the quantization noise. By having a bigger time delay between the branches, the same frequency response can be used but in a smaller bandwidth. Using its repetition in frequency, one of the filtering effect image replicas can be used to filter the signal while using a tighter passing band. Figure 3.29 shows three examples of the filtering structure proposed with the same number of branches but using different time delays between them.



(a) $d_n = 1 \times d_0$ (b) $d_n = 2 \times d_0$ (c) $d_n = 4 \times d_0$

Figure 3.29: Example spectra of filtered signals with the proposed method. It shows the combination filter with different time delays while using the same number of branches, 8.

In the examples shown in Figure 3.29, all the combination paths gains a_n were equal,

changing only the time delay. However, further attenuation of the noise can be obtained using different gain coefficients. It is possible to use the DSM spectrum to facilitate the quantization noise attenuation. Using the zeros of the DSM (in the example figures located at DC and 2 GHz), it is possible to use less constraints for the filtering frequency response allowing a passband for the frequencies with DSM zeros, while having narrower bands to filter the signal. In the filtering examples shown, this effect is used in in Figure 3.29 c), which allows for a higher noise rejection. In the appended paper E a method is proposed and used to optimized the gain coefficients and improve both the noise rejection and the coding efficiency.

The proposed filter structure was used in a fully digital transmitter architecture as shown in Figure 3.30. This architecture allows for the full integration of the digital transmitter up to the filtering gain stage into a single FPGA SoC. For the signal combination, a high bandwidth 8-to-1 power combiner was used.

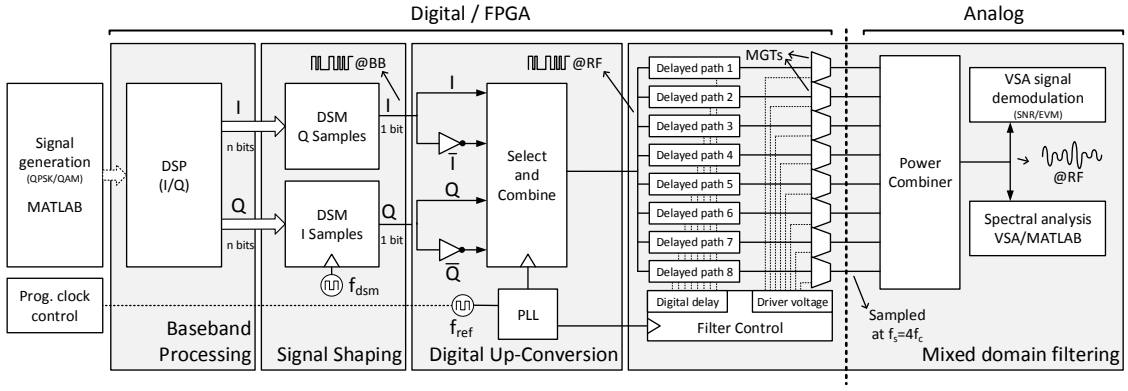


Figure 3.30: Hardware FPGA-based implementation of the proposed filtering method.

Results

The transmitted spectrum is shown on Figures 3.31 and 3.32 for three different filtering options using the proposed FPGA-based architecture. The blue plotted line shows the original ADT signal without any filtering using a 2-level signal. The green line is the output signal using 8 branches with equal gain a_n and a time delay between the branches of $d_n = 1/f_c$. Finally, the last plot, in red, shows the combination signal output spectrum using the optimized filtering coefficients a_n. These coefficients are obtained using a finite impulse response filter design method explained in detail in the appended paper E.

The figures show a high quantization noise decrease, in fact the noise peak power is reduced to more than 40 dB below the carrier as shown in Figure 3.31. While Figures 3.31 and 3.32 only show a 1 GHz, the transmitter was tested for a set of carrier frequencies between 500 MHz and 1.6 GHz. Figure 3.33 shows the variation of the CE across the transmitter carrier frequencies. For each CE measurement the same baseband signal was used within a carrier frequency span between 500 MHz and 1.6 GHz.

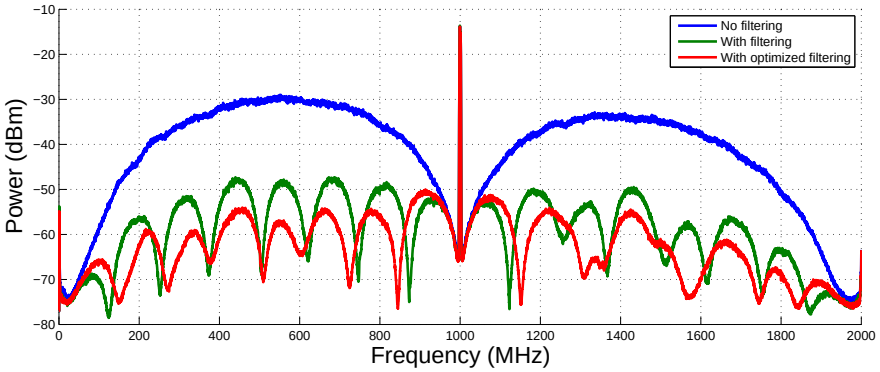


Figure 3.31: Measured spectra captured with a 2GHz span for 3 different filtering scenarios. Signal at 1 GHz carrier frequency with an sampling frequency of 4 GHz.

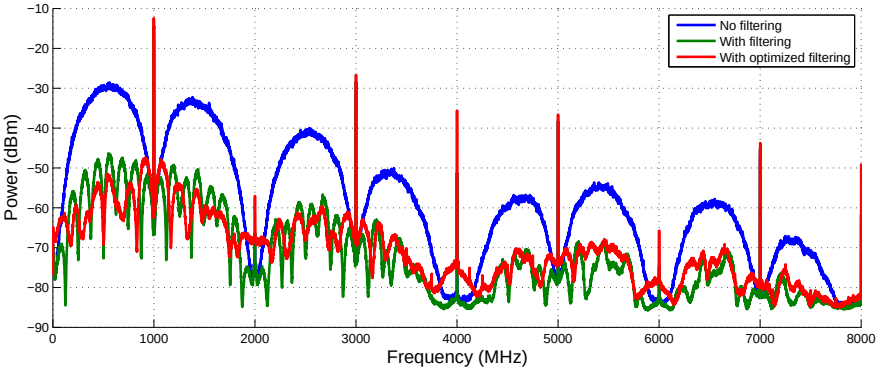


Figure 3.32: Measured spectra captured with a larger span. With this span it is possible to observe the filtering effect for the f_c harmonics as previously shown in 3.28.

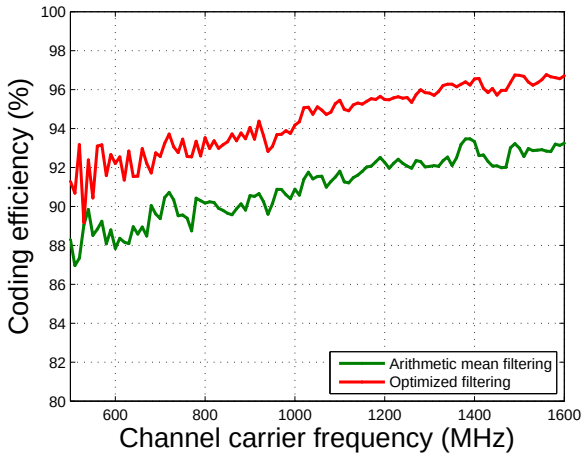


Figure 3.33: Transmitter coding efficiency across multiple carrier frequencies from 500 MHz to 1.6 GHz.

From these measures, it is possible to see that this method allows to achieve a CE of more than 89% within the transmitter's band using the optimized filtering. The small increase of the CE with the carrier frequency is due to the progressive attenuation of the f_c as the frequency increases. This happens because, while a high speed device (up to 10 Gbps), the output of the transmitter has a limited bandwidth. With the increase of the carrier frequency, its harmonics progressively start to be outside of the output sampler's bandwidth.

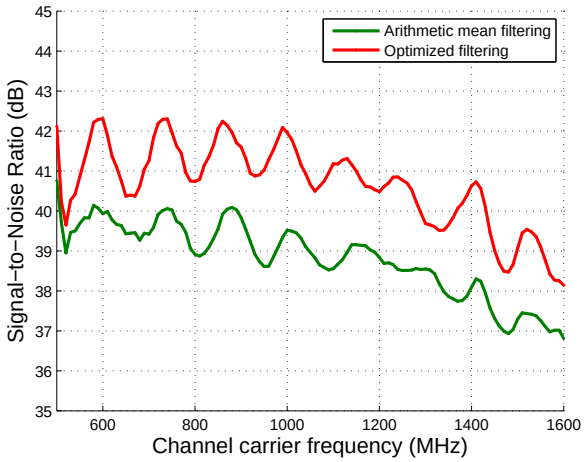


Figure 3.34: Transmitter SNR measurements of a 5 MHz QPSK signal across the carrier frequencies between 500 MHz and 1.6 GHz.

The results show a high carrier-to-noise power ratio improvement as well as a significant advance in the ADTs state-of-art for the achievable CE. As can be seen, the proposed transmitter with this new filtering method provides a very high CE without adding in-band distortion, as proved by the achievable SNR results seen in Figure 3.34. The attenuation of the majority of the quantization noise also improves the flexibility of ADT by removing the necessity of an output narrow-band filter.

Summary

In this section, a new filtering technique for all-digital transmitters was presented to extend their flexibility to the filtering stage. It uses signal interference to cancel the signal at the designated frequencies enabling the reduction of the quantization noise common to ADT radios. With the proposed filtering technique the design of the output narrow band filter can be avoided. Even more, the filtering characteristics can be easily digitally controlled to suit the transmitter carrier frequency improving the overall transmitter flexibility.

From the work presented in this section, two major publications were achieved. The initial proposal of the digital filtering method is presented in the appended paper E and the development of a transmitter system including an highly efficient PA is presented in paper [JCOC16].

3.4 High Flexibility All-Digital Topologies

The focus in this section of the document is the presentation and description of new noise shaping methods developed on the scope of this thesis. The methods presented have the objective of shaping, in the frequency, the quantization noise produced by typical pulsed modulation techniques. The adjustment of the noise frequency distribution allows to mitigate some electrical or physical constraints for the ADT. Specifically, the deliberate change of the noise shape allows to relax the output transmission filter requirements, in terms of central frequency as well as bandwidth.

A considerable advantage of pulse transmitters is the easy and cost-effective implementation of multi-band and multi-carrier transmission, which is impracticable in conventional RF transmitter architectures without hardware replication. It is expected from a multi-carrier transmitter to have a high degree of flexibility to quickly change its carrier frequency. In this sense, the transmitter flexibility is of great importance since the purpose of a digitally controlled transmitter is to easily adapt the radio to its environment and accordingly to the user needs. However, for ADTs using pulsed modulators, the quantization noise at the output signal must be filtered. More often than not, this implies the use of very narrow band filters at the transmitter's output that will constrain the transmitter to work in a very limited frequency band.

Quantization noise shaping systems can be divided into two main types of topologies, open-loop and close-loop converters. The main difference between them is the need to use past states to find equivalent output pulsed signal. The choice of topology has repercussions into the achievable sampling frequency, the hardware complexity of the transmitter and its signal quality. These three factors change accordingly to the type of modulation used. An illustrative qualitative overview showing this is displayed in Figure 3.35.

In open-loop topologies, each output sample depends only on the current input with no interference of past or future samples, this is the case of a hard quantizer or PWM. In these cases the same input value will originate a specific output value disregarding the previous states or outputs of the modulator. Usually this allows for the implementation of very fast hardware architectures, either due to the simplicity of the hardware or by the use of parallel architectures, which are easily implemented as a result of the lack of feedback in the system. However, these techniques usually have low performance in terms of signal quality since there is no feedback to differentiate the quantization noise from the input signal.

Other approach is the use of closed-loop pulsed modulators. In this case besides a quantization block there must some kind of feedback loop to correct the output signal by comparing it to the input. Unlike the open-loop topology, in this scenario previous samples or states are necessary to find the current modulator state, hence its output. The most known case of these modulators is the DSM, which is a particular case of a quantizer with a feedback loop. While this approach allows for a better SNR and a controllable noise transfer function,

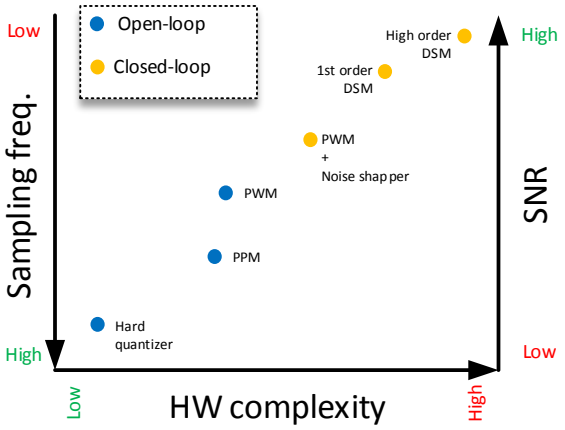


Figure 3.35: Variation of achievable sampling frequency, hardware complexity and signal quality accordingly different pulsed modulations using both open-loop and closed-loop cases.

its complexity in terms of hardware makes these systems quite slower when compared to the open-loop case.

It is important to understand that these topologies have their merits as well as their limitations, so in many cases the choice of one of them relies on the target application and signal properties.

3.4.1 Relaxing all-digital transmitter Filtering requirements through improved PWM waveforms

Pulse-width modulation, or PWM, is one of the most used pulsed modulations for ADTs. It is a well known pulsed modulation that converts high amplitude resolution signals into high time resolution signals with low resolution in amplitude. For a 2-level PWM signal this is achieved by converting the input signal into a square wave with a modulated duty-cycle.

The uniform sampling PWM is a nonlinear process that modulates the input signal as a time pulse with a certain duration or duty cycle. As can be seen in Figure 3.36, the PWM is a square wave with a modulated duty cycle during the period T. The duty cycle is the pulse duration, t_{on}, over the total wave operiod T. Its modulation, as shown in Figure 3.36 can be defined as:

$$\frac{t_{on}}{T} = \frac{s(t)+1}{2} \tag{3.11}$$

The PWM input signal is defined in the interval $s(t) \in [-1, 1]$ hence the duty cycle, t_{on}/T, will be defined as member of the interval $[0, 1]$. This guaranties that the signal will use the

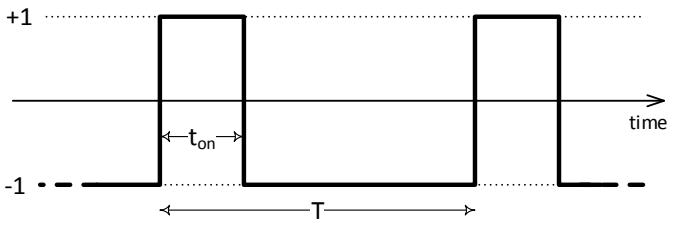


Figure 3.36: Rectangular wave with a variable duty cycle for PWM modulation.

entire duty cycle excursion of the PWM square wave.

Considering that PWM modulation has an relatively high OSR to the input signal, it is possible to approximate the input signal as a constant over the period T. The Fourier series approximation $P_t(t)$ of this periodic square wave with variable duty cycle t_{on}/T is given be the equation (3.12).

$$P_t(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos\left(2n\pi\frac{t}{T}\right) + b_n \sin\left(2n\pi\frac{t}{T}\right) \tag{3.12}$$

With the coefficients a_0, a_n and b_n defined as (3.13), (3.14) and (3.15) respectively.

$$a_0 = 4\frac{t_{on}}{T} - 2 \tag{3.13}$$

$$a_n = \frac{2}{n\pi}\sin\left(2n\pi\frac{t_{on}}{T}\right) \tag{3.14}$$

$$b_n = \frac{2}{n\pi}\left(1 - \cos\left(2n\pi\frac{t_{on}}{T}\right)\right) \tag{3.15}$$

Simplifying all the terms, the final $P_t(t)$ result comes as the one presented in (3.16).

$$P_t(t) = \underbrace{2\frac{t_{on}}{T} - 1}_{S_t(t)} + \underbrace{\sum_{n=1}^{\infty} \frac{4}{n\pi}\sin\left(n\pi\frac{t_{on}}{T}\right)\cos\left(2n\pi\left(\frac{t}{T} - \frac{t_{on}}{2T}\right)\right)}_{N_t(t)} \tag{3.16}$$

With a careful look into this solution for the PWM wave, it is possible to observe that the wave can be divided into two different parts. The first term, $S_t(t)$, is a DC or baseband component that is not modulated to higher frequencies. This term corresponds to the input signal part of the PMW modulated signal and, after solving it for the duty cycle as in (3.17) this term is the input signal it self.

$$S_t(t) = 2\frac{t_{on}}{T} - 1 = 2\left(\frac{s(t)+1}{2}\right) - 1 = s(t) \tag{3.17}$$

On the other hand, the term $N_t(t)$ is a sum of infinite modulated sinusoidal waves. These

tones, are modulated both in amplitude and phase by the duty cycle. Since the duty cycle is given by the input signal, these tones are in fact modulated by the signal. This means that the tones do not have an infinitesimal bandwidth, but instead have a bandwidth that depend on the input signal bandwidth. Even more, the modulated tones in $N_t(t)$ are spaced between them in frequency by $1/T$, which is the frequency of the PWM square wave as in Figure 3.36.

By analyzing the term $N_t(t)$ in the frequency spectrum trough its Fourier transform, $N_f(f)$ as in (3.18), it is evident that the spectrum is infinite, as expected from a PWM signal. The term $N_f(f)$ in (3.18) corresponds to the quantization noise from the PWM modulation and defines the power of the PWM harmonic tones.

$$N_f(f) = 4\sum_{n=1}^{\infty} \frac{4}{n\pi} \left|\sin\left(n\pi\frac{t_{on}}{T}\right)\right| \left(\delta(f - \frac{n}{T}) + \delta(f + \frac{n}{T})\right) \tag{3.18}$$

The value n is the PWM harmonic frequency of index n. When the signal is up-converted to RF the low values of n are closer to the carrier frequency and the high values are further from it. So, the value in (3.19) defines their decreasing power in frequency according to the harmonic index n as seen in Figure 3.37.

$$\frac{4}{n\pi} \left|\sin\left(n\pi\frac{t_{on}}{T}\right)\right| \tag{3.19}$$

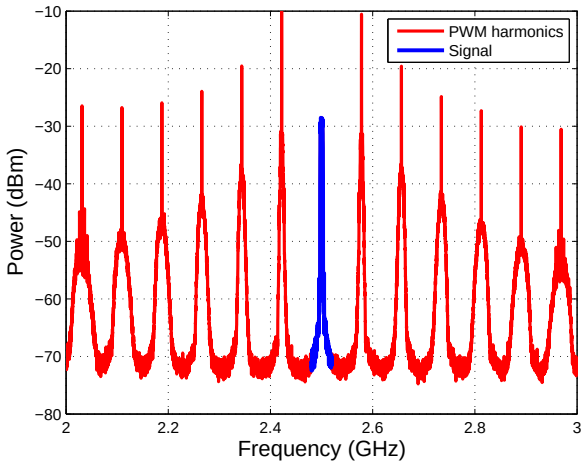


Figure 3.37: PWM spectrum with the signal centered at 2.5 GHz and the PWM distortion quantization noise in the side bands.

While it is normal that the PWM power decreases for higher frequencies, this means that almost all the quantization noise is at frequencies near the signal. Looking to the Figure 3.37 it is evident that the first PWM harmonic has a peak power that is even superior to the signal itself, which is common for high PAPR signals. With such high power level peaks, the filtering becomes more difficult in order to comply with standards spectral masks.

Analyzing equation (3.18) the relationship between the noise peaks and PWM period T

becomes evident. Ideally, decreasing the period T would allow to push the noise peaks further in frequency, away from the signal. However, this would mean an increasing in the sampling frequency of the digital circuit, which in many cases can't be done due to hardware speed limitations.

Proposal

In appended paper F, we take advantage of the high speed serielizer hardware and propose a new approach to decrease the expected T value. The presented method uses a different PWM wave in order to guarantee the minimum T possible for each input value. To achieve this, the initial PWM wave, as presented on Figure 3.36, is shapped in a different way. Its pulse width t_{on} can be divided into smaller pulses over the period T such that the relationship t_{on}/T remains the same.

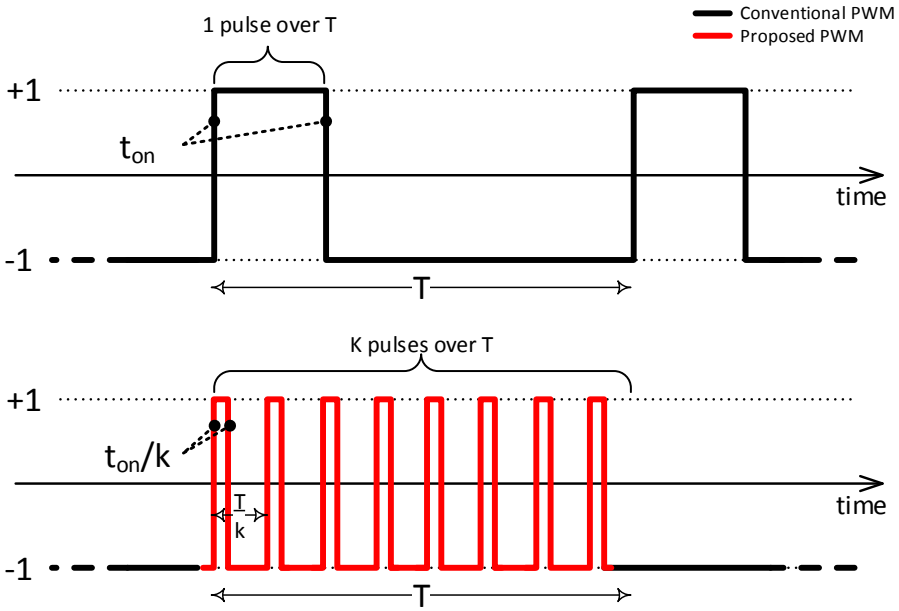


Figure 3.38: Comparison between the conventional and the proposed PWM with smaller and more frequent rectangular pulses.

An example of the PWM proposed in F is shown in Figure 3.38 where the common PWM wave is compared to the proposed method wave. In the original PWM, in black, the entire time span t_{on} is in a contiguous wave. For the proposed method, in red, the same t_{on} is spread in k pulses equally spaced between them, each one with the duration of t_{on}/k. The total time t_{on} is the same for the two waves, however the proposed method wave has a different wave period that will change its frequency spectrum. In fact, now the wave period is no longer T, but instead T/k resulting on a reduction of the PWM wave period.

This means that the equation (3.18) changes to (3.20), which implies the waveform in time as in (3.21). Notice that all PWM harmonics are in a k times higher frequency, hence further away from the carrier frequency.

$$N_f(f) = 4\sum_{n=1}^{\infty}\frac{4}{n\pi}\left|\sin\left(n\pi\frac{kt_{on}}{T}\right)\right|\left(\delta(f-\frac{nk}{T})+\delta(f+\frac{nk}{T})\right) \tag{3.20}$$

$$P_t^*(t) = 2\frac{t_{on}/k}{T/k} - 1 + \sum_{n=1}^{\infty}\frac{4}{n\pi}\sin\left(n\pi\frac{t_{on}/k}{T/k}\right)\cos\left(2n\pi\left(\frac{t}{T/k}-\frac{t_{on}/k}{2T/k}\right)\right) \tag{3.21}$$

Even considering that the waveform is now different, the baseband signal component remains the same. This happens because even with a different time and frequency distribution, the energy over the period T is the same. Realizing the time integral over the period for the equations (3.16) and (3.21) the final PWM signal energy over the period T is the same without depending of k.

$$E_{PWM} = \frac{1}{T}\int_0^T |P_t(t)|^2 dt = \frac{1}{T}\int_0^T |P_t^*(t)|^2 dt \tag{3.22}$$

$$E_{PWM} = \frac{4t_{on}^2}{T} - 4t_{on} + T + \sum_{n=1}^{\infty}\frac{4}{n\pi}\sin\left(n\pi\frac{t_{on}}{T}\right) \tag{3.23}$$

In a further look into equations (3.16) and (3.21), it is also possible to see that the conventional PWM, is just a particular case of the proposed PWM wave where $k = 1$ for every input signal. However, the value k for the proposed PWM method should be chosen such that the period would be as small as possible for all the inputs. Considering this, the value of k should be an integer number as high as possible with two restrictions. First, T/k and t_{on}, should be multiples of the PWM output sampling period $1/f_s$. Secondly, during the period T the total time of high and low levels, must be the same as in the conventional PWM in order to maintain the baseband signal energy, hence not changing the low-pass equivalent signal.

Creating this wave in hardware, using a typical PWM comparator architecture, is not trivial and relies on an higher hardware complexity. However, as shown in section 3.1, a PWM look-up table can be used with the encoded wave levels in memory bits. As an example, in Figures 3.39 and 3.40, the high level of the PWM can be represented as a sequence of '1's and the low level as a sequence of '0's.

These encoded waves can be stored in a memory with all the possible wave outputs. To each input sample, the corresponding input level addresses one memory position with the output wave information stored in it. Using this strategy the PWM outputs are stored in a memory as a LUT and the PWM conversion will be reduced to the serialization of the corresponding PWM word from the correct position of the LUT.

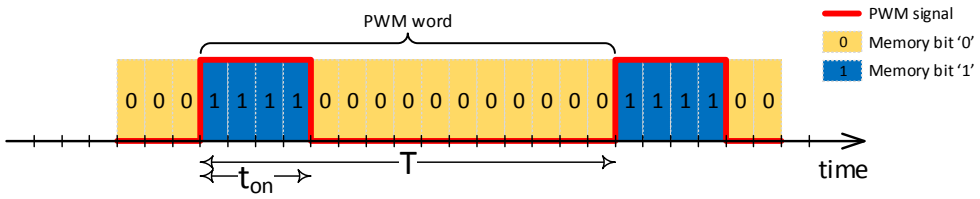


Figure 3.39: Conventional PWM wave with memory bits encoding the output wave levels.

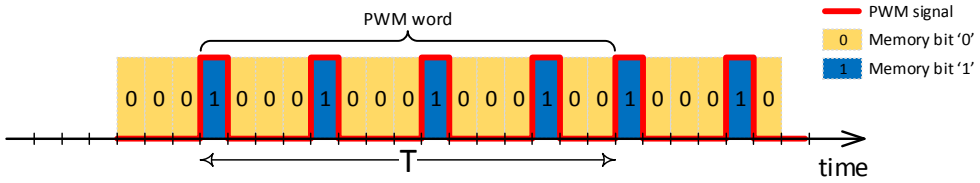
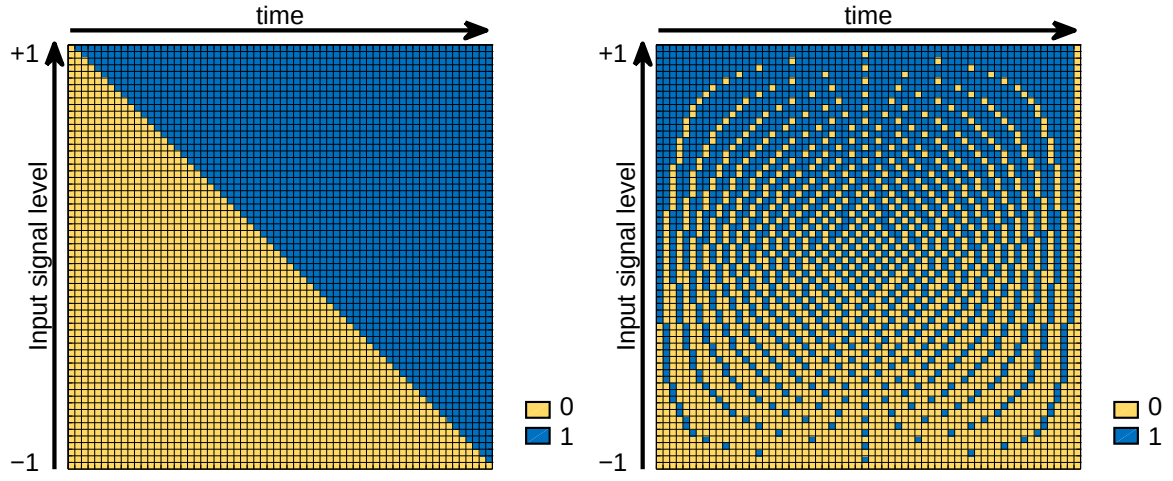


Figure 3.40: Proposed PWM wave with memory bits encoding the output wave levels.

Figure 3.41 shows a visual example of the memories used for the PWM conversion, as well as its output wave across time (horizontal lines) for each input signal level. As can be seen the waveform suggested in 3.38 can be easily achieved simply changing the PWM look-up table memory. In fact, this change doesn't increase the complexity of the PWM since both the necessary memory size and the PWM sampling frequency remains the same as in the conventional approach. In a closer look to the LUT representations, one can observe that the number of bits with the value 0 or 1 are same between memories for the same input signal level. Just the distribution of the 0's and 1's is different, changing the frequency spectrum



(a) Regular PWM memory.

(b) Proposed PWM memory.

Figure 3.41: Illustration of the PWM memories used, with conventional PWM modulation in 3.41a and the proposed PWM in 3.41b.

during the time period T. Even so, the wave energy remains the same during that period since the wave integral over the time T is the same.

With this simple change, the PWM now has different wave period that depends on the input level, contrary to the constant value of T for the conventional PWM. This will spread the harmonics of the PWM in frequency. Even more, since the purpose of the altered waveform is to minimize the PWM wave period, hence increasing the PWM harmonics frequency, it will shape the PWM harmonics to higher frequencies (as shown in equation (3.21)).

To test this method a set of MATLAB simulations was made using both the regular PWM and proposed PWM. On Figure 3.42, the test flow for simulations and measurements is shown. An IQ digital baseband signal is generated and then converted in two different PWM blocks. The conversion is done using the look-up table concept previously explained and after up-converted to the desired carrier frequency, in this case 2.5 GHz. The digital RF signal is analyzed in terms of emitted spectrum and transmitted signal quality. The two PWM methods are then compared with each other using their SNR and their PWM distortion harmonics peak power.

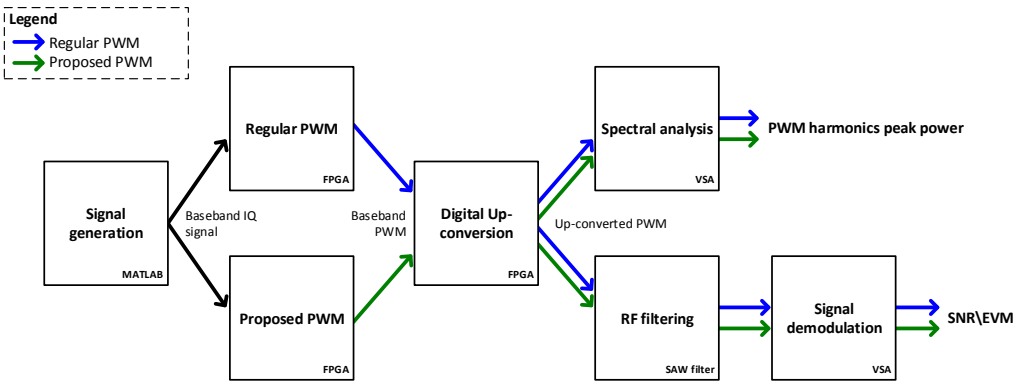


Figure 3.42: Diagram with the flow for measurement setup presented in the appended paper F. The same method was used in MATLAB simulations and system measurements.

Results

The simulation results are shown in Figures 3.43 and 3.44. In these figures, the decrease of the harmonic peak power is noticeable for the PWM harmonics closer to the carrier frequency. These simulations prove the concept, however they assume ideal square waves for the PWM. In practice this is not true, since the transceiver has a limited band and non-ideal behaviors. Nonetheless, the limited bandwidth should behave as a low-pass filter for the simulated spectra, which should not influence the achieved results with the proposed PWM.

The proposed PWM method was published in appended paper F, where a FPGA-based ADT architecture is presented to show the different of the conventional PWM technique and

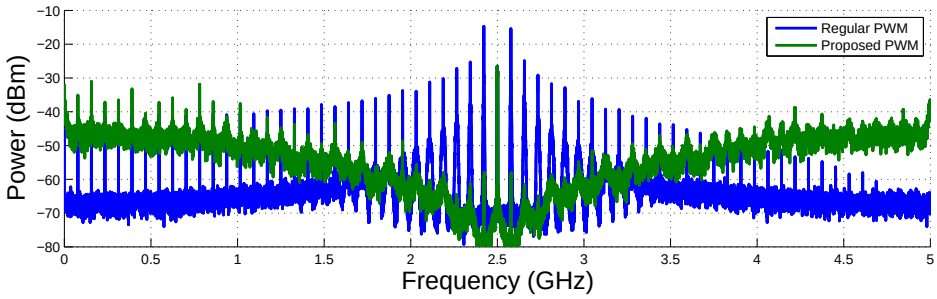


Figure 3.43: MATLAB simulation results for the regular and proposed PWM spectra.

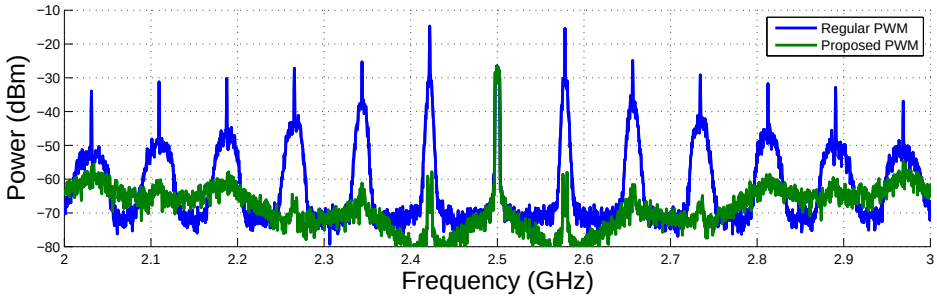


Figure 3.44: MATLAB simulation results for the nearest PWM harmonics to the carrier.

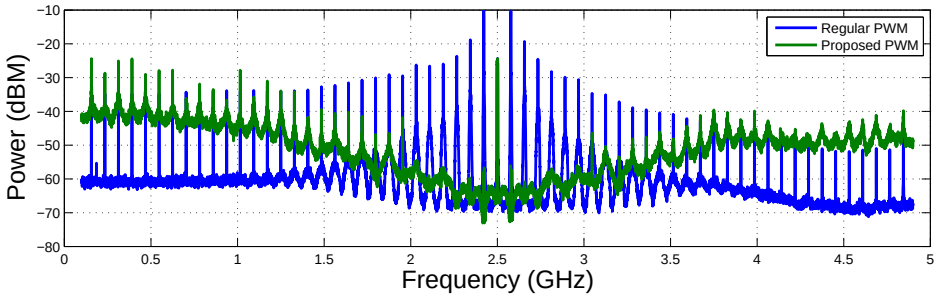


Figure 3.45: Spectrum measurement results for the regular and proposed PWM spectra using the FPGA-based ADT prototype.

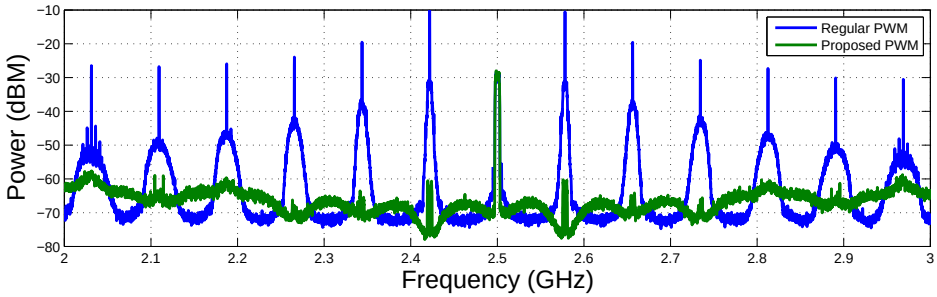


Figure 3.46: Spectrum measurements for the first PWM harmonic frequencies near the carrier frequency.

the proposed modified method. The proof of concept prototype was designed using the same architecture for both the regular PWM and the proposed method, but using different look-up tables to convert the baseband signal. The implemented FPGA architecture allows to use both PWM memories and switch between them. The prototype was also tested using the flow presented in 3.42 using MATLAB for baseband signal generation, a FPGA prototype as the digital transmitter and the VSA for RF signal acquisition, demodulation and analysis. The measurements results for comparison with simulation are presented on Figures 3.45 and 3.46.

Simulation and measurement spectra have quite similar results overall for the regular PWM and the proposed waveform. However, Figures 3.43 and 3.45 have a slight discrepancy between simulation and measurements within 4 GHz and 5 GHz. This happens, because contrary to simulations, the implemented prototype has a limited frequency response for the transceiver. This is clearly visible through the attenuation in the measurements results for this frequencies. Even so, this effect is an attenuation in the frequency response, hence it is a linear effect that does not interfere with the effects of the proposed PWM.

In both the simulation and measurement results it is clear the benefit of the proposed method PWM with the substantial decrease of the peak power in the PWM harmonic frequencies near the carrier frequency. The larger portion of the noise, that used to be concentrated in the first harmonics around the carrier frequency for the regular PWM is now shaped to frequencies further way from the carrier in the proposed method. With just the change of the PWM look-up table, the PWM waveform was changed to provide lower wave periods, which becomes evident as less energy is concentrated near these harmonic frequencies.

In table 3.1 it is shown the amount of attenuation for each of the PWM harmonic peaks for the lower harmonic frequencies (left side of the carrier) and higher harmonic frequencies (right side of the carrier). The test signals used were three different QAM signals with 3 MHz, 6 MHz and 12 MHz of bandwidth at 2.5 GHz carrier frequency.

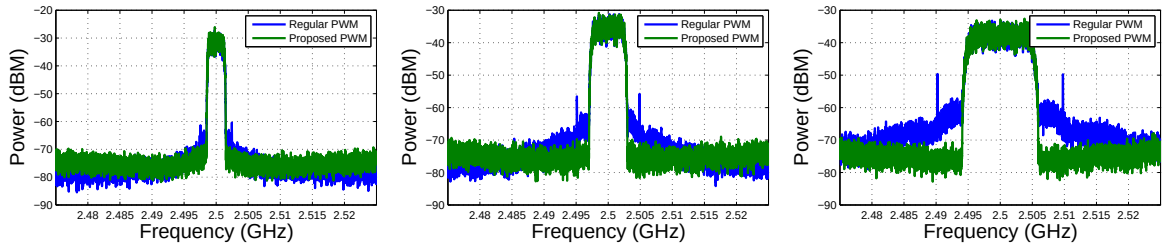
The measured values suggest that the quantization noise peak reduction becomes less effective as the signal bandwidth increases. However, it should be noted that the reduction in the first harmonic was more than 45 dB for all signals, proving that the proposed PWM concept works.

Upon further inspection to the measurement results, it is possible to find another advantage of the proposed method. In Figure 3.46 a smaller span around the carrier frequency of the measurements results is shown. Note that as the signal bandwidth increases for the regular PWM, there is a spectral degradation of the signal in the carrier frequency. This happens because the input baseband signal is not a tone, it has a certain bandwidth. Recovering equation (3.16) one can perceived that the PWM harmonics are amplitude modulated by the signal s(t) as in (3.24).

$$\left[\frac{4}{n\pi}\sin\left(n\pi\frac{t_{on}}{T}\right)\right] = \left[\frac{4}{n\pi}\sin\left(n\pi\frac{s(t)+1}{2}\right)\right] \tag{3.24}$$

Table 3.1: PWM noise power peak reduction

	Harmonic peak	Carrier Offset	Test Signal Bandwidth 3MHz	6MHz	12MHz
Lower harmonics	6th	-468.7 MHz	28.2 dB	31.2 dB	32.5 dB
	5th	-390.6 MHz	32.6 dB	32.2 dB	36.2 dB
	4th	-312.5 MHz	33.0 dB	33.7 dB	34.8 dB
	3rd	-234.3 MHz	39.3 dB	42.3 dB	39.9 dB
	2nd	-156.2 MHz	46.5 dB	44.0 dB	42.8 dB
	1st	-78.1 MHz	**51.8 dB**	**50.5 dB**	**45.5 dB**
Higher harmonics	1st	78.1 MHz	**52.1 dB**	**49.7 dB**	**45.3 dB**
	2nd	156.2 MHz	44.7 dB	44.6 dB	41.8 dB
	3rd	234.3 MHz	38.5 dB	40.7 dB	39.5 dB
	4th	312.5 MHz	30.5 dB	33.1 dB	33.8 dB
	5th	390.6 MHz	31.5 dB	31.2 dB	34.9 dB
	6th	468.7 MHz	25.5 dB	28.2 dB	30.3 dB



(a) 3 MHz bandwidth signal. (b) 6 MHz bandwidth signal. (c) 12 MHz bandwidth signal.

Figure 3.47: Spectra comparison between the regular PWM digital transmitter and the proposed PWM for a 50 MHz span around the 2.5 GHz carrier.

Since the PWM harmonics are modulated by a function of the type $sin(s(t))$, this means that there will be a spread frequency spectrum from each harmonic frequency that grows with the $s(t)$ signal bandwidth. For larger bandwidths, this will spread to the carrier signal and interfere within its band as in-band noise for the transmitted signal and will degrade its SNR. To prove this, the SNR of different bandwidth transmitted signals was measured for both the regular and proposed PWM, the results are on Figure 3.48.

As can be seen from the measured SNR, its degradation with the increase of the bandwidth can be quite significant. However, the same degradation does not happen for the proposed method. This can be explained because the energy of the PWM harmonics closer to the carrier frequency is much lower with the proposed method, hence the distortion spread to the carrier frequency will be of a much lower power creating no significant interference with the signal. As it is possible to see from the results, the proposed PWM method allows for significant advantages when compared to regular PWM modulation with the same hardware and sampling frequency characteristics. The main advantages are the shaping of the PWM

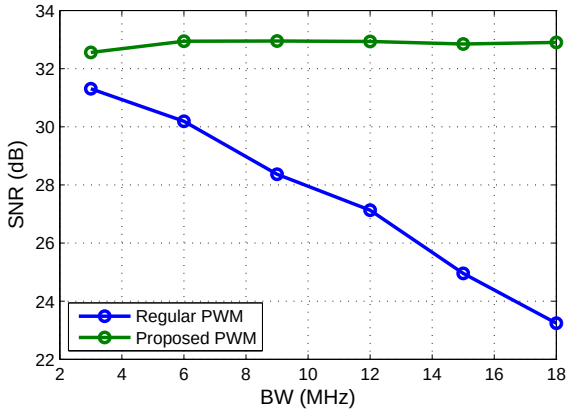


Figure 3.48: Comparison of the measure SNR between the regular and proposed PWM for multiple bandwidth values.

---

noise to higher frequencies as well as the improvement of the SNR figure-of-merit.

3.4.2 All-Digital Transmitter with Waveform Design for SDR

One of the main limitations that hinges the flexibility of ADTs is the ability to change its carrier frequency. While most of the architectures allow for a quick change of the carrier, most of the times this variation is limited to a very strict frequency band. A well known way to change the ADT carrier frequency is using bandpass DSM with tunable NTF. Contrary to PWM, the noise shaping of the DSM turns this modulation suitable to be used in variable bandpass scenarios. This is achieved adjusting the internal loop filter of the DSM, which changes its quantization noise shaping and frequency response.

However, the use of tunable filters in the DSM loop introduces complex high order modulations that have several limitations. A bandpass DSM that allows a good noise rejection necessarily have high order, and consequently have instable loops, difficult to maintain stable without the use of complicated optimization algorithms for DSM [ST05]. This becomes a demanding task if one wants to have a real-time flexible carrier for the ADT since it either relies, on the use of a large amount of stored parameters, or in the increase of computational power to find a suitable loop filter.

Other limitation, which is aggravated by the increased system complexity, is the hardware implementation. Simple DSM loops already have stringent time constrains that limit its sampling frequency. This is mainly due to the fact that they use a closed feedback loop architecture that relies on previous samples to find the current state. Tunable bandpass DSM architectures, have an additional degree of complexity for the loop filter. Additional multiplications and sums are necessary to find the adequate filter coefficients in order to properly shape the quantization noise. For both reasons, typically bandpass DSM have a small sampling frequency and are limited to a very restricted frequency range. Considering

this, the flexibility achieved by the close-loop architecture loses its advantages due to its reduced bandwidth.

Proposal

In the appended paper G a new simplistic hardware architecture based on the original SDR approach is presented. This hardware architecture together with an adaptable processing algorithm, enables the fast switching between multiple tunable carriers. It allies the noise shaping characteristic and tune ability of the DSM together with a high sampling frequency open-loop architecture.

The proposed system uses a look-up table (LUT) in a concept similar to the previous PWM presented. The hardware architecture for the system is presented in Figure 3.49. The system uses a LUT memory to store the output RF wave to be transmitted. The memory output is serialized at the sampling frequency such that one bit in the memory word of the LUT corresponds to the sampling period T_s. To choose between the LUT entries the output to be serialized, the baseband signal is converted to a memory address. Each input signal IQ sample will correspond to a LUT entry and consequently to a different output.

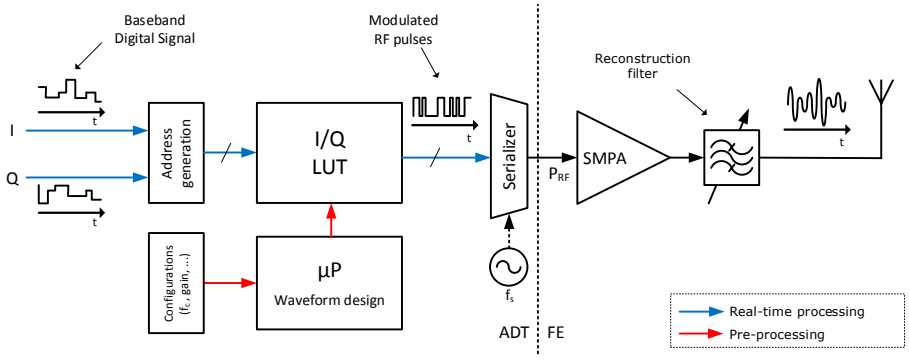


Figure 3.49: Proposed all-digital SDR transmitter hardware architecture.

A hardware architecture such as the one presented, is agnostic and can be used with a multiplicity of modulations or pulse shapers since it all depends on what is stored in the LUT and how the signal is interpreted. In this sense, the LUT generation algorithm for the waveform design plays an important role for this architecture since all the RF signal modulation is done at this stage. The use of a software modulator for RF signals is unrealizable in real-time for frequencies at the GHz range.

Nonetheless, software gives a significant freedom and flexibility for the modulator. In this particular process, the micro-controller will be used for an off-line generation of the output waveforms that will change with the carrier frequency. For each different carrier frequency, a new LUT is generated with all the possible outputs then stored in memory. To do so, the wave generation algorithm must run once for all the possible combination of inputs

and generate the appropriate RF output to store. This process can occur off-line, or even during transmission, but not at the signal rate. With a slower rate, the generation of the output signal and corresponding modulation, can be done via software without any hardware frequency constraint.

In order to generate the correct RF wave, an algorithm is used to do the DSM signal conversion. The used algorithm can be divided into the following steps:

1. Quantize the input complex signal I and Q components to N levels

$$S_i(n) = Quant[I(n)] \quad S_q(n) = Quant[Q(n)] \tag{3.25}$$

2. Compute a complex carrier wave, CW, for the corresponding carrier frequency f_c with M samples.

$$CW_i(n) = \cos\left(2\pi\frac{fc}{fs}n\right); \quad CW_q(n) = \sin\left(2\pi\frac{fc}{fs}n\right); \tag{3.26}$$

3. Compute RF wave for specific amplitudes considering S_i and S_q constant during M samples.

$$S_{rf}(n) = S_i \times CW_i(n) + S_q \times CW_q(n); \quad n \in \{0, 1, 2, ..., M-1\} \text{ for all } [S_i; S_q] \text{ pairs.} \tag{3.27}$$

4. Convert the RF signal to pulsed a RF representation using delta-sigma modulation.

$$P_{rf}(n) = DSM(S_{rf}(n)); \text{ for all } [S_i; S_q] \text{ pairs.} \tag{3.28}$$

5. Store RF wave in LUT memory.

$$LUT(S_i, S_q, n) = P_{rf}(n); \quad n \in \{0; 1; ...; M-1\} \text{ for all } [S_i; S_q] \text{ pairs.} \tag{3.29}$$

Once the algorithm runs for all the $[S_i; S_q]$ pairs, the LUT contains the necessary information to convert the signal to the specified carrier frequency f_c.

For the DSM any modulator can be used, as long as it is a passband modulator at the same frequency as the carrier wave CW. While there are many different DSM topologies, from the functional point of view most of DSM loops can be simplified to the trivial system presented in Figure 3.50.

In the presented topology the feedback quantization error, $E(z)$, is filtered by the loop filter, $H(z)$, and is fed back to be subtracted to the input signal $X(z)$. The combination of

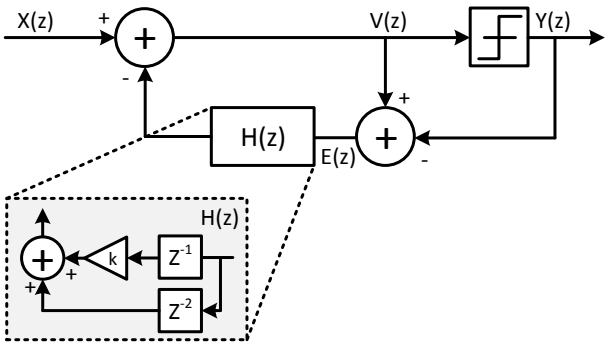


Figure 3.50: DSM feedback loop architecture with tunable $H(z)$ filter.

---

the original input signal and a filtered, $V(z)$ in the figure, will be quantized to the signal $Y(z)$, which is the system output. The resulting noise transfer function, $NTF(z)$ will be defined be the tunable loop filter as in (3.30).

$$Y(z) = X(z) - \underbrace{(1 + H(z))}_{NTF(z)} E(z) \tag{3.30}$$

The complexity of $H(z)$ for the proposed ADT architecture in paper G is not significant since the loop filter can be calculated off-line. The final LUT is an approximation to a high speed bandpass DSM with a sampling frequency that is not affected by its complexity. Since growing complexity is not an issue for this architecture, it is the perfect candidate to use elaborate filters capable of changing its frequency response.

A simple, yet interesting application case is shown in Figure 3.50 where a filter $H(z)$ is proposed using a variable k to change the $NTF(z)$ notch frequency. Let $H(z)$ be as in (3.31).

$$H(z) = kz^{-1} + z^{-2} \tag{3.31}$$

The corresponding $NTF(z)$ filter will be as in (3.32).

$$NTF(z) = 1 + kz^{-1} + z^{-2} \tag{3.32}$$

The $NTF(z)$ is a filter with two complex conjugated zeros defined by the variable k. Solving it for its Fourier transform, the frequency response is as shown in (3.33).

$$NTF(f) = NTF(e^{j2\pi}) = 1 + ke^{-j2\pi} + e^{-j2\pi\times 2} \tag{3.33}$$

Forcing a notch in the normalized frequency f_0, or $NTF(f_0) = 0$, the value k is given by the equation (3.34).

$$k = -2\cos(2\pi f_0); f_0 \in [0; 0.5] \tag{3.34}$$

Knowing this, the DSM's NTF response, particularly the NTF notch, can be changed for a specific frequency band as an tunable bandpass converter. Figure 3.51 shows the NTF frequency response for different k values, and therefore f_0 values, creating different zeros with the change of the loop filter $H(z)$.

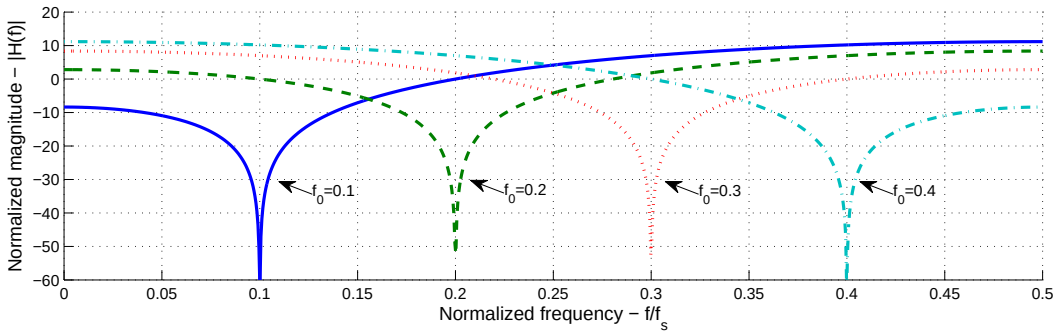


Figure 3.51: Different NTF frequency responses of a tunable bandpass DSM. The notch frequency, is decided by the value of k in the loop filter as in Figure 3.50.

This simple tunable modulator was tested with the above mentioned transmitter architecture. Using a simulation for the entire LUT-based ADT transmitter, several carrier frequencies were tested with the proposed algorithm and tunable DSM.

In Figure 3.52 the simulation results of the proposed ADT output are shown for different frequencies. Notice that the DSM zero changes between LUT algorithm runs to tune the zero to the appropriate signal band.

Using tunable bandpass DSM it is possible to design a variable frequency DSM-based all-digital transmitter. The carrier frequency should be on the NTF notch of the bandpass DSM to have a two level output with a signal centered at the desired carrier frequency. The carrier frequency will be defined according to the specified f_0 value and the output sampling frequency f_s such that the carrier frequency is given by $f_c = f_0 \times f_s$.

Without hard frequency constraints for the signal modulator allows to have a very fast sampling, imposed only by the maximum clock frequency allowed for the used technology. Additionally, it allows to use modulators with the benefits of a closed-loop modulation but the

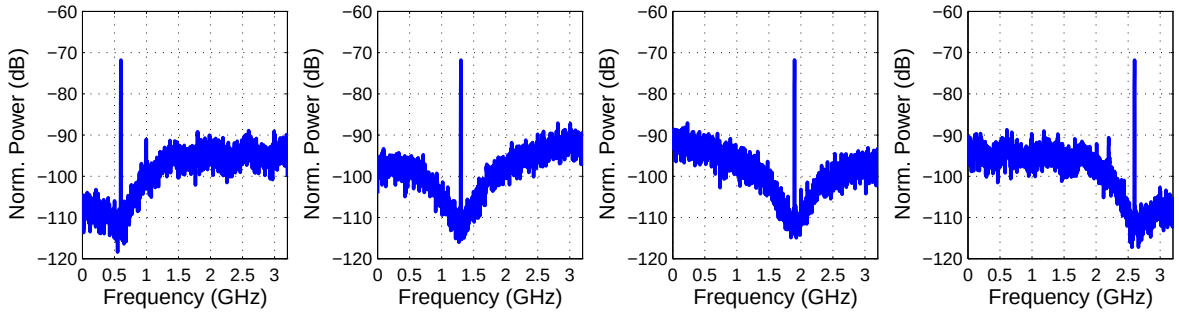


Figure 3.52: Simulation of the output spectrum of the proposed LUT-based transmitter using the complex conjugated zeros NTF.

---

simplicity and speed of open-loop modulation hardware. While this approach has a beneficial trade-off between two different topologies of modulation, it is still a compromise that is not a true closed-loop modulation.

The use of the LUT as a signal modulator is an approximation of the real DSM modulation and therefore there will be some signal degradation when compared to the ideal high speed DSM. It is important to understand that the ideal high speed DSM is not feasible with a conventional hardware architecture, however it is used here as a comparison term in the simulations to understand the approximation effects of the proposed method.

The DSM process can be viewed as an amplitude quantization of the input signal. This is already a well known process that as been analyzed many times in multiple publications and is not the focus of this analysis. However, in this system, there is also an approximation of an infinite length pulse stream to a finite length one when the DSM pulses are approximated by a LUT entry. This occurs during the LUT creation for a fixed number of input entries in the previously shown algorithm.

The first step in the proposed algorithm is the input signal quantization to a specified number of levels N. This quantization to the signals $S_i(n)$ and $S_q(n)$ is necessary to reduce the number of entries in the LUT. Since every $[S_i(n); S_q(n)]$ pair will have have a specific LUT entry, a high number of levels will dramatically increase the size of the LUT as it grows quadratically with N. On the other hand, the quantization factor, N will largely determine the achievable SNR of the system, as in (3.35), since it introduces quantization error to the input signal.

$$SNR_{dB} = \underbrace{20\log(N)}_{quantization} + 1.76 + \underbrace{10\log\left(\frac{f_{bb}}{2BW}\right)}_{process\ gain} \tag{3.35}$$

In (3.35), the SNR depends on the number of levels N but also on other factor that is the process gain. Since the baseband sampling, f_{bb}, is considerably higher than the signal's bandwidth BW, the baseband signal already has a considerable OSR. This excess in sampling

will spread the quantization noise evenly in the entire sampling spectrum, slightly reducing the noise power in the signal's bandwidth.

After quantization the signal must be interpolated up to a higher sampling rate, $fs = M \times f_{bb}$, to allow for direct digital RF up-conversion. This interpolation happens in the algorithm when the constant signals $S_i(n)$ and $S_q(n)$ are multiplied by the carrier wave CW. By considering that the baseband signal is constant during M samples, this multiplication process will consider an up-sampling operation. The equivalent signal processing scheme is a interpolation by a M factor, followed by a zero order hold (ZOH) filtering. The size M will influence the RF wave size at the output, for larger values of M the wave will last longer and will be a better approximation of the RF signal for the same $S_i(n)$ and $S_q(n)$ samples. However, larger interpolation factors M imply longer time periods with constant $S_i(n)$ and $S_q(n)$ values, which reduces the bandwidth of the baseband signal, since the baseband sampling f_{bb} is reduced.

Due to the above mentioned relationships, there must be a well balanced trade-off for the N and M values between LUT dimension ($N \times N \times M$), available bandwidth and achievable SNR. A comprehensive study of this trade-off is done in the appended paper G. The main results are shown in Figure 3.53. This figure shows the variation of signal SNR in dB for a set of N and M values with the proposed transmitter architecture. The dashed plot, used for comparison, is the theoretical SNR limit of a quantized signal for a specified number of N levels, as in equation (3.35) while considering a 5 MHz tone sampled at 100 MHz. The black plot below corresponds to a real-time DSM simulation of a 5 MHz bandwidth signal with a sampling frequency of f_s. In the simulations, the hardware is considered ideal and only the variation analyzed is in the values N and M. The plotted data, in Figure 3.53, allows to see how the choice of N and M influences the SNR, and allows to choose the necessary dimensions for the LUT considering the target signal quality.

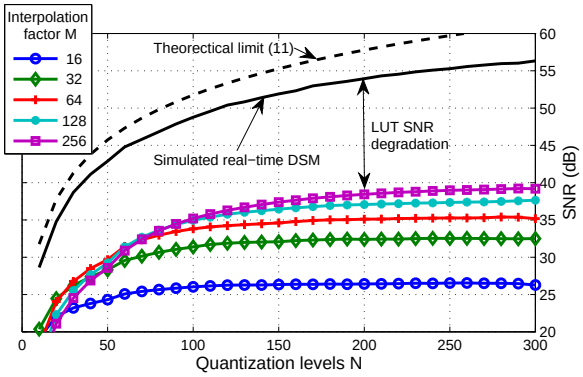


Figure 3.53: Variation of the proposed transmitter SNR depending on the LUT size given by $N \times M$. The values presented are simulation results for a 5 MHz signal.

Results

The proposed ADT system was implemented on an FPGA circuit as depicted in Figure 3.54. Further details about the implementation are shown on the appended paper G.

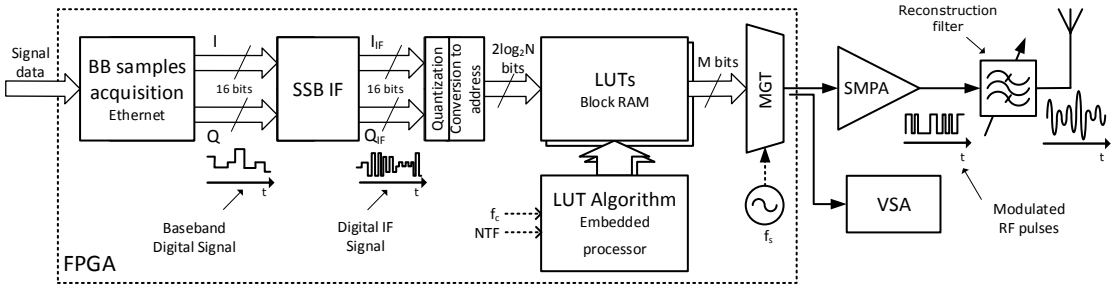


Figure 3.54: FPGA-based prototype hardware architecture of the proposed transmitter.

The hardware architecture has an output sampling, defined by the MGT, set to 6.4 Gsps making the maximum achievable carrier frequency 3.2 GHz. The wave size, M, was set to 64, which implies that the f_{bb} is 100 MHz. For the specified M value, the chosen value N was such that it would be possible to have SNR values between 33 dB and 35 dB. Using the data in Figure 3.53, this would correspond to a LUT size N around 100. In the paper G the chosen value is $N = 128$ because it is a power of 2 allowing for the simplification of the quantization process with a simple truncation to the most significant bits. The used DSM in the algorithm was the tunable bandpass modulator as presented in Figure 3.50.

The RF output signal was connected to a Vector Signal Analyzer for signal and spectral analysis. An example of the transmitted output spectrum is shown on Figure 3.55 with the complete spectrum from DC up to 6.4 GHz.

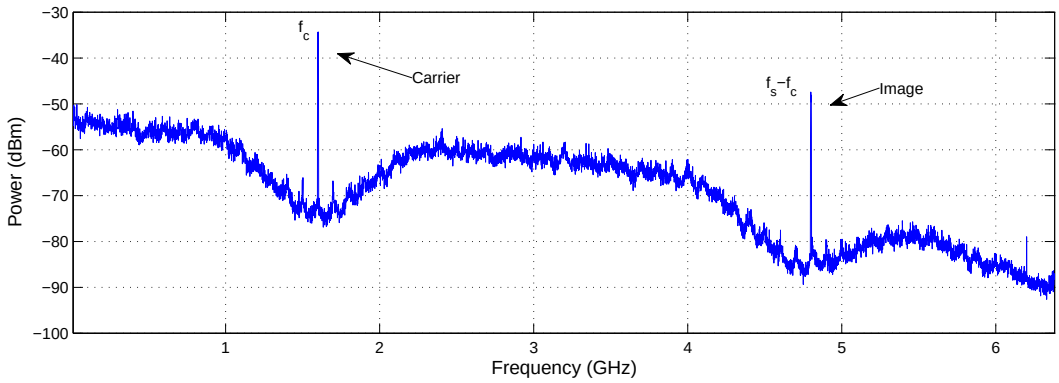


Figure 3.55: Captured spectrum of the proposed FPGA prototype.

In the figure above, it is possible to see the transmitted spectrum that is comparable to a very high sampling DSM modulator. The spectrum has a noise shaping equivalent to a DSM

with 3.2 GHz sampling frequency. It is also possible to see the image of the carrier frequency at $f_s - f_c$ as a result of the sampling function.

Different carrier frequencies were tested to prove the versatility of the LUT generation algorithm. Figure 3.56 shows four different carrier frequencies, which correspond to four different values of f_0 in the algorithm. The plotted spectra have 1 GHz span around the center frequencies of 0.9 GHz, 1.6 GHz, 2.4 GHz and 2.8 GHz.

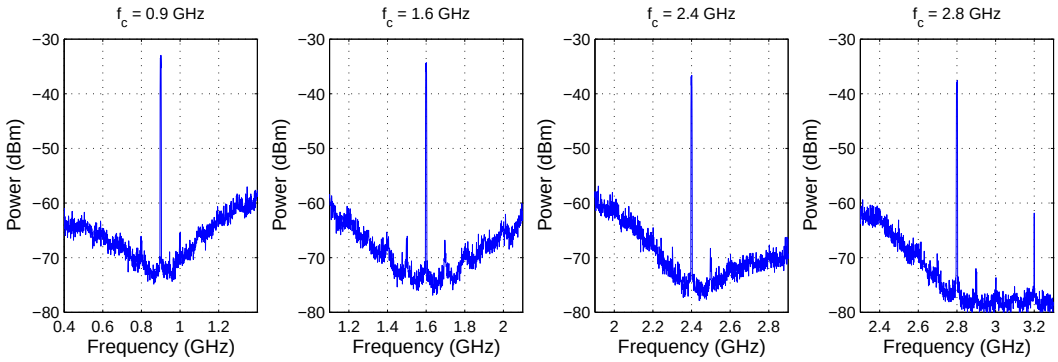


Figure 3.56: Detailed captured spectrum of the proposed FPGA prototype for different carrier frequencies by changing LUTs.

To achieve a higher degree of flexibility, two different LUTs are used for a faster switch between carriers. Using this scheme, one of the LUTs can be created (by running the algorithm) during a signal transmission that uses the other LUT. The transition between LUTs will happen in just a clock cycle that takes only 10 ns.

Other improvement was the addition of single sideband band (SSB) IF converter to allow for a fine tuning of the carrier wave. Although the LUT can change the carrier frequency, it is limited to multiples of the baseband signal sampling f_{bb}. In the particular case presented in the paper G, this frequency is 100 MHz. The added IF stage allows for the change of the IF frequency between -50 MHz and 50 MHz resulting in the full coverage of the entire frequency range between 400 MHz and 3.1 GHz for the carrier frequency.

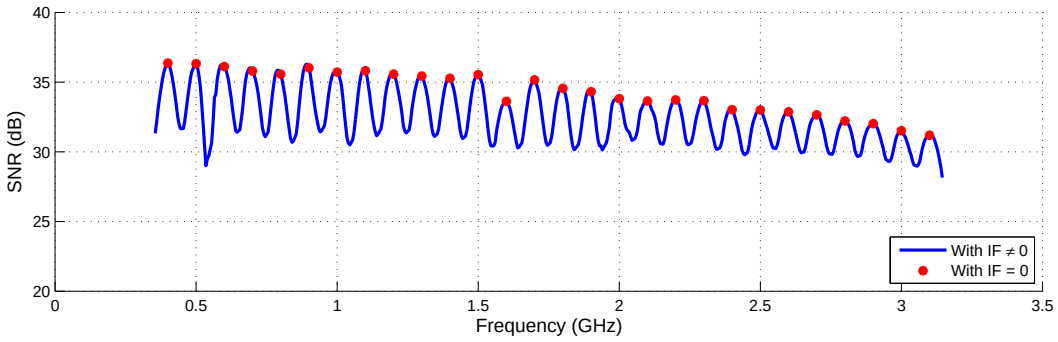


Figure 3.57: Measured SNR sweep for the tested carrier frequencies. The sweep uses a 5 MHz step for the carrier frequency.

The quality of transmission was evaluated across its carrier frequency range using the SNR value of the output signal. The measured SNR is relative to a demodulated 64-QAM constellation. A more detailed analysis of the results is made on paper G, but from the presented results a reasonable SNR is obtained for the entire frequency range. This shows the feasibility of the proposed architecture as a SDR capable of fast changing its carrier frequency using only a different parameter in a software algorithm.

This architecture shows the feasibility of a very flexible ADT, in which the carrier frequency, the modulation and its noise shaping can be defined and adjusted by software. This allows for the use of a fixed hardware architecture for multiple transmitters, greatly improving the flexibility of the radio system.

Summary

In this section, new noise shaping techniques were presented for all-digital transmitters. The purpose of these techniques is to provide a broader shaping of the quantization noise added by pulsed modulators and granting a higher degree of flexibility to the ADT system.

The presented techniques not only allow for less constraints for the output filter but also allow for a fast changing in the carrier frequency configuration. This is achieved by combining the speed of open-loop modulator systems with the noise shaping advantages of closed-loop topologies.

From the work presented in this section two publications were presented with the development of a new PWM method in the appended paper F and a new, highly flexible, LUT-based ADT architecture in the appended paper G.

Chapter 4

Conclusion and Future Work

4.1 Conclusions

The work presented in this PhD thesis focused on the study and design of agile digital hardware architectures for efficient and spectrum flexible all-digital transmitters. For this, innovative and flexible architectures were developed and prototyped, resulting in the improvement of some state-of-the-art figures-of-merit such as bandwidth, signal-to-noise ratio and coding efficiency.

In the initial part of this thesis, a general explanation of the ADTs was shown, as well as the motivation for the adoption of this radio concept in modern wireless networks. Also, a general approach for the implementation of ADT architectures in FPGAs was presented along with the discussion of its benefits and limitations. Together with some optimization techniques, DSM and PWM-based architectures were shown and compared as enabling techniques for pulsed-based ADT.

After this, a thorough discussion about the ADT bandwidth limitations and possible improvements were examined. Different enhancements to the pulsed-modulator sampling frequency were revealed as feasible solutions for the increase of the typical ADT bandwidth values in previous state-of-the-art work. The solutions converge on the advantages of parallel architectures, taking advantage of FPGA's inherent hardware integration as well as its hardware replication potential. The proposed techniques for the parallelization of the pulsed-modulators hardware resulted in an important understanding about its hardware frequency scalability. This knowledge has culminated on the improvement of the state-of-the-art bandwidth for ADTs.

Other important focus of this thesis was on the overall efficiency of the transmission system as a result of the used pulsed-signal transmitters. The proposed combined signal method was demonstrated as a new approach to reduce the quantization noise from low-resolution pulse-signals. To improve the low coding efficiency typical in ADT, this method uses multiple high-speed pulsed transmitters to reduce the out-of-band noise at specific frequencies. This

has largely improved the transmitter coding efficiency and it is also an important step towards an highly flexible ADT, adding the capability of a flexible digital filtering technique.

Lastly, two novel noise shaping techniques were presented in order to provide a further degree of flexibility for ADTs while maintaining a completely digital transmission system. In the presented work, a new way of producing a pulsed modulated RF signal is demonstrated using a minimalistic hardware architecture. The main novelty of this technique is that the pulsed modulator characteristics can be directly modeled and described in software. The use of a generic hardware architecture allows for further digitalization of the radio and establishes an important step towards the fully digital SDR.

Overall, in this PhD thesis it was shown the improvement of ADT figures-of-merit in terms of SNR, bandwidth, spectral purity and efficiency while using efficient and flexible hardware architectures based on common FPGA circuits.

4.2 Future work

The potential for pulsed-based all-digital transmitters is deeply related to the high degree of integration that modern digital logic delivers. The modern proliferation of radio wireless networks in new challenging environments, as is expected for the Internet-of-Things era, will further push the radio designs into smaller and smaller devices. At the same time it is expected that a single radio device is capable to cope with multiple standards using different frequencies, diverse coding and modulation schemes. Even more, the simultaneous use of multiple standards can be the way to make a more efficient use of the radio hardware, saving power and circuit area.

Considering the points described above, future work for the ADT can be explored through massive integration of radios in digital circuitry. One possible use, is the construction of a large array of radios that use multiple independent transmitters to achieve spacial gain of diversity in massive MIMO and space power combining systems. The conventional large-scale antenna systems rely mainly into a single conventional RF architectures using multiple antennas and equal number of parallel conventional RF chains. The replication of the analog frontends is a major obstacle to the integration and scalability of these systems, therefore, alternative approaches must be found. Digital reconfigurable all-digital transmitters can take advantage of the large number of I/O resources, together with a massive number of antennas and miniaturized filters, to implement scalable, compact and all-digitally controlled antenna arrays targeting 5G systems.

Another interesting possibility is on the development of flexible, simultaneous multichannel and multistandard digital transmitters. For this system, the use of multiple multigibabit outputs produced from a single FPGA can be used for the production of simultaneous multiple independent outputs. Such a solution would rely on the precise cancelation of the quantization

noise in the multiple transmitting frequency bands through the signal combination at the output of the system. The big advantage of this type of implementations in FPGAs is the large amount of I/O resources that would allow for the use of highly integrated solutions with multiple radios on the same chip.

Appendix A

All-Digital Transmitter with RoF Remote Radio Head

Rui F. Cordeiro, Arnaldo S. R. Oliveira, and José Vieira

in ***2014 IEEE MTT-S International Microwave Symposium (IMS)***

DOI: 10.1109/MWSYM.2014.6848470

All-Digital Transmitter with RoF Remote Radio Head

Rui F. Cordeiro,Arnaldo S. R. Oliveira and José Vieira
Departamento de Electrónica, Telecomunicações e Informática and Instituto de Telecomunicações
Universidade de Aveiro
Campus Universitário de Santiago, Aveiro, 3810-193, Portugal
Email: ruifiel@ua.pt, arnaldo.oliveira@ua.pt, jnvieira@ua.pt

***Abstract*—This paper presents a new radio-over-fiber system that uses an all-digital transmitter architecture enabling a very simple remote radio head comprised only by an amplifying stage, a bandpass filter and an antenna. An all-digital transmitter is proposed to implement a flexible centralized digital radio, able to perform the baseband processing and transmission of radio signals at radio frequencies (RF) over an optical fiber. The digital signal at RF is transmitted over fiber using a simple on-off digital modulation, reducing the limitations of conventional analog radio-over-fiber systems, but maintaining the advantages of a reduced complexity transmitter radio head.**

***Index Terms*—All-Digital Transmitter, Digital Radio-over-Fiber, RF-over-Fiber.**

I. Introduction

The increasing need for more flexible and cost effective wireless networks has been a major concern over the last years in telecommunications. Modern access networks have seen an increasing number of base-stations needed to fulfill the utilization demands, and at the same time a convergence between several different wireless standards to an unique access point.

In order to reduce the wireless systems cost but maintaining their easy manageability and updatability, a possible approach is to concentrate all the system complexity in a central station (CS) where a greater portion of the signal processing and network management is focused, leaving the network edge, base-stations or remote radio heads (RRH), with simpler, low power and more cost effective solutions. This solution heavily relies in an effective method to connect the CS to the RRH. A promising solution for this is the use of Radio over Fiber (RoF) transmission, using the high bandwidth capacity of optical fiber to sustain the high data-rates necessary to send the radio signals, allied with low losses enabling greater distances. Several RoF approaches can be used depending on the signal to be transmitted and distance ranges.

Most of the RoF systems use analog modulation in the fiber, modulating the wavelength of the transmitter laser accordingly to a baseband (BB), intermediate frequency (IF) or radio frequency (RF) signal. However, analog modulation is more prone to non-ideal behaviors such as non-linear effects, that cause intermodulation distortion reducing the dynamic range, and fiber chromatic dispersion that limits the transmission distance due to the signal attenuation in the fiber especially when modulating RF signals [1].

Digitized RoF techniques have been proposed to surpass the common RoF limitations [2]. Instead of analog modulation, digital samples are sent over the fiber and converted with a DAC at the RRH. This type of solution can increase substantially the complexity at the RRH side depending if the transmitted signal is BB, IF or RF. For the BB case, a complete radio is needed at the RRH resulting in a relatively complex and costly radio head. A similar case applies for the IF case. Even with no BB processing at the RRH, a complex radio is still needed for the digital to analog conversion and the signal up-conversion to RF frequencies. In the case of digital RF-over-fiber no additional hardware besides the DAC is necessary, however for RF frequencies there is a need of a high sampling rate DAC which will increase the cost per RRH unit, diminishing the gains obtained from a simpler radio [3].

In this article a new RoF approach is shown using a two-level digital RF signal from an all-digital transmitter (ADT) and a Gbps optical link to transmit the signal to a very simple RRH that uses only a bandpass filter and a RF amplifier. This solution stands for its simplicity for the RRH unit, similar to the analog RF-over-fiber solution but using a digital modulation in the fiber.

II. All-Digital Transmitters State of the Art

All-digital transmitters have been explored over the last years as a system-on-chip (SoC) solution for Software Defined Radio for their potential flexibility and reconfigurability. While the completely digital generation of RF signals is already a well known concept [4], the full advantages in flexibility, reconfigurability and integration are yet to be fully explored.

A technology that promises to be an interesting platform to the ADT concept is the field-programmable gate array (FPGA). Its hardware integration, reconfigurability, flexibility and processing power in modern FPGA's seem to be a convenient solution for a modern fully integrated SDR system.

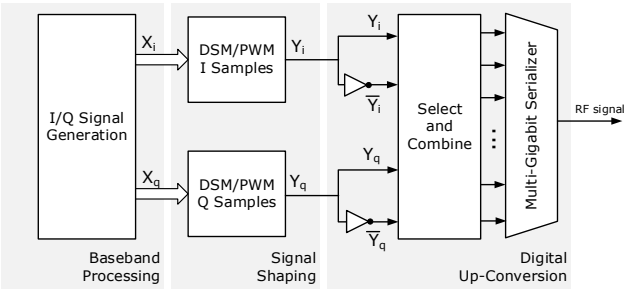


Fig. 1. FPGA based all-digital transmitter architecture.

FPGA-based ADT systems were already presented in [5] and [6] with similar architectures (see Fig. 1). The baseband signal is processed using a pulse modulator, with delta-sigma modulation (DSM) or pulse width modulation (PWM), and a digital up-conversion conversion stage that modulates the binary signal with a square wave at RF. More recent advances to these architectures were made to improve the DSM noise shaping characteristics using parallel architectures in [7] and [8], and to allow multimode and multichannel transmission in [9] improving ADT's flexibility.

III. All-Digital Transmitter with Remote Radio Head

The proposed system architecture is shown on Fig. 2. It is composed by a completely digital CS that receives the digital information to be transmitted. The CS applies the baseband processing and then the RF up-conversion. The signal at the fiber is binary and is generated by the ADT and converted with an electrical-optical (E-O) converter in the CS. This signal, can be converted back into a digital electric signal at the RRH using an optical-electrical (O-E) converter. The RRH unit receives the signal that only needs to be filtered and amplified to be sent to the antenna.

A. ADT Central Station

An ADT is used to implement the signal shapping and up-conversion up to RF frequencies of the BB signal. The output is a 2-level electric signal centered at the carrier frequency and with quantization noise in the side bands. The quantization noise may vary depending on the pulse modulator chosen, DSM or PWM. It was used DSM to shape the quantization noise out of the signal's band and improve its signal to quantization noise ratio. The transmitter architecture (Fig. 1) uses a Time-Interleaved Delta Sigma approach that achieves higher equivalent frequency for the delta-sigma modulator by parallelizing its outputs [7].

The DSM output is then up-converted to RF using a bit combiner block and a FPGA's integrated multi-gigabit serializer. Jointly these blocks perform the equivalent to a multiplication by a square wave up-converting the signal to the desired carrier frequency.

The high frequency pulsed signal is then converted into a series of optical pulses at a certain wavelength λ using an E-O converter. This conversion uses a very simple amplitude shift key modulation (ASK), in this particular case it uses on-off shift keying (OOK). By using such simple 2-level modulations, the systems becomes insensitive to the potential non-linearities of the laser-driver and diode.

B. Remote Radio Head

At the RRH, the optical signal is converted back to an electric one, reconstructing the original signal generated by the ADT.

This signal can therefore be filtered and amplified as the original signal at the ADT output.

The proposed system's RRH unit stands for its simplicity similar to the analog RF-over-fiber case using only an O-E converter, a bandpass filter to attenuate the quantization noise from the delta-sigma modulation and an RF amplifier.

For the signal amplification at least two distinct approaches can be used. The most common is to amplify the analog signal after the bandpass filter as depicted in Fig. 2. However a potentially more efficient alternative can be used with a switched class-S amplifier, directly fed by the digital signal from the O-E converter, followed by a reconstruction bandpass filter.

IV. Tests and Results

A laboratorial prototype implemented as a proof of concept for the proposed system is shown on Fig. 3. The ADT CS was implemented using a KC705 board from Xilinx with a Kintex-7 XC7K325T FPGA. The DSM equivalent sampling frequency is 920MHz (4 parallel paths at 230MHz). The RF output generated signal is centered at 920MHz and has a bit rate of 3680Gbps, this is the rate of the serializer output and therefore the digital rate of the signal in the fiber.

The E-O and O-E conversions were made using SFP transceivers, with 850nm wavelength, connected to the KC705 board, at the ADT output, and to the RRH input using a Finisar FDB-1027 development kit to recover the electric signal. A saw filter centered at 915MHz with 26MHz bandwidth was

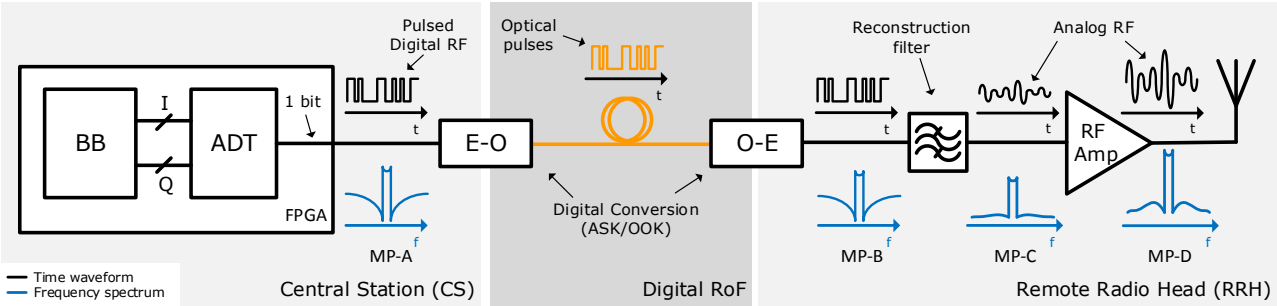


Fig. 2. Proposed RoF transmission system with waveforms and frequency spectra along the transmitter chain.

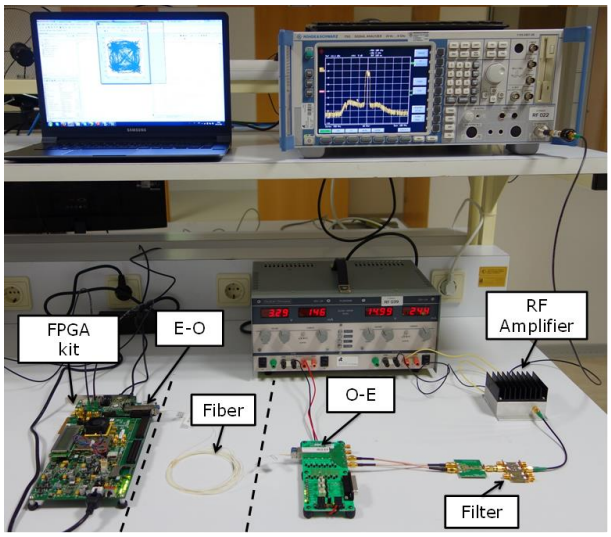


Fig. 3. ADT-based Digital RoF system.

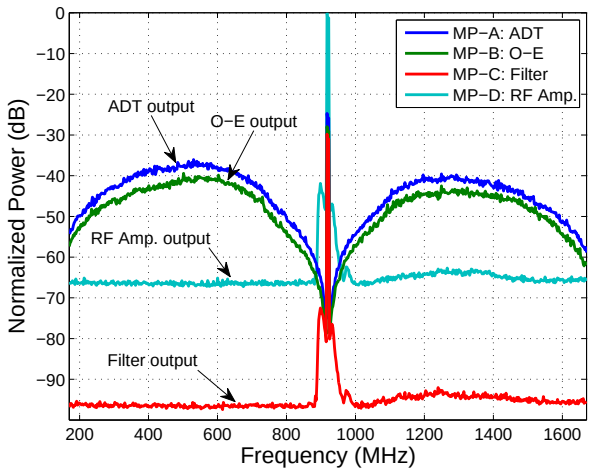


Fig. 4. Signal spectra from the VSA for the measurement points defined in Fig. 2 centered at 920MHz with a 1500MHz frequency span, 30kHz resolution bandwidth and 1kHz video bandwidth.

used to filter the quantization noise. The amplification stage uses a wideband amplifier from Mini-Circuits (ZHL-1042J).

Several baseband signals were created and pre-processed offline using MATLAB and were loaded into the FPGAs internal memory. The signal to noise ratio (SNR) along the transmitter chain was measure to evaluate the whole transmission path using a vector signal analyzer (VSA) from Rohde & Schwarz (model FSQ 8). The measure points (MP) A,B,C and D are shown in Fig. 2 and correspond to:

- MP-A - ADT output.
- MP-B - O-E conversion output.
- MP-C - Reconstruction bandpass filter output.
- MP-D - RF amplifier output.

The images presented at Fig. 4 and Fig. 5 show the spectra measured at the defined measurement points.

The quantization noise is visible in Fig. 4 for the ADT and O-E conversion outputs. This is because both of these signal are 2-level signals resulting from the DSM.

Table I presents the SNR results for several test signals transmitted using the proposed system and demodulated using the VSA. The SNR measurements along the transmission path were considered to evaluate the behavior of the system. The overall SNR degradation for this system was computed for the test signals as a figure of merit for the system's performance.

The SNR results show that the proposed system is feasible without a significant end-to-end SNR loss, in these particular tests, the losses were never greater than 2.4dB.

For the same signals an EVM analysis was conducted. The results are in table II and it is shown that for the tested signal modulations and symbol rates, the EVM along the measure points, and particularly at the systems output is relatively low and always inferior to 1.5%.

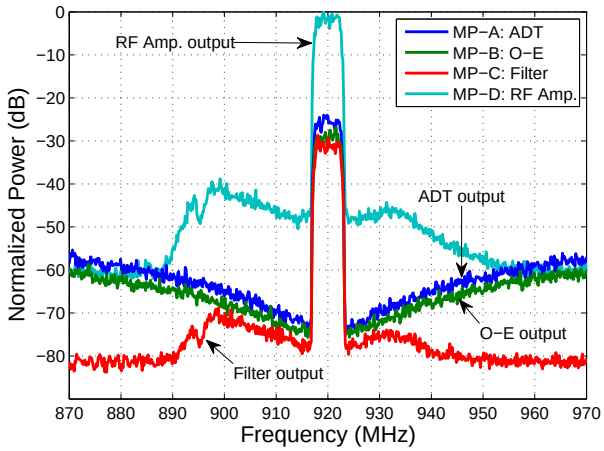


Fig. 5. Signal spectra from the VSA for the measurement points defined in Fig. 2 with a 100MHz frequency span, 100kHz resolution bandwidth and 5kHz video bandwidth.

TABLE I
COMPARATIVE SNR VALUES

Signal modulation	Symbol rate	Measure Point SNR (dB) A	B	C	D	SNR loss (dB)
QPSK	2Mbps	40.4	39.9	39.4	38.8	1.6
	5Mbps	40.1	39.3	38.3	37.7	2.4
	10Mbps	38.6	38.3	36.2	36.4	2.2
64-QAM	2Mbps	40.0	39.4	38.6	37.6	2.4
	5Mbps	39.4	38.7	37.9	37.2	2.2
	10Mbps	38.0	37.0	36.0	35.7	2.3

V. CONCLUSION

In this article, a new digital RoF transmission architecture was proposed and proven to be feasible. The use of an ADT allows the generation of a binary digital signal at RF frequencies that can be used to reconstruct the analog RF

TABLE II
COMPARATIVE EVM VALUES

Signal modulation	Symbol rate	Measure Point EVM (%) A	B	C	D
QPSK	2Mbps	0.83	0.86	0.93	1.00
	5Mbps	0.89	0.93	1.06	1.14
	10Mbps	1.01	1.06	1.37	1.34
64-QAM	2Mbps	0.85	0.92	1.01	1.12
	5Mbps	0.92	1.01	1.10	1.21
	10Mbps	1.08	1.23	1.40	1.44

signal at the RRH side with reduced hardware complexity and low cost. The digital signal over the fiber can benefit from the more favorable propagation characteristics of digital modulations for RoF systems.

ACKNOWLEDGMENT

This work was partially supported by the Portuguese Foundation for Science and Technology (FCT) under PhD scholarship ref. SFRH/BD/91533/2012 and by the Instituto de Telecomunicações under project CReATION (ref. EXCL/EEI-TEL/0067/2012.).

REFERENCES

[1] U. Gliese, S. Norskov, and T. Nielsen, "Chromatic dispersion in fiber-optic microwave and millimeter-wave links," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 44, no. 10, pp. 1716–1724, 1996.

[2] D. Novak, A. Nirmalathas, C. Lim, C. Marra, and R. Waterhouse, "Fibre-radio: challenges and possible solutions," in *Microwave Photonics, 2003. MWP 2003 Proceedings. International Topical Meeting on*, 2003, pp. 49–54.

[3] Y. Yang, *Investigation of Digitized RF Transport Over Fiber*. University of Melbourne, Department of Electrical and Electronic Engineering, 2011.

[4] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital generation of rf signals for wireless communications with band-pass delta-sigma modulation," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, vol. 3, 2001, pp. 2127–2130.

[5] M. Helaoui, S. Hatami, R. Negra, and F. Ghannouchi, "A novel architecture of delta-sigma modulator enabling all-digital multiband multistandard RF transmitters design," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 11, pp. 1129–1133, 2008.

[6] N. Silva, A. Oliveira, and N. Carvalho, "Evaluation of pulse modulators for all-digital agile transmitters," in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, 2012, pp. 1–3.

[7] M. M. Ebrahimi, M. Helaoui, and F. Ghannouchi, "Time-interleaved delta-sigma modulator for wideband digital GHz transmitter design and SDR applications," *Progress In Electromagnetics Research B*, vol. 34, pp. 263–281, 2011.

[8] S. Hatami, M. Helaoui, F. Ghannouchi, and M. Pedram, "Single-bit pseudoparallel processing low-oversampling delta–sigma modulator suitable for SDR wireless transmitters," pp. 1–1, 2013.

[9] N. Silva, A. Oliveira, U. Gustavsson, and N. Carvalho, "A novel all-digital multichannel multimode RF transmitter using delta-sigma modulation," *Microwave and Wireless Components Letters, IEEE*, vol. 22, no. 3, pp. 156–158, 2012.

Appendix B

Agile All-Digital RF Transceiver Implemented in FPGA

R. F. Cordeiro, André Prata, Arnaldo S. R. Oliveira, J. M. N. Vieira, and Nuno Borges Carvalho

in ***IEEE Transactions on Microwave Theory and Techniques (Volume: 65, Issue: 11, Nov. 2017)***

DOI: 10.1109/TMTT.2017.2689739

Agile All-Digital RF Transceiver Implemented in FPGA

R. F. Cordeiro, *Student Member, IEEE*, André Prata, *Student Member, IEEE*, Arnaldo S. R. Oliveira, *Member, IEEE*, J. M. N. Vieira, and Nuno Borges Carvalho, *Fellow, IEEE*

***Abstract*—This paper presents a new all-digital transceiver architecture fully integrated into a single field-programmable gate array (FPGA) chip. Both the radio-frequency (RF) receiver and the transmitter were entirely implemented using a digital datapath from the baseband up the RF stage without the use of conventional analog-to-digital converter (ADC), digital-to-analog converter (DAC) or analog mixer.**

The transmitter chain uses delta-sigma modulation and digital up-conversion to produce a two level RF output signal. The receiver uses a high-speed comparator and pulse-width modulation to convert the RF signal into a single bit data stream which is digitally filtered and then down-converted. Both the transmitter and the receiver are agile with flexible carrier frequency, bandwidth and modulation capabilities.

The transceiver error vector magnitude (EVM) and signal-to-noise ratio (SNR) figures-of-merit were analyzed in a point to point transmission to evaluate the transmitter's performance. The results show the feasibility of this approach as a more flexible alternative to common radio architectures.

***Index Terms*—Software Defined Radio (SDR), All-Digital Transceivers, Delta-Sigma Modulation (DSM), Pulse-Width Modulation (PWM).**

I. Introduction

In the last two decades mobile wireless communications have witnessed a phenomenal growth in terms of users, mobile terminals and throughput requirements to drive multimedia and video services. This has led to successive generations of mobile cellular standards from the highly successful 2G networks (GSM), going through the 3G (HSPA), up the current 4G (LTE). During the next decade this trend will continue, due to the proliferation of personal communication devices and the Internet of Things (IoT) phenomena. This will spread Machine-to-Machine (M2M) communications by embracing billions of constantly connected devices and seeking the integration of different standards to provide ubiquitous high-rate and low-latency experience [1].

Therefore, 5G must be capable to efficiently answer the new communication challenges and, at the same time, act as an integrator over the previous standards. A number of new ideas and concepts are being suggested and evaluated by the industry and academia for 5G support technologies such as Massive MIMO, exploitation of higher radio-frequency (RF) bands (such as millimeter wave range) and Centralized Radio Access Networks (C-RAN) for highly digital radio access networks [1], [2]. Nonetheless, the increasing use of new wireless standards using different frequencies, diverse coding and modulation schemes and targeting various applications is already taking place. The need for cooperation between access-points and devices in the network using different heterogeneous technologies will be essential to support the required flexibility and spectral efficiency for 5G networks.

Ultimately, 5G and all networks beyond will be extremely dense, flexible and heterogeneous, which introduces many new challenges for network modeling, analysis, design and optimization. The core network will also have to reach unprecedented levels of flexibility. Spectrum regulation will need to be rethought and energy and cost efficiencies will become even more critical [2]. Furthermore, there will be an increasing trend to digitalization motivated by the flexibility and high performance allowed by the cognitive radio (CR) and software defined radio (SDR) approaches, where mixed-signal and all digital systems will have a rising importance in the design of radio and telecommunication systems. The all-digital transceivers will be the focus of this paper due to their improved flexibility permitted by the completly digital signal processing up to the RF stage.

In this work a new all-digital RF transceiver architecture, fully integrated into a single field-programmable gate array (FPGA) chip, will be presented and evaluated. The entire signal processing from the baseband up to the RF stage for the transmitter, and the opposite for the receiver, is completely performed in the digital domain. In this sense the proposed system does not use conventional analog-to-digital (ADC) and digital-to-analog (DAC) converters neither any kind of analog mixing device, enabling the creation of a much more compact and integrated radio. To best of the authors knowledge, this is the first time a fully integrated all-digital RF transceiver architecture is presented.

The remainder of this paper is divided as follows. In Section II the state-of-the-art of SDR transceiver architectures is presented. Section III presents the proposed transmitter and receiver architectures and their hardware implementation. To validate the proposed system, measurement results of Error Vector Magnitude (EVM) and Signal-to-Noise Ratio (SNR) will be presented and discussed in Section IV. Finally, some conclusions are drawn in Section V.

This work was supported by the FCT - Fundação para a Ciência e a Tecnologia under Project EXCL/EEI-TEL/0067/2012: Cognitive Radio Transceiver Design for Energy Efficient Data Transmission (CReATION). The work of R. F. Cordeiro was supported by FCT under Ph.D. Grant SFRH/BD/91533/2012. The work of A. Prata was supported by FCT under Ph.D. Grant SFRH/BD/92746/2013. The authors are with the Departamento de Electrónica, Telecomunicações e Informática, Instituto de Telecomunicações, Universidade de Aveiro, 3810-193 Aveiro, Portugal (e-mail: ruifiel@ua.pt; andre.prata@ua.pt; arnaldo.oliveira@ua.pt; jnvieira@ua.pt; nbcarvalho@ua.pt).

II. State of the art

SDR transceiver architectures will be fundamental in future radio communication systems in order to endow the physical layer with high flexibility, spectral and energy efficiency [3]. Therefore this section addresses the state-of the art on SDR transceivers focusing on all-digital platforms, due to the enormous advantages that such architectures can provide.

A. Transmitters

All-digital transmitter architectures typically use pulsed-modulation approaches to allow the full digitalization of the radio system, which poses an important step towards the complete software description of RF signals proposed in SDR.

Recent advances involving pulsed RF transmitters include the development of novel all-digital transmitter architectures where the radio datapath is digital from the baseband up to the RF stage. These transmitters perform a conversion from an m-bit digital representation to a 2-level signal, usually done by means of delta-sigma modulation (DSM) or pulse-width modulation (PWM) schemes. State-of-the-art pulsed transmitters can use amplitude and phase modulation of the RF carrier using PWM [4]–[7], band-pass DSM [8], [9] or low-pass DSM with digital up-conversion [10]–[14]. To improve signal quality, many works have focused into the increase of the signal over-sampling ratio (OSR). Most of pulsed-RF transmitters achieve higher OSR by optimizing the digital design for a higher frequency [15]. However, digital switching logic has frequency limits that bound the achievable OSR to a maximum value depending on the used technology. An alternative approach for higher OSR is to use parallelized processing followed by dedicated high-speed logic such as a multiplexer or serializer [16]–[18]. This eases the design of higher bandwidth transmitters working at reduced logic frequencies and the competitive integration with lower-cost technologies.

The functionality and flexibility of the transmitter is also of great importance since the purpose of a digitally controlled transmitter is to easily adapt the radio to its environment and user needs. Carrier frequency flexibility means that a single digital chip can be a wideband radio with multiple channels and standards. In this paper we present a transmitter capable of covering signal bands from 400 MHz to 2.4 GHz.

B. Receivers

Traditional RF receivers are commonly based on homodyne or heterodyne architectures, usually performing analog down-conversion up to the baseband or up to an IF stage, where the signal is sampled by an I/Q analog-to-digital converter (ADC) or by an IF ADC. These architectures present a high dependence on analog components imposing problems such as limited bandwidth, due to the analog components frequency response. Alternatively the IF ADC can be replaced by an RF ADC, allowing sampling the spectrum directly at the RF stage and therefore performing the entire signal processing in the digital domain, as it was envisioned as the ideal SDR receiver [3], Fig 1. These architectures present high flexibility

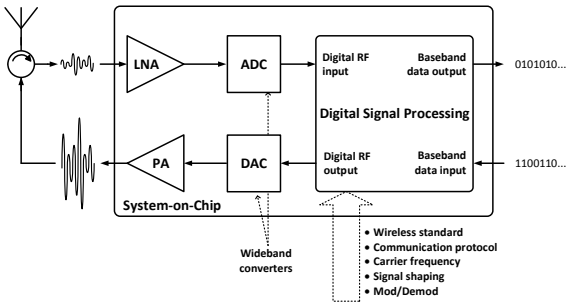


Fig. 1: Ideal SDR transceiver architecture.

and high bandwidth and allow taking profit of the high efficient and accurate digital signal processing techniques, avoiding the analog impairments and mismatches [19].

Modern SDR receiver performance and flexibility is susceptible to the ADC's bandwidth as well as its linearity. Current commercial RF ADCs have reached a few GHz of sampling frequency and analog input bandwidth. However, they are expensive and have a significant energy consumption, which may reduce the overall systems efficiency.

Recently new possibilities to build RF ADCs based on pulsed-modulation converters were proposed, such as; DSM [20], pulse frequency modulation (PFM) [21], [22] or PWM [23], [24]. All these types of ADCs are single-bit ADCs, i.e., all deal with a digital pulsed representation of the analog signal. The DSM ADCs are often used in audio applications, due to their high resolution that they provide [19]. Several research works presented RF DSM ADCs, such as [20] where a high resolution ADC was built, however with low analog input bandwidth. A PFM ADC is based on a voltage controlled oscillator (VCO) to create a PFM representation of the input analog signal [21]. These types of ADCs present high undesirable nonlinear behavior related with the VCO, that may be improved using techniques as the ones presented in [22]. A PWM ADC is made of a single comparator, whose inputs are the analog signal and a given reference wave (usually a triangular wave), generating a PWM representation of the analog signal [25]. They are commonly used in low-frequency applications [25], nevertheless, they are also being applied in the RF world, as presented in [23], [24]. In [23] high speed comparators to generate the PWM representation are used and in [24] a single FPGA-chip is used to build the ADC and the remaining receiver, presenting a flexible and promising architecture. However, none of these works present an exact way to obtain the best reference waveform to optimize the receiver figures-of-merit. In this work, the authors present an algorithm that optimizes the frequency of a reference triangular wave in order improve the receiver performance.

III. Proposed architecture

This section presents and explains the proposed architecture for the all-digital transceiver. For the sake of clarity, the transmitter and receiver architectures will be presented separately, but implemented and tested together.

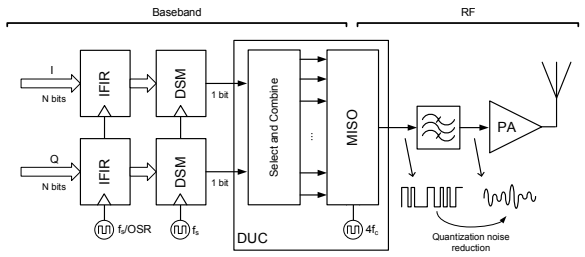


Fig. 2: DSM-based ADT architecture. Baseband delta-sigma clock frequency is f_s while the digital up-conversion works at a 4 times the carrier frequency f_c.

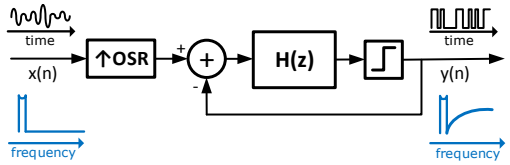


Fig. 3: Delta-sigma modulation loop with loop filter $H(z)$.

A. Proposed Transmitter Architecture

This sub-section presents and explains the proposed architecture for the all-digital transmitter. The digital transmitter architecture used is shown in Fig. 2. The baseband complex signal is divided into two components, the in-phase (I) and quadrature (Q) signals. It should be noted that for the purpose of this paper no particular protocol or standard is considered, i.e., the digital baseband processing can be performed as in conventional transmitter architectures, for any particular standard use.

The proposed architecture uses DSM with a two-level output. The delta-sigma modulator is a signal shaping stage of the modulator which converts the I and Q signals with N bits resolution, into single bit representation signals, at the trade off a higher resolution in time. The signal is initially up-sampled to improve the OSR using a digital interpolation filter. The filter inside the delta-sigma loop shapes the quantization noise inserted by the 1-bit quantizer at the output by feeding back the error signal. The output of the modulator is a binary signal with added out-of-band quantization noise.

The DSM loop filter will define the transmitted signal resolution and consequent signal quality in terms of SNR. Higher order DSM allows higher noise rejection for the signals band at the same OSR. However, the higher in-band noise rejection increases the noise in the adjacent bands. In [26] an extensive study was made on the influence of the DSM's order on the signal to quantization noise ratio (SQNR). An approximation of the SQNR value given by the equation (1) and equivalent signal resolution in number of bits, is shown in Fig. 4 for a 1^{st}, 2^{nd} and 3^{rd} order DSMs. In the presented equation OSR is the over-sampling ratio and L is the DSM order. Higher DSM orders require lower values of OSR to achieve the same performance when compared to lower DSM orders and therefore lower sampling frequencies could be used. Hence, it should be desirable to use a higher order modulator

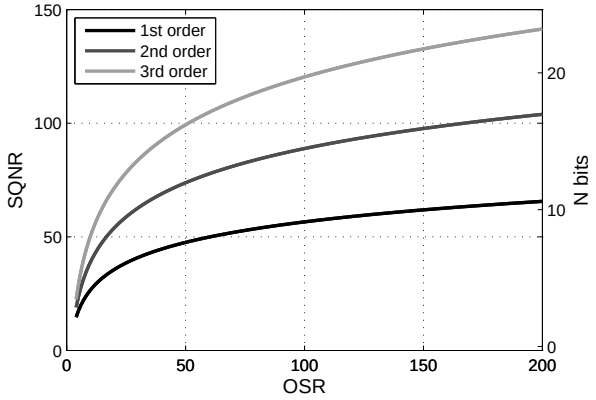


Fig. 4: Signal to quantization noise ratio and effective number of bits for two-level delta-sigma modulation with different orders of modulation.

to improve the transmitter SNR.

$$SQNR_{dB} = 3.01 \times log_2(OSR) \times (2L+1) - 9.36L - 2.76 \quad (1)$$

In RF applications this becomes a problem since additional out-of-band noise reduces the transmitter efficiency. The relationship between in-band power and total transmitted power is the modulator coding efficiency (CE). It can be defined as the signal channels power P_s over the total transmitted power P_t [27], as it is shown in (2).

$$CE = \frac{P_s}{P_t} \quad (2)$$

The CE of DSM varies subject to the nature of the input signal, particularly its peak-to-average power ratio (PAPR), and is typically lower than 30%. However, higher orders of modulation will decrease even further the CE of the transmitter. Fig. 5 shows a representative graph of CE measurements for an all-digital transmitter with both 1st and 2nd order modulators for different PAPR signals. It is perceptible that for common wireless communication standards with PAPR varying from 3 dB up to 12 dB the CE is considerably low, especially for higher order modulators.

Since higher order DSM limits the transmitters CE, increasing the modulators order is not a satisfactory solution to improve the signal SNR. A possible alternative is to increase the OSR of the modulator by increasing its operation speed. However, a key limitation in digital DSM is the typically low bandwidth of the signal modulator due to frequency restrictions for the digital logic clock because of the loop-filter propagation delays. To overcome this, it was used a time-interleaved DSM to improve the maximum modulator sampling frequency. This parallel DSM architecture used was initially presented in [18] to improve the modulator OSR by allowing the processing of multiple parallel delta-sigma samples in a single clock period.

The DSM used is a first order modulator because it has a higher CE for the transmitted signal. Additionally, a simpler loop-filter can be implemented with fewer logic elements. Less

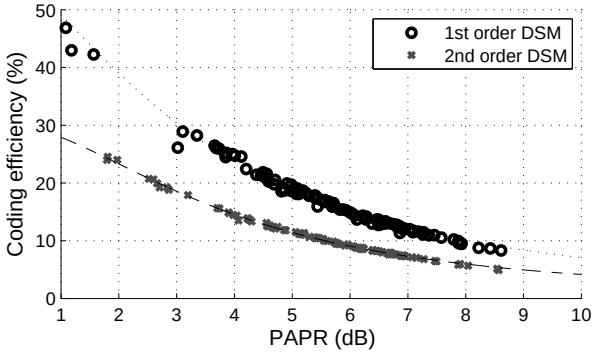


Fig. 5: Coding efficiency variation with input signal for 1^{st} and 2^{nd} order DSM. The measured PAPR and CE values are from random phase and amplitude multi-sine signals.

logic gates allow for a smaller logic delay path and therefore a higher sampling rate and signal bandwidth.

The digital up-conversion (DUC) is achieved by time-interleaving the delta-sigma modulated 2-level samples (I and Q) in time with their inverted versions. The resulting wave, w in (3), is equivalent to the multiplication of the I and Q baseband components with two square waves with a 90 degree phase shift between them. To do this, a parallel to series block with a switching frequency 4 times superior to the desired carrier frequency f_c can be used.

$$w = [I; Q; \overline{I}; \overline{Q}] \tag{3}$$

The resulting output signal has the baseband complex signal up converted to f_c with added quantization noise in the sidebands added by the delta sigma modulation. This noise can be filtered and the RF signal recovered.

B. Proposed Receiver Architecture

In this sub-section the receiver architecture will be presented and explained, considering a PWM-based topology, which was chosen mainly due to the high analog input bandwidth and flexibility that such topology can provide.

The generic block diagram architecture for the proposed receiver is presented in Fig. 6, where the signal $x(t)$ represents the RF signal, centered at f_c with bandwidth BW, received at the antenna after filtering and low noise variable gain amplification (LNA/VGA). The $x(t)$ signal is one of the inputs of a comparator, while the other is a reference signal $(r(t))$, of frequency f_r, which is usually a triangular wave. At the output of this comparator, there is a continuous time PWM signal $p(t)$, that contains the information of the $x(t)$ signal. The $p(t)$ signal is a natural sampling PWM representation of $x(t)$ [28], which implies that no quantization noise is added into the signal's band. Following the comparator, there is a single-bit register responsible to sample and discretize the continuous time PWM signal $p(t)$, at a sampling rate of f_s, with ($f_s > 2f_c$ and $f_s >> BW$). Thereafter the signal is available for further processing regarding digital down conversion and filtering in order to recover the baseband signals information.

The analog-to-digital conversion stage, which is the key element of this receiver, as any other converter can be separated in

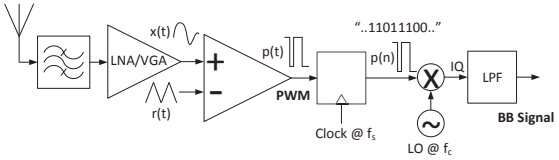


Fig. 6: PWM-based all-digital receiver architecture.

two processes; sampling and quantization, which are related with discretization in both time and amplitude respectively. The proposed way to implement the conversion (PWM) is similar to the stochastic ergodic converter (SEC) presented in [29], which was a popular idea in the nineteen-sixties to build low cost and low frequency ADCs. However, at the time, due to the lack of enabling technology, the idea was abandoned and sigma-delta converters were preferred [29]. This converter is mainly based on adding a dithering wave to an analog signal and then feeding it to a single bit quantizer. The theoretical demonstration of this converter can be developed based on statistical quantization theory, which shows that if the dithering signal presents uniform distribution, the input signal will be equally quantized, i.e., the mean of the input signal will be contained in the output quantized signal, allowing its recovering. A common selection for the dithering wave is a triangular or sawtooth wave, since both present uniform amplitude distributions [29], [30]. This dithering wave can be directly transposed for the PWM RF ADC, playing the same role as the reference signal $r(t)$, which should also present uniform amplitude distribution.

In addition to the reference signal amplitude distribution, two other important characteristics are the reference frequency and the sampling frequency of the sampler after the comparator, which define the maximum bandwidth of the signal to acquire. The latter two variables will also impose the converters resolution, since the ratio between the effective sampling frequency (f_s) and the reference signal frequency (f_r) indicates the number of PWM levels and therefore, the number of bits of the converter (4) and its signal-to-noise ratio (SNR) (5), as follows:

$$N_{bits} = log_2(N_{levels}) = log_2 \frac{f_s}{f_r} \tag{4}$$

$$SNR = 6.02N_{bits} + 1.76 \tag{5}$$

The previous relationships indicate that the higher the ratio between the sampling frequency and the reference signal, the higher will be the converter effective resolution. Therefore, we may consider that the limit for the f_s will be imposed by the maximum frequency allowed by a given technological process or by a set of requirements such as resolution or power consumptions of a certain application. Nonetheless and without loss of generality, in order to simplify the digital architecture and to provide the maximum resolution, the f_s should be fixed to the maximum achievable value and maintaining the previous assumptions $f_s > 2f_c$ and $f_s >> BW$. Thereafter, considering an analog signal occupying a given bandwidth (BW), it is

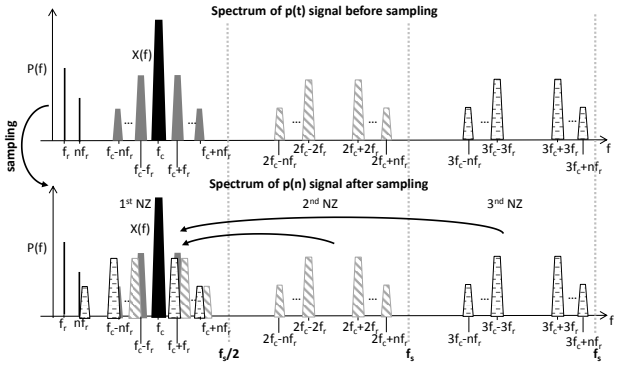


Fig. 7: Conceptual representation of the PWM signal spectrum, in the first three Nyquist zones (NZ), before and after sampling.

important to select the minimum reference signal frequency to provide the higher resolution. While a selection of a minimum reference frequency, f_r, of $2BW$ for a sawtooth waveform or of BW for a triangular waveform allows achieving the same resolution, it creates a different harmonic content in the PWM spectrum. The sawtooth wave puts the first distortion band closer to the interest band, making the triangular wave a preferable way to acquire the signal and to provide a relaxation of the filtering requirements in the digital down-convert (DDC) chain.

At the register's input, ideally, there is a perfect square wave with varying duty-cycle of infinitesimal resolution, which presents a infinite power spectrum, as shown in spectrum before sampling in Fig. 7. Then, the single-bit register running at f_s samples the continuous time $p(t)$ waveform, generating a discrete-time $p(n)$ PWM waveform. As already mentioned, the relation $f_s > 2f_c$ imposes the signal of interest $x(t)$ to be in the first Nyquist Zone (NZ). However, the sampling process causes a frequency overlap at the first NZ due to the aliasing of PWM harmonics coming from higher NZs, as shown in Fig. 7 after sampling. This aliasing is unavoidable since an anti-aliasing filter can not be included between the comparator and the register, in order to maintain a 2-level signal. The use of a binary signal allows to simplify the sampling hardware to a single bit register. Therefore, an analysis of the $p(t)$ PWM spectrum signal should be considered, in order to understand how this overlapping can be avoided in the signal's band.

The PWM modulation process (6), which is the comparison between the RF signal, $x(t)$, and the reference signal, $r(t)$, can be described by the sign function (7).

$$p(t) = sign(x(t) - r(t)) \tag{6}$$

$$sign(x(t)) = \begin{cases} -1, & \text{if } x(t) < 0 \\ +1, & \text{if } x(t) > 0 \end{cases} \tag{7}$$

In [31], a general mathematical model to approximate (6) is presented in (8), and is valid for every $x(t)$ signals:

$$p(t) = x(t) + \frac{2}{\pi} \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{1}{n} e^{jn\omega_r t} sin\left(\frac{n\pi}{2}(1 + x(t))\right) \tag{8}$$

where ω_r is the angular reference signal frequency and $x(t)$ is the RF signal that can be described as $x(t) = x_{BB}(t)sin(\omega_c t)$, where $x_{BB}(t)$ is the baseband signal's envelope modulated by a carrier centered at ω_c. Then, replacing $x(t)$ by the previous description and applying some well-known trigonometric identities (8) can be simplified into (9):

$$p(t) = x(t) + \sum_{n=1}^{+\infty} \frac{4}{n\pi} cos(n\omega_r t) sin\left(\frac{n\pi}{2} x_{BB}(t) sin(\omega_c t) + \frac{n\pi}{2}\right). \tag{9}$$

Consequently, applying the sum-to-product trigonometric identity, (9) becomes (10):

$$p(t) = x(t) + \sum_{n=1}^{+\infty} \frac{4}{n\pi} cos(n\omega_r t) sin\left[A(t)_{n\,even} + A(t)_{n\,odd}\right] \tag{10}$$

where, $A(t)_{n\,even}$ and $A(t)_{n\,odd}$ are respectively given by (11) and (12).

$$A(t)_{n\,even} = cos(\frac{n\pi}{2}) sin(\frac{n\pi}{2} x_{BB}(t) sin(\omega_c t)) \tag{11}$$

$$A(t)_{n\,odd} = sin(\frac{n\pi}{2}) cos(\frac{n\pi}{2} x_{BB}(t) sin(\omega_c t)) \tag{12}$$

To know the spectrum of the PWM signal $p(t)$, a Fourier transform must be applied on (10). However the Fourier transform of all the elements is not trivial since it implies to calculate the transform of a function in the format $sin(\beta sin(\theta))$ and $cos(\beta sin(\theta))$. It can be further simplified using the Jacobi-Anger expansion, which uses the first order kind Bessel function (13) and (14) [32]:

$$sin(\beta sin(\theta)) = 2 \sum_{k=1}^{+\infty} J_{2k-1}(\beta) sin((2k-1)\theta) \tag{13}$$

$$cos(\beta sin(\theta)) = J_0(\beta) + 2 \sum_{k=1}^{+\infty} J_{2k}(\beta) cos(2k\theta) \tag{14}$$

where, $J_k, k \geq 0$ represents the first order kind Bessel function. Therefore, by applying (13) and (14) on (11) and (12) a new approximation for $A(t)_{n\,even}$ and $A(t)_{n\,odd}$ can be achieved in the form of (15) and (16):

$$A(t)_{n\,even} = cos\left(\frac{n\pi}{2}\right) 2 \sum_{k=1}^{\infty} J_{2k-1}\left(\frac{n\pi}{2} x_{BB}(t)\right) sin((2k-1)\omega_c t) \tag{15}$$

$$A(t)_{n\,odd} = sin\left(\frac{n\pi}{2}\right) \left[J_0\left(\frac{n\pi}{2} x_{BB}(t)\right) + 2 \sum_{k=1}^{\infty} J_{2k}\left(\frac{n\pi}{2} x_{BB}(t)\right) cos(2k\omega_c t) \right] \tag{16}$$

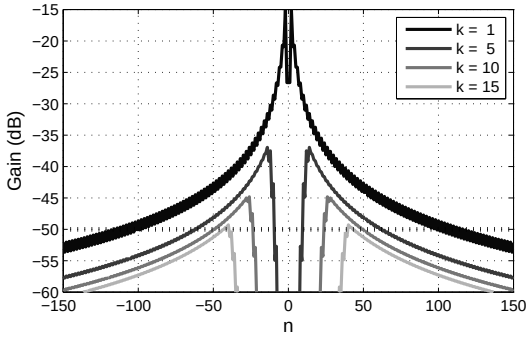


Fig. 8: Magnitude of the amplitude response of $P^*(f)$.

Considering now (10) with the new expressions for $A(t)_{n\,even}$ and $A(t)_{n\,odd}$ it is possible to reach an approximation of the central frequency bins where the PWM distortion will fall. In fact it is not relevant to solve the entire Fourier transform of (10), since the idea is just to choose a reference frequency $r(t)$ to avoid the distortion overlap in the first NZ and consequently optimize the receiver SNR. Thus, (17) and (18) present the center frequencies of the PWM distortion bands:

$$P^*_{n\,even}(f) = \sum_{n=1}^{\infty} \frac{2}{n\pi}\delta(f - nf_r) * \left[\sum_{k=1}^{\infty} |J_{2k-1}(B(t))|_{max}\delta(f - (2k-1)f_c)\right] \tag{17}$$

$$P^*_{n\,odd}(f) = \sum_{n=1}^{\infty} \frac{2}{n\pi}\delta(f - nf_r) * \left[|J_0(B(t))|_{max} + \sum_{k=1}^{\infty} |J_{2k}(B(t))|_{max}\delta(f - 2kf_c)\right] \tag{18}$$

where, $P^*_n(f)$ are the central bins of the positive part of the $p(t)$ spectrum, $\delta(f)$ is the Dirac delta function, $|J_k(B(t))|_{max}$ with, $B(t) = \frac{n\pi}{2}x_{BB}(t)$, is the maximum absolute value of the amplitude response for a given distortion bin.

At this point, it is important to note that (17) and (18) give the information of the central frequencies of each PWM harmonic, as shown in spectrum before sampling in Fig. 7. Thus, considering a certain level of required or imposed SNR, it should be guaranteed that the PWM harmonics do not fall over the interest band in the first NZ. Therefore, the folding frequency bins placement in the first NZ should be calculated using (19):

$$f_{fold} = \left| f_c - \left\lfloor \frac{f_c}{f_s} \right\rceil f_s \right| \tag{19}$$

where f_{fold} is the folding frequency in the first NZ, f_c is the carrier frequency, f_s is the sampling frequency, $\lfloor ... \rceil$ is the rounding operation towards nearest integer and $|...|$ is the absolute value. Additionally, the amplitude response of $|J_k(B(t))|_{max}$ must be analyzed, up to an n and k value that guarantee the calculation of all distortion bands above the SNR limit.

The maximum k and n values from (17) and (18) can be extrapolated from an imposed limit of the amplitude response of $P^*_n(f)$. In Fig. 8, a limit of -50 dB is considered for the amplitude gain which immediately imposes a maximum value of 15 for the maximum carrier frequency harmonic k.

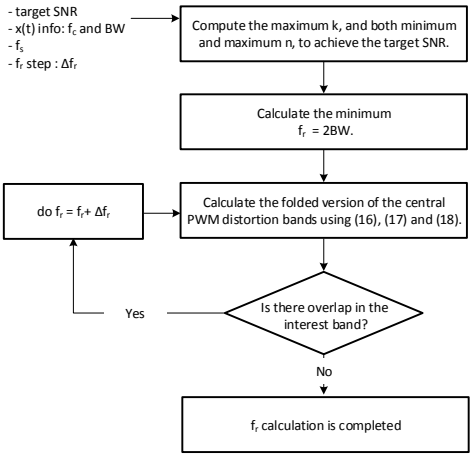


Fig. 9: Flowchart diagram of the proposed algorithm to find the best reference frequency to improve the SNR.

Then, after obtaining the n, k that will be considered, for the calculation of the folding spectrum version using (19), this information must be used in an algorithm to obtain the best reference frequency (Fig. 9).

The proposed algorithm starts with a set of inputs which are the target SNR, the carrier frequency, f_c and the bandwidth, BW, of the signal $x(t)$, the sampling frequency, f_s, and a step for the reference frequency (Δf_r). It should be noted that BW here considered is the channel bandwidth instead of the signal bandwidth in order to allow for a small frequency margin for filtering, usually a small percentage of the signal bandwidth, for example 30% is considered reasonable.

Regarding the algorithm, it starts by computing the k and both minimum and maximum n to guarantee the target SNR, as previously described. Then, it calculates the minimum reference frequency, which is given by $2BW$. Following, there is the calculation of the folded version of the spectrum and the verification of the presence of any overlap that may jeopardize the SNR. If there are no overlaps, the reference frequency calculation finishes, otherwise a new reference frequency is tested, given by the previous frequency plus a given step (Δf_r). This step should be small enough to allow a small loss of resolution and should have an irrational relation to f_s in order to avoid successive occurrences of overlaps from various NZs. Therefore, this step was fixed to be a sub-multiple of π. An alternative should also be to vary the f_s, however that would increase the complexity of the DDC chain due to the need of irrational decimation filters. This procedure will allow to obtain a f_r that will generate a sampled signal which obeys to the target SNR limit.

In order to exemplify the proposed algorithm, Fig. 10 presents the simulation results of the proposed receiver considering an ideal comparator. The simulation was performed considering a carrier frequency of 1650 MHz and a 16-QAM signal with 5 MHz of symbol rate. The minimum reference is 14 MHz and the optimized reference after computing the proposed algorithm is 30.9 MHz. As it is possible to verify in Fig. 10 the signal's spectrum using the minimum reference

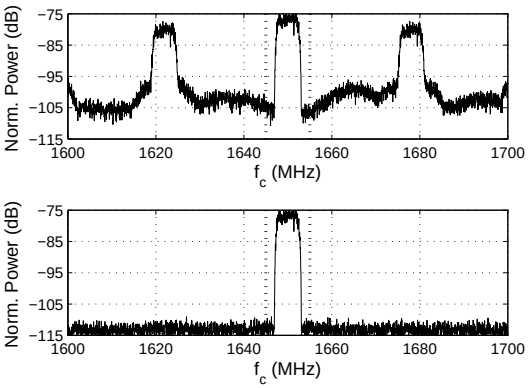


Fig. 10: Receiver simulation results with and without best reference calculation, top and bottom plot respectively.

frequency presents a degraded SNR when comparing with the spectrum with the best reference. In fact, after computing the EVM of both situations is was verified an SNR improvement of 9 dB, which validates the proposed technique.

Finally, during laboratorial measurements new spectral bins, different from the ones predicted by (17) and (18) were detected. In fact these new distortion bins are associated to a DC offset error α at the input of the comparator, which can be modeled by (8) considering that $x(t)$ is now given by $x(t) + \alpha$. Therefore, applying the mathematical steps presented previously, a new expressions for $P_n^*(f)$ considering the mismatch , can be reached (20) and (21).

C. FPGA Implementation

A proof of concept prototype was developed using the proposed transmitter and receiver architectures presented in the previous sub-sections. The hardware design was implemented in a KC705 board from Xilinx with a Kintex-7 XC7K325T FPGA. FPGA design allows for a completely integrated approach of both the all-digital transmitter and receiver due to the high logic capacity of modern FPGAs. Also, their inherent re-configurability allows for a fast adjustment of the radio hardware to different purpose scenarios, which strongly falls within the concept of SDR. The FPGA-based transceiver architecture, shown in Fig. 11, can be separated into its two main functional blocks, the transmitter (ADT) and the receiver (ADR). The implemented system has an Ethernet connection to a local PC running a Matlab routine responsible for the baseband signal generation and demodulation, transceiver carrier control and reference signal frequency calculation. The transmitter interpolation filter defines the datapath sampling rate. Higher sampling frequencies will improve the signal OSR in the DSM and therefore the transmitted signal quality. However the sampling rate must be adjusted depending on the carrier frequency. For carriers between 400 MHz and 1 GHz the sampling frequency is equal to f_c, and the RF waveform is the following parallel word w_{low} on (22). The use of repeated samples in (22) reduces the carrier frequency to half while maintaining the transceiver clock within the FPGA PLL frequency lock range. This allows to use this ADTx architecture for carrier frequencies between 400 MHz and 2.4 GHz.

$$w_{low} = [I_0; I_0; Q_0; Q_0; \overline{I_1}; \overline{I_1}; \overline{Q_1}; \overline{Q_1}; I_2; I_2; Q_2; Q_2; \overline{I_3}; \overline{I_3}; \overline{Q_3}; \overline{Q_3}] \tag{22}$$

The input IQ signal is up-sampled to an equivalent sampling frequency of $f_s = f_c$ using a polyphase interpolation filter with four parallel paths. This enforces a digital hardware clock frequency of $f_c/4$ (between 100 MHz and 250 MHz depending on f_c) for the interpolation filter, DSM and select and combine logic. For carriers above 1 GHz and up to 2.4 GHz the sampling frequency is half of f_c and the RF waveform is given by the word w_{high} as in (23)

$$w_{high} = [I_0; Q_0; \overline{I_0}; \overline{Q_0}; I_1; Q_1; \overline{I_1}; \overline{Q_1}; I_2; Q_2; \overline{I_2}; \overline{Q_2}; I_3; Q_3; \overline{I_3}; \overline{Q_3}] \tag{23}$$

In this case the equivalent sampling rate varies between 500 MHz and 1200 MHz (four parallel paths), and the logic clock will be between 150 MHz and 300 MHz depending on f_c. The DSM stage is built with two parallel modulators, one for each of the I and Q datapath, with polyphase implementation of a first order modulator with four parallel paths. The DSM hardware runs with the same clock as the interpolation filter, being able to process up to 1200 Msps. The output will be a parallel word of 4 bits for each modulator correspondent to 4 consecutive time samples. The up-conversion to the carrier frequency is done by combining the DSM outputs accordingly to a specific order as stated in equation (20) or (21) subject to the carrier frequency. The word w is then serialized accordingly to the specified order. The serialization of the word is using an integrated high speed transceiver capable of data-rates up to 10 Gbps. The transceiver's clock frequency will be either $4f_c$ or $8f_c$ depending on whether the word at the input is w_{low} or w_{high}. At the output of the serializer the two-level signal will be centered in f_c surround by quantization noise from the DSM in the sidebands. To remove the quantization noise, an output filter at the target frequency band can be used.

Similarly to the RF output signal, the proposed transceiver also uses a binary output to produce the reference waveform for the receiver. In this case, a baseband PWM is used to generate a triangular wave at the specified reference frequency, varying between 4 MHz and 30 MHz. The signal is filtered with a low-pass filter to recover the required waveform by removing the PWM quantization noise. The reference signal is compared with the input RF signal using the FPGA

$$P^*_{n\,even}(f) = \sum_{n=1}^{\infty} \frac{n\pi}{2}\delta(f - nf_r) * \left[|sin(\frac{n\pi}{2}\alpha)||J_0(B(t))|_{max} + |cos(\frac{n\pi}{2}\alpha)| \sum_{k=1}^{\infty} |J_{2k-1}(B(t))|_{max}\delta(f - (2k-1)f_c) + |sin(\frac{n\pi}{2}\alpha)| \sum_{k=1}^{\infty} |J_{2k}(B(t))|_{max}\delta(f - (2k)f_c) \right] \tag{20}$$

$$P^*_{n\,odd}(f) = \sum_{n=1}^{\infty} \frac{n\pi}{2}\delta(f - nf_r) * \left[|cos(\frac{n\pi}{2}\alpha)||J_0(B(t))|_{max} + |cos(\frac{n\pi}{2}\alpha)| \sum_{k=1}^{\infty} |J_{2k}(B(t))|_{max}\delta(f - 2kf_c) - |sin(\frac{n\pi}{2}\alpha)| \sum_{k=1}^{\infty} |J_{2k-1}(B(t))|_{max}\delta(f - (2k-1)f_c) \right] \tag{21}$$

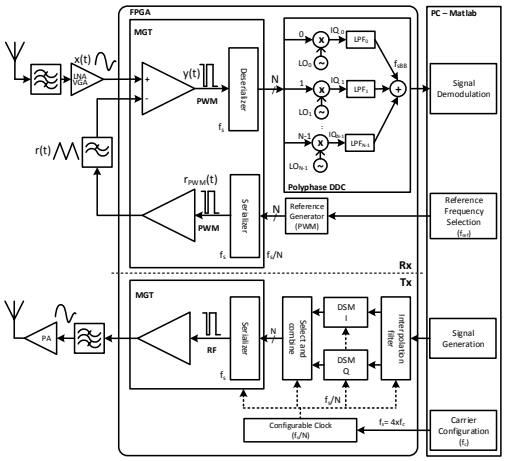


Fig. 11: Block diagram representation of the proposed FPGA-based all-digital transceiver architecture.

high speed differential input buffers as a comparator. This comparator is followed by a register working at 10 GHz of sampling frequency, generating a digital bitstream that will be deserialized by a factor of N as indicated in Fig . 11. Therefore, the sampled PWM waveform arrives at the remaining FPGA logic at f_s/N, with N=64. Then the RF data has to be down-converted to baseband, filtered and decimated. The down-conversion and filtering are performed using a polyphase digital direct synthesizer (DDS) and a polyphase filter, in this case with N=64 parallel branches. After the DDC the signal is transferred to the local PC via an Ethernet connection, where the baseband data is demodulated and analyzed for its EVM.

IV. Measurement Results

The transceiver performance was measured in terms of signal quality for both the transmitted and received signals. The figure of merit used to evaluate the signal quality is the EVM using two different signals 16-QAM and 64-QAM, with 2 MHz and 5 MHz of symbol rate, both generated using a root raised cosine filter with a roll-off of 0.22, which implies a channel bandwidth of 2.44 MHz and 6.1 MHz. The following subsections show the performance results for the isolated transmitter (Fig. 13 and 14), isolated receiver (Fig. 16) and transceiver point to point configuration.

A. Transmitter

The transmitter performance was measured in terms of SNR performing a sweep over the carrier frequencies between 400 MHz and 2.425 GHz with a step of 25 MHz. The measurement setup was assembled as depicted in Fig. 12. In Fig. 13a and 13b the EVM results are shown for 2 MHz and 5 MHz symbol rate. The results show that for the tested modulations and symbol rates, the EVM along the measured carrier frequencies is always inferior to 2.5%.

The adjacent channel power ratio (ACPR) was measured for both the 2 MHz and 5 MHz channels along the tested carrier frequencies. The measured ACPR values are shown in Fig. 14, the maximum and minimum values correspond to the best and worst ACPR scenarios considering the tested modulation of

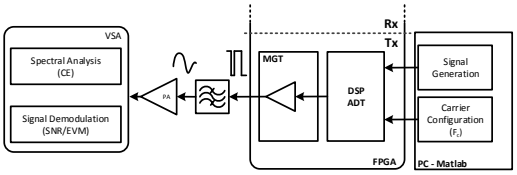
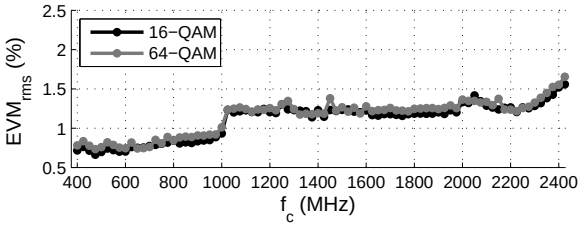
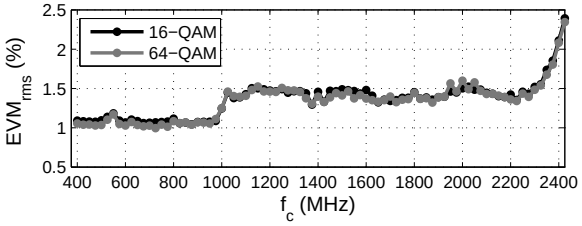


Fig. 12: Block diagram of the transmitter measurement setup.

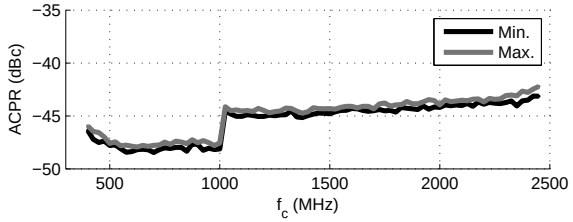


(a)

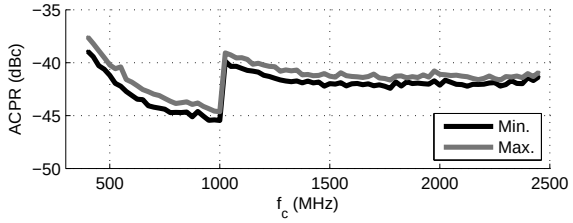


(b)

Fig. 13: Transmitter EVM using 16-QAM and 64-QAM signals. (a) 2 MHz bandwidth signal. (b) 5 MHz bandwidth signal.



(a)



(b)

Fig. 14: Transmitter ACPR measurement. (a) 2 MHz bandwidth channels. (b) 5 MHz bandwidth channels.

16-QAM and 64-QAM. Both the lower and upper channel were measured for every frequency and the worst case was considered as the ACPR value for that carrier frequency.

The CE for the transmitted signal of 16-QAM and 64-QAM was also measured and was found to vary between 15% and 22% depending on the PAPR of the signal. The EVM variation around 1 GHz occurs due to the change from w_{low} to w_{high} which presents worst jitter behavior. The EVM

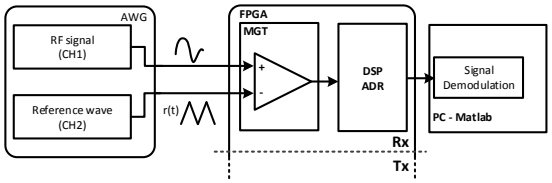
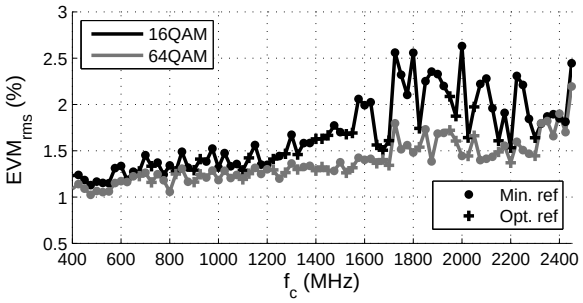
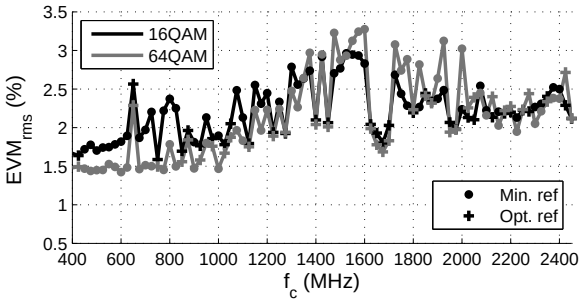


Fig. 15: Block diagram of the receiver measurement setup.



(a)



(b)

Fig. 16: Receiver EVM measurement. (a) 2 MHz symbol rate signal. (b) 5 MHz symbol rate signal.

change around 2.4 GHz however, appears because the DSM reaches its maximum clock operation and starts to present errors. Nonetheless, these results demonstrate the viability for this transmitter to be used over the measured frequencies.

B. Receiver

The receiver performance was measured performing a sweep over the carrier frequency from 400 MHz up to 2400 MHz with a step of 25 MHz considering the setup presented in the block diagram of Fig. 15. A two channel arbitrary waveform generator (AWG) (AWG7000A from Tektronix) is directly connected to the receiver and is responsible to generate both the reference and RF signal. For each carrier frequency the reference signal frequency was previously optimized, considering the algorithm described in the previous Section.

The EVM sweep results for 2 MHz and 5 MHz symbol rate signals are depicted in the Fig. 16a and Fig. 16b. In both these sweeps it is possible to see the points that were measured using the minimum reference and optimized reference. The

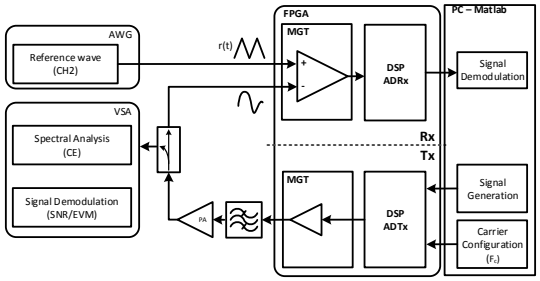


Fig. 17: Block diagram of the transceiver loop-back measurement setup.

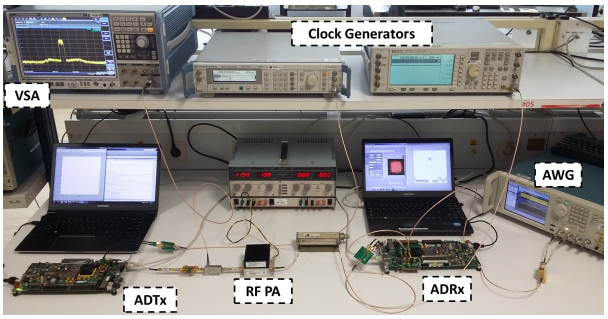


Fig. 18: Measurement setup photo.

use of the optimized reference allows for the EVM to maintain relatively constant value for the swept carrier frequencies, despite of the PWM folded harmonics. Regarding the 2 MHz signal, it was possible to reach an EVM below 2.7% for the entire bandwidth.

C. Full System Transceiver

The implemented all-digital transceiver was tested in a Tx/Rx point to point configuration for some frequency bands of interest and feasible with the proposed architecture. For this measurement, the transmitted signal is filtered by a band-pass filter, and is sent directly to the receiver that acquires the signal. Then after the DDC the signal quality is analyzed in terms of EVM. Simultaneously, the signal is also analyzed and demodulated in a VSA, in order to have a reference EVM measurement for the transmission. The measurement setup is depicted in Fig. 17. Fig. 18 presents a photo of measurement setup. Additionally, Fig. 19 shows the spectrum of the transmitted and the received signals at 1850 MHz. In the latter, it is possible to observe the PWM distortion around the carrier frequency.

The test signals are 64-QAM with 2 MHz and 5 MHz sampling rate varying the carrier frequency over the selected bands with a step of 5 MHz. Fig. 20 shows a sweep over f_c in the 900 MHz ISM band starting on 903 MHz and up to 923 MHz. Fig. 21 shows a sweep over f_c in the 1800 MHz LTE band starting on 1827 MHz and up to 1881 MHz. The presented measurements show the feasibility of the proposed transceiver architecture for some of common frequency bands.

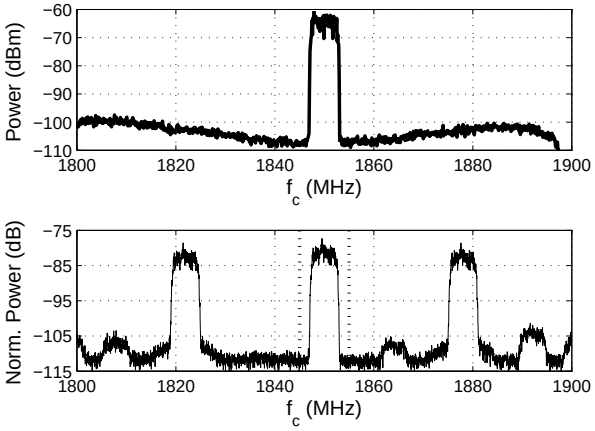


Fig. 19: Spectral capture of the transmitted signal with a VSA (top plot) and the RF received signal at the all-digital receiver (bottom plot).

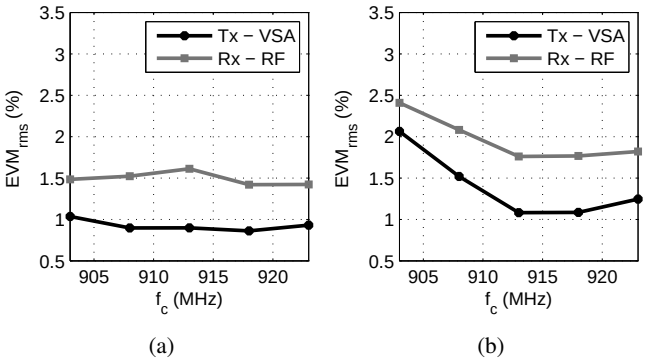


Fig. 20: Measurement over the 900 MHz ISM band. (a) Using a 2 MHz 64-QAM signal. (b) Using a 5 MHz 64-QAM.

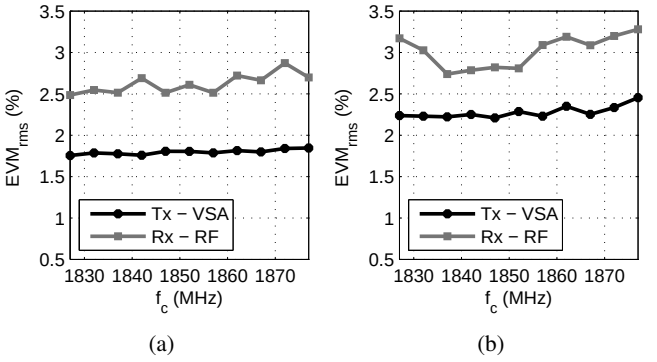


Fig. 21: Measurement over the 1800 MHz LTE band. (a) Using a 2 MHz 64-QAM signal. (b) Using a 5 MHz 64-QAM.

Finally, an overall comparison between the proposed architecture and other similar state-of-the-art transceivers must be considered. However, since this is the first time such an architecture is presented, this comparison can only be done to the transmitter and receiver independently with the respective state-of-the-art architectures.

The proposed transmitter uses polyphase architecture as presented in [18] which is in line with state-of-the-art figures of merit in terms of bandwidth, SNR and CE. However, the transmitter architecture was designed to allow for fast carrier frequency flexibility, in fact this is the first time that such a large set of carrier frequencies were tested showing the feasibility and functionality of this transmitter for those frequencies. On the receiver side, the same carrier frequencies were also tested presenting reasonable results. When comparing this system with [23], focusing on the 5 MHz signals, there were improvements in terms of SNR/EVM. Despite the fact that in [23] the PWM sampling is two times superior to the 10 GHz used in this work, the proposed technique allowed to obtain an EVM lower than 3.5%, whereas in [23] the presented EVM is about 6%. Moreover, when comparing the current work with [24], an improvement was also obtained. Both the previous improvements are due to the new technique for selecting the reference frequency.

In order to consider a receiver evaluation in terms of sensitivity and dynamic range, the LNA/VGA should be mandatorily included, which is out of the scope of this paper. However, it is possible to get an estimation of the instantaneous dynamic range transposing the EVM values into SNR by applying the formulation presented in [33]. Therefore, considering that the best and the worse obtained EVM values are respectively 1% and 3.5%, by applying the previous formulation it is possible to get an SNR of 40 dB and 30 dB. Hence, this leads to an indicative value of the receiver instantaneous dynamic range.

V. Conclusion

In this paper, it was presented for the first time a fully integrated single FPGA-based all-digital RF transceiver, which marks a breakthrough in digital RF system design. The entire signal processing from the baseband up to the RF stage for the transmitter, and the opposite for the receiver, is completely performed in the digital domain. The transmitter chain of the radio is implemented recurring to DSM modulation and the receiver based on PWM modulation, which was optimized with a non-linear analysis of its behavior.

The proposed system presents high flexibility in a bandwidth of almost 2.5 GHz, while maintaining reasonable EVM results for 2 MHz and 5 MHz symbol rate signals. The obtained results make this system highly suitable for the future radio transceivers, specifically focusing on the integration of previous standards that operated in sub 2.5 GHz bands. An FPGA was used as an implementation proof of concept, due to its faster verification and deployment capability, nevertheless an application specific integrated circuit (ASIC) could be built following the proposed architecture. However, due to the FPGA's reconfigurability capabilities it adds an increase degree of flexibility required by SDR applications.

References

[1] J. G. Andrews, S. Buzzi, W. Choi, S. V. Hanly, A. Lozano, A. C. K. Soong, and J. C. Zhang, "What will 5G Be?,"
[2] C. Mobile, "C-RAN: the road towards green RAN,."
[3] J. Mitola, "The software radio architecture," *IEEE Communications Magazine*, vol. 33, no. 5, pp. 26–38, May 1995.

[4] M. zen, C. M. Andersson, T. Eriksson, M. Acar, R. Jos, and C. Fager, "Linearization study of a highly efficient CMOS-GaN RF pulse width modulation based transmitter," in *Microwave Conference (EuMC), 2012 42nd European*, Oct 2012, pp. 136–139.

[5] B. Park and J. Jung, "A fully integrated pulsewidth modulator for class-s system," in *Advanced Communication Technology (ICACT), 2012 14th International Conference on*, Feb 2012, pp. 274–277.

[6] M. Ozen, R. Jos, C. M. Andersson, M. Acar, and C. Fager, "High-Efficiency RF pulsewidth modulation of Class-E power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 11, pp. 2931–2942, Nov 2011.

[7] M. Nielsen and T. Larsen, "A 2-GHz GaAs HBT RF pulsewidth modulator," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 2, pp. 300–304, Feb 2008.

[8] T. Johnson and S. P. Stapleton, "Comparison of bandpass sigma delta modulator coding efficiency with a periodic signal model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3763–3775, Dec 2008.

[9] ——, "RF Class-D amplification with bandpass sigma ndash;Delta modulator drive signals," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 12, pp. 2507–2520, Dec 2006.

[10] M. Helaoui, S. Hatami, R. Negra, and F. M. Ghannouchi, "A novel architecture of Delta-Sigma modulator enabling All-Digital multiband multistandard RF transmitters design," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 11, pp. 1129–1133, Nov 2008.

[11] A. Frappe, A. Flament, B. Stefanelli, A. Kaiser, and A. Cathelin, "An All-Digital RF signal generator using High-Speed Delta-Sigma modulators," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 10, pp. 2722–2732, Oct 2009.

[12] A. Frappe, B. Stefanelli, A. Flament, A. Kaiser, and A. Cathelin, "A digital delta sigma RF signal generator for mobile communication transmitters in 90nm CMOS,."

[13] A. Jerng and C. G. Sodini, "A wideband Delta-Sigma Digital-RF modulator for high data rate transmitters," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1710–1722, Aug 2007.

[14] S. Hori, A. Wentzel, M. Hayakawa, W. Heinrich, and K. Kunihiro, "A Watt-Class digital transmitter with a Voltage-Mode Class-S power amplifier and an envelope Delta-Sigma modulator for 450 MHz band," in *2012 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct 2012, pp. 1–4.

[15] J. Chen, L. Rong, F. Jonsson, and L. R. Zheng, "All-digital transmitter based on ADPLL and phase synchronized delta sigma modulator," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE*, June 2011, pp. 1–4.

[16] M. M. Ebrahimi, M. Helaoui, and F. Ghannouchi, "Time-Interleaved Delta-Sigma modulator for wideband digital GHz transmitter design and SDR applications," *Progress In Electromagnetics Research B*, vol. 34, pp. 263–281, 2011.

[17] S. Hatami, M. Helaoui, F. M. Ghannouchi, and M. Pedram, "Single-Bit pseudoparallel processing Low-Oversampling DeltaSigma modulator suitable for sdr wireless transmitters," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, no. 4, pp. 922–931, April.

[18] R. F. Cordeiro, A. S. R. Oliveira, J. Vieira, and N. V. Silva, "Gigasample Time-Interleaved Delta-Sigma modulator for FPGA-Based All-Digital transmitters," in *Digital System Design (DSD), 2014 17th Euromicro Conference on*, Aug 2014, pp. 222–227.

[19] F. Luo, *Digital Front-End in Wireless Communications and Broadcasting: Circuits and Signal Processing*. Cambridge University Press, 2011.

[20] A. Ashry and H. Aboushady, "A 4th order 3.6 GS/s RF Sigma-Delta ADC with a FoM of 1 pj/bit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 10, pp. 2606–2617, Oct 2013.

[21] L. Hernandez and E. Gutierrez, "Analytical evaluation of VCO-ADC quantization noise spectrum using pulse frequency modulation," *IEEE Signal Processing Letters*, vol. 22, no. 2, pp. 249–253, Feb 2015.

[22] H. C. Hor and L. Siek, "Review on VCO based ADC in modern deep submicron CMOS technology," in *Radio-Frequency Integration Technology (RFIT), 2012 IEEE International Symposium on*, Nov 2012, pp. 86–88.

[23] S. Maier, X. Yu, H. Heimpel, and A. Pascht, "Wideband base station receiver with analog-digital conversion based on RF pulse width modulation," in *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, June 2013, pp. 1–3.

[24] A. Prata, A. S. R. Oliveira, and N. B. Carvalho, "An agile and wideband All-Digital SDR receiver for 5G wireless communications," in *Digital System Design (DSD), 2015 Euromicro Conference on*, Aug 2015, pp. 146–151.

[25] C. Zet, C. Damian, and C. Foşalău, "New type ADC using PWM intermediary conversion," *Proceedings of 12th TC4 International Workshop on ADC Modelling and Testing, Iasi, Romania*, pp. 113–117, 2007.

[26] R. Schreier and G. C. Temes, *Understanding delta-sigma data converters*. New York, NY: Wiley, 2005.

[27] F. M. Ghannouchi, S. Hatami, P. Aflaki, M. Helaoui, and R. Negra, "Accurate power efficiency estimation of GHz wireless Delta-Sigma transmitters for different classes of switching mode power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 11, pp. 2812–2819, Nov 2010.

[28] Z. Song and D. V. Sarwate, "The frequency spectrum of pulse width modulated signals," 2003.

[29] I. Bilinskis, *Digital Alias-free Signal Processing*. Wiley, 2007.

[30] B. Widrow, I. Kollar, and M.-C. Liu, "Statistical theory of quantization," *IEEE Transactions on Instrumentation and Measurement*, vol. 45, no. 2, pp. 353–361, Apr 1996.

[31] H. d. T. Mouton, B. McGrath, D. G. Holmes, and R. H. Wilkinson, "One-Dimensional spectral analysis of complex PWM waveforms using superposition," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6762–6778, Dec 2014.

[32] F. W. Olver, D. W. Lozier, R. F. Boisvert, and C. W. Clark, *NIST Handbook of Mathematical Functions*, 1st ed. New York, NY, USA: Cambridge University Press, 2010.

[33] K. M. Gharaibeh, K. G. Gard, and M. B. Steer, "Accurate estimation of digital communication system metrics - SNR, EVM and rho; in a nonlinear amplifier environment," in *64th ARFTG Microwave Measurements Conference, Fall 2004.*, Dec 2004, pp. 41–44.

Rui Cordeiro (S12) received the M.S. degree in electronic engineering from the University of Aveiro, Potugal. Since 2012, he is working towards the Ph.D. under the doctoral program in Electrical Engineering at the same university.

He worked at the Telecommunications Institute, Aveiro where he performed researching activities under the subjects of re-configurable embedded systems, digital signal processing, wireless communications and software defined radio.

Currently he is working in Bosch Car Multimedia where he performs hardware development activities in the area of automotive wireless communications.

Andr Prata (S13) was born in Santa Comba Do, Portugal, in 1990. He received the M.Sc. degree in electronics and telecommunications engineering from the Universidade de Aveiro, Aveiro, Portugal, in 2013. He is currently working towards the Ph.D. degree in electrical engineering at the Universidade de Aveiro. His main research interests are software-defined radio, mixed-signal systems and digital signal processing. Mr. Prata was the recipient of the 2013 IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS) Undergraduate Software Defined Radio and Digital Signal Processing Student Design Competition.

Arnaldo Oliveira (M10) received the Ph.D. degree on Electrical Engineering in 2007 from the University of Aveiro, Portugal. He also holds the B.Sc. and M.Sc. degrees, both on Electronics and Telecommunications, from the same university. He is currently a researcher at Telecommunications Institute - Aveiro and since 2001 he teaches computer architecture, digital systems design, programming languages and embedded systems at the University of Aveiro, where he is now an Assistant Professor. His research interests include reconfigurable digital systems, software defined radio and next generation radio access networks. He participates in several national and European funded research projects. He is the author or co-author of more than 80 journal and international conference papers.

Jos Vieira received the BSc degree in Electrical Engineering in 1988, from University of Coimbra, Portugal and in 1993 the MSc in Systems and Automation from the same university. In 2000 we received the PhD degree in Electrical Engineering from the Aveiro University, Portugal and since then he is an assistant professor at the same University. In 2004 he founded the AES Portuguese section being its president from 2005 to 2011. In 2010 we won the Plug award from APRITEL with the 'Bio-inspired cochlear radio';. Its main research interests are: digital audio signal processing, ultrasonic location, software defined radio and all-digital radio front-ends.

Nuno Borges Carvalho (S97-M00-SM05-F15) was born in Luanda, Angola, in 1972. He received the Diploma and Doctoral degrees in electronics and telecommunications engineering from the University of Aveiro, Aveiro, Portugal, in 1995 and 2000, respectively. He is currently a Full Professor and a Senior Research Scientist with the Institute of Telecommunications, University of Aveiro and an IEEE Fellow. He coauthored Intermodulation in Microwave and Wireless Circuits (Artech House, 2003), Microwave and Wireless Measurement Techniques (Cambridge University Press, 2013) and White Space Communication Technologies (Cambridge University Press, 2014). He has been a reviewer and author of over 200 papers in magazines and conferences. He is associate editor of the IEEE Transactions on Microwave Theory and Techniques, IEEE Microwave Magazine and Cambridge Wireless Power Transfer Journal. He is the co-inventor of four patents. His main research interests include software-defined radio front-ends, wireless power transmission, nonlinear distortion analysis in microwave/wireless circuits and systems, and measurement of nonlinear phenomena. He has recently been involved in the design of dedicated radios and systems for newly emerging wireless technologies. Dr. Borges Carvalho is the co-chair of the IEEE MTT-20 Technical Committee and the past-chair of the IEEE Portuguese Section and MTT-11, he also belong to the technical commitees, MTT-11, MTT-20 and MTT-26. He is also the chair of the URSI-Portugal Metrology Group. He was the recipient of the 1995University of Aveiro and the Portuguese Engineering Association Prize for the best 1995 student at the University of Aveiro, the 1998 Student Paper Competition (Third Place) of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS), and the 2000 IEE Measurement Prize.

Appendix C

Gigasample Time-Interleaved Delta-Sigma Modulator for FPGA-based All-Digital Transmitters

Rui F. Cordeiro, Arnaldo S. R. Oliveira, José Vieira, Nelson V. Silva

in *2014 17th Euromicro Conference on Digital System Design (DSD)*

DOI: 10.1109/DSD.2014.70

Gigasample Time-Interleaved Delta-Sigma Modulator for FPGA-based All-Digital Transmitters

Rui F. Cordeiro, Arnaldo S. R. Oliveira, José Vieira, Nelson V. Silva
Departamento de Electrónica, Telecomunicações e Informática and Instituto de Telecomunicações
Universidade de Aveiro
Aveiro, Portugal
Email: ruifiel@ua.pt, arnaldo.oliveira@ua.pt, jnvieira@ua.pt, nelsonsilva@ua.pt

***Abstract*—This paper presents the architecture and implementation of an FPGA-based all digital transmitter with a baseband sampling rate of 1 GHz. Hardware complexity and operation frequency analysis are performed to find the best hardware topology to improve the transmitter performance. The used polyphase decomposition techniques for delta sigma modulators considerably improve the bandwidth and SNR figures of merit of state-of-the-art FPGA integrated RF transmitters.**

The experimental results obtained show the feasibility of this approach and the improvement in the signal modulator oversampling ratio, enabling higher bandwidth in all-digital transmitters.

***Index Terms*—All-Digital Transmitter(ADT), Time-Interleaved Delta-Sigma (TIDS), Polyphase Decomposition, Field-Programmable Gate Array (FPGA).**

I. Introduction

Software defined radio is already a key technology in modern communication systems and this trend towards to the full digitalization of the radio systems is likely to continue in the future. The complete integration of a flexible radio in a System-on-Chip (SoC) seems to be a logical step for the development and deployment of SDRs. FPGA-based all-digital transmitters (ADTs) have a set of convenient characteristics such as hardware integration, reconfigurability and flexibility that make them a viable approach for a modern and fully integrated SDR.

All digital transmitters are an alternative approach to conventional radio transmission architecture (see Fig. 1). In a general way, ADTs can be defined as radio transmitters in which the signal generation is completely digital including the radio frequency (RF) stage. Usually, ADTs have a stage where the baseband information is converted to a 2-level representation using some type of signal conversion as delta-sigma modulation (DSM) or pulse width modulation (PWM). This is followed by a high frequency digital circuity that up-converts the signal to RF frequencies. The 2-level output signal has a considerable amount of noise due to the quantization process in the signal shaping stage. However, the noise is out of the band of interest and can be posteriorly filtered at the output of the ADT system thus obtaining an analog RF signal with minimal quantization noise. Several architectures for ADTs were already presented in [1], [2], [3], [4] and [5].

Some advantages can be taken from this approach for radio transmitters. One of them is the use of reconfigurable circuits

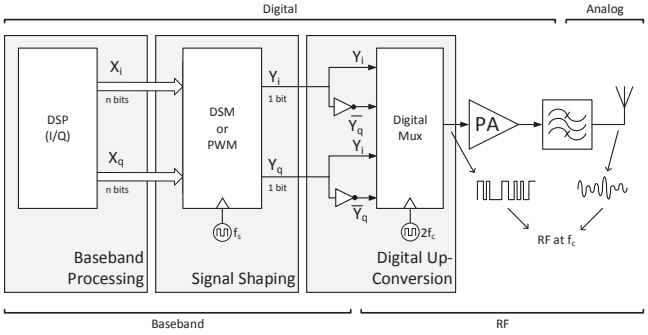


Fig. 1. All-digital transmitter architecture.

that change or adapt their physical layer to support different communication standards, different protocols and different frequency bands. Also, this type of transmitters are a natural choice to use with switched-mode power amplifiers to amplify the radio signal. In theory these amplifiers can reach 100% power efficiency leading to a very efficient transmitter.

The architecture used as a base reference for this work was originally presented in [4] and it is shown in Fig. 1. It uses two DSMs for each of the in phase (I) and in quadrature (Q) components, which are then combined at the parallel input of a high speed serializer that outputs the RF signal at a higher carrier frequency.

Besides the flexibility and potential advantages of this approach, some limitations still need to be addressed for these transmitter architectures. A key limitation is the low bandwidth (typically up to hundreds of kHz) achieved in the signal shaping stage due to the low oversampling ratio (OSR) from the DSM or PWM. This problem is directly connected to the frequency limitations for the FPGA logic that cannot easily achieve frequencies high enough for the modulators to work with reasonable bandwidths.

Low OSR in DSM not only minimizes the transmitted bandwidth but also deteriorates the SNR for the output signal. Because of these limitations, some effort to overcome the disadvantages of the low SNR factor has already been attempted. In [6] a multi-path approach together with a bandpass DSM is presented, to improve both the SNR and the transmitter band-

width. However, this represents a fairly complex architecture with the need of multiple serializer outputs. In [7] a parallel DSM is presented that performed delta-sigma modulation with a smaller OSR, but the high hardware complexity limited the hardware validation to signals with low bandwidths. The improvement of the OSR was also addressed in [8] using a parallelization technique called time-interleaved delta sigma (TIDS). Although this technique allows simultaneous delta-sigma output samples in one clock period, to the best of our knowledge no considerations about complexity scaling and the hardware frequency limitations in this type of approach were made, which limits its application in real systems.

In this paper we show several optimizations to increase the OSR on a DSM modulator. Analysis in terms of hardware scaling, complexity and critical path delay are done to maximize the hardware frequency. This results in a polyphase modulator working at an equivalent frequency of 1GHz in a fully integrated FPGA-based transmitter, representing a considerable increase in the OSR when compared to other FPGA-based ADTs.

II. Time-Interleaved Delta-Sigma

Delta-sigma modulation is used to convert a multiple bit signal to a lower resolution signal, in this case a 1-bit signal, adding the minimum quantization error possible. For a better signal to quantization noise ratio (SQNR) the DSM filtering eliminates the feedback error for the low frequencies, shaping the noise out of the signal's bandwidth.

To improve the SQNR two different approaches can be used, either the filter order is incremented to allow a better noise rejection for the signal's band or the OSR is increased. While both approaches can be used together, typically the filter order increase leads to an higher hardware complexity and consequently lower frequencies of operation and lower OSR.

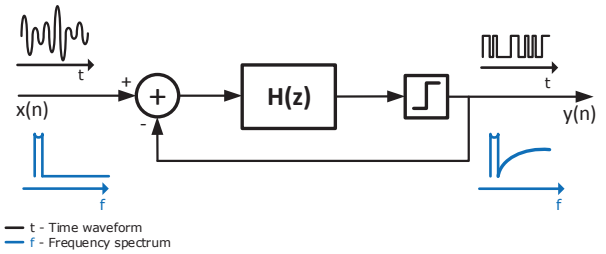


Fig. 2. Delta-sigma modulator.

Parallel delta-sigma modulation techniques have been used to achieve higher working frequency at the cost of hardware resources and more complex implementations. Using these techniques it is possible to increase the modulator OSR and consequently improve its signal to noise ratio (SNR) and signal bandwidth.

A TIDS modulator uses polyphase equivalent with M different phases producing M outputs in a single clock cycle, resulting in a M times higher equivalent frequency.

However, because of the FPGA's hardware nature, one must acknowledge that the increased logic complexity can limit severely the potential gains for TIDS approaches if inadequate architectures and topologies are employed.

The following subsections show how conventional polyphase equivalents can be found, and how they can be adapted to suit the FPGA hardware characteristics, in the case of a DSM to minimize the increased complexity impact.

A. Polyphase Decomposition

Time-Interleaved Delta-Sigma architectures take advantage in polyphase representations of the modulators internal filter $H(z)$ so that hardware speed requirements can be relaxed and higher OSR can be achieved.

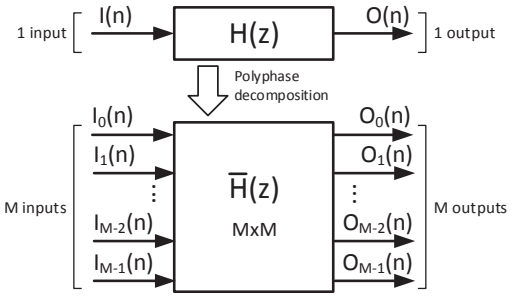


Fig. 3. Polyphase decomposition.

Given any transfer function $H(z)$ from a FIR or IIR filter it is possible to decompose it into an equivalent $M \times M$ transfer function $\overline{H}(z)$ [9] (see Fig. 3) as the one in equation (1).

$$\overline{H}(z) = \begin{bmatrix} P_0(z) & P_1(z) & \cdots & P_{M-1}(z) \\ z^{-1}P_{M-1}(z) & P_0(z) & \cdots & P_{M-2}(z) \\ z^{-1}P_{M-2}(z) & z^{-1}P_{M-1}(z) & \cdots & P_{M-3}(z) \\ \vdots & \vdots & \ddots & \vdots \\ z^{-1}P_1(z) & z^{-1}P_2(z) & \cdots & P_0(z) \end{bmatrix} \quad (1)$$

Where the $P_k(z)$ are the polyphase components of from $H(z)$ re-written as the sum in equation (2).

$$H(z) = \sum_{k=0}^{M-1} z^{-k} P_k(z^M) \quad (2)$$

The transfer function $\overline{H}(z)$ is the polyphase equivalent, with M distinct phases, for the $H(z)$ transfer function. $\overline{H}(z)$ shows all the relations between the polyphase system M inputs and M outputs. Each output phase $O_i(z)$ is now given by a sum of the input phases $I_j(z)$ as in equation 3.

$$O_i(z) = \sum_{j=0}^{M-1} \overline{H}_{ij}(z) I_j(z) \quad (3)$$

It's fairly easy to understand that $\overline{H}(z)$ can be much more complex than $H(z)$ depending on the original transfer function and the M factor.

B. Polyphase Decomposition Hardware Problems

Polyphase decomposition seems to be a interesting approach for an hardware implementation of an high speed DSM. By changing the DSM from a single-input single-output (SISO) block to a multiple-input multiple-output (MIMO) the data rate can be potentially increased by the number of used paths M. Depending on the modulator's filter function $H(z)$ this might not be as trivial as expected.

Two main reasons can limit the gains from a polyphase decomposition parallelization: the lack of delays to break the critical path and additional logic for the phases combination.

From equation 3 one can understand that each system output will now depend on a combination of all the input phases. More than that, this dependence might be on other phases at the present sample and not a delayed one. In a common MIMO system this would not represent a implementation problem, however DSM uses a feedback path. This originates a time dependence of some input phases relatively to other's outputs. If the resulting transfer function does not add a register delay then the outputs can not be compute independently. By this reason, polyphase decomposition does not create a truly parallel system because some paths are still in series with each other without a delay breaking them. Even more, pipeline techniques cannot be used inside a feedback loop because the resulting transfer function would be changed.

Other problem that decreases the gains also comes from the fact that now each output depends on all inputs. To combine all the effects from all the phases additional logic must be added. In fact, because a output phase is a sum of all the input phases logic adders are necessary. For each doubling of the number of paths M, one additional level of adders is needed.

C. Hardware Implementation and Optimization

In the DSM case, the polyphase decomposition can be applied to the internal filter $H(z)$ on the DSM loop. For a practical example, and without any loss of generality we will use the example of a first order DSM modulator with an delayed integrator as the function $H(z)$ (See Fig. 4)

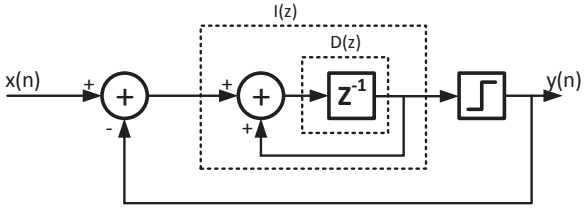


Fig. 4. DSM with delayed integrator. I(z) is the delayed integrator transfer function and D(z) is the delay transfer function.

DSM's transfer functions $H(z)$ is in equation (4).

$$H(z) = I(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{4}$$

Re-writing the integrator function, using the equations (1) and (2), the polyphase representation with $M = 4$ parallel paths is found in (5).

$$\overline{H}(z) = \begin{bmatrix} \frac{z^{-1}}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} & \frac{z^{-1}}{1-z^{-1}} \end{bmatrix} \tag{5}$$

The result is a sum of four integrators and delayed integrators for each phase. This is a more complex system, but in theory can output M parallel paths at a time, representing a M times gain in the OSR.

The four phases polyphase equivalent for an integrator was found to be a 4×4 transfer function. Regarding the hardware complexity, this solution adds additional levels of logic to the critical path decreasing the maximum operating frequency. This happens because every phase output depends on all the system input phases, so with the increasing number of phases, the number of sum levels also increases, affecting the delay in the critical path.

Consider now, as in equation 6, that the transfer function to find the polyphase equivalent is not the integrator, but only the delay $D(z)$ (Fig. 4) in the integrator. Applying the polyphase decompostion to this transfer function we obtain the result presented in equation (7).

$$H(z) = D(z) = z^{-1} \tag{6}$$

$$\overline{H}(z) = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ z^{-1} & 0 & 0 & 0 \end{bmatrix} \tag{7}$$

Each of the output phases is a function of only one input phase and no additional sums are needed. By reducing the number of logic elements needed for each output path, the data path delay will also be decreased. This greatly reduces the degree of hardware complexity in the parallel system and can be easily scaled for higher values of M.

An analysis of the maximum clock frequency was made for the hardware implementation of two DSM architectures, a first order low-pass DSM (Fig. 5) and a second order low pass DSM (Fig. 6).

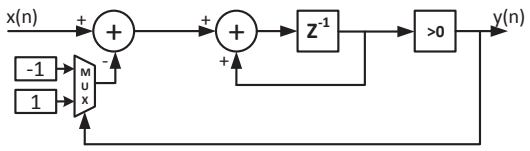


Fig. 5. First order modulator.

For each architecture, the maximum achievable frequency was found for different number of parallel paths. Also for these two architectures, both the delayed integrator decomposition and the delay decomposition were tested. The clock frequency analysis was done using Xilinx synthesis tools (ISE Design

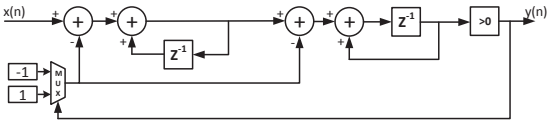


Fig. 6. Second order modulator.

Suite 14.4). For each different DSM implementation mapping, place and routing routines were run to maximize the operation frequency. For each implementation it was considered the highest path delay as the frequency limitation.

Fig. 7 shows the maximum equivalent frequency of the modulators for the specified cases.

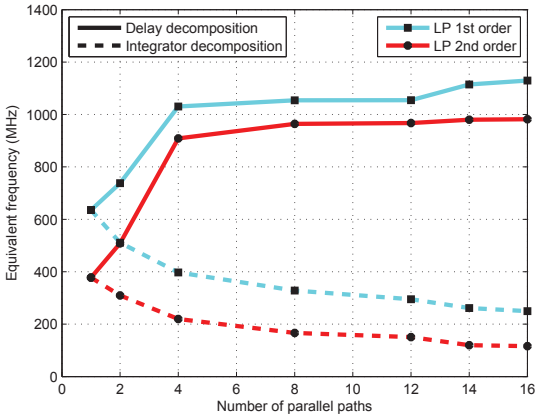


Fig. 7. Maximum equivalent frequency for the modulator depending on the number of parallel paths M.

Fig. 8 shows how the critical path logic grows for the different approaches taken.

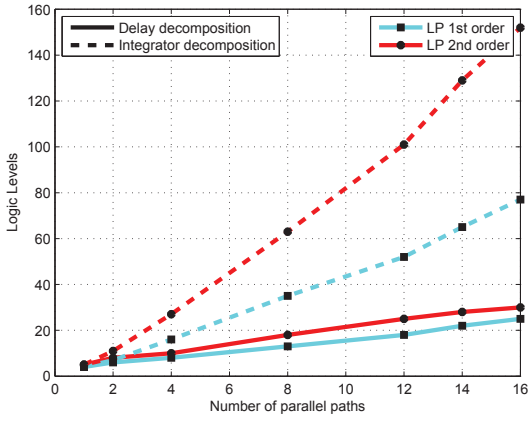


Fig. 8. Logic levels at the critical path delay depending on the number of parallel paths M.

From 7 it is possible to see that the frequency gains are far from increase linearly with M. In fact, for the integrator decomposition there is no gain in using multiple parallel paths for the DSM. This happens because with the integrator decomposition the logic levels in the critical path have additional logic for the sum operation.

By contrast, the delay decomposition does not need for additional adder logic. This leads to lower logic levels for the critical path and allows equivalent frequency gains for M parallel paths. Fig. 8 shows the difference between the two decomposition methods and how the number of logic levels is affected for both topologies. As the levels of logic increase, the critical path delay will also grow leading to a lower clock frequency.

The highest increase in frequency happens for 4 parallel paths, achieving more than 1GHz equivalent frequency for the first order DSM. This architecture with four paths was used to implement the ADT proposed in this article. The following section shows the implemented architecture for the DSM using the delay decomposition approach.

III. FPGA-BASED DSM MODULATOR ARCHITECTURE

The DSM topologies chosen for the transmitter were a 1st order low-pass (Fig. 5) and 2nd order low-pass (Fig. 6). A 4-path time-interleaved decomposition was used to achieve a equivalent sampling frequency up to 1Gsps.

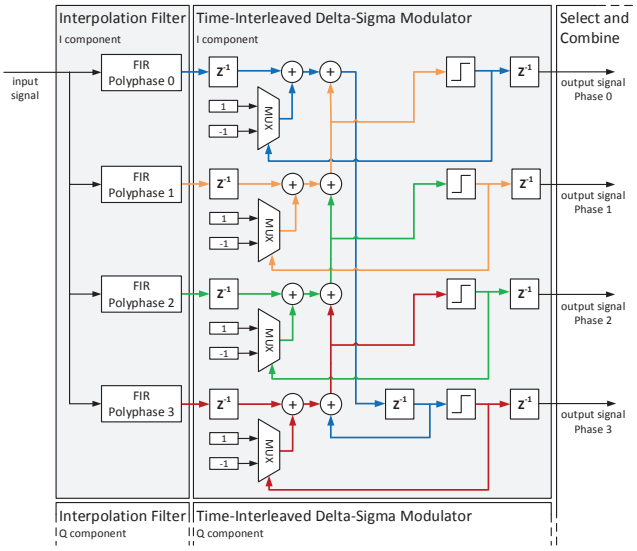


Fig. 9. First order time-interleaved shaper architecture.

The FPGA implemented 4-path TIDS first order architecture is depicted in Fig. 9. Tables I and II show the logic resources for the polyphase interpolation filter and the TIDS modulator implementation in a Virtex-6 HX380T FPGA. A polyphase interpolation FIR filter is used to interpolate the data up to modulator data rate (1Gsps for the first order DSM and 900Msps for the second order DSM).

These tables show a minimal use of resources for the implemented modulators. This means that the increase complexity in a time-interleaved DSM does not come at a high cost of resources for the implementation in transmitter systems.

TABLE I
TIDS FIRST ORDER MODULATOR AND INTERPOLATION FILTER OCCUPIED RESOURCES ON VIRTEX-6 HX380T FPGA

Logic resources	Used	Total	Percentage used
Flip Flops	233	478080	0.05%
LUTs	108	239040	0.05%
DSP48E1	8	864	0.93%

Logic max. frequency - 257.625MHz

TABLE II
TIDS SECOND ORDER MODULATOR AND INTERPOLATION FILTER OCCUPIED RESOURCES ON VIRTEX-6 HX380T FPGA

Logic resources	Used	Total	Percentage used
Flip Flops	245	478080	0.05%
LUTs	159	239040	0.07%
DSP48E1	8	864	0.93%

Logic max. frequency - 227.214MHz

Moreover, the resources usage difference between the first and second order modulators is minimal.

The use of a polyphase interpolation approach greatly simplifies the generation of a 1Gsps sample stream that in fact is made by four paths at 250Msps each. The parallel polyphase outputs are directly connected to the TIDS in such a way that the correct signal phase is used for the parallel DSM inputs.

The number of filter coefficients must be a multiple of the path number so that the delays between the filter and DSM inputs are correct, or additional delays should be added to correctly align the signal phase.

IV. EXPERIMENTAL EVALUATION AND RESULTS

The experimental setup as seen on Fig. 11 uses the proposed TIDS approach for an all-digital transmitter architecture as shown in Fig. 10 fully implemented in a Virtex-6 HX380T FPGA using the Xilinx ML628 development board.

Table III shows the logic resources for the complete transmitter implementation. It is possible to see that a large area is still available for other system functionalities such as baseband processing, protocol layers or user interfaces.

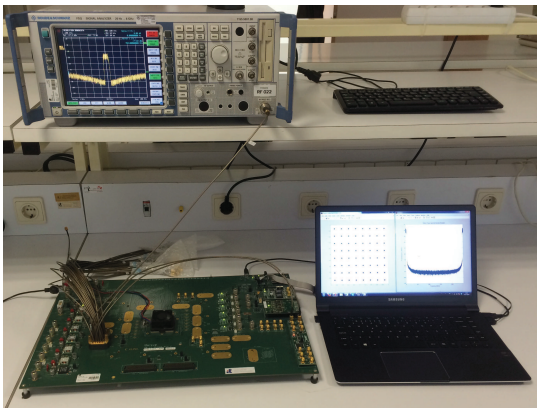


Fig. 11. Experimental setup.

TABLE III
ALL-DIGITAL TRANSMITTER OCCUPIED RESOURCES ON VIRTEX-6 HX380T FPGA

Logic resources	Used	Total	Percentage used
Flip Flops	919 (943)*	478080	0.19% (0.20%)*
LUTs	685 (787)*	239040	0.29% (0.33%)*
DSP48E1	16	864	1.85%
RAMB36E	59	768	7.68%
GTXE1s	1	40	2.50%

*In brackets values are for the 2nd order DSM

The transmitter was configured to use a 1GHz carrier frequency for all the signals and the DSM logic working frequency is 250MHz.

Several signals were created and pre-processed offline using MATLAB's Communications System and Signal Processing Toolboxes and were loaded into the FPGA's internal memory. The samples are interpolated to a 250Msps rate with a squared-root raised cosine filter with a roll-off factor of 0.22.

The input signals used were modulated using QPSK, 16-QAM and 64-QAM with symbol rates of 1.5625Msps, 3.125Msps, 6.250Msps and 12.5Msps.

The transmitted signal was directly connected to a vector

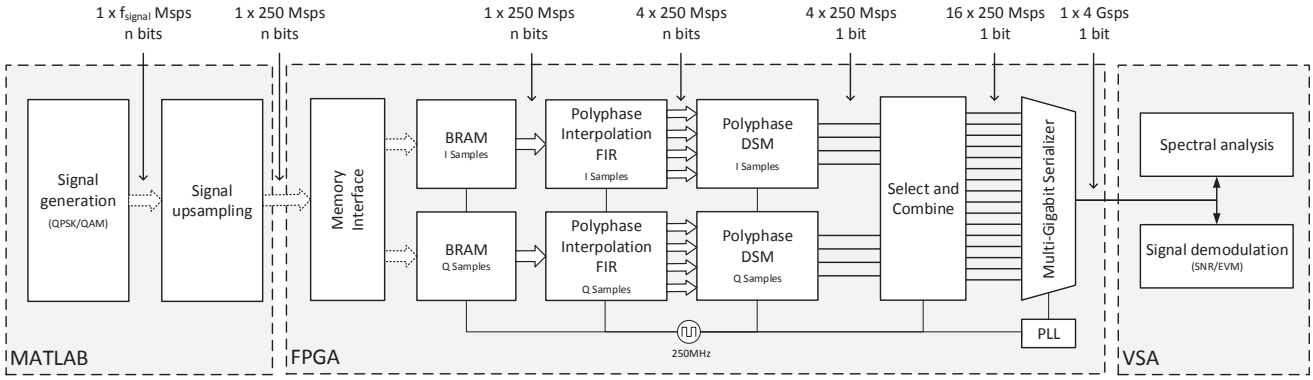


Fig. 10. All-digital transmitter architecture implemented for experimental evaluation (frequency values are for the 1Gsps 1st order modulator).

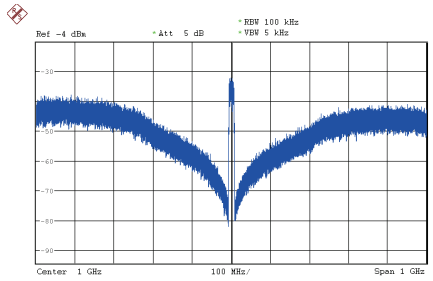


Fig. 12. Spectrum of the transmitted signal using a 1st order DSM with 12.5Msps 64-QAM signal.

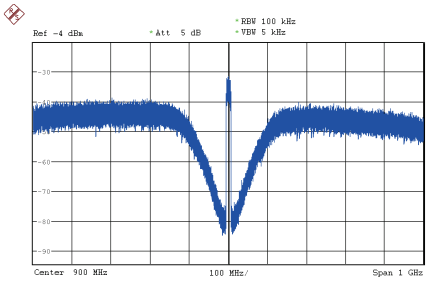


Fig. 13. Spectrum of the transmitted signal using a 2nd order DSM with 12.5Msps 64-QAM signal.

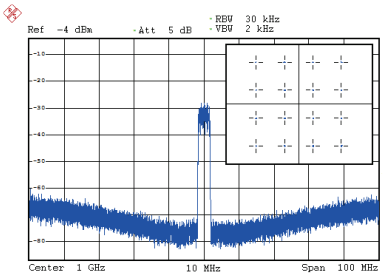


Fig. 14. Detailed view of a 16-QAM signal at 3.125Msps spectrum with 100MHz span and its received constellation in the VSA.

signal analyzer (VSA) from Rohde & Schwarz (model FSQ 8). From the VSA demodulation, error vector magnitude (EVM) and signal to noise ratio (SNR) were obtained for all the test signals.

Fig. 12 and Fig. 13 show the obtained spectrum directly at the FPGA's serializer output for a 16-QAM modulated signal at 3.125Msps resulting in a signal bandwidth of about 4MHz. Fig. 12 uses a first order TIDS modulator and Fig. 13 uses the second order TIDS modulator. Fig. 14 shows a details view of the signal's channel with a smaller span.

Table IV shows the results obtained with the VSA for the EVM and SNR figures of merit for the used test signals. It is possible to see that the EVM is always under 2% resulting in a well defined constellation as the example shown in Fig. 14.

TABLE IV
COMPARATIVE EVM AND SNR VALUES

	Signal modulation	Symbol rate (Msps) 1.5625	3.125	6.250	12.5
First order DSM at 1Gsps					
SNR (dB)	QPSK	41.1	40.2	38.5	36.4
	16-QAM	40.5	39.7	38.4	35.9
	64-QAM	40.4	40.0	37.8	35.2
EVM (%)	QPSK	0.77	0.87	1.04	1.32
	16-QAM	0.82	0.90	1.05	1.41
	64-QAM	0.80	0.89	1.12	1.52
Second order DSM at 900Msps					
SNR (dB)	QPSK	41.6	41.3	40.5	38.7
	16-QAM	41.6	41.4	40.3	38.3
	64-QAM	41.8	41.3	40.1	37.9
EVM (%)	QPSK	0.72	0.76	0.84	1.02
	16-QAM	0.72	0.73	0.85	1.05
	64-QAM	0.70	0.76	0.86	1.11

The difference between the two presented modulators is more evident for higher bandwidth signals. For this case, the second order modulator presents a slightly better performance compared to the first order DSM. This happens because the second order modulator introduces less noise near the signal's frequency band.

The quality of the results obtained with our approach, in terms of SNR and usable bandwidth of the ADT, is similar to the state-of-the-art approach presented in [6], but with much smaller hardware complexity, requiring only one output.

V. CONCLUSION

In this paper, a fully integrated SoC all-digital transmitter was presented and evaluated. What distinguishes this implementation is the fact that both signal processing techniques and hardware limitations were taken in account to maximize the quality of the transmitted signal in terms of SNR and bandwidth. To achieve this goal, a DSM at an equivalent frequency of 1GHz was designed, implemented and tested showing the advantages of parallel processing for embedded FPGA all-digital transmitters.

ACKNOWLEDGMENT

This work is funded by National Funds through FCT - Fundação para a Ciência e a Tecnologia under the project CReATION (ref. EXCL/EEI-TEL/0067/2012) and under the PhD scholarship ref. SFRH/BD/91533/2012.

REFERENCES

[1] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital generation of rf signals for wireless communications with band-pass delta-sigma modulation," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, vol. 3, 2001, pp. 2127–2130.

[2] Z. Ye, J. Grosspietsch, and G. Memik, "An fpga based all-digital transmitter with radio frequency output for software defined radio," in *Design, Automation Test in Europe Conference Exhibition, 2007. DATE '07*, April 2007, pp. 1–6.

[3] M. Helaoui, S. Hatami, R. Negra, and F. Ghannouchi, "A novel architecture of delta-sigma modulator enabling all-digital multiband multistandard RF transmitters design," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 11, pp. 1129–1133, 2008.

[4] N. Silva, A. Oliveira, and N. Carvalho, "Evaluation of pulse modulators for all-digital agile transmitters," in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, 2012, pp. 1–3.

[5] N. Silva, M. Ventura, A. Oliveira, and N. Carvalho, "Evaluation of an fpga-based reconfigurable soc for all-digital flexible rf transmitters," in *Digital System Design (DSD), 2012 15th Euromicro Conference on*, 2012, pp. 890–895.

[6] N. Silva, A. Oliveira, and N. Carvalho, "Design and optimization of flexible and coding efficient all-digital rf transmitters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, no. 1, pp. 625–632, 2013.

[7] S. Hatami, M. Helaoui, F. Ghannouchi, and M. Pedram, "Single-bit pseudoparallel processing low-oversampling delta–sigma modulator suitable for SDR wireless transmitters," pp. 1–1, 2013.

[8] M. M. Ebrahimi, M. Helaoui, and F. Ghannouchi, "Time-interleaved delta-sigma modulator for wideband digital GHz transmitter design and SDR applications," *Progress In Electromagnetics Research B*, vol. 34, pp. 263–281, 2011.

[9] P. P. Vaidyanathan, *Multirate systems and filter banks*. Upper Saddle River, NJ, USA: Prentice-Hall, Inc., 1993.

Appendix D

Wideband All-digital Transmitter Based on Multicore DSM

R. F. Cordeiro, Arnaldo S. R. Oliveira, José Vieira, and Tomás Oliveira e Silva

in *2016 IEEE MTT-S International Microwave Symposium (IMS)*

DOI: 10.1109/MWSYM.2016.7540117

Wideband All-digital Transmitter Based on Multicore DSM

R. F. Cordeiro*†, Arnaldo S. R. Oliveira*†, José Vieira*†, and Tomás Oliveira e Silva†
*Instituto de Telecomunicações
†Departamento de Electrónica, Telecomunicações e Informática Universidade de Aveiro
Campus Universitário de Santiago, Aveiro, 3810-193, Portugal
Email: ruifiel@ua.pt, arnaldo.oliveira@ua.pt, jnvieira@ua.pt, tos@ua.pt

***Abstract*—This paper presents a new wideband all-digital pulsed transmitter architecture based on delta-sigma modulation. The proposed architecture uses a parallel approach for the signal modulator to augment the digital system sampling frequency. The improvement of the sampling frequency allows to enhancement of the transmitter bandwidth without the need of high speed digital logic for the pulse modulator.**

The FPGA prototype results show the feasibility and advantages of the proposed architecture in terms of bandwidth. The measurements show that the proposed transmitter is capable of a 122 MHz bandwidth signal transmission, which represents a significant improvement over the current state-of-the-art bandwidth for all-digital pulse transmitters.

***Index Terms*—All-digital transmitter, delta-sigma modulation, pulsed-transmitters.**

I. Introduction

The next generation of wireless communications is expected to continue the trend towards the full digitalization of the radio transceiver, motivated by the flexibility of software defined radio (SDR) implementations, which have gained a substantial importance in the radio's hardware design. Moving the software and the digital signal generation closer to the antenna and removing most of the conventional RF hardware from the path would be a fundamental improvement for both mobile terminals and base-stations. The radio digitalization allows for the massive miniaturization of the radio hardware since digital logic blocks continue to shrink with technology evolution, following Moore's Law, which barely happens with the analog components. While decreasing the area of analog circuits is usually a requirement for mobile terminals, more often that not, shrinking the analog circuit leads to worse component tolerances and deteriorates the performance. This will eventually decrease the analog circuit performance or render it unpractical for some radio applications.

Completely digital radio transmitter implementations based on pulsed modulators, often entitled all-digital transmitters (ADT), have already shown promising results on achieving a fully digital and therefore potentially tunable or configurable transmitter architecture using a very compact radio design [1], [2]. For this reason, ADTs have the necessary degree of flexibility and integration for highly dense and heterogeneous wireless networks while providing exceptionally integrated architecture for the RF transceiver.

However, these architectures are still subject to some performance issues that restraint their use when compared to conventional radio architectures, in particular the transmitter bandwidth. Most of the ADTs presented in the literature have very small bandwidth signals, around a few units of MHz, which limits the achievable data-rates in practical application scenarios [3]–[5]. The bandwidth limitation is due to the digital implementation of the signal pulsed modulators in DSM or PWM architectures in which the logic switching frequency limit defines the achievable sampling frequency to a maximum value depending on the technology used, constraining either the maximum oversampling ratio (OSR) or the maximum signal bandwidth.

To overcome these limitations, some papers presented the use of parallel processing followed by dedicated high-speed logic such as a multiplexer or serializer to reach a higher equivalent sampling frequency [3], [4], [6]. Parallel architectures make possible the design of considerable higher bandwidth transmitters working at reduced logic frequencies for most of the design and allow the competitive integration with lower-cost technologies. However, even with parallel architectures the transmitter bandwidth is often limited to a few tenths of MHz due to the feedback logic on DSM topologies which limits the clock frequency.

In this paper, a new scalable wideband ADT architecture for SDR systems is proposed. It distinguishes itself from other architectures by improving the achievable bandwidth in ADTs, comparing to other state-of-the-art transmitters, from less than 20 MHz up to a maximum of 122 MHz.

II. All-digital Transmitter Architecture

This section details the digital transmitter architecture used to implement the wideband all-digital transmitter.

The proposed architecture is based on a truly parallel system using multiple DSM cores working separately. In particular, it uses 16 parallel paths as shown in block diagram of Fig. 1.

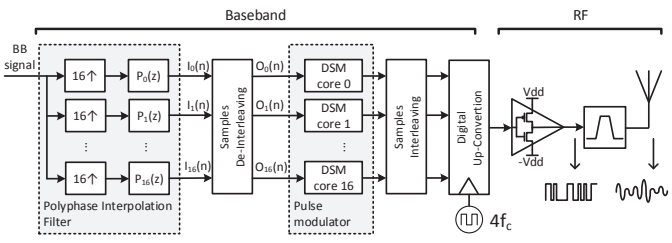


Fig. 1. Proposed architecture for the wideband all-digital transmitter. The signal paths are 2 channel paths with the in-phase (I) and quadrature (Q) samples.

This architecture differs from common parallel DSM implementations that use polyphase decomposition to achieve a time-interleaved DSM. Conventional DSM polyphase architectures do not scale linearly with the number of parallel branches, since the multiple phases are not independent between each other, limiting the achievable frequency gains [4].

The proposed system uses a polyphase interpolation filter with 16 phases to achieve a high OSR. Each one of the 16 phases is feed to a de-interleaver block. In this block the high sampling rate samples from the interpolation filter are reorganized into 16 different time blocks with N oversampled samples. By changing the signal sample order accordingly, each one of the independent DSM can process a portion of the baseband signal corresponding to a contiguous time block. Although the processing is done at lower clock frequency, it is equivalent to the higher sampling frequency imposed by the polyphase filter.

The de-interleaved block input signal is defined as in (1) with 16 parallel phases $I_k(n)$, where k is the signal phase from the interpolation filter.

$$\begin{aligned}
I_0(n) &= [\quad P_0(0) \quad P_0(1) \quad P_0(2) \quad \cdots \quad P_0(N)] \\
I_1(n) &= [\quad P_1(0) \quad P_1(1) \quad P_1(2) \quad \cdots \quad P_1(N)] \\
I_2(n) &= [\quad P_2(0) \quad P_2(1) \quad P_2(2) \quad \cdots \quad P_2(N)] \\
&\qquad\qquad\qquad\qquad\qquad \ddots \\
I_{16}(n) &= [\quad P_{16}(0) \quad P_{16}(1) \quad P_{16}(2) \quad \cdots \quad P_{16}(N)]
\end{aligned} \tag{1}$$

In the time domain, these phases are related between each other at each sampling instant n, such that $P_0(n)$ is the first sample then $P_1(n)$, followed by $P_2(n)$ up to $P_{16}(n)$. However, this sequence is in parallel because it would be impossible to process at the equivalent sampling frequency. The de-interleaver stores these parallel samples and at the trade of a small amount of added latency re-arranges the samples order such that the output $O_k(n)$ is now as presented in (2).

$$\begin{aligned}
O_0(n) &= [P_0(n) \quad P_1(n) \quad \cdots \quad P_{16}(n)] \\
O_1(n) &= [P_0(n+N) \quad P_1(n+N) \quad \cdots \quad P_{16}(n+N)] \\
O_2(n) &= [P_0(n+2N) \quad P_1(n+2N) \quad \cdots \quad P_{16}(n+2N)] \\
&\qquad\qquad\qquad\qquad \ddots \\
O_{16}(n) &= [P_0(n+16N) \quad P_1(n+16N) \quad \cdots \quad P_{16}(n+16N)]
\end{aligned} \tag{2}$$

The output has now the baseband samples arranged into N contiguous samples blocks for each output. The de-interleaver outputs can be processed by a independent DSM. This means, that although the sampling frequency of the DSM is f_s, the equivalent sampling frequency is 16 times higher, considerably improving the achievable bandwidth.

The block size in samples, N, influences the signal error, since the transition between different time blocks will introduce some errors. This occurs because the memory of the ideal DSM is infinite, and by separating the signal into N samples groups, at each N samples there will be a small transient error in the signal from the transition between blocks. To analyze the introduced error, the DSM outputs of the conventional DSM (at high clock rate) and the proposed parallel DSM architecture were compared by simulation and the signal degradation in terms of signal-to-noise ratio (SNR) was analyzed. The simulation results in Fig. 2 shown that for block sizes N above 2000 samples, the maximum SNR degradation is always less than 1 dB. Hence the chosen value for the block size was 2000 samples.

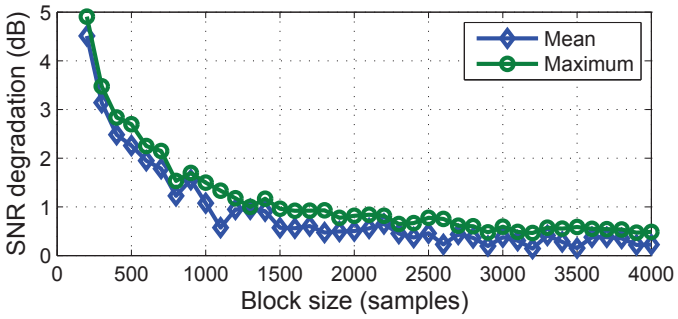


Fig. 2. SNR degradation between a single phase DSM and the proposed parallel multiple core DSM. The simulation was run using a set of random signals with PAPR values between 3 dB and 12 dB and bandwidths from 5 MHz to 100 MHz.

The modulator cores are the same first-order low-pass DSM replicated 16 times. The choice of a first-order modulator over a higher order modulator with better noise rejection is due to the fact that the first order modulator provides a better coding efficiency for the transmitted signal [7]. This has a considerable importance to improve the overall transmitter power efficiency.

After modulation, the samples must be re-arranged to their original order, corresponding to the polyphase filter output. This is done in the samples interleaving block which re-organizes the 2-level signals from the DSM cores back to the original configuration as in (1).

The digital up-conversion is implemented combining the I and Q samples as well as their inverted versions $\overline{I}$ and $\overline{Q}$. The vector is defined as a repetition of the (I Q $\overline{I}$ $\overline{Q}$) pattern sampled at a $4 \times f_c$ (carrier frequency). The serialization of this vector with dedicated high speed serializer allows a high sampling frequency at the system output while maintaining a lower clock frequency, f_s, for the baseband hardware blocks. Once serialized at a frequency $4 \times f_c$, this pattern is equivalent to the multiplication of the I and Q signals with two square waves at f_c, with 90 degrees phase shift between them [2]. The ADT generated output is the baseband DSM signal up-converted to a RF carrier at f_c.

III. Experimental Results

A proof of concept prototype of the wideband ADT was designed using the architecture presented in Fig. 1. The FPGA-based ADT was implemented in a ML628 board from Xilinx

with a Virtex-6 VHX280T FPGA. The RF ADT 2-level output signal was directly connected to a Vector Signal Analyzer (VSA) from Rohde & Schwarz (model FSW 8) for signal and spectral analysis. Baseband signals were generated offline and loaded into the FPGA's internal I and Q memories. The generated baseband signals used are QPSK, 16-QAM and 64-QAM signals with a symbol rate varying from 5 Msps up to 100 Msps with 5 Msps steps. This is equivalent to signals with bandwidths from 6.1 MHz up to 122 MHz.

The DSM equivalent frequency is 3200 MHz (16 parallel paths at 200 MHz). In Fig. 3 three examples of a transmitted 64-QAM signal spectra are shown, the blue plot is the spectrum of the transmitter with a 6.1 MHz signal, the green plot has a 61 MHz bandwidth and finally the red plot is the 122 MHz bandwidth signal, all centered at a 1.6 GHz carrier.

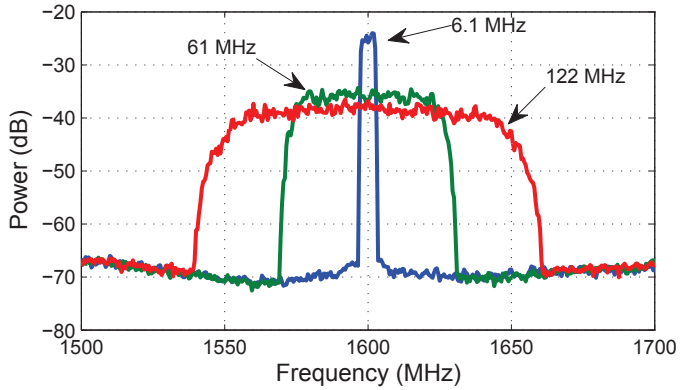


Fig. 3. All-digital transmitter spectra for 6.1 MHz, 61 MHz and 122 MHz bandwidth 64-QAM signals.

The signal to noise ratio (SNR) and the error vector magnitude (EVM) were measured to evaluate the transmitter signal quality using the VSA demodulator. The SNR and EVM measurements are displayed, respectively, in Fig. 4 and Fig. 5.

The results show that for the tested signals, the achievable SNR is always above 30dB for all the modulations used, including the 122 MHz bandwidth signal. This corresponds to a transmission with less than 3.1% EVM for all modulations in a transmitter capable of transmit up to 600 Mbits/s signals. The coding efficiency was also measured for all the signals varying between 11% and 27% depending on the signal modulation.

Table I shows a comparison between this work and other state-of-the-art ADT focusing on the transmitter signal bandwidth. As it is possible to see, this work largely exceeds the common signal bandwidths for these category of transmitters.

TABLE I
MAXIMUM TRANSMITTER BANDWIDTH STATE-OF-THE-ART COMPARISON.

	Bandwidth	SNR	Modulation
Ebra11 [3]	8 MHz	60	TIDS
Cord13 [4]	19 MHz	35.2 dB	TIDS
Chun15 [5]	5 + 10 MHz	-	BPDSM and RFPWM
This work	122 MHz	31.4	Parallel DSM

IV. CONCLUSION

In this paper it was presented a new all-digital transmitter architecture to improve the digital transmitter's bandwidth. The system uses a set of parallel DSM cores that are independent between each other but allow for the linear scaling improvement of the sampling frequency of the transmitter modulator. The proposed architecture prototype measurements shown the improvement in terms of transmitter bandwidth comparing to other state-of-the art transmitters. In fact, this architecture allowed the improvement of the state-of-the-art bandwidth from less than 20 MHz to more than 120 MHz.

ACKNOWLEDGMENT

This work is funded by National Funds through FCT - Fundação para a Ciência e a Tecnologia under the project PEst-OE/EEI/LA0008/2013; UID/EEA/50008/2013 and PhD scholarship SFRH/BD/91533/2012 and by the Instituto de Telecomunicações under project CReATION (ref. EXCL/EEI-TEL/0067/2012).

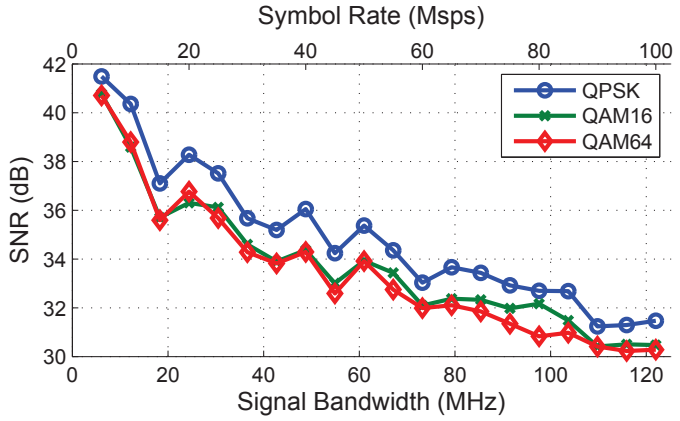


Fig. 4. SNR measurement for a bandwidth sweep from 6.1 MHz to 122 MHz with a carrier frequency of 1.6GHz.

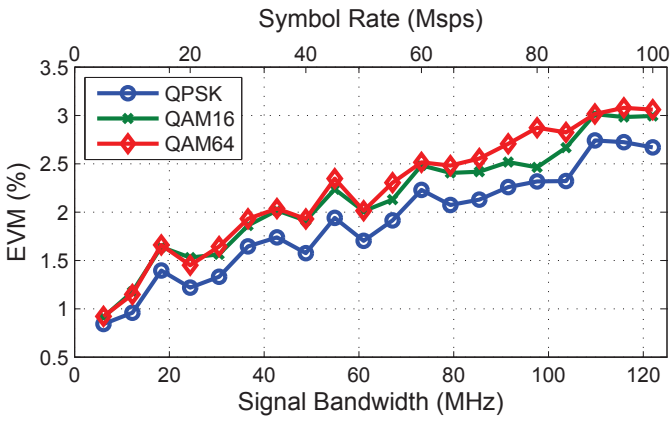


Fig. 5. EVM measurement for a bandwidth sweep from 6.1 MHz to 122 MHz with a carrier frequency of 1.6GHz.

REFERENCES

[1] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital generation of RF signals for wireless communications with band-pass delta-sigma modulation," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, vol. 3, 2001, pp. 2127–2130.

[2] Z. Ye, J. Grosspietsch, and G. Memik, "An FPGA based all-digital transmitter with radio frequency output for software defined radio," in *Design, Automation Test in Europe Conference Exhibition, 2007. DATE '07*, April 2007, pp. 1–6.

[3] M. M. Ebrahimi, M. Helaoui, and F. Ghannouchi, "Time-interleaved delta-sigma modulator for wideband digital GHz transmitter design and SDR applications," *Progress In Electromagnetics Research B*, vol. 34, pp. 263–281, 2011.

[4] R. F. Cordeiro, A. Oliveira, J. Vieira, and N. V. Silva, "Gigasample time-interleaved delta-sigma modulator for fpga-based all-digital transmitters," *Digital System Design (DSD), 2013 Euromicro Conference on*, 2013.

[5] S. Chung, R. Ma, S. Shinjo, H. Nakamizo, K. Parsons, and K. H. Teo, "Concurrent multiband digital outphasing transmitter architecture using multidimensional power coding," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 63, no. 2, pp. 598–613, Feb 2015.

[6] S. Hatami, M. Helaoui, F. Ghannouchi, and M. Pedram, "Single-bit pseudoparallel processing low-oversampling delta–sigma modulator suitable for SDR wireless transmitters," pp. 1–1, 2013.

[7] M. Ebrahimi and M. Helaoui, "Reducing quantization noise to boost efficiency and signal bandwidth in delta sigma-based transmitters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, no. 12, pp. 4245–4251, Dec 2013.

Appendix E

All-digital Transmitter with Mixed-domain Combination Filter

R. F. Cordeiro, Arnaldo S. R. Oliveira, and José Vieira

in ***IEEE Transactions on Circuits and Systems II: Express Briefs (Volume: 63, Issue: 1, Jan. 2016)***

DOI: 10.1109/TCSII.2015.2483198

All-digital Transmitter with Mixed-domain Combination Filter

R. F. Cordeiro, *Student Member, IEEE*, Arnaldo S. R. Oliveira, *Member, IEEE* and J. M. N. Vieira

***Abstract*—In this paper we present a new reconfigurable filtering technique for all-digital transmitters using signal interference and cancellation. The proposed method allows the change of some filtering characteristics digitally. This technique is used to reduce the quantization noise from the all-digital transmitter's output, reducing the analog output filter requirements. Without a narrow band filter, a greater degree of flexibility for the transmitter's carrier frequency and bandwidth is attained, improving its suitability for multiband and multistandard operation.**

The presented results show the quantization noise reduction without an output analog filter, contributing to an increase of the transmitter's coding efficiency up to more than 95%.

***Index Terms*—All-Digital Transmitter; Delta-sigma modulation; Coding efficiency; FPGA; Software-Defined Radio.**

I. Introduction

ONE of the technology trends for 5G communications is the convergence of many different wireless communication standards and their implementation into a single integrated radio. To do this, the complete integration of multiband and multi-standard radios into System-on-Chip devices is fundamental and expected to be a widely adopted trend in next generation communication systems. Modern multistandard communications may rely on the use of more advanced Software-Defined Radios (SDR) with reconfigurable transmitters and receivers that are easier to adapt to different communication scenarios than conventional analog radios.

In the last decade, there has been a significant research effort in the area of radio-frequency (RF) transceivers using novel hardware implementations that rely on full digitalization of the RF datapath. In [1] the concept of using high-speed delta-sigma modulation (DSM) was introduced by encoding an RF signal into 1-bit stream at a very high sampling rate (4 times the carrier frequency). State-of-the-art all-digital transmitters typically use baseband delta-sigma (DSM) or pulse-width modulation (PWM) architectures to convert the digital signal into pulses, followed by digital up-conversion stages [2]–[4]. Baseband pulse modulation enables the use of Field-Programmable Gate Array (FPGA) devices for implementing the radio, providing additional flexibility due to the FPGA inherent reconfigurability. FPGA's logic capacity, resource diversity and dedicated high-speed I/O transceivers, if efficiently explored, can be used in the development of agile all-digital transmitters (ADTs). However, ADT architectures share a set of key limitations that reduce their usability in real implementations. Two-level encoded signals have the drawback of adding a significant amount of quantization error to the transmitted signal, which affects the relation between signal and noise power, reducing the coding efficiency (CE) of the output signal and thus decreasing the overall transmitter efficiency [5]. Multilevel quantization transmitters can be used to decrease the quantization noise power and improve CE, however they are more prone to nonlinearities at the combination of the signals due to mismatch amplitudes which increases the in-band distortion. To decrease the quantization noise power in two level signals, analog filters with high quality factor (Q), such as SAW, BAW or cavity filters, are necessary at the output of the transmitter. However, the introduction of an analog filter will impair the flexibility gained using a digital transmitter, binding the transmitter to the central frequency of the filter.

In this paper, a method to filter the ADT quantization noise without the use of a high Q analog filter is proposed. This technique uses signal interference to cancel the ADT's quantization noise and improve its CE.

II. All-Digital transmitters and their limitations

This section summarizes the ADT architecture used in FPGA-based transmitters and highlights some of the limitations that digital transmitters still have. DSM-based ADTs use delta-sigma pulse modulators to convert high resolution signals into lower amplitude resolution, while maintaining an adequate signal-to-noise ratio (SNR) within the signal's bandwidth. The lower bit resolution, namely two-level signals, allow for RF wave generation using an entirely digital datapath.

Fig. 1 shows a DSM-based digital transmitter architecture. The baseband processing block may vary depending on the protocol and standards used. This block does not differ from the digital baseband processing used for common radio architectures. The signal shaping stage uses DSM to convert the in-phase and quadrature N bit samples to single bit representation signals. The up-conversion block up-converts the 1-bit baseband signal to RF using an high speed multiplexing of the I and Q 1-bit signals. The multiplexing is equivalent to multiplying the I and Q samples by two square waves with a 90° phase relation between them.

The resulting frequency spectrum has the RF signal centered at f_c with added quantization noise from DSM. While reducing the added quantization noise within signal's bandwidth is possible using higher order DSM, removing the noise in the sidebands is impossible without filtering the output signal.

There is a direct relationship between the quantization noise and the overall transmitter efficiency. This relation, called

The authors are with the Instituto de Telecomunicações, Universidade de Aveiro, Campus Universitário de Santiago, Aveiro, 3810-193, Portugal (Email: ruifiel@ua.pt, arnaldo.oliveira@ua.pt, jnvieira@ua.pt)

This work is funded by National Funds through FCT - Fundação para a Ciência e a Tecnologia under the project PEst-OE/EEI/LA0008/2013; UID/EEA/50008/2013 and PhD scholarship SFRH/BD/91533/2012 and by the Instituto de Telecomunicações under project CReATION (ref. EXCL/EEI-TEL/0067/2012).

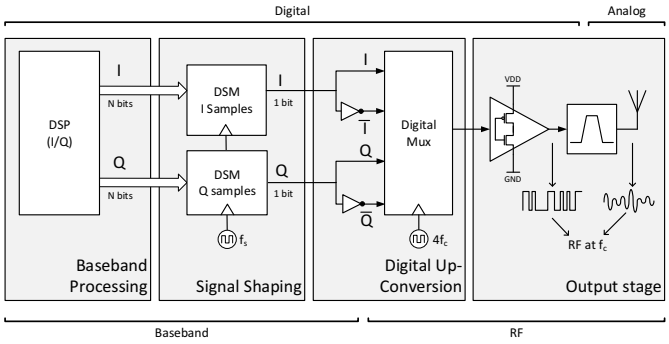


Fig. 1. DSM-based ADT architecture. Baseband delta-sigma conversion occurs at f_s while the digital up-conversion works at a frequency of $4 \times f_c$, being f_c the carrier frequency.

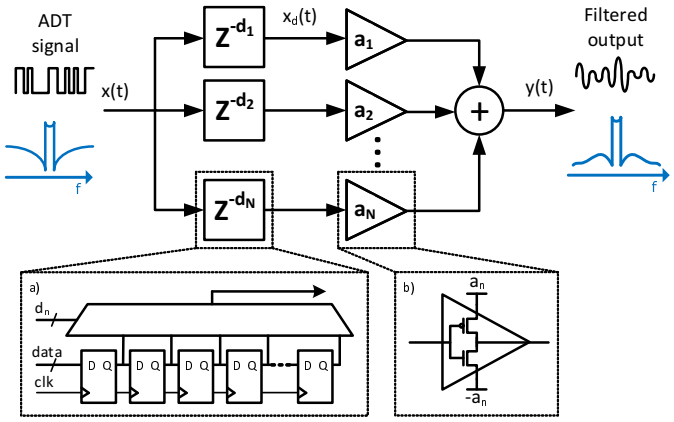


Fig. 2. Simplified structure of a combination filter. Each branch has a specific time delay d_n and signal gain a_n.

coding efficiency (CE) is dependent on the modulator added noise. The average CE is defined as the power on the signal's channel P_s, over the total transmitted power P_t [6].

$$CE = \frac{P_s}{P_t} \tag{1}$$

The CE in DSM depends on the input signal characteristics, particularly on its peak-to-average power ratio (PAPR) [7], and is typically low for common wireless communications signals, which frequently use QAM or OFDM modulations, with high PAPR. In [7] it is shown that for signals with 3dB PAPR or more, the transmitter efficiency is below 30%, regardless on the DSM order, and it will decrease with increasing PAPR. Low CE means that only a small fraction of the transmitter's power is, in fact, signal power, the remaining being quantization noise, which needs to be filtered. The output analog filter, necessary for these transmitters, must have a high Q to attenuate the quantization noise close to the signal's bandwidth, which imposes difficult filter requirements. The output of the transmitter thus requires a fixed, narrow band filter. For a multi-band and flexible carrier transmitter, this imposes a significant limitation to its flexibility.

III. Proposed Filtering Method

This section describes the proposed method to create a digitally controllable output filtering of the transmitter's signal. This architecture significantly decreases the ADT output quantization noise, improving its CE and flexibility by relaxing the output filter quality factor requirements.

The proposed method, shown in Fig. 2, uses a mixed-mode digital-analog combination filter with delayed versions of the transmitter's output. Using multiple delayed outputs that are weighted and combined, it is possible to cancel the signal's power at particular frequencies. By adjusting the delays d_n and the coefficients a_n, the filter's frequency response can be changed. This type of filter has a finite impulse response, however the signals are combined in analog domain using a power combiner. Similar techniques were used in [8], [9] to improve digital transmitter's ACLR and dynamic range. However, in both works the noise removed was in a very narrow bandwidth, which do not improve the transmitter CE and still requires a narrow band output filter.

Using the structure of Fig. 2, any frequency response can be approximated with an error dependency on the filter order (number of delayed branches). For a narrow band frequency response a high order is required, making this filter impractical. Despite this, for reasonably narrow band responses it is possible to use this filter technique with a low number of combination branches using interpolated filter responses.

Combining several RF branches to create an interference using analog circuitry is challenging since it is difficult to guarantee a constant delay over a large bandwidth, specially if that delay has to be adjustable. On the other hand, with an ADT architecture, the signal can be delayed using digital shift registers to handle the time delays (Fig. 2). Since the RF signal is digital, the control of the delays is simple and can be used to adjust the filter to different situations.

The weight gain stage, which for analog implementations has to be implemented using a set of variable amplifiers or attenuators, can be implemented by regulating the supply voltage of the output buffers. This is possible because the output wave from the ADT is a two level square wave.

The number of combination branches used in the combination filter (shown in Fig. 2) depends on the desired CE or noise attenuation. A higher number of branches leads to higher noise rejection and CE, however, for DSM the CE and potential filtering gains are conditioned on the signal's PAPR. Since the modulator's quantization noise hinges on the signal, higher PAPR signals require additional noise attenuation to achieve the same CE.

Fig. 3 shows simulation results for the ADT CE variation with the number of combination branches for different PAPR values. While, as expected, for higher number of branches the CE approaches 100%, the hardware complexity also increases, which should be taken into account. For each branch, a delay shift register and a high speed digital output buffer are required. A compromise between hardware complexity and CE was found with 8 branches guaranteeing a CE above 80% for signals up to 12dB PAPR.

The filter's time response can be deduced from the combined signals as shown in (2). The conversion to the frequency domain, as shown in (3), is found using the Fourier transform.

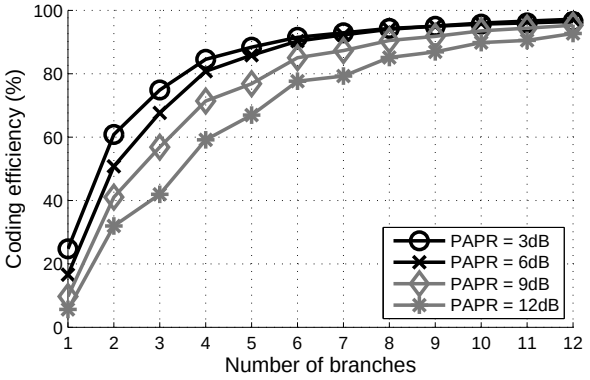


Fig. 3. Coding efficiency depending on the number of branches and signal PAPR.

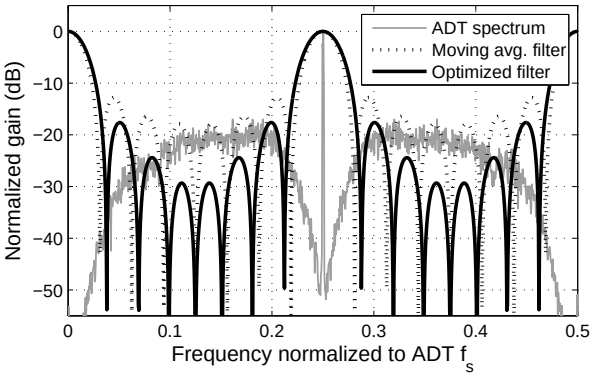


Fig. 4. DSM-based digital transmitter spectrum and two proposed ideal frequency responses for the combination filter.

$$y(t) = \sum_{n=1}^{N} a_n x(t - d_n) \tag{2}$$

$$Y(f) = \underbrace{\Big(\sum_{n=1}^{N} a_n e^{-j2\pi f d_n} \Big)}_{H(f)} X(f) \tag{3}$$

The first term of (3), $H(f)$, gives the equivalent filter frequency response generated from the interference between the combined signals.

Fig. 4 shows an example of an ADT frequency power spectrum for the transmitter's first Nyquist zone. Since the majority of the quantization noise is located around the center of the delta-sigma side lobes, the filter coefficients, a_n and d_n, should be adjusted for higher attenuation at those frequencies.

On the other hand, DC and $f_s/2$ frequencies have quantization noise power nulls, which allows relaxation of $H(f)$ at those points. Considering this simplification, Fig. 4 shows two filter magnitude frequency responses of $H(f)$, with ideal a_n and d_n values, to attenuate the quantization noise using 8 parallel branches, according to the architecture in Fig. 2. The presented frequency responses were obtained assuming that the delays d_n are fixed step delays, so that $d_n = k_n d_0$, because the delay implementation is done using digital registers. The minimum delay step d_0 is inverse of the ADT sampling frequency f_s, $d_0 = 1/f_s$. The first shown filter response (doted plot in Fig. 4) is a moving average interpolated filter with coefficients $a_n = [0.125, 0.125, 0.125, 0.125, 0.125, 0.125, 0.125, 0.125]$ and $k_n = [0, 4, 8, 12, 16, 20, 24, 28]$. This is a sum of the 8 signal phases with the same square wave amplitude.

The optimized filter (black line plot in Fig. 4) is a filter optimization to further reduce the quantization noise from the side lobes using different a_n values. The chosen coefficients were $a_n = [0.4375, 0.8125, 0.9375, 1, 1, 0.9375, 0.8125, 0.4375]$ and $k_n = [0, 4, 8, 12, 16, 20, 24, 28]$. This solution was obtained using an adapted Parks-McClellan algorithm, which finds the coefficients that provide the best approximation to the desired frequency response in the minimax sense [10]. The adapted algorithm performs successive weight adaptations to reduce the error in the magnitude response of the filter only above the desired frequency response. Doing this, it is possible to maximize the filter attenuation for frequencies in which the quantization noise is still higher than the desired carrier to noise ratio. The real values for the a_n coefficients will depend on the hardware limitations of the buffer's differential voltage. Presented values were the best case achievable for the current hardware implementation, but do not represent the best case achievable for arbitrary non-quantized values of a_n.

IV. Hardware implementation

The proposed ADT architecture uses a combination filtering technique that significantly reduces the transmitter quantization noise and improves the transmitter CE. Comparing to similar pulse ADTs, it reduces the transmitter's output filtering requirements improving the system flexibility.

The proposed transmitter architecture, presented in Fig. 5, shares a similar topology to the previous architecture, Fig. 1, up to the digital up-conversion stage.

The baseband signal was previously generated off-line and loaded into a memory to emulate a typical transmitter chain. The DSP stage of the transmitter increases the sampling rate up to f_{dsm}. This frequency may vary but it must be guaranteed that the oversampling ratio is enough for the DSM to provide a good SNR. Hardware frequency limitations constrain the OSR to a maximum achievable value.

The DSM stage converts the I and Q signals to a 1-bit equivalent at f_{dsm}. The modulator used in this work is a time-interleaved first order low-pass delta-sigma modulator presented in [11]. This architecture is a parallel polyphase DSM with 4 phases capable of achieving the combined sampling frequency (f_{dsm}) of 1.6GHz.

The digital up-conversion is done using an integrated high speed serielizer, the FPGA's multi-gigabit transceiver (MGT), that multiplexes in time the I and Q signals from the DSM with their inverted version. This is done accordingly to the DSM sample order defined in the Select and Combine block. The carrier frequency is defined by setting the ADT sampling frequency f_s so that $f_s = 4 \times f_c$.

The mixed domain filter was implemented by adding the hardware block shown in Fig. 2 to process the RF signal from the select and combine block. The digital RF signal is

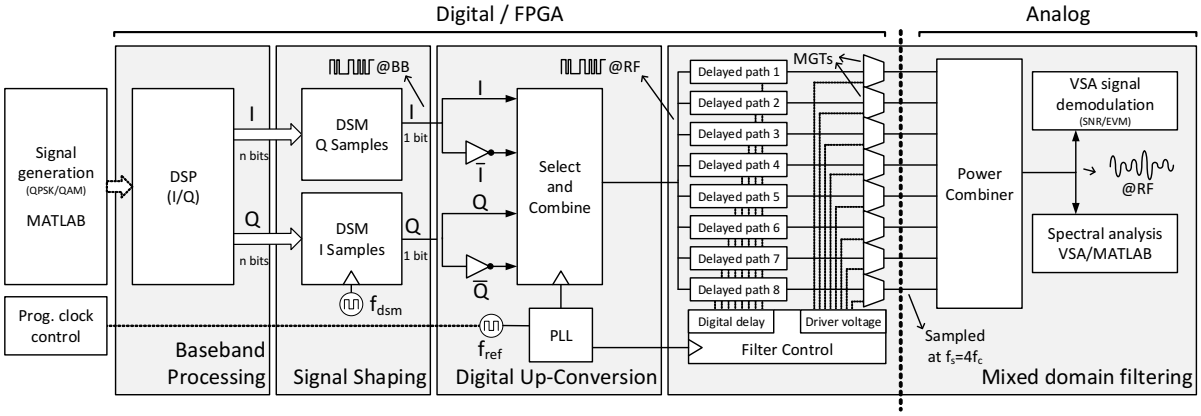


Fig. 5. Hardware FPGA-based implementation of the proposed method.

delayed into 8 different delay paths, each one used as input to an embedded MGT. These delays are integer multiples of the minimum delay step d_0. Each delayed path feeds a high speed digital output driver (up to 6.4 Gbps). The voltage swing of these drivers is digitally controlled, acting as an adjustable gain a_n, for each filter path. The voltage swing had a limited number of possible values, hence the optimized values of a_n were quantized. The filtering effect is achieved by combining the 8 different paths in the analog domain using a power combiner. The power combiner is wide-band to allow for noise cancellation over the whole bandwidth of the delta-sigma modulated signal. For higher level of integration, the power combining can be achieved using fully-integrated CMOS combiners [12], consenting a small size factor for the transmitter architecture.

V. Experimental setup and results

This section presents the main experimental results for the implementation of the proposed ADT. The used experimental scheme setup is detailed in Fig. 5. For the proposed prototype, a ML628 board from Xilinx was used. The digital hardware project was developed for a Virtex6 HX380T FPGA as a proof-of-concept. The used power combiner is an 8:1 RF power combiner ZN8PD1-53+ from Mini-Circuits. A set of fixed delay lines is used to guarantee the correct time alignment of the 8 delayed outputs. This is done because the development board layout does not guarantee a perfect time alignment for different MGT outputs. The signals were aligned using microstrip lines with the appropriate length.

The transmitter output was connected to a Vector Spectrum Analyzer (VSA) as shown in Fig. 5. From the VSA, the error vector magnitude (EVM), signal to noise ratio (SNR), coding efficiency and spectrum were obtained. The input signals, to test the transmitter were QPSK and 64-QAM modulations with symbol rates between 1.5625 Msps and 15.625 Msps.

The transmitted spectrum is shown on Fig. 7 for three different cases and can be compared with the simulation results on Fig. 6. The first plot, in black, shows the original ADT signal without any filtering. The dark gray plot is the output signal using 8 branches with the moving average filtering. Finally, the last plot in light gray is the output spectrum using the optimized filtering coefficients.

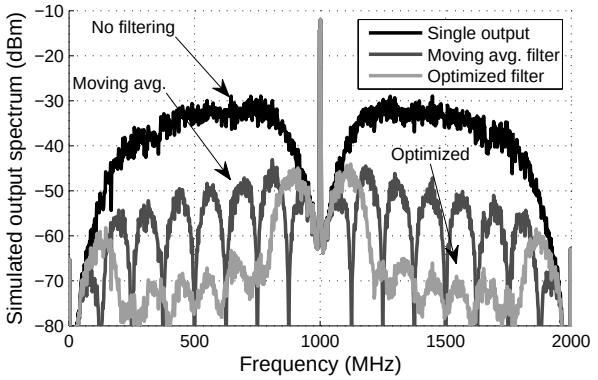


Fig. 6. Simulated transmitter spectrum with 500kHz resolution bandwidth for the two proposed ideal frequency responses of the combination filter.

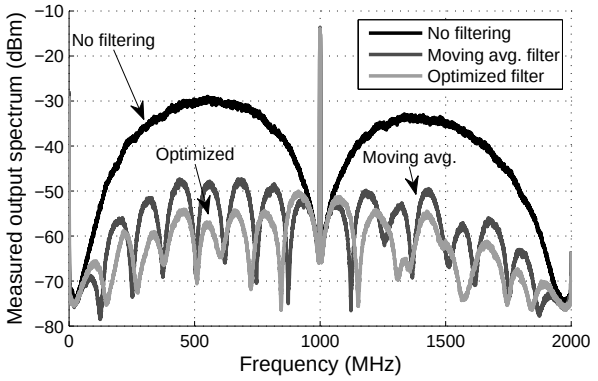


Fig. 7. Measured spectra, with 500kHz resolution bandwidth and 5kHz video bandwidth, captured with a 2GHz span. Signal at 1GHz carrier frequency.

Comparing the simulation with the measured results it is possible to see that for the optimized filter the obtain results are quite different from the expected in simulation. This is due to the time misalignments at the outputs of the parallel delay paths and the amplitude mismatch between the different drivers. While these errors are small, for very low gain frequencies in the filter frequency response, any small mismatch in the coefficients a_n or d_n result in considerable changes on the logarithmic scale.

The carrier to noise power ratio without filtering is very low,

TABLE I
COMPARISON WITH OTHER ALL-DIGITAL TRANSMITTER APPROACHES

	Ghan10 [6]	Pods12 [13]	Silv13 [4]	Ebra13 [7]	Chun15 [14]	This work			
Signal	WiMAX	QPSK	QAM64	OFDM	LTE	QPSK	QAM64	QAM64	2×QAM64*
Bandwidth	1.25MHz	0.625MHz	1.5MHz	1.4MHz	5+10MHz	3.5MHz	3.5MHz	19MHz	2×9.5MHz*
PAPR	3.8dB - 11.9dB	8dB	-	7.8dB	11.7dB	3.8dB	6.8dB	6.9dB	9.5dB
Cod. Eff.	25.8 - 3.8%	21%	79.3%	18.7%	35.4 - 47.1%	94.1%	91.9%	93.8%	88.5%
SNR	45dB	-	50dB	41dB	-	39.5dB	42.6dB	35.2dB	32.9dB
Modulation	2-level DSM	2-level DSM	Multi-path PWM	QNRIF DSM	BPDSM and RFPWM	2-level DSM w/ mixed-domain filtering			

*Two adjacent channels with simultaneous transmission.

TABLE II
TRANSMITTER CODING EFFICIENCY AND CARRIER TO NOISE RATIO

Carrier frequency		$0.5GHz$	$1GHz$	$1.6GHz$
		Transmitter Coding Efficiency		
QPSK 1.5625Msps	No filtering	19.03%	19.16%	20.05%
	Moving avg.	88.29%	90.89%	93.25%
	Optimized	91.28%	94.18%	96.71%
QAM 15.625Msps	No filtering	11.66%	11.14%	11.02%
	Moving avg.	85.22%	88.09%	89.08%
	Optimized	89.87%	92.89%	93.84%
		Carrier to noise ratio		
QPSK 1.5625Msps	No filtering	18.67dB	19.21dB	19.47dB
	Moving avg.	35.17dB	37.12dB	37.13dB
	Optimized	39.93dB	40.89dB	41.49dB
QAM 15.625Msps	No filtering	7.21dB	6.05dB	5.70dB
	Moving avg.	24.74dB	23.77dB	22.61dB
	Optimized	28.49dB	28.27dB	28.46dB

which reduces CE and aggravates the need of a high quality factor analog filter. Table II shows the CE and the carrier to noise ratio for the first Nyquist zone results using two signals for the worst and best tested scenario in terms of CE, QPSK at 1.5625Mbps and 64QAM at 15.625Mbps respectively.

From these measures, it is possible to see that this method allows to achieve a CE of more than 89% for both scenarios within the transmitter's band (500MHz to 1600MHz) using the optimized filtering. The table also shows the noise peak power reduction from the carrier to noise measure which improves from about 19dB to more than 40dB in the best case and from 6dB to 28dB for the worst case.

The results show a high carrier-to-noise power ratio improvement as well as a significant advance in the ADTs state-of-art for the achievable CE. A comparison between several state-of-the-art all-digital transmitters is shown in Table I. As can be seen, the proposed transmitter with mixed-mode filtering provide a very high CE and high SNR, while improving the flexibility of ADT by removing the necessity of an output narrow-band filter.

VI. CONCLUSION

In this paper, a new filtering technique for all-digital transmitters was presented to extend their flexibility to the filtering stage. It uses signal interference to cancel the signal at the designated frequencies enabling the reduction of the quantization noise common to all-digital transmitter radios.

With the proposed filtering technique the design of the output narrow band filter can be avoided. Even more, the filtering characteristics can be easily digitally controlled to suit the transmitter carrier frequency improving the overall transmitter flexibility.

REFERENCES

[1] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital generation of RF signals for wireless communications with band-pass delta-sigma modulation," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, vol. 3, 2001, pp. 2127–2130.

[2] M. Helaoui, S. Hatami, R. Negra, and F. Ghannouchi, "A novel architecture of delta-sigma modulator enabling all-digital multiband multistandard RF transmitters design," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 11, pp. 1129–1133, 2008.

[3] N. Silva, A. Oliveira, U. Gustavsson, and N. Carvalho, "A novel all-digital multichannel multimode RF transmitter using delta-sigma modulation," *Microwave and Wireless Components Letters, IEEE*, vol. 22, no. 3, pp. 156–158, 2012.

[4] N. Silva, A. Oliveira, and N. Carvalho, "Design and optimization of flexible and coding efficient all-digital RF transmitters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, no. 1, pp. 625–632, 2013.

[5] T. Johnson and S. Stapleton, "RF class-d amplification with bandpass sigma-delta modulator drive signals," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, no. 12, pp. 2507–2520, Dec 2006.

[6] F. Ghannouchi, S. Hatami, P. Aflaki, M. Helaoui, and R. Negra, "Accurate power efficiency estimation of GHz wireless delta-sigma transmitters for different classes of switching mode power amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, no. 11, pp. 2812–2819, Nov 2010.

[7] M. Ebrahimi and M. Helaoui, "Reducing quantization noise to boost efficiency and signal bandwidth in delta sigma-based transmitters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, no. 12, pp. 4245–4251, Dec 2013.

[8] D. Barkin, A. Lin, D. Su, and B. Wooley, "A CMOS oversampling bandpass cascaded D/A converter with digital FIR and current-mode semi-digital filtering," in *VLSI Circuits, 2003. Digest of Technical Papers. 2003 Symposium on*, June 2003, pp. 79–82.

[9] S. Taleie, T. Copani, B. Bakkaloglu, and S. Kiaei, "A bandpass delta-sigma RF-DAC with embedded FIR reconstruction filter," in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, Feb 2006, pp. 2370–2379.

[10] T. Parks and J. McClellan, "Chebyshev approximation for nonrecursive digital filters with linear phase," *Circuit Theory, IEEE Transactions on*, vol. 19, no. 2, pp. 189–194, Mar 1972.

[11] R. F. Cordeiro, A. Oliveira, J. Vieira, and N. V. Silva, "Gigasample time-interleaved delta-sigma modulator for FPGA-based all-digital transmitters," *Digital System Design (DSD), 2013 Euromicro Conference on*, 2013.

[12] K. H. An, O. Lee, H. Kim, D. H. Lee, J. Han, K. S. Yang, Y. Kim, J. J. Chang, W. Woo, C.-H. Lee, H. Kim, and J. Laskar, "Power-combining transformer techniques for fully-integrated cmos power amplifiers," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 5, pp. 1064–1075, May 2008.

[13] T. Podsiadlik, J. Dooley, and R. Farrell, "Improved coding-efficiency two-level source encoder for RF switch-mode power amplifiers," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 59, no. 10, pp. 618–622, Oct 2012.

[14] S. Chung, R. Ma, S. Shinjo, H. Nakamizo, K. Parsons, and K. H. Teo, "Concurrent multiband digital outphasing transmitter architecture using multidimensional power coding," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 63, no. 2, pp. 598–613, Feb 2015.

Appendix F

Relaxing All-digital Transmitter Filtering Requirements Through Improved PWM Waveforms

R. F. Cordeiro, Arnaldo S. R. Oliveira, and José Vieira

in *2015 IEEE MTT-S International Microwave Symposium (IMS)*

DOI: 10.1109/MWSYM.2015.7166799

Relaxing All-digital Transmitter Filtering Requirements Through Improved PWM Waveforms

R. F. Cordeiro, Arnaldo S. R. Oliveira and José Vieira
Departamento de Electrónica, Telecomunicações e Informática and Instituto de Telecomunicações
Universidade de Aveiro
Campus Universitário de Santiago, Aveiro, 3810-193, Portugal
Email: ruifiel@ua.pt, arnaldo.oliveira@ua.pt, jnvieira@ua.pt

***Abstract*—This paper presents a new pulse-width modulation (PWM) technique for all-digital transmitters (ADT) that reduces the PWM harmonic distortion near the transmitted carrier frequency. This technique is used to shape the ADT's quantization noise by changing the PWM waveform patterns, avoiding the need of a high quality factor analog output filter. With this approach, the ADT gains an additional degree of flexibility for the carrier frequency since it is not bound to any fixed narrow-band filter.**

The results show the feasibility and advantages of the approach without increasing the complexity for the overall system. The noise peak power reduction shown is quite significant, reaching more than 50 dB reduction for the first PWM harmonic.

***Index Terms*—All-digital transmitter, pulse-width modulation, quantization noise.**

I. Introduction

The unprecedented growing of wireless access networks over the last years has encouraged a vast effort in the research and development of efficient and highly flexible radios. The convergence of different communication standards into a single universal radio, is not only necessary, but it is also expected to be a trend in the future. The concept of having a single radio device capable of multi-band, multi-rate and multi-standard communications using an adaptable physical layer was already suggested in [1]. However, only in recent years the technology has made the crucial advances to shorten the gap towards the ideal Software Defined Radio (SDR) system.

The development of novel all-digital transmitters (ADT) [2]–[4] poses an important step for SDR systems since it enables the transmission of radio signals using a fully digital datapath. The inherent reconfigurability in digital logic stands as a convenient feature to grant the ADT the flexibility demanded for SDR designs. However, current state-of-the-art ADTs still have fundamental limitations which restrain their proliferation as a common solution. Most of cited ADTs still have low power efficiency, do not support multiple carrier or require high quality factor output filters to remove the out-of-band noise.

A key limitation is the quantization noise introduced by most of ADTs due to the modulation techniques used to encode the signal. State-of-the-art all-digital transmitters typically use delta-sigma (DSM) or pulse-width modulation (PWM) architectures to convert the digital signal into pulses [5], [6]. While DSM applies noise shaping which reduces the quantization noise near the carrier, it doesn't allow large bandwidths due to logic clock frequency limitation [7]. On the other hand, PWM logic is fairly easier to design and implement at higher rates, but introduces high power harmonic noise near the carrier frequency. In both situations, a high quality factor filter must be used to attenuate the out-of-band quantization noise. However, introducing an analog filter reduces the flexibility of the ADT by binding the transmitter output to the filter bandwidth and central frequency.

In this paper, we propose a change to the PWM technique used in ADTs that reduces the quantization noise power near the carrier frequency. This new technique allows the reduction of the quality factor for the transmitter output filter without any change in hardware complexity when compared to conventional PWM-based ADTs.

II. All-digital transmitter architecture

This section details the FPGA-based architecture used to implement an all-digital transmitter with PWM similar to the one presented in [6]. This architecture uses PWM modulation to generate a two-level RF output. The RF transmitter prototype block diagram is shown in Fig. 1.

The baseband complex input signal is divided into In-phase (I) and Quadrature (Q) data components, respectively s_i and s_q. Because the PWM has a fixed number of levels, in this particular case 64 levels, the signal must be quantized to a signal with the same number of levels. Hence, s_i and s_q are quantized into $\hat{s}_i$ and $\hat{s}_q$ signals with $log_2(64) = 6$ bits.

The PWM is done using look-up tables (LUTs) with the associated PWM level matrix stored. Each memory line corresponds to a signal level and its output has a rectangular waveform with the respective duty-cycle width. The digital

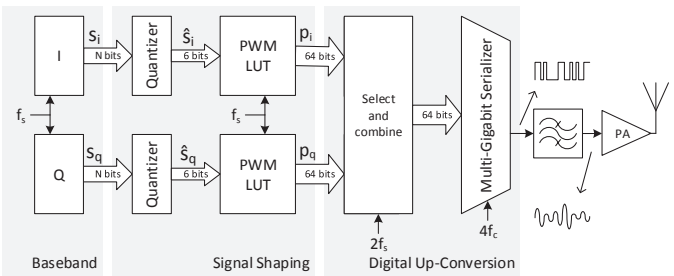


Fig. 1. FPGA-based all-digital transmitter architecture with PWM modulation.

PWM implementation forces the duty-cycle width to be discretized into possible 64 rectangular waves. The 64 bit outputs, p_i and p_q, have a duty-cycle defined by the number of '1's in the sequence.

In this architecture, the up-conversion is implemented using the select and combine block and multi-gigabit serializer (MGS). The select and combine generates a parallel vector that is the combination of p_i, p_q and their inverted versions $\overline{p}_i$ and $\overline{p}_q$. The vector is defined as a repetition of the (p_i p_q $\overline{p}_i$ $\overline{p}_q$) pattern sampled at a $4 \times f_c$ frequency. The serialization of this vector with the multi-gigabit serializer allows a high sampling frequency at the system output while maintaining a lower clock frequency, f_s, for the baseband hardware blocks. Once serialized at a frequency $4 \times f_c$, this pattern is equivalent to the multiplication of the I and Q signals with two square waves at f_c, with 90 degrees phase shift between them [3]. The ADT generated output is the baseband PWM signal up-converted to a RF carrier at f_c.

III. Pulse width modulator design

This section explains the design of the regular PWM for the used ADT architecture and the proposed improvement to the modulator. The first part focus on analysis of the regular PWM frequency response and the problems it poses for signal filtering. The second part shows the proposed improvement to the PWM method to reduce the harmonic distortion power closer to the carrier frequency.

A. Conventional PWM

The uniform-sampling PWM is a nonlinear process that modulates a signal into a pulse time span. In time, a PWM signal is a rectangular wave, as in Fig. 2, with a variable duty cycle defined as t_{on}/T.

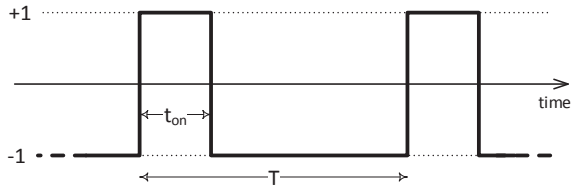


Fig. 2. Rectangular PWM wave with period T and duty cycle t_{on}/T.

Considering the PWM high oversampling ratio, we can assume that for time spans closer to the period T, the input signal $s(t)$ is constant and the waveform can be approximated by a periodic rectangular wave. This approximation is sufficient for the purposes of this work. Hence, for a normalized signal $s(t) \in [-1, +1]$, it is possible to encode it as a PWM wave with the duty cycle given by (1).

$$\frac{t_{on}}{T} = \frac{s(t)+1}{2}, \quad \frac{t_{on}}{T} \in [0,1] \tag{1}$$

PWM quantizes a continuous amplitude signal into a two-level signal, but, as a strongly nonlinear process, it introduces distortion to the signal. Assuming an high oversampling ratio, an approximation to this time wave can be described by its Fourier series approximation $p(t)$, as in (2), with the Fourier coefficients a_0, a_n and b_n given by the equations (3) and (4) respectively.

$$p(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos\left(2n\pi\frac{t}{T}\right) + b_n \sin\left(2n\pi\frac{t}{T}\right) \tag{2}$$

$$a_0 = 4\frac{t_{on}}{T} - 2; \quad a_n = \frac{2}{n\pi}\sin\left(2n\pi\frac{t_{on}}{T}\right) \tag{3}$$

$$b_n = \frac{2}{n\pi}\left(1 - \cos\left(2n\pi\frac{t_{on}}{T}\right)\right) \tag{4}$$

The solution for $p(t)$ is expressed in (5). The resulting signal is a sum of the original modulating signal $s(t)$ and amplitude and phase modulated signals centered at integer multiple frequencies of $1/T$, here defined as $n_q(t)$.

$$p(t) = \underbrace{\frac{t_{on}}{T} - 1}_{s(t)} + \underbrace{\sum_{n=1}^{\infty} \frac{4}{n\pi}\sin\left(n\pi\frac{t_{on}}{T}\right)\cos\left(2n\pi\left(\frac{t}{T} - \frac{t_{on}}{2T}\right)\right)}_{n_q(t)} \tag{5}$$

The sum of the modulated signals $n_q(t)$, can be interpreted as the PWM quantization noise. The quantization noise magnitude in the frequency domain is given by its Fourier transform as in (6).

$$N_q(f) = 4\sum_{n=1}^{\infty} \frac{4}{n\pi}\left|\sin\left(n\pi\frac{t_{on}}{T}\right)\right|\left(\delta(f - \frac{n}{T}) + \delta(f + \frac{n}{T})\right) \tag{6}$$

From (6), it is clear that the PWM quantization noise is centered around integer multiple frequencies of $1/T$, with amplitude decreasing with the harmonic index n. Therefore, the higher magnitude noise peak is located near the signal, in the first harmonic $1/T$, which makes it the most crucial and also harder harmonic peak to filter.

B. Improved PWM

Since the PWM noise power is higher for frequencies at multiples of $1/T$, it is desirable to diminish the value of T to push the noise away from the signal. This can be done increasing the sampling frequency of the PWM, however the maximum frequency is usually constrained by hardware clock limitations. Instead of increasing the sampling frequency, the rectangular wave period T can be decreased modifying the PWM waveform used to encode the signal.

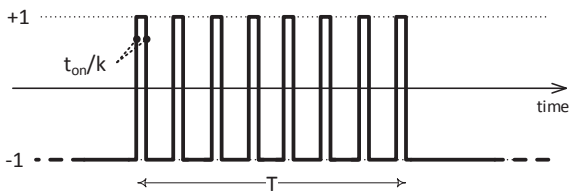


Fig. 3. Improved PWM wave with period T and duty cycle t_{on}/T, but divided into various rectangular waves to maximize the number of transitions.

The pulse width t_{on} over the period T can be divided in smaller time steps, while maintaining the relationship t_{on}/T over the period T. Fig. 3 shows the example of the conventional PWM wave presented in Fig. 2 modified accordingly to the proposed approach.

The number of rectangular pulses over the period T depends on the PWM level to be transmitted and the PWM time resolution. A PWM LUT with N levels has a minimum pulse time duration of T/N. The t_{on} value is given for the level k (where k is a N level quantized form of the signal $s(t)$ accordingly to (1)) as kT/N, assuming k is an integer from 1 to the PWM LUT size.

The improved PWM LUT in Fig. 4 b) was constructed by maximizing the number of transitions between -1 and +1 during the period T while maintaining the relation t_{on}/T. The index values that have the value +1 in the improved PWM LUT can be found using the equation (7). While the index values with amplitude -1 are the remaining $N - k$ time slots.

$$LUT^{i}_{+1} = round(\frac{N}{k} \times [1...k]) \tag{7}$$

Fig. 4 shows the differences between the regular and the proposed PWM LUT bitmaps. The gray squares represent the equivalent time slot with the value -1 and the white squares the ones with the value +1.

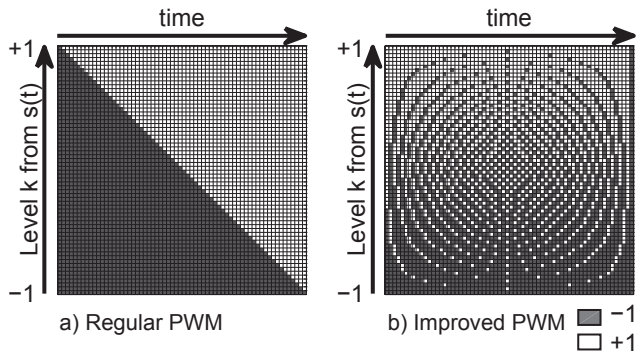


Fig. 4. PWM LUT representation. a) At the left it is presented the LUT used in the conventional uniform-sampled PWM. b) In the right, the improved LUT to reduce the harmonic distortion near the carrier frequency.

In Fig. 4 b) the time t_{on} is evenly distributed over the PWM word period. This transformation changes the rectangular wave period but keeps the PWM word energy and preserves the relation t_{on}/T over the word period. According to (5) and (6), reducing T shapes the quantization noise to higher frequencies, away from the pulse-width modulated baseband signal.

IV. Experimental Results

A proof of concept prototype was designed using the architecture presented in Fig. 1, with both the regular uniformly-sampled PWM and the proposed improved PWM. The FPGA-based ADT was implemented in a KC705 board from Xilinx with a Kintex-7 XC7K325T FPGA. The RF ADT two-level output signal was directly connected to a Vector Signal Analyzer (VSA) from Rohde & Schwarz (model FSQ 8) for signal and spectral analysis. Several baseband signals were generated using MATLAB and loaded into the FPGAs internal I and Q memories. The ADT up-conversion was set to shift the baseband signal to a 2.5 GHz carrier frequency. The maximum PWM sampling frequency achievable for a 64 bits PWM word, as in Fig. 4, is 78.125 MHz.

The measured spectrum results at the FPGA output for the regular PWM-based ADT signal and the proposed PWM are depicted in Fig. 5. The harmonic noise for the proposed method is shaped away from the carrier frequency as intended, with most of the quantization noise power concentrated in the farthest harmonics.

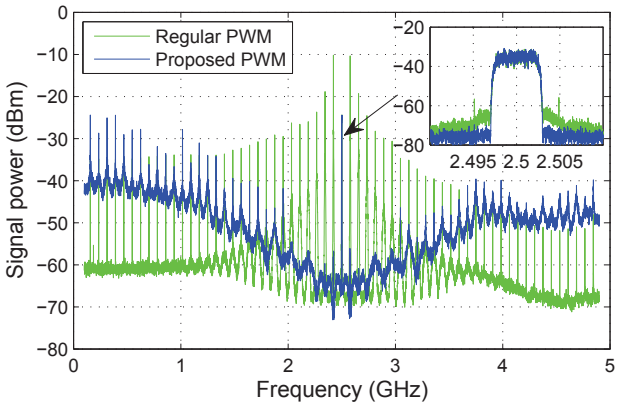


Fig. 5. Measured ADT spectrum with regular pulse-width modulation and the proposed PWM. The carrier, centered at 2.5 GHz can be viewed, in more detail in the small figure in the top right corner. Resolution bandwidth is 300kHz and video bandwidth is 3kHz.

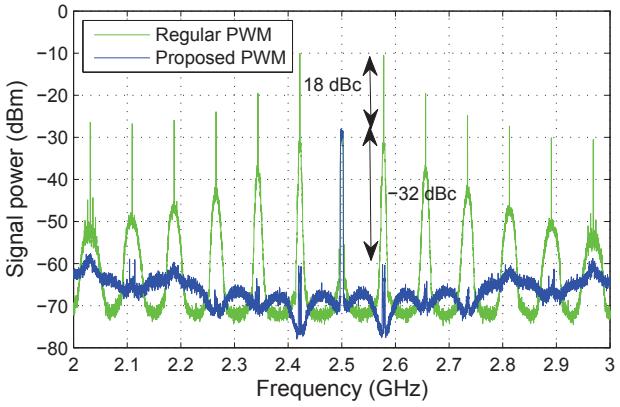


Fig. 6. Detailed view of the peak power noise from the regular PWM and the proposed PWM. Resolution bandwidth is 100kHz and video bandwidth is 10kHz.

A detailed view of the harmonic noise reduction for the twelve PWM harmonics closer to the carrier frequency is shown in Fig. 6 over a 1GHz span. It is easily observable the difference between the regular PWM and the proposed PWM spectral noise. In fact, for the presented signal, the peak noise

power for the regular PWM was 18dB above the carrier located at the first harmonic. On the other hand, with the proposed method, the peak noise power is now more than 30dB below the carrier, and its located at the sixth harmonic.

Table I shows the peak noise power reduction between regular PWM and the proposed PWM for three different QAM signals with 3 MHz, 6 MHz and 12 MHz of bandwidth at 2.5 GHz. The measured values suggest that the peak quantization noise reduction reduces as the signal bandwidth increases. However, it should be noted that the noise reduction in the first harmonic was more than 45 dB for all tested signals.

TABLE I
PWM NOISE POWER PEAK REDUCTION

		Carrier	Test Signal Bandwidth		
		Offset	3MHz	6MHz	12MHz
Lower harmonics	6th	-468.7 MHz	28.2 dB	31.2 dB	32.5 dB
	5th	-390.6 MHz	32.6 dB	32.2 dB	36.2 dB
	4th	-312.5 MHz	33.0 dB	33.7 dB	34.8 dB
	3rd	-234.3 MHz	39.3 dB	42.3 dB	39.9 dB
	2nd	-156.2 MHz	46.5 dB	44.0 dB	42.8 dB
	1st	-78.1 MHz	**51.8 dB**	**50.5 dB**	**45.5 dB**
Higher harmonics	1st	78.1 MHz	**52.1 dB**	**49.7 dB**	**45.3 dB**
	2nd	156.2 MHz	44.7 dB	44.6 dB	41.8 dB
	3rd	234.3 MHz	38.5 dB	40.7 dB	39.5 dB
	4th	312.5 MHz	30.5 dB	33.1 dB	33.8 dB
	5th	390.6 MHz	31.5 dB	31.2 dB	34.9 dB
	6th	468.7 MHz	25.5 dB	28.2 dB	30.3 dB

V. CONCLUSION

In this paper a new pulse-width modulation method for ADTs was presented. Its complexity is the same as regular PWM, but it allows to drastically reduce the harmonic quantization noise near the carrier frequency. Results show, not only the feasibility of the proposed PWM-based ADT approach, but also the reduction of the quality factor requirements for the output RF reconstruction filter.

ACKNOWLEDGMENT

This work is funded by National Funds through FCT - Fundação para a Ciência e a Tecnologia under the project PEst-OE/EEI/LA0008/2013; UID/EEA/50008/2013 and PhD scholarship SFRH/BD/91533/2012 and by the Instituto de Telecomunicações under project CReATION (ref. EXCL/EEI-TEL/0067/2012).

REFERENCES

[1] J. Mitola and G. Q. Maguire, "Cognitive radio: making software radios more personal," *Personal Communications, IEEE*, vol. 6, no. 4, pp. 13–18, Aug 1999.

[2] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital generation of RF signals for wireless communications with band-pass delta-sigma modulation," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, vol. 3, 2001, pp. 2127–2130.

[3] Z. Ye, J. Grosspietsch, and G. Memik, "An FPGA based all-digital transmitter with radio frequency output for software defined radio," in *Design, Automation Test in Europe Conference Exhibition, 2007. DATE '07*, April 2007, pp. 1–6.

[4] M. Helaoui, S. Hatami, R. Negra, and F. Ghannouchi, "A novel architecture of delta-sigma modulator enabling all-digital multiband multistandard RF transmitters design," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 11, pp. 1129–1133, 2008.

[5] F. Ghannouchi, "Power amplifier and transmitter architectures for software defined radio systems," *Circuits and Systems Magazine, IEEE*, vol. 10, no. 4, pp. 56–63, Fourthquarter 2010.

[6] N. Silva, A. Oliveira, and N. Carvalho, "Design and optimization of flexible and coding efficient all-digital RF transmitters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, no. 1, pp. 625–632, 2013.

[7] M. M. Ebrahimi, M. Helaoui, and F. Ghannouchi, "Time-interleaved delta-sigma modulator for wideband digital GHz transmitter design and SDR applications," *Progress In Electromagnetics Research B*, vol. 34, pp. 263–281, 2011.

Appendix G

All-digital Transmitter with Waveform Design for SDR

R. F. Cordeiro, Arnaldo S. R. Oliveira, and José Vieira

Paper submitted to *IEEE Transactions on Circuits and Systems - Part I: Regular Papers*

All-Digital Transmitter with Waveform Design for SDR

R. F. Cordeiro, *Student Member, IEEE*, Arnaldo S. R. Oliveira, *Member, IEEE*, J. M. N. Vieira

***Abstract*—In this paper it is presented a new all-digital transmitter architecture for software defined radio systems that is fully re-configurable by software. The proposed architecture uses direct digital radio frequency waveform design by constructing a look-up table encoding map with the radio frequency wave. This method uses a simple hardware architecture that allows changing transmitter properties, such as frequency response, bandwidth or central frequency only by changing its software algorithm.**

The design of a specific digital modulator encoded in a look-up table allows for the output of high speed binary stream that approximates a bandpass delta-sigma signal without the need of complex high frequency digital architectures. This creates a wideband quantization noise shaping that drastically reduces the need for high quality bandpass filters at the systems output resulting in reduced transmitter complexity and cost.

I. Introduction

The next generation of wireless communications is expected to exacerbate the tendency towards the digitalization of the radio transceiver, motivated by the flexibility of software defined radio (SDR) systems, which have gained a substantial importance in the design of the radio hardware for mobile communication systems [1]. Modern wireless standards using different frequencies, diverse coding and modulation schemes are already being deployed and used in many commercial applications, taking advantage of features such as frequency hoping or multi-band and multi-standard transmission. In practice, these features require the RF transceiver to have some intelligence and adapt itself to the environment or user requirements [2], [3]. Most of these capabilities are either unfeasible or too complex to implement with conventional analog RF transmitter architectures [4].

All-digital transmitters (ADT) have already shown promising results on achieving a fully digital and therefore potentially tunable or configurable architecture. However, they are yet far from the ideal SDR defined radio where the transceiver can be completely described by software and digital hardware followed by an high speed DAC as in Fig. 1. In such SDR architectures, a great processing effort is put into the digital signal processing (DSP) that must handle the high clock rates necessary to up-convert the signal to RF [5]. This is yet a significant limitation for RF SDR which transmit at GHz frequencies since digital up-conversion comes with a high energy cost for the digital datapath.

In many cases, all-digital transmitters can reduce digital logic power by employing lower resolution modulations such as delta-sigma (DSM) or pulse-width modulation (PWM) while maintaining an highly flexible hardware. Lower bit resolution at the radio output allows not only for lower power consumption of the digital hardware but also to use more efficient amplification methods such as switch-mode power amplifiers (SMPA). Although configurable, most of digital transmitters are bond to a fixed set of frequencies, modulations or transmitter behavior in terms of spectral spurious emissions and coding efficiency [6]–[9]. Nonetheless, some digital transmitters have near carrier IF control allowing the use of different channels in the same band. However, these IF frequencies are usually restricted to a small tuning bandwidth that do not exceed the tens of MHz [10], [11].

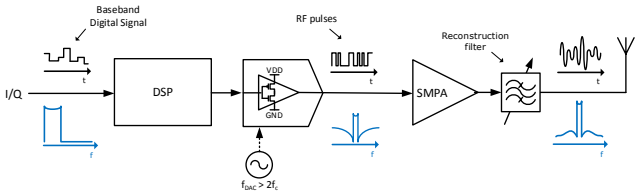


Fig. 1. Ideal all-digital SDR transmitter hardware architecture.

Although advantageous in terms of hardware simplicity, energy cost and achievable clock frequency, low resolution (particularly 2-level) digital transmitters create a substantial amount of noise. This noise, due to quantization, is a surplus of transmitted power that needs to be filtered. Most of these ADTs require a narrow-band output filter to remove the out-of-band quantization noise that often binds the transmitter output to a very strict number of carrier frequencies, limiting the overall transmitter flexibility.

Usually, most of the proposed solutions rely on the use of dedicated high speed hardware to be capable to cope with the high speed rates necessary for the GHz range RF signals. While the use of dedicated hardware solve the problem of outputting an high frequency binary stream, the generation of such stream dependent on DSM or PWM is not trivial. Usually polyphase approaches can be used but the feedback error correction limits the processing frequency to the hundreds of MHz [12], [13]. The use of high order DSM is quite limited since it relies on a complex digital circuitry with substantial datapath delays. So in most ADTs, the solution is the use of either PWM, with high harmonic power, or low order DSM with poorer noise rejection.

To overcome this problem, we propose the offline generation of binary sequences that approximate the up-conversion and DSM of the transmitted signal depending on the baseband signal. In order to do this, a novel all-digital transmitter architecture for SDR systems is proposed in this paper. This

The authors are with the Instituto de Telecomunicações, Universidade de Aveiro, Campus Universitário de Santiago, Aveiro, 3810-193, Portugal (Email: ruifiel@ua.pt, arnaldo.oliveira@ua.pt, jnvieira@ua.pt)

This work is funded by National Funds through FCT - Fundação para a Ciência e a Tecnologia under the project PEst-OE/EEI/LA0008/2013; UID/EEA/50008/2013 and PhD scholarship SFRH/BD/91533/2012 and by the Instituto de Telecomunicações under project CReATION (ref. EXCL/EEI-TEL/0067/2012).

architecture has a strong integration between hardware and software into an RF transmitter which allows for a great degree of flexibility.

The paper introduces a simplistic hardware architecture based on the original SDR approach, that together with a adaptable processing algorithm, enables the fast switching between multiple carriers. The generated RF pulse stream can be adapted not only in terms of carrier frequency but also the transmitter's frequency response, bandwidth or coding efficiency.

II. Conventional Pulse Modulation Limitations

Pulsed modulation schemes, such as delta-sigma, pulsed-width or pulse-position modulation have been used in RF to convert a signal into a constant envelope wave granting the use of highly efficient switched-mode power amplifiers (PA) [1], [14]. All these modulations share the same principle that a signal can be properly approximated by a two-level pulse sequence assuming an appropriate oversampling ratio.

Pulse modulators can be divided into two sets of systems in what concerns their memory. DSM is an infinite memory system since the signal at any point depends on all the previous inputs. This type of modulator allows for a very efficient noise shaping of the signal, particularly with lower amplitude resolutions. However, infinite memory systems must use feedback topologies of some kind which will result in slower systems. On the other hand, higher sampling rate modulations can be achieved using uniform sampling PWM mainly due to its simplicity as a memoryless system. The conversion of the baseband input signal, to a PWM modulated version, is usually much faster comparing to DSM for the same technology, which allows for higher bandwidth systems. However, without a feedback loop to shape the quantization error, the achieved SNR and the adjacent channel power ratio (ACPR) are usually worser. The choice between these two methodologies, relies on a trade-off between noise shaping, hardware complexity and maximum sampling frequency.

PWM is done with a comparison between a baseband signal and a reference wave. From the hardware point of view, this is a very simple system requiring only a digital comparator. For a fixed set of digital inputs the PWM operation can be reduced to a look-up table (LUT). For each one of the signal inputs, a memory can be addressed with the respective output PWM waveform. Although PWM can be achieved with a simple architecture, both baseband and RF PWM only allow a fixed set of carrier frequencies that depend on the sampling frequency. Additionally, PWM quantization noise is typically higher than DSM for the same signals. In fact, the quantization noise in uniform sampling PWM, not only is higher in the signal's band, but has very high distortion peaks near the carrier frequency [15]. This turns the filtering of the output signal a much harder task for the transmitter design.

On the other hand, DSM allows for a much more efficient noise shaping architecture. The DSM internal loop can be adjusted for a higher noise rejection but also for a tunable rejection band allowing a fine variation of the carrier frequency, which is not possible with PWM. In this sense, DSM

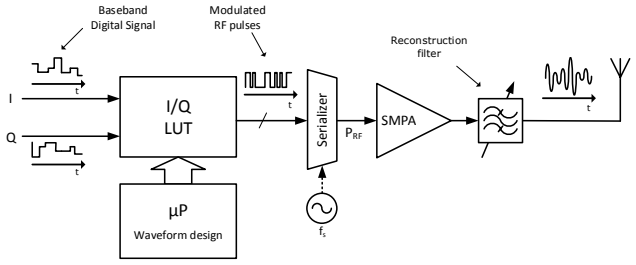


Fig. 2. Proposed all-digital SDR transmitter hardware architecture.

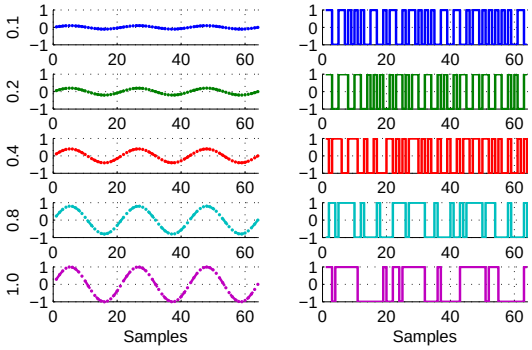


Fig. 3. Amplitude variation of the LUT input and respective 2-level output.

allows for better SNR values when compared to equivalent PWM systems at the same sampling clock and signal levels. However, the loop-back filter of the DSM comes at the cost of hardware complexity and clock frequency. In practical terms, this means that the noise shaping of the DSM is more effective but in a narrow bandwidth and bandpass DSM present low carrier frequencies.

III. RF Waveform LUT Transmitter Architecture

In this paper, we propose a system that uses fixed length two level RF pulses as the transmitter's output. The output signal is modulated by an equivalent bandpass DSM system without the physical hardware implementation of a complex bandpass DSM. To achieve this, the DSM hardware is replaced by a LUT that encodes the DSM modulation and digital up-conversion. This LUT allows for the modulation of a baseband signal into RF pulses at a specified carrier frequency.

The proposed LUT system architecture is presented in Fig. 2. This architecture is quite trivial, being composed only by a memory based LUT, a micro processor and a high speed digital serializer. The memory has stored the RF pulses correspondent to each combination of the digital IQ baseband samples. The baseband signal is converted to a LUT address, hence for every combination of IQ samples there is an equivalent RF output represented in the LUT memory. An example of this is shown in Fig. 3 where, at the left, it is presented the multi-level waveform that corresponds to a certain amplitude and, at the right, the equivalent pulse based RF output.

The RF pulses of the LUT are computed in the micro processor by a pre-determined algorithm. This algorithm runs

before transmission for a set of parameters and stores the RF pulses into a RAM memory that will act as LUT. During transmission, the baseband signal addresses the LUT entries accordingly to the in-phase (I) and quadrature (Q) samples. For each I/Q signal pair, a RF wave is extracted from the LUT and used as the output signal, with the specified signal coding, output frequency and noise shaping. Assuming a certain oversampling ratio (OSR) for the input signal, the baseband samples will modulate the up-converted wave signal at the output of the system.

The main novelty of this work is the use of a RF waveform look-up table to modulate the bandpass DSM waveform at a high sampling rate. This is a resource efficient approximation of a bandpass DSM at high frequency and therefore the LUT behavior as a modulator is not ideal in comparison with real-time DSM. The following subsections describe further details about the synthesis and analysis of the LUT waveforms.

A. Look-up table generation algorithm

The generation of the waveform LUT is done in the micro-processor prior to signal transmission. To complete the LUT, the algorithm performs a small simulation of the DSM output for all the possible digital IQ sample pairs. For each specified carrier frequency, f_c, the algorithm must used in order to generate the correspondent LUT. This means that the difference between different carrier frequencies relies in a software operation instead of a change or reconfiguration of hardware parameters. Moreover, the time spent in the LUT generation does not affect the modulation and up-conversion times during signal transmission. Since the LUT is fixed after the initial generation, the complexity of the modulation doesn't add any delay to the signal conversion.

The RF pulses are computed accordingly to the following algorithm:

- Find the quantized amplitude values I_q and Q_q for the N quantized levels of the I and Q signals.
- Compute the complex carrier wave, CW, for the corresponding carrier frequency f_c with M samples.

$$CW_i(n) = \cos\left(2\pi\frac{fc}{fs}n\right); \quad CW_q(n) = \sin\left(2\pi\frac{fc}{fs}n\right); \tag{1}$$

- Compute RF wave for specific amplitudes considering I_q and Q_q constant during M samples.

$$S_{RF}(n) = I_q \times CW_i(n) + Q_q \times CW_q(n); \tag{2}$$

- Convert the RF signal to pulsed a RF representation using delta-sigma modulation.

$$P_{RF}(n) = DSM(S_{RF}(n)); \tag{3}$$

- Store RF wave in LUT memory.

$$LUT(I_q, Q_q, n) = P_{RF}(n); \quad n \in \{0; 1; \dots; M-1\} \tag{4}$$

Once the algorithm runs for all the $[I_k; Q_k]$ pairs, the LUT contains the necessary information to convert the signal to the specified carrier frequency f_c. Fig. 3 shows five examples of LUT entries and their respective output waveform. The example uses a 64 sample binary RF wave per baseband input sample for the signal amplitudes of 0.1, 0.2, 0.4, 0.8 and 1.0.

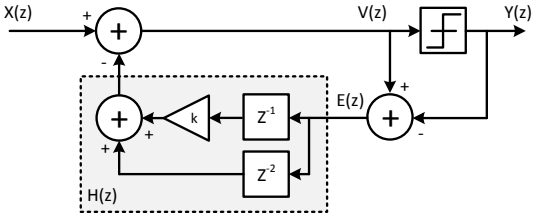


Fig. 4. DSM feedback loop architecture.

B. Modulator Topology

Delta-sigma modulation is already a well known technique and has already been used in RF transmitters as a purely digital RF DAC. One of the main limitations of DSM in RF is the sampling frequency limitations imposed by most of modulator architectures. The existence of a feedback loop in the DSM effectively limits the achievable bandwidth for an RF transmitter because it increases the critical path delay. The limitation comes from the fact that DSM loops need previous samples to compute the next output level.

While there are many different architectures, from the functional point of view most of DSM loops can be simplified to the system presented in Fig. 4. The input, $X(z)$, is quantized to the output, $Y(z)$, directly while the feedback quantization error, $E(z)$, is filtered by the loop filter, $H(z)$, and is fed back to be subtracted to the input signal. The final output signal will be a combination of the original input signal and a filtered error component as shown in (5) and (6). Where $NTF(z)$ is the noise transfer function of the DSM which shapes the quantization noise.

$$Y(z) = X(z) - \underbrace{(1 + H(z))}_{NTF(z)} E(z) \tag{5}$$

$$H(z) = NTF(z) - 1 \tag{6}$$

Since it is impossible to process the loop filter, $H(z)$, in a infinitesimal small amount of time, the overall DSM has a maximum operation frequency. Higher loop filter order is desired since it allows for better in-band noise rejection and noise shaping, but will also increase digital hardware complexity and therefore decrease the maximum operation frequency. Depending on the filter complexity, this is usually well below GHz speeds which constrains the use direct RF DSM. The use of polyphase approaches has been used to improve the sampling frequency and therefore the achievable bandwidth. However, even these approaches, do not scale properly with the number of parallel phases and have critical path delay problems as single phase DSM [12].

Using the proposed architecture, some of DSM limitations at RF speeds can be ignored since the modulation output is

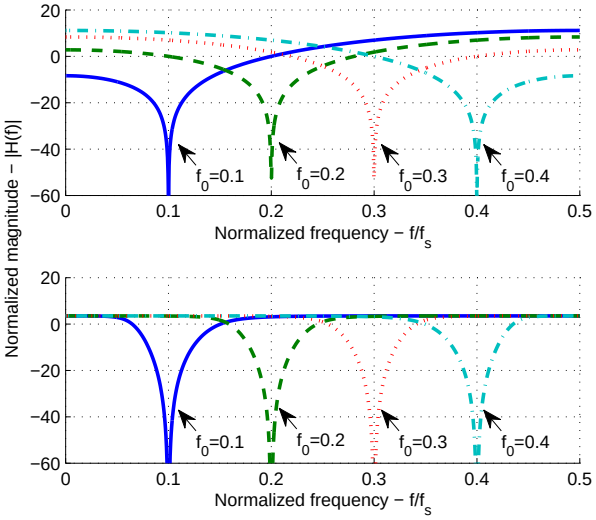


Fig. 5. Different NTF frequency responses of a tunable bandpass DSM. On top the NTF functions are design using transfer functions only with zeros. On the bottom plots poles are inserted to flatten the passbands.

found offline using the software processing algorithm and not in a real time system. Considering this, one can have a LUT that is equivalent to a high speed bandpass DSM independently of the complexity of the loop filter.

Fig. 4 shows the $H(z)$ filter for a simple bandpass NTF implementation, composed by two delays and a constant k. The $H(z)$ filter response is given by (7)

$$H(z) = kz^{-1} + z^{-2} \tag{7}$$

Assuming both (6) and (7), the NTF filter response results in (8).

$$NTF(z) = 1 + kz^{-1} + z^{-2} \tag{8}$$

The $NTF(z)$ is a filter with two complex conjugated zeros defined by the variable k. Solving for its Fourier transform, the frequency response is as shown in (9).

$$NTF(f) = NTF(e^{j2\pi}) = 1 + ke^{-j2\pi} + e^{-j2\pi\times 2} \tag{9}$$

In (9) the $NTF(f)$ zeros depend on k according to (10) where f_0 is the normalized frequency location for the NTF response zero.

$$k = -2\cos(2\pi f_0);\, f_0 \in [0; 0.5] \tag{10}$$

Knowing this, the DSM's NTF response can be changed for a specific frequency band as an tunable bandpass converter. Fig. 5 shows the NTF frequency response for different f_0 values creating different zeros with the change of the loop filter $H(z)$. The top plot displays the NTF that corresponds to (8) with k given by (10). More complex transfer functions can be used for $H(z)$ using infinite impulse response filters. Adding poles to $H(z)$ allows to flatten the $NTF(z)$ passbands and

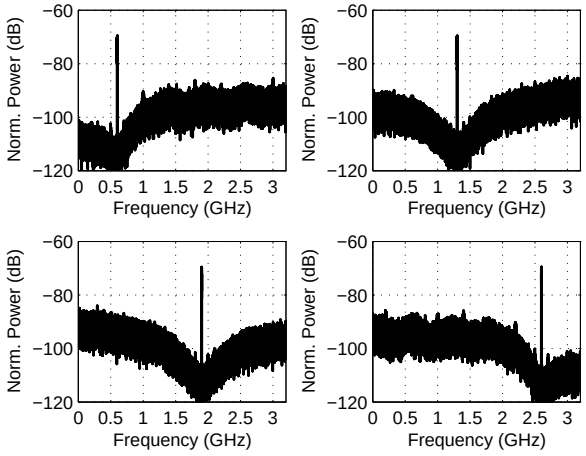


Fig. 6. Simulation of the output spectrum of the proposed LUT-based transmitter using the complex conjugated zeros NTF presented in (9).

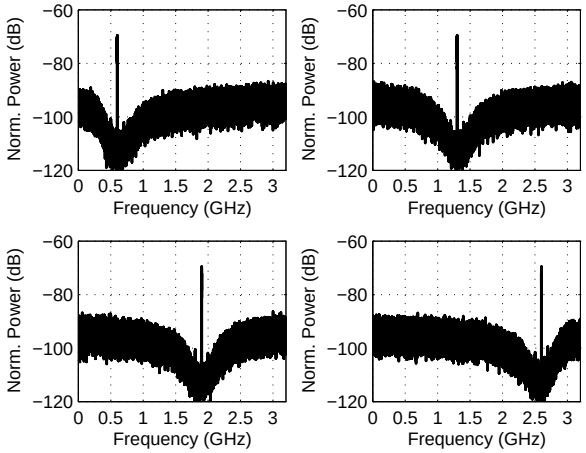


Fig. 7. Simulation of the output spectrum of the proposed LUT-based transmitter using a Chebyshev NTF filter.

uniformize the noise distribution around the carrier frequency. Fig. 5 shows some examples of possible DSM NTF with only zeros (top plot) and zeros and poles, using Chebyshev filters (bottom plot), for different central frequencies. Usually, complex NTF, with both zeros and poles require higher hardware complexity and therefore higher logic delay datapaths that will decrease the achievable logic frequency. However, using this system's LUT, this limitation does not exist since the complexity of the transfer function $H(z)$ does not interfere with the LUT signal modulation time.

Both the single zero and the Chebyshev NTFs were tested tested in a simulation of the full LUT radio architecture. In Fig. 6 the simulation results of the output RF signal are shown for different frequencies. Notice that the DSM zero changes between LUT algorithm runs to tune the zero the the appropriate signal passing band. In Fig. 6 however, there seems to be some out-of-band spurious emissions from the DSM. This is caused by the loop filter gain of the modulator that might cause some instability outside the signal's band.

To overcome this, in Fig. 7 it is shown the same system,

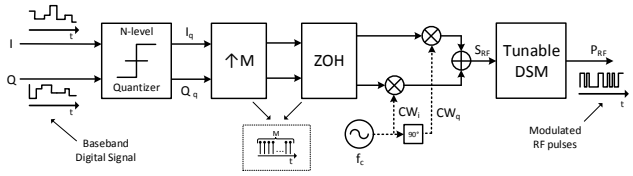


Fig. 8. Equivalent signal processing system for the proposed hardware architecture in Fig. 2 using the proposed LUT generation algorithm.

with exactly the same hardware complexity, but now using Chebyshev filter in the LUT generation algorithm. Since Chebyshev filter structure uses both zeros and poles, it is possible to control the gain of the NTF filter outside the signal's bandwidth. This eliminates the spurious emissions of the transmitter since it stabilizes the DSM loop.

Using tunable bandpass DSM it is possible to design a variable frequency DSM-based all-digital transmitter. The carrier frequency should be on the NTF zero of the bandpass DSM. In this sense, it becomes possible to output a bi-level signal centered at a desired carrier frequency between DC and $f_s/2$.

C. Look-up table model

The use of the LUT as a signal modulator is an approximation of the real DSM modulation and therefore there will be some signal degradation when compared to the ideal high speed DSM modulation. The DSM process can be viewed as a quantization in amplitude. However in this system, besides quantization there is still an approximation of a infinite length pulse to a fixed length. This process is equivalent to system presented in Fig. 8. It is important to notice that the system in Fig. 8 is not directly implemented in the hardware but is an equivalent description of the process done in the LUT generation algorithm.

First there is a quantization of the baseband signal to a specified number of levels N. The quantization happens because the resolution of the digital system is finite and also, the modulation LUT size is largely defined by this value. In fact, the number of LUT entries is equal to $N \times N$ since the quantization enforces N levels for both the I and Q samples. This quantization factor, N, will mainly define the achievable SNR for the transmitter even considering the ideal case. In fact, the maximum SNR of a quantized signal depends on N accordingly to (11):

$$SNR_{dB} = \underbrace{20\log(N)}_{quantization} + 1.76 + \underbrace{10\log\left(\frac{f_{bb}}{2BW}\right)}_{process\ gain} \qquad (11)$$

In (11), the SNR depends on the number of levels N but also on other factor that is the process gain. Since the baseband sampling, f_{bb}, is considerably higher than the signal's bandwidth BW, the baseband signal already has a considerable OSR. This excess in sampling will spread the quantization noise evenly in the entire sampling spectrum, slightly reducing the noise power in the signal's bandwidth.

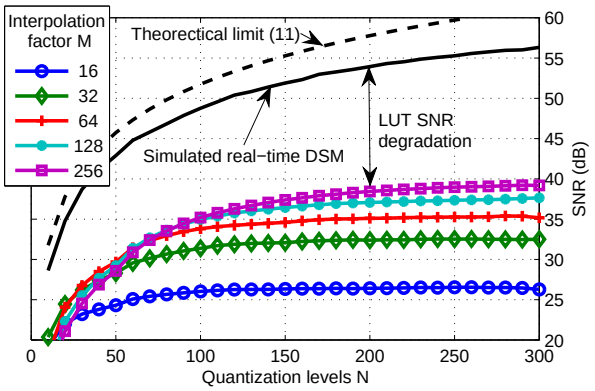


Fig. 9. Variation of the proposed transmitter SNR for a 5 MHz signal depending on the LUT size in terms of the factors N and M (system simulation results).

After quantization the signal must be interpolated up to an higher sampling rate, $f_s = M \times f_{bb}$, to allow for direct digital RF up-conversion. This interpolation happens by considering that the baseband signal is constant during M samples at higher sampling rate. The equivalent signal processing scheme is a interpolation block followed by a zero order hold (ZOH) filtering. The size M will influence the RF wave size in samples at the output, for larger values of M the wave will last longer and will be a better approximation of the RF signal with I and Q input samples. However, larger interpolation factors M imply longer time periods with constant I and Q values, which restrains the bandwidth of the baseband signal.

Following the interpolation stage and the ZOH filtering, the signal is up-converted using a quadrature digital up-conversion scheme using the algorithm operation shown in (2). The signal at this point, S_{RF}, is a multilevel signal at RF. For the conversion to analog to happen without the use of a conventional DAC, the multilevel signal should be converted to two levels. The DSM converts the multilevel signal to a binary signal at f_s. After this conversion the LUT can be stored in a $N \times N \times M$ memory to be addressed by the input signal.

There must be a trade-off between the LUT size, signal bandwidth and the values N and M. The implications of these constants choice will be crucial for the quality of the generated RF signal, particularly in terms of SNR as seen in Fig. 9. This figure shows the variation of signal SNR in dB for a set of N and M values with the proposed transmitter architecture. The dashed plot shows the theoretical SNR limit for the specified number of N levels considering the equation in (11) for a 5 MHz tone sampled at 100 MHz. The black plot below corresponds to a real-time DSM simulation of a 5 MHz bandwidth signal with a sampling frequency of f_s.

In the proposed system simulations, the hardware is considered ideal and only the variation with the values N and M is analyzed. The number of quantization levels analyzed varies from 10 up to 300 levels with a step of 10, and tested for sizes M that were powers of 2, from 16 up to 256. As it possible to see in Fig. 9, the values of N and M largely influence the achievable SNR. Using this data it is possible to choose the necessary dimensions for the LUT for the needed

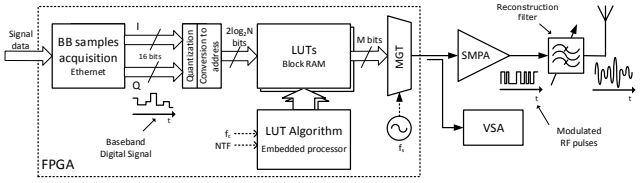


Fig. 10. FPGA-based prototype hardware architecture of the proposed transmitter.

signal quality.

IV. Hardware implementation

The proposed transmitter architecture was implemented on an FPGA circuit as depicted in Fig. 10. The input baseband complex signal is received trough an Ethernet connection in the form of IQ samples. The sampling frequency of the baseband signal, f_{bb}, is defined by the output circuit frequency, f_s, and the interpolation factor, M, such that $f_{bb} = f_s/M$. This frequency value remains constant independently of the input signal or carrier frequency.

The input signal resolution is originally 16 bits, but it must be quantized to the appropriate number of levels to be considered in the LUT. The number of levels for each I and Q signals is equal to the number of LUT entries N for the real and imaginary components of the signal, hence the number of bits for each I and Q datapath is $log_2(N)$. The concatenation of the quantized I and Q samples will become an index that will address the LUT block RAM (BRAM) memory to the appropriate RF wave for those IQ samples.

The output of the LUT table is a binary RF wave, stored as 0's and 1's in the BRAM. The level 0 corresponds to an output low voltage level and the 1 to a high level. However, this wave is read in parallel as a length M vector at a sampling f_{bb}. To be an RF signal, the parallel vector is serialized using an embedded multi-gigabit transceiver (MGT). The MGT serializes the LUT vector and at its output, and therefore the FPGA, we have a binary signal with the wave from the LUT sampled at f_s.

The LUT table is calculated using an embedded FPGA processor using the previously specified algorithm. The processor works at clocking speed of 100 MHz since the LUT computation is not a critical process. With the growing size of the LUT dimensions, the algorithm duration will increase and higher clock frequency might be used for the processor. In fact, the duration increases with a linear factor of M and a quadratic factor of N. However, for the used values of M and N, the LUT generation period is below 1 second which is more than reasonable for a initial transmitter configuration. In order for the system to be viable for frequency hoping scenarios, where the carrier frequency of the transmitter must be quickly changed, a second LUT was added. For fast switching between different carriers, the second LUT with a different carrier frequency can be used to switch between carriers in single clock cycle, which corresponds to 10 ns.

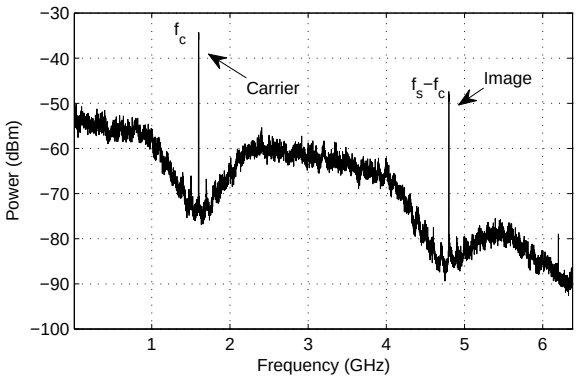


Fig. 11. Transmitted frequency spectrum of the proposed all-digital transmitter. It is shown a 6.4 GHz span with 10 kHz resolution bandwidth and 40 kHz video bandwidth.

V. Experimental setup and measurements

A laboratory prototype implemented as a proof of concept for the proposed system is shown on Fig. 10. The ADT was implemented using a KC705 board from Xilinx with a Kintex-7 XC7K325T FPGA.

The output sampling, defined by the MGT, was set to 6.4 Gsps making the maximum achievable carrier frequency 3.2 GHz. DSM noise shaping will by similar to a modulator working at a 6.4 GHz clock. The parallel input of the MGT, correspondent to the wave size M was set to 64, which implies that the f_{bb} is 100 MHz. For the specified value of M, the choosen value N was such that it would be possible to have SNR values between 33 dB and 35 dB. Using the data in Fig. 9, this would correspond to a LUT size of $N \approx 100$. The chosen value was $N = 128$ because it is a power of 2 allowing for the full use of the 7 bits in the input signals and simplifying the quantization process with a simple truncation.

Several baseband signals were created, pre-processed using MATLAB and loaded into the FPGA internal memory. The generated signals were QPSK, 16-QAM and 64-QAM modulated signals at a data rate of 5 Msps, which corresponds to a 6.1 MHz bandwidth signal.

The RF ADT 2-level output signal was connected to a Vector Signal Analyzer (VSA) from Rohde & Schwarz (model FSW 8) for signal and spectral analysis as shown in Fig. 10. An example of the transmitted output spectrum is shown on Fig. 11 the complete spectrum from DC up to 6.4 GHz is shown. It is possible to see the image of carrier as a result of the sampling function. The same signal, a 16-QAM, is shown in a smaller span around the carrier in Fig. 12. In this figure, it is also shown the received signal in the VSA with QAM constellation being easily perceivable.

Different carrier frequencies were tested to test the versatility of the LUT generation algorithm. In Fig. 13 four different carrier frequencies which correspond to four different algorithm runs are shown. The plotted spectra have 1 GHz span around the center frequencies of 0.9 GHz, 1.6 GHz, 2.4 GHz and 2.8 GHz.

Different carrier frequencies show distinct power levels between because of the non-return-to-zero sampling at the

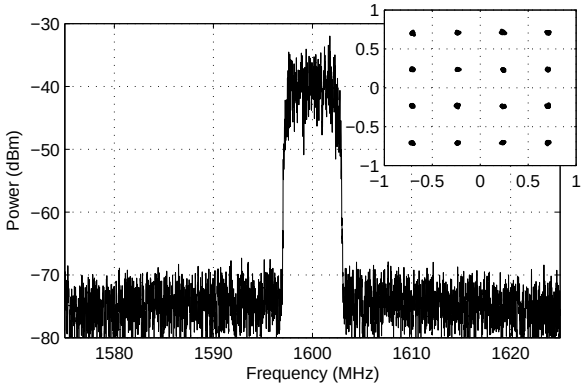


Fig. 12. Frequency spectrum of the 5 Msps 16-QAM transmitted signal. The signal center frequency is 1600 MHz, shown in a 50 MHz span plot with 20 kHz resolution bandwidth and 10 kHz video bandwidth. On the right upper corner it is presented the constellation of the demodulated signal.

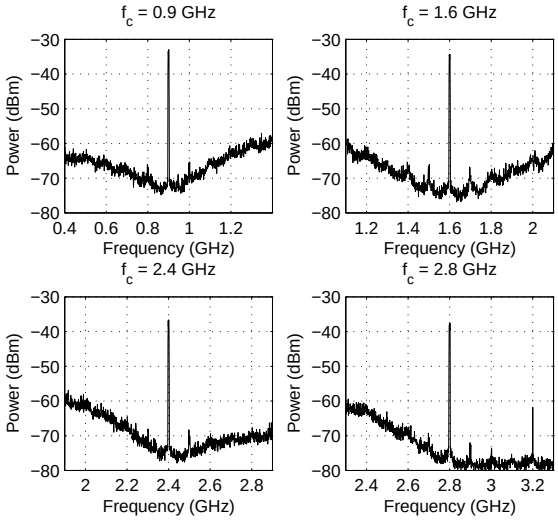


Fig. 13. Multiple captured spectra of the proposed transmitter output using different carrier frequencies f_c.

output of the FPGA making the output attenuated in frequency by the $sinc(x)$ function. This power attenuation will also have impact in the measured SNR as it will degrade the SNR for higher carrier frequencies.

To analyze the transmitted signal quality over the transmitter bands, a measurement sweep with 5 Msps signal was made for different frequencies. Fig. 14 and 15 show, respectively, the sweeps of SNR and EVM measurements, for frequencies between 400 MHz and 3100 MHz with a 100 MHz step. The measured SNR values were obtained using the VSA and are relative to the demodulated QAM constellation as in the example on Fig. 12. As it is possible to see, there is a small decrease in the SNR as the frequency becomes higher, explained by the decrease in power produced by the $sinc(x)$ attenuation.

From the presented results it is shown that for the tested signals, the achievable SNR is always above 30dB for all the modulations used and for any frequency tested between 400 MHz and 3.1 GHz. This shows the feasibility of the

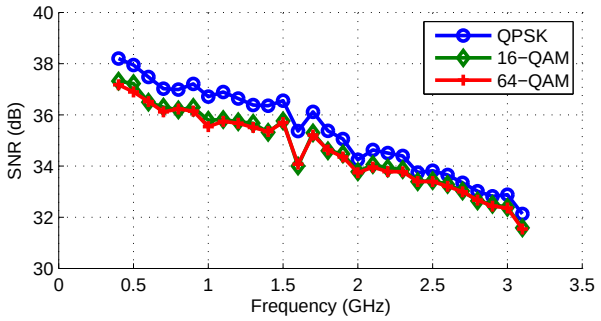


Fig. 14. Measured SNR sweep for the tested carrier frequencies.

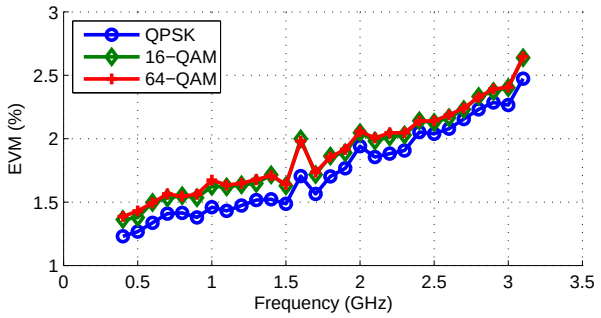


Fig. 15. Measured EVM sweep for the tested carrier frequencies.

proposed architecture as a SDR capable of fast changing its carrier frequency (in 10 ns) and signal shaping only using a different software algorithm.

VI. Conclusion

In this paper a new LUT-based transmitter architecture was shown and tested. The proposed transmitter is a result of a simple hardware architecture that matches the ideal SDR architecture with a software algorithm that creates the specified RF wave through a limited set of computations.

The advantages of this transmitter mainly rely on its simplicity and the flexible manner how transmitter properties, such as noise shaping or carrier frequency can be changed. In the presented paper, the functionality of these characteristics was shown and it was proved the feasibility of this transmitter for a wide range of carrier frequencies.

References

[1] F. Ghannouchi, "Power amplifier and transmitter architectures for software defined radio systems," *Circuits and Systems Magazine, IEEE*, vol. 10, no. 4, pp. 56–63, Fourthquarter 2010.

[2] J. Andrews, S. Buzzi, W. Choi, S. Hanly, A. Lozano, A. Soong, and J. Zhang, "What will 5G Be?,"

[3] S. Haykin, "Cognitive radio: brain-empowered wireless communications," *IEEE Journal on Selected Areas in Communications*, vol. 23, no. 2, pp. 201–220, Feb 2005.

[4] S. Balasubramanian, S. Boumaiza, H. Sarbishaei, T. Quach, P. Orlando, J. Volakis, G. Creech, J. Wilson, and W. Khalil, "Ultimate transmission," *Microwave Magazine, IEEE*, vol. 13, no. 1, pp. 64–82, Jan 2012.

[5] S. Balasubramanian, G. Creech, J. Wilson, S. M. Yoder, J. J. McCue, M. Verhelst, and W. Khalil, "Systematic analysis of interleaved Digital-to-Analog converters," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 58, no. 12, pp. 882–886, 2011.

[6] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital generation of RF signals for wireless communications with band-pass delta-sigma modulation," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, vol. 3, 2001, pp. 2127–2130.

[7] U. Gustavsson, T. Eriksson, H. Nemati, P. Saad, P. Singerl, and C. Fager, "An RF carrier bursting system using partial quantization noise cancellation," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, no. 3, pp. 515–528, March 2012.

[8] C. Haslach, D. Markert, A. Frotzscher, and A. Pascht, "New efficient architectures for RF pulse width modulators," in *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, June 2013, pp. 1–4.

[9] S. Chung, R. Ma, S. Shinjo, H. Nakamizo, K. Parsons, and K. H. Teo, "Concurrent multiband digital outphasing transmitter architecture using multidimensional power coding," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 63, no. 2, pp. 598–613, Feb 2015.

[10] A. Frappe, A. Flament, B. Stefanelli, A. Kaiser, and A. Cathelin, "An All-Digital RF signal generator using High-Speed Delta-Sigma modulators," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 10, pp. 2722–2732, Oct 2009.

[11] N. Silva, A. Oliveira, and N. Borges Carvalho, "Novel fine tunable multichannel all-digital transmitter," in *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, June 2013, pp. 1–3.

[12] R. F. Cordeiro, A. Oliveira, J. Vieira, and N. V. Silva, "Gigasample Time-Interleaved Delta-Sigma modulator for FPGA-based all-digital transmitters," *Digital System Design (DSD), 2013 Euromicro Conference on*, 2013.

[13] M. M. Ebrahimi, M. Helaoui, and F. Ghannouchi, "Time-Interleaved Delta-Sigma modulator for wideband digital GHz transmitter design and SDR applications," *Progress In Electromagnetics Research B*, vol. 34, pp. 263–281, 2011.

[14] T. Johnson and S. Stapleton, "RF Class-D amplification with bandpass Sigma-Delta modulator drive signals," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, no. 12, pp. 2507–2520, Dec 2006.

[15] Z. Song and D. V. Sarwate, "The frequency spectrum of pulse width modulated signals," *Signal Processing*, vol. 83, no. 10, pp. 2227 – 2258, 2003.

Bibliography

[ABC+14] J.G. Andrews, S. Buzzi, Wan Choi, S.V. Hanly, A. Lozano, A.C.K. Soong, and J.C. Zhang. What will 5G be? *Selected Areas in Communications, IEEE Journal on*, 32(6):1065–1082, June 2014.

[BBS+12] S. Balasubramanian, S. Boumaiza, Hassan Sarbishaei, T. Quach, P. Orlando, J. Volakis, G. Creech, J. Wilson, and W. Khalil. Ultimate transmission. *Microwave Magazine, IEEE*, 13(1):64–82, Jan 2012.

[BCW+11] S. Balasubramanian, G. Creech, J. Wilson, S. M. Yoder, J. J. McCue, M. Verhelst, and W. Khalil. Systematic analysis of interleaved digital-to-analog converters. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 58(12):882–886, 2011.

[BMK+11] Z. Boos, A. Menkhoff, F. Kuttner, M. Schimper, J. Moreira, H. Geltinger, T. Gossmann, P. Pfann, A. Belitzer, and T. Bauernfeind. A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, pages 376–378, Feb 2011.

[CHV13] Shuli Chi, K. Hausmair, and C. Vogel. Coding efficiency of bandlimited PWM based burst-mode RF transmitters. In *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on*, pages 2263–2266, May 2013.

[CMS+15] SungWon Chung, Rui Ma, S. Shinjo, H. Nakamizo, K. Parsons, and Koon Hoo Teo. Concurrent multiband digital outphasing transmitter architecture using multidimensional power coding. *Microwave Theory and Techniques, IEEE Transactions on*, 63(2):598–613, Feb 2015.

[CMST15] SungWon Chung, Rui Ma, S. Shinjo, and K.H. Teo. Inter-band carrier aggregation digital transmitter architecture with concurrent multi-band delta-sigma modulation using out-of-band noise cancellation. In *Microwave Symposium (IMS), 2015 IEEE MTT-S International*, pages 1–4, May 2015.

[COVS13] Rui F. Cordeiro, A.S.R. Oliveira, José Vieira, and Nelson V. Silva. Gigasample time-interleaved delta-sigma modulator for FPGA-based all-digital transmitters. *Digital System Design (DSD), 2013 Euromicro Conference on*, 2013.

[CRJZ11] Jian Chen, Liang Rong, F. Jonsson, and Li-Rong Zheng. All-digital transmitter based on ADPLL and phase synchronized delta sigma modulator. In *Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE*, pages 1–4, June 2011.

[CSV11] Shuli Chi, P. Singerl, and C. Vogel. Coding efficiency optimization for multilevel PWM based switched-mode RF transmitters. In *Circuits and Systems (MWSCAS), 2011 IEEE 54th International Midwest Symposium on*, pages 1–4, Aug 2011.

[CVS10] Shuli Chi, C. Vogel, and P. Singerl. The frequency spectrum of polar modulated PWM signals and the image problem. In *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on*, pages 679–682, Dec 2010.

[EH13] M.M. Ebrahimi and M. Helaoui. Reducing quantization noise to boost efficiency and signal bandwidth in delta sigma-based transmitters. *Microwave Theory and Techniques, IEEE Transactions on*, 61(12):4245–4251, Dec 2013.

[EHG09] M.M. Ebrahimi, M. Helaoui, and F.M. Ghannouchi. Efficiency enhancement of a WiMAX switching mode GaN power amplifier through layout optimization of distributed harmonic matching networks. In *Microwave Conference, 2009. EuMC 2009. European*, pages 1732–1735, Sept 2009.

[EHG11] M. M. Ebrahimi, M. Helaoui, and F. Ghannouchi. Time-interleaved delta-sigma modulator for wideband digital GHz transmitter design and SDR applications. *Progress In Electromagnetics Research B*, 34:263–281, 2011.

[EHG13] M.M. Ebrahimi, M. Helaoui, and F.M. Ghannouchi. Delta-sigma-based transmitters: Advantages and disadvantages. *Microwave Magazine, IEEE*, 14(1):68–78, 2013.

[EKR+11] M. Eron, Bumman Kim, F. Raab, R. Caverly, and J. Staudinger. The head of the class. *Microwave Magazine, IEEE*, 12(7):S16–S33, Dec 2011.

[FFS+08] A. Frappe, A. Flament, B. Stefanelli, A. Cathelin, and A. Kaiser. All-digital RF signal generation for software defined radio. In *Circuits and Systems for Communications, 2008. ECCSC 2008. 4th European Conference on*, pages 236–239, July 2008.

[GEN+12] U. Gustavsson, T. Eriksson, H.M. Nemati, P. Saad, P. Singerl, and C. Fager. An RF carrier bursting system using partial quantization noise cancellation. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 59(3):515–528, March 2012.

[Gha10a] F.M. Ghannouchi. Power amplifier and transmitter architectures for software defined radio systems. *Circuits and Systems Magazine, IEEE*, 10(4):56–63, Fourthquarter 2010.

[GHA+10b] F.M. Ghannouchi, S. Hatami, P. Aflaki, M. Helaoui, and R. Negra. Accurate power efficiency estimation of GHz wireless delta-sigma transmitters for different classes of switching mode power amplifiers. *Microwave Theory and Techniques, IEEE Transactions on*, 58(11):2812–2819, Nov 2010.

[HHGP13] S. Hatami, M. Helaoui, F.M. Ghannouchi, and M. Pedram. Single-bit pseudoparallel processing low-oversampling delta–sigma modulator suitable for SDR wireless transmitters. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, PP(99):1–1, 2013.

[HHNG08] M. Helaoui, S. Hatami, R. Negra, and F.M. Ghannouchi. A novel architecture of delta-sigma modulator enabling all-digital multiband multistandard RF transmitters design. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 55(11):1129–1133, 2008.

[HMFP13] C. Haslach, D. Markert, A. Frotzscher, and A. Pascht. New efficient architectures for RF pulse width modulators. In *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, pages 1–4, June 2013.

[JCOC16] W. Jang, R. Cordeiro, A. Oliveira, and N. B. Carvalho. A broadband almost-digital RF transmitter with an efficient power amplifier. *IEEE Transactions on Microwave Theory and Techniques*, 64(5):1526–1534, May 2016.

[JS06] T. Johnson and S.P. Stapleton. RF Class-D amplification with bandpass sigma-delta modulator drive signals. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 53(12):2507–2520, Dec 2006.

[JS07] A. Jerng and C. G. Sodini. A wideband $\Delta\Sigma$ digital-RF modulator for high data rate transmitters. *IEEE Journal of Solid-State Circuits*, 42(8):1710–1722, Aug 2007.

[JS08] T. Johnson and S.P. Stapleton. Comparison of bandpass sigma-delta modulator coding efficiency with a periodic signal model. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 55(11):3763–3775, Dec 2008.

[KHM+01] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck. Digital generation of RF signals for wireless communications with band-pass delta-sigma modulation. In *Microwave Symposium Digest, 2001 IEEE MTT-S International*, volume 3, pages 2127–2130, 2001.

[KI10] T. Kitayabu and H. Ishikawa. Generalized architecture of concurrent dual-band transmitter for spectrum aggregation system. In *Personal Indoor and Mobile Radio Communications (PIMRC), 2010 IEEE 21st International Symposium on*, pages 111–116, Sept 2010.

[Mal07] Franco Maloberti. *Data Converters*. Springer US, 2007.

[MFK17] R. C. Marin, A. Frappé, and A. Kaiser. Digital complex delta-sigma modulators with highly configurable notches for multi-standard coexistence in wireless transmitters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, PP(99):1–10, 2017.

[MHFP12] D. Markert, C. Haslach, G. Fischer, and A. Pascht. Coding efficiency of RF pulse-width-modulation for mobile communications. In *Signals, Systems, and Electronics (ISSSE), 2012 International Symposium on*, pages 1–5, Oct 2012.

[MHH+14] D. Markert, C. Haslach, H. Heimpel, A. Pascht, and G. Fischer. Phase-modulated DSM-PWM hybrids with pulse length restriction for switch-mode power amplifiers. In *Microwave Conference (EuMC), 2014 44th European*, pages 1364–1367, Oct 2014.

[MHL+13] D. Markert, C. Haslach, G. Luz, G. Fischer, and A. Pascht. Wideband measurements and linearization of a simplified architecture for analog RF-PWM. In *Microwave Conference (EuMC), 2013 European*, pages 716–719, Oct 2013.

[Mit93] III Mitola, J. Software radios: Survey, critical evaluation and future directions. *Aerospace and Electronic Systems Magazine, IEEE*, 8(4):25–36, April 1993.

[MTKS13] T. Maehata, K. Totani, S. Kameda, and N. Suematsu. Concurrent dual-band 1-bit digital transmitter using band-pass delta-sigma modulator. In *Microwave Integrated Circuits Conference (EuMIC), 2013 European*, pages 552–555, Oct 2013.

[NFDR12] P.A.J. Nuyts, B. Francois, W. Dehaene, and P. Reynaert. A CMOS burst-mode transmitter with Watt-level RF PA and flexible fully digital front-end. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 59(10):613–617, Oct 2012.

[NL08] M. Nielsen and T. Larsen. A 2-GHz GaAs HBT RF pulsewidth modulator. *Microwave Theory and Techniques, IEEE Transactions on*, 56(2):300–304, Feb 2008.

[OAE+12] M. Ozen, C.M. Andersson, T. Eriksson, M. Acar, R. Jos, and C. Fager. Linearization study of a highly efficient CMOS-GaN RF pulse width modulation based transmitter. In *Microwave Conference (EuMC), 2012 42nd European*, pages 136–139, Oct 2012.

[OJA+11] M. Ozen, R. Jos, C.M. Andersson, M. Acar, and C. Fager. High-efficiency RF pulsewidth modulation of Class-E power amplifiers. *Microwave Theory and Techniques, IEEE Transactions on*, 59(11):2931–2942, Nov 2011.

[PJ12] Bonghyuk Park and Jaeho Jung. A fully integrated pulsewidth modulator for class-S system. In *Advanced Communication Technology (ICACT), 2012 14th International Conference on*, pages 274–277, Feb 2012.

[SADERH08] K.A. Shehata, M.A. Aboul-Dahab, S.H. El Ramly, and K.A. Hamouda. An FPGA based 1-bit all digital transmitter employing delta-sigma modulation with RF output for SDR. In *Signals, Circuits and Systems, 2008. SCS 2008. 2nd International Conference on*, pages 1–6, Nov 2008.

[SC11] Bo Shi and M.Y.W. Chia. On the performance of class-D power amplifiers with RF pulse-width modulation. In *Microwave Conference Proceedings (APMC), 2011 Asia-Pacific*, pages 1550–1553, Dec 2011.

[Sch93] R. Schreier. An empirical study of high-order single-bit delta-sigma modulators. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 40(8):461–466, Aug 1993.

[Sch02] D.P. Scholnik. A parallel digital architecture for delta-sigma modulation. In *Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on*, volume 1, pages I–352–5 vol.1, Aug 2002.

[SOBC13] N.V. Silva, A.S.R. Oliveira, and N. Borges Carvalho. Novel fine tunable multichannel all-digital transmitter. In *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, pages 1–3, June 2013.

[SOC13] N.V. Silva, A.S.R. Oliveira, and N.B. Carvalho. Design and optimization of flexible and coding efficient all-digital RF transmitters. *Microwave Theory and Techniques, IEEE Transactions on*, 61(1):625–632, 2013.

[SOGC12] N.V. Silva, A.S.R. Oliveira, U. Gustavsson, and N.B. Carvalho. A novel all-digital multichannel multimode RF transmitter using delta-sigma modulation. *Microwave and Wireless Components Letters, IEEE*, 22(3):156–158, 2012.

[SS03] Zukui Song and Dilip V. Sarwate. The frequency spectrum of pulse width modulated signals. *Signal Processing*, 83(10):2227 – 2258, 2003.

[ST05] Richard Schreier and Gabor C Temes. *Understanding delta-sigma data converters*. Wiley, New York, NY, 2005.

[Vai93] P. P. Vaidyanathan. *Multirate systems and filter banks*. Prentice-Hall, Inc., Upper Saddle River, NJ, USA, 1993.