**Cristiano José
Calado Castela**

**Desenvolvimento e teste de pré - distorçor
analógico
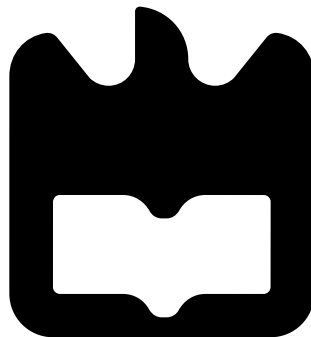Development and testing of an analogue
pre-distorter**

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Desenvolvimento e teste de pré - distorçor analógico
Development and testing of an analogue pre-distorter

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Resumo

Uma nova geração de sistemas de telecomunicações celulares está atualmente sob desenvolvimento. Os novos requisitos implicam grandes modificações nos sistemas atuais.

A utilização de bandas de frequência superiores implica uma redução da área de cobertura de cada célula e, consequentemente, uma redução da potência radiada. Para linearizar amplificadores de potência reduzida, é necessária uma abordagem mais eficiente que os pré-distorçores digitais frequentemente usados. Assim, um pré-distorçor analógico representa uma solução interessante para os desafios do futuro.

Este trabalho consiste no desenvolvimento e teste desta possível solução recorrendo a componentes eletrónicos discretos e a uma abordagem de aproximação analógica por ramos. A solução proposta é descrita e simulada. Uma implementação em hardware de parte da solução é descrita e testada. Apesar dos resultados da implementação em hardware não serem tão satisfatórios quanto os resultados da simulação, é provado que a solução proposta é viável.

Abstract

A new generation of cellular telecommunications systems is currently under standardization. The new requirements urge deep modifications to the current systems.

The use of higher frequency bands implies a reduction of the coverage area of each cell, hence, a reduction of the radiated power. To linearise less powerful amplifiers, a more efficient approach than the common digital pre-distortion is required. Therefore, an analogue pre-distorter becomes an interesting solution to the future challenges.

This work consists on the development and testing of such solution using discrete electronic components and a piecewise analogue approximation approach. The proposed solution is described and simulated. A hardware implementation of part of the solution is described and tested. Even though the results of the hardware implementation are not as satisfactory as the simulation ones, the proposed solution is proven to be viable.

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Acronyms

5G   fifth generation of cellular communications.

ACPR   adjacent channel power ratio.

ADC   analogue-to-digital converter.

ADS   advanced system design.

AM/AM   amplitude to amplitude characteristic.

AM/PM   amplitude to phase characteristic.

APD   analogue pre-distortion.

atan2   inverse tangent with two input arguments.

BB-APD baseband analogue pre-distorter.

BJT   bipolar junction transistor.

BPSK   binary phase shift keying.

DAC   digital-to-analogue converter.

dc   direct current.

DPD   digital pre-distortion.

f_t   transition frequency.

FET   field effect transistor.

FPGA   field-programmable gate array.

FR-4   flame retardant grade four.

GSM   global system for mobile communications.

I   in-phase.

IC   integrated circuit.

IF   intermediate frequency.

IMD   intermodulation distortion.

IMD3   third order intermodulation distortion.

IMD5   fifth order intermodulation distortion.

JFET   junction gate field-effect transistor.

LTE   long term evolution.

NPN   negative-positive-negative doped transistor.

OP-AMP   operational amplifier.

PA   power amplifier.

PAPR   peak to average power ratio.

PCB   printed circuit board.

PNP   positive-negative-positive doped transistor.

Q   in-quadrature.

RC   resistor-capacitor.

RF   radio frequency.

SNR   signal to noise ratio.

SPICE   simulated program with integrated circuits emphasis.

V_k   knee voltage.

VGA   variable gain amplifier.

Chapter 1

Introduction

Wireless communication systems, particularly cellular systems, are crucial for today's society lifestyle, therefore, the demand for a better service is in constant growth.

As in any business, the requirements are mainly set by the costumers or users, and the most common demands are well known: better coverage area, faster access to mobile data, and cheaper service. Even though these demands are simple enough to be understood by the users, they represent a great challenge that engineers and the scientific community need to overcome.

1.1 Object of work

The mentioned challenges can be translated into specific improvements to the systems in use nowadays, in fact, these improvements are defined as requirements for the new standard of fifth generation of cellular communications (5G). Although 5G (at the writing date of this report) is yet to be completely defined, the guidelines and minimum specifications are set:

1. Minimum downlink peak data-rate of 20 Gb/s.

2. 100 MHz minimum bandwidth and up to 1 GHz at the upper frequency bands.

3. Frequencies of operation above 6 GHz.

These standards require considerable modifications in the hardware currently used in cellular networks [1].

Restructuring the hardware will affect many components of the system, from the antennas, that need to be redesigned to operate at higher frequencies and to support technologies

like millimetre-wave beamforming [2], to the signal processing units, that will need to be able to handle the much wider bandwidths [1]. More examples could be given, however, this work has its focus on the power amplifier (PA).

Power amplifiers are a central component in a communications system representing one of the greatest expenses for telecommunications companies. Most of the power consumed by a cellular base station is due to the PA. The power drawn by a base station serves not only to supply the PA's operation, but also to dissipate the heat produced by the PA, therefore, improving the efficiency of the PA has an enhanced effect on the overall system's efficiency.

The improvement of the efficiency of a PA has other consequences, thus it can be said that there is a trade-off in this process. The PA is more efficient when working near the saturation region, however, near this region the PA has a nonlinear behaviour.

The nonlinearities caused by the PA's operation have multiple negative effects both on the transmitted signals and on the frequency spectrum that are analysed in the next chapter.

This work focuses on compensating those nonlinearities resorting to analogue pre-distortion (APD). The motivations for this work and the reason to choose an analogue implementation of a pre-distorter are clarified in the following section.

1.2   Motivation for the work

During the early years of wireless telecommunications, especially for satellite communications, APD was a widely used linearisation method [3]. However, with the advent of digital processors, it was possible to apply more complex pre-distortion functions which led to considerable improvements on linearity and efficiency. Since then, digital pre-distortion (DPD) has been object of much research.

Contrasting with the trend of research, the aim of this work is the implementation of an APD. The expected increase in bandwidth for 5G implies the increase of the clock and sampling frequencies of digital processors. The higher the clock frequency, the higher the power consumption of the processor, further reducing the efficiency of the system.

With the new standards of 5G, namely the operation on the millimetre wave region, where the range is smaller due to the higher channel attenuation and restricted line of sight requirements, each cell of the system is smaller, thus the radiated power is also lower. Therefore, the PAs operate at much lower powers which increases the overall influence of the lineariser's power consumption (the digital signal processor in DPD).

Considering as a general and only illustrative example, a long term evolution (LTE) base station that uses a 500 W PA can afford to operate a 40 W digital processor for linearisation, consuming around 8% of the PA's power [4]. However, a 5G base station in a densely populated area might operate a 5 W or less PA. If the same digital processor was used, it would draw around eight times the power of the PA. A lineariser consuming more power than the PA would never be feasible.

An analogue implementation of a pre-distorter has the potential to achieve a wider bandwidth drawing less power. This is the main motivation to focus the work on this topic.

Even though the linearity improvement provided by APD is smaller when compared to DPD, it is important to explore new solutions using this topology. It is also important to redirect some of the research towards APD to achieve better performances and lower implementation costs.

The goal of the work described in this report is to design and test an APD circuit, which could be used to evaluate the difficulties and more relevant issues that are associated with baseband analogue pre-distortion.

This work does not comprise, by any means, the full potential of analogue pre-distortion. The aim is to implement a first iteration of what could be a new trend in linearisation methods. Further research is required and different implementations must be pursued, especially in integrated circuit form.

1.3   Roadmap of the report

This report is divided in six chapters. The next chapter introduces the definitions of the terms and figures of merit used along the text. Then an overview of the existing linearisation methods is presented, with a special emphasis on pre-distortion, since this method is the object of study in this work.

In chapter three, two possible architectures for the APD are exhibited. The motives that lead to select one rather than the other are also explained. Furthermore, this chapter contains an overview of the implemented circuits that build up the APD.

The simulation results of the implemented circuits are exhibited in chapter four, as well as a simulation of those results when applied to a static PA model.

Chapter five contains the practical results achieved with a printed circuit board (PCB) implementation of the two main blocks of the APD: the amplitude to amplitude characteristic (AM/AM) and the amplitude to phase characteristic (AM/PM) distortion blocks.

The last chapter draws conclusions from the work reported, and comprises a future work proposal.

Chapter 2

Linearity and Linearisation methods - A brief overview

2.1 Definitions and figures of merit

To fully understand the work reported it is important to be familiarised with fundamental concepts, definitions and figures of merit.

An essential concept regarding this work is linearity. This and other relevant definitions are given in the following section.

2.1.1 Definitions

Linearity

Linearity is mathematically defined as a function that complies with two properties:

- Additivity: Given a function $f(x(t))$ and two vectors $x(t)$ and $y(t)$, $f(x)$ obeys additivity if:

$$f(x(t) + y(t)) = f(x(t)) + f(y(t)) \tag{2.1}$$

- Homogeneity: Given a function $f(x(t))$ a vector $x(t)$ and a constant a, $f(x(t))$ satisfies the homogeneity condition if:

$$a \cdot f(x(t)) = f(a \cdot x(t)) \tag{2.2}$$

The plot of the most basic linear function $f(x(t)) = x(t)$ is represented in figure 2.1, it is obviously represented by a straight line with unitary slope.
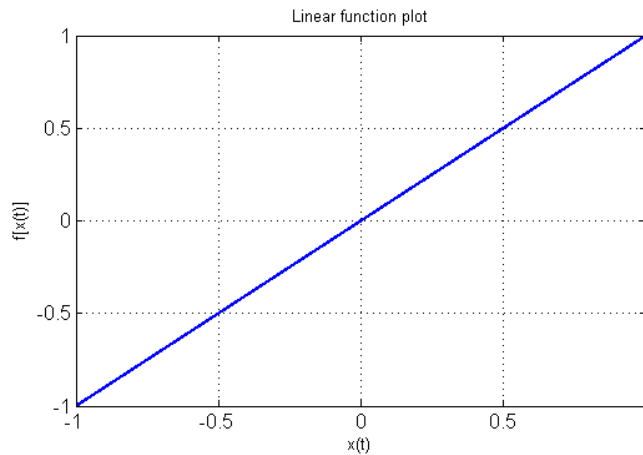
Figure 2.1: Example of a basic linear function $f(x(t)) = x(t)$

Shifting this definition to the interest domain of this report, it means that if a PA is static and linear, its output is merely the input multiplied by a gain G, according to:

$$f(x(t)) = G \cdot x(t) \tag{2.3}$$

However, as mentioned previously, this is usually not the case.

Non-linearity

After defining linearity, it may seem redundant to define its opposite, however, it is important to demonstrate its effects on the signal and spectrum.

Obviously, nonlinearity can be mathematically defined as a function that does not satisfy the properties of additivity and/or homogeneity, but this is a rather vague definition. It is, therefore, important to provide more specific information, according to the object of the work.

A PA is usually a transistor biased to operate around a determined point. The characteristic operation curves of a field effect transistor (FET) resemble the ones depicted in figure 2.2. Moreover, the position of the bias point determines the overall efficiency of the amplifier. The closer the bias point is to the horizontal axis of the referential when the signal is null, the more efficient the amplifier is. However, this added efficiency comes at the cost of linearity.

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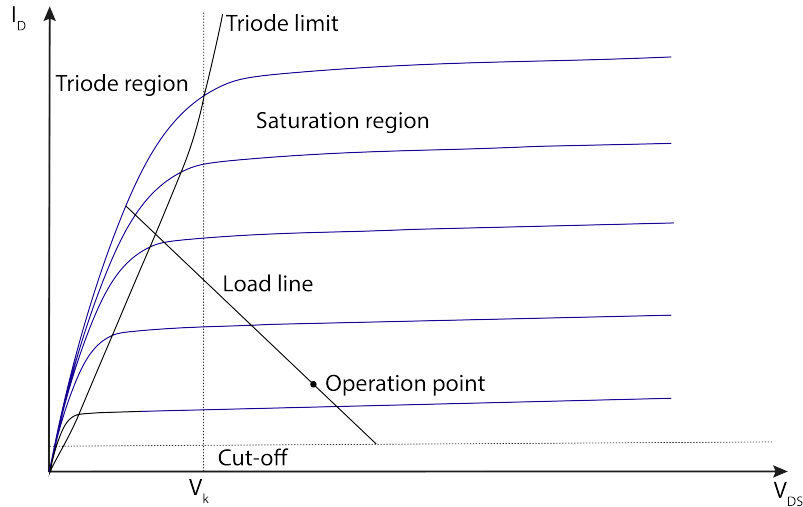
Figure 2.2: FET amplifier characteristic curves

The input signal of the FET shifts the operation along the load line. The particular bias point depicted in 2.2 belongs to a class AB amplifier. Non-linearities appear when the operation goes beyond the knee voltage (V_k) line, since the gain in that region is compressed. Non-linear behaviour also occurs when the operation of the transistor falls into the cut-off region. These are two briefly mentioned causes of nonlinear behaviour, a more detailed description would be too extensive to include in this work, and can be found in literature [5].

Memory effects

Whilst this work approaches exclusively static nonlinearity, it is important to mention memory effects. When the output of the PA is affected not only by the present input conditions of the input but also by past conditions, the PA introduces distortion associated, to memory effects which affect the signal by making the intermodulation components to grow more and asymmetrically [6] [7].

Memory effects are known to arise due to three main causes:

- Changes in the PA nonlinearity over frequency [8];

- Biasing memory effects appear due to the behaviour of the bias network in the presence of a (slowly) varying envelope signal [9];

- Temperature and electron trapping [8] [9].

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Intermodulation distortion

Intermodulation distortion is commonly defined as a form of adjacent channel distortion (side-bands) near the fundamental frequency of a two tone signal.

This distortion components are created by the mixing action introduced by the nonlinear behaviour on the two or more tones of the signal. The frequencies at which intermodulation distortion (IMD) appears are conveniently described in the following section, where a nonlinear component is analysed [5].

Spectral regrowth

Spectral regrowth appears when signals that occupy a region of the spectrum (and not just a single frequency point) are processed by a nonlinear system. These signals can be seen (or approximated) as a sequence of equally spaced tones, which the nonlinear behaviour of the PA will transform also into a high number of intermodulation distortion components. Such distortion will occupy, at the fundamental band, the frequency region of the original signal and its surroundings, being observed as spectral regrowth.

2.1.2 Relevant figures of merit

To compare results, it is necessary to have proven methods and figures of merit that objectively quantify the performance and behaviour of a given device.

To evaluate the linearity performance of a PA it is common to refer to the following figures of merit:

Adjacent channel power ratio

As its name states, this figure of merit evaluates the ratio between the average power of the adjacent channel and the average power of the main signal component. It is usually used to quantify the level of nonlinearity in a system since it compares the main signal to its intermodulation components (in the adjacent channel region only), therefore, measuring the spectral regrowth caused by nonlinearities.

Peak to average power ratio

This figure of merit measures the difference between the peak power of a signal and its average power. The peak to average power ratio (PAPR) usually increases with the

modulation order of the signal. It is an important metric since it helps to predict the best placement of the biasing point of a transistor that builds up a PA.

2.2 The effects of nonlinearity

Prior to analyse the available linearisation methods it is important to understand the consequences of nonlinearity in a PA's operation.

Recalling figure 2.2, the obvious consequence of the curve presented is a gain compression near the transistor's saturation point. As a matter of illustration, figure 2.3 depicts the gain characteristic of a static (i.e. memoryless) model (which also includes a realistic noise generator) that was obtained from measuring a real class-AB PA circuit in the laboratory. As can be observed, from a certain level of the input signal, the PA gain starts to compress, leading to distortion generation. The gain in function of the input power is also called AM/AM.
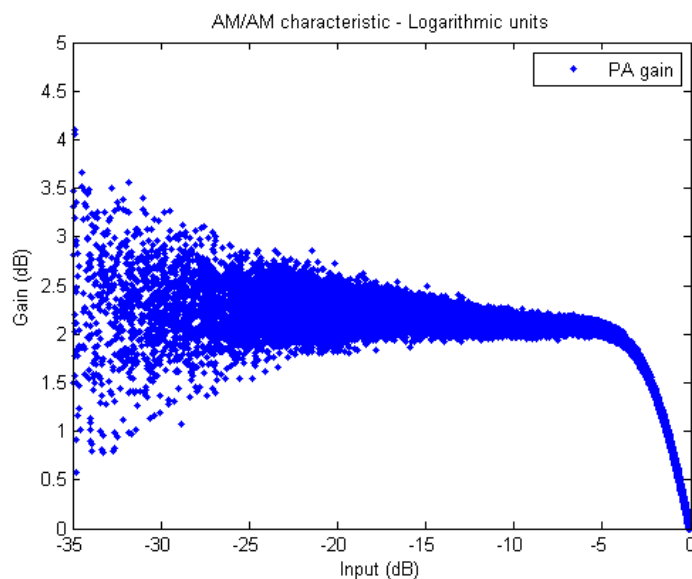
Figure 2.3: PA gain characteristic

The operating conditions of the transistor affect not only the signal's amplitude, but also the phase of the modulating signal. The phase shift dependency with the input power is refered to as AM/PM. Figure 2.4 depicts this dependency for the same PA model used for the AM/AM illustration.
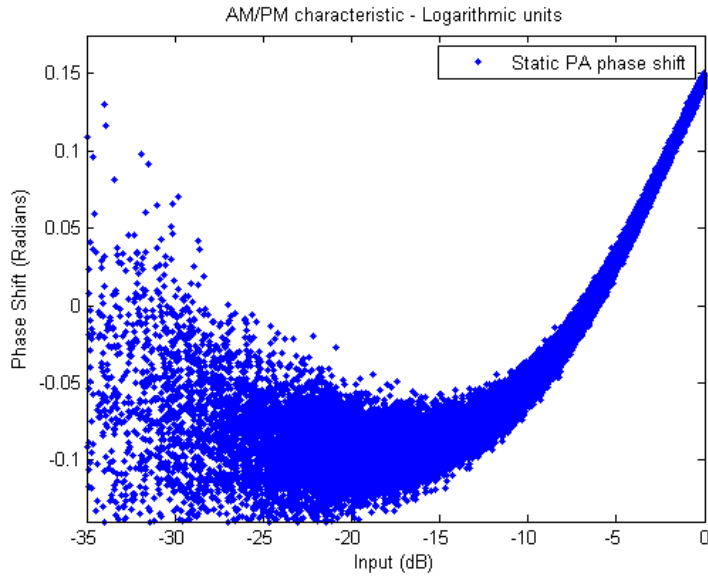
Figure 2.4: PA phase characteristic

The AM/PM is mainly attributed to the nonlinear capacitances that vary with the input signal, altering the input matching conditions of the PA [10], thermal drifts and power supply ripple.

Although the previous figures are useful to exemplify the impact of the PA nonlinear behaviour in its transfer characteristics, they do not completely illustrate the problems it creates. There are other two important aspects to consider: the errors introduced in the signal, which will affect the reception after demodulation, and the effects on the spectrum of the transmitted signal. Both aspects are illustrated and clarified hereafter.

To improve the spectral efficiency is to achieve higher bit-rates maintaining the bandwidth. Complex modulation schemes can be used for this purpose. Instead of sending one bit in each symbol, it is possible to send multiple bits per symbol. The drawback is that the higher the order of the modulation scheme, the closer the symbols are to each other, as depicted in figure 2.5.
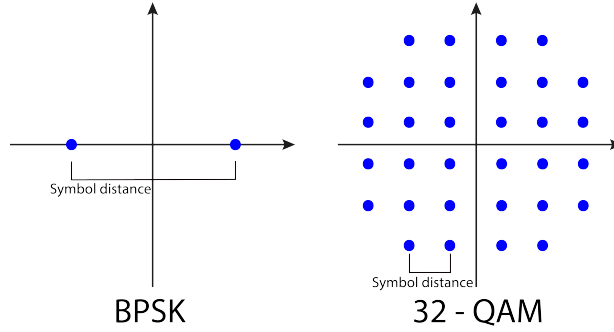
Figure 2.5: BPSK and 32-QAM modulation schemes

As stated above, nonlinearities cause errors in both the amplitude and phase of the signal. The points represented in figure 2.5 become clusters. The larger the clusters, the higher the probability of errors on the reception end, although distortion may not be the only factor to influence the size of the clusters, it strongly influences the latter.

Moreover, the order of the modulation scheme strongly affects the PAPR which strongly contributes to increase distortion, since the placement of the operation point is done by taking the average output power into account.

The repercussions of nonlinear distortion in the spectrum are the factor that contributes the most to the very strict regulations imposed by the entities that manage it. To understand why these limitations are so strict it is important to observe the effects of nonlinear distortion.

Spectral regrowth occurs due to the PA nonlinear characteristics. A simple method to illustrate this is to consider a polynomial approximation for the PA gain function. Although the order of the polynomial approximation is usually equal or greater than 5, for the sake of simplicity, a third order approximation is considered in the following example:

$$G(x(t)) = a_1 \cdot x(t)^3 + a_2 \cdot x(t)^2 + a_3 \cdot x(t) + a_4 \tag{2.4}$$

where $x(t)$ is the PA input signal which, in this analysis, will be assumed to be a two-tone excitation:

$$x(t) = b_1 \cdot cos(w_1 \cdot t) + b_2 \cdot cos(w_2.t) \tag{2.5}$$

After expanding the PA approximation with the applied input signal, the result shows that the amplifier's output has distortion components at the following frequencies:

- Baseband components: DC (0 Hz) and $w_2 - w_1$;

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- In-band components (IMDs): $2w_1 - w_2$ and $2w_2 - w_1$;

- Second order harmonic components: $2w_1$, $2w_2$ and $w_1 + w_2$;

- Third order harmonic components: $2w_1 + w_2$, $w_1 + 2w_2$, $3w_1$ and $3w_2$.

As the previous list states, the power is distributed by a larger spectrum area. Figure 2.6 depicts the frequency spectrum of the output of a PA with a third order and a fifth order approximation, respectively, for a two-tone signal.

(a) 3rd order PA   (b) 5th order PA
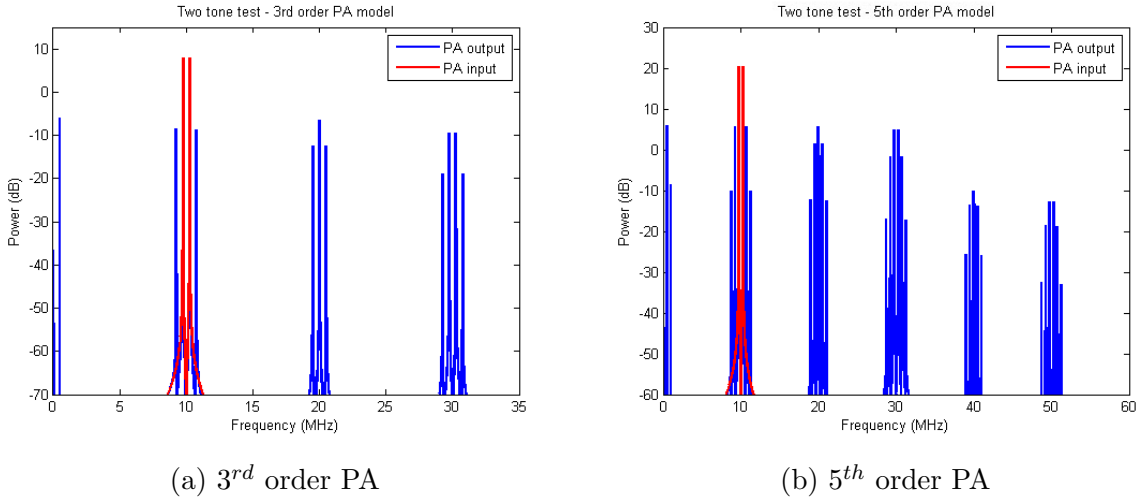
Figure 2.6: Two-tone test of two PA polynomial models (whole spectrum)

As proven by the output function of the PA and depicted in 2.6 there are considerable frequency components appearing over a wide range of the spectrum. However, the frequency components that constitute the out of band distortion can be filtered. Figure 2.7 depicts a detail of the problematic in-band distortion components.

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(a) 3rd order PA   (b) 5th order PA
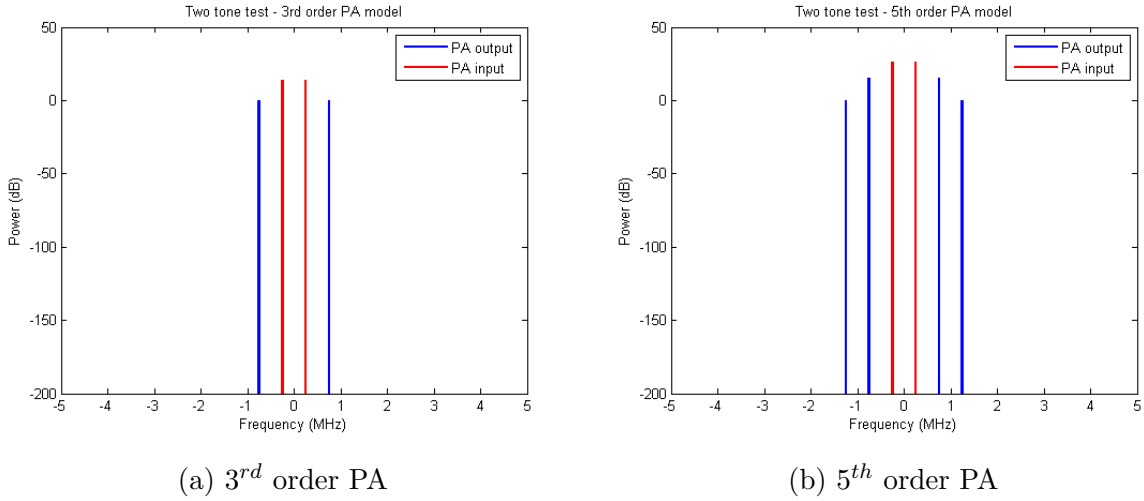
Figure 2.7: Two-tone test of two PA polynomial models (in-band distortion detail)

As the figure illustrates there are considerable distortion components near the signal's fundamental frequency. Those components are the previously defined IMD components, which in this particular case are of third and fifth order. IMDs represent an issue due to their proximity to the signal, which makes them very difficult to filter. Other frequency components also created by the nonlinearities, are usually less relevant due to the possibility to filter the signal at the output of the PA.

Figures 2.6 and 2.7 depict the processing of a two-tone signal by two different polynomials (third and fifth orders). To provide an additional illustration of the distortion effects over a common telecommunication signal, figures 2.8a and 2.8b show a four carrier global system for mobile communications (GSM) signal and a LTE signal, respectively, before and after being amplified by the static PA model based on a real PA. With more complex signals the spectral regrowth phenomenon is even more evident, introducing power in frequencies beyond the original signal.

Due to the available spectrum being limited and densely used, the signal bands allocated to each company and user are constrained and close to each other, implying strict limitations of the spectral regrowth by the telecommunication regulation agencies. These limitations and the difficulty in filtering determine that the means to cancel the spectral regrowth is resorting to dedicated linearisation techniques.

(a) GSM signal spectrum

(b) LTE signal spectrum
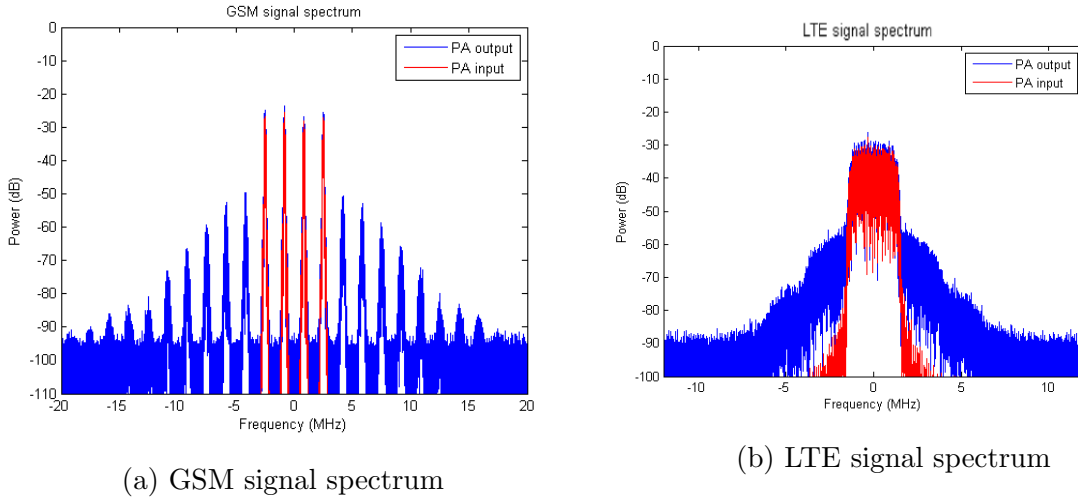
Figure 2.8: Static PA

2.3 Linearisation methods

As stated earlier in this work, the strict spectrum regulations and the energy efficiency requirements urge the necessity to linearise PAs, this section presents an overview of the linearisation methods currently in use.

Since the work to be developed is focused on analogue techniques, the digitally operating linearisers are only briefly mentioned in this evaluation of the state of the art.

The techniques of linearisation can be divided in three groups that are here described. These groups are feedforward, feedback and pre-distortion although, nowadays, this division is becoming more tenuous because researchers are proposing novel approaches in which two or more methods are combined to improve the linearisation and power efficiency. Power back-off is also mentioned, however it is not included in any of the previously mentioned groups since its purpose is to avoid the appearance of nonlinearities, and commonly leads to a decrease of power efficiency.

As one can presume from the title, a higher emphasis in given to the analogue pre-distortion method.

2.3.1 Power back-off

Power back-off is hardly considered a linearisation method, but instead a method of avoiding the occurrence of distortion. This is accomplished by operating the transistor at

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its highly linear region. However, the transistor is less efficient in this region, hence the urge to approximate the operation point to the saturation region.

Even though this method, by itself, does not lead to an efficient PA, when allied with other linearisation techniques, power back-off facilitates the obtainment of the required linearity/efficiency relation for each application.

2.3.2   Feedforward

Feedforward linearisation emerged in the 1920's from the work of Howard Black, during the expansion of the telecommunications industry. The concept behind this linearisation technique is simple to apprehend, but on the other hand quite difficult to implement, especially if one considers the technology available at the time of its development. In fact, Black spent years trying to get his design to work but it was not possible with the technology he had available, due to the absence of linearity on tube amplifiers, as it will be shown later [3].

The original concept idealised by Black is shown in figure 2.9. There are two paths, a main path where the main signal is amplified and, of course, distorted, and an auxiliary path where the input signal and the output of the main amplifier are subtracted in order to obtain an accurate sample of the distortion (error) introduced by the radio frequency (RF) PA. That error signal is then amplified by a very linear amplifier and added to the output of the main PA, thus cancelling the nonlinearities introduced by the PA [11].
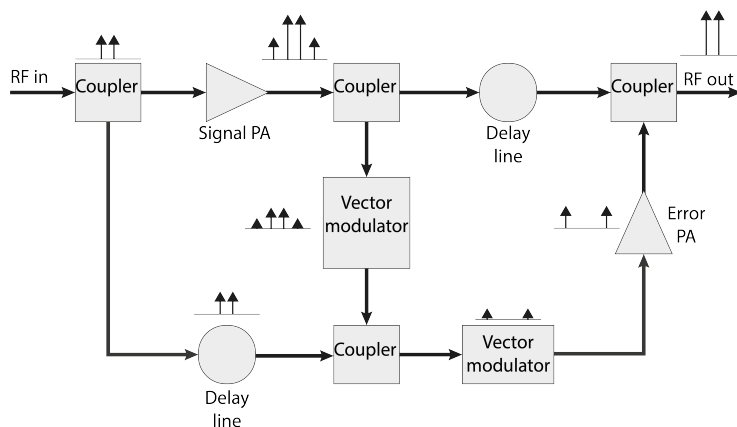
Figure 2.9: Feedforward lineariser diagram

The result of this simple concept is a considerable improvement of the linearity of the PA. It also allows the designer to control the output power and the linearity separately [12], by choosing different devices for the main amplifier and the error amplifier, unlike

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what happens with feedback techniques where the output power and the linearity depend on each other (RF feedback). Unfortunately, this advantage comes with a great cost, the extra amplifier increases the complexity and the power consumption of the circuit. The auxiliary (error) amplifier needs to be as linear as possible, therefore it works on a low efficiency region, causing an significant limitation on the efficiency achieved with this method [3].

Due to the reasons exposed above this method was ignored for a long period of time and for that reason it may be less commonly known for the majority of people [3]. Nevertheless, it is used nowadays, when higher bandwidths are required [13], and as it would be expected there were developments on the technology. Starting with the introduction of semiconductor based power amplifiers which minimized the issue of low linearity of the vacuum tube amplifiers, the integration of adaptive characteristics also allowed that linearity to endure the changing of conditions such as: temperature, ageing and frequency [11]. The latter were the main problems that Black tried to solve, unsuccessfully, during the 1920's.

Further challenges are presented to this technique as the bandwidth requirements of communication links increases. Error cancelling, at the output, needs to be performed throughout a considerably wide bandwidth, and this is not easy to achieve in practice, as it implies maintaining a constant phase offset of -180 degrees between the two channels (main and auxiliary) for the entire bandwidth.

2.3.3 Feedback

Feedback is another method of linearisation also envisioned by Howard Black, after much time trying to solve all the problems encountered on the implementation of a feedforward lineariser he proposed this new concept [3].

Presently, this method is widely used in many amplifier applications, but in RF it is occasionally avoided due to stability problems at high frequencies. In fact, when Black proposed this method it was not well accepted as it was believed to be somewhat similar to a perpetual-motion machine [3]. Despite that scepticism Black built a functional feedback linearised amplifier.

The conception behind this technique is depicted in figure 2.10 and consists of sampling both the input and output signal of the PA, and then the two signals are subtracted, hence an error signal is obtained. As the loop gain increases, the error signal tends to decrease, hence the signal improving the linearity of the output signal [7].
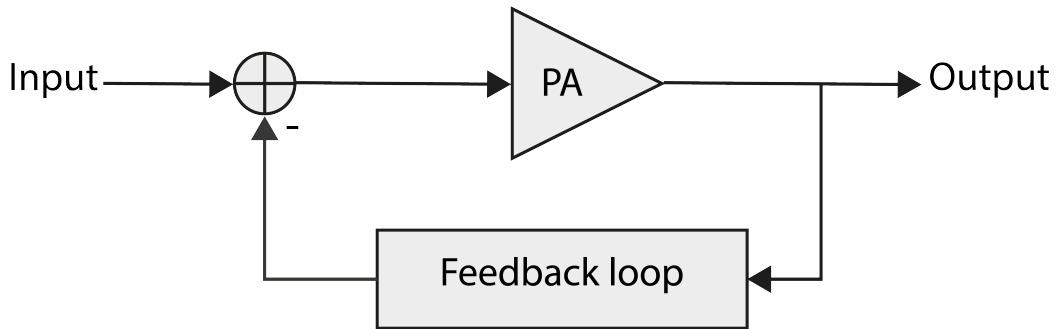
Figure 2.10: Simplified feedback lineariser diagram

Therefore, feedback linearisation is a simple and effective linearisation method, it is possible to achieve a substantial improvement of linearity with a simple and power efficient circuit. However, it has some problems associated with it, from which the following stand out:

- It is difficult to implement feedback linearisation on larger bandwidths due to the delay inherent to the RF path through the feedback loop that leads to an instability problem, which is a known characteristic of closed loop systems, and must be considered when designing such a device [7].

- Unlike feedforward, it is impossible to independently manage the gain and linearity of the PA. Instead, a compromise between gain and distortion must be reached [3].

Feedback linearisation has been a subject of study for many years, therefore improvements were made to this method and new variants and different approaches were created. In the following sections the two main baseband feedback linearisation techniques are described.

Polar feedback

Polar loop feedback is, as the name implies, applied to the polar coordinates of the baseband signal. Two error signals are generated to adjust the amplitude and the phase components separately.

To correct both components, a scheme as the one depicted on figure 2.11 can be used. The figure shows the main path of the signal from the input to the output passing through the PA, the two feedback paths are also evident. The first loop, envelope correction loop, consists of two envelope detectors which output the baseband amplitude coordinates of both the input and the amplified signals. These two signals are then compared and an

error signal is generated. The error signal controls a variable gain amplifier which adjusts the amplitude of the input signal.

The second loop, for the phase correction, consists of two phase detectors that retrieve the input and output phases. These phase coordinates are then compared and the result is fed into a phase shifter completing the linearisation of the signal.
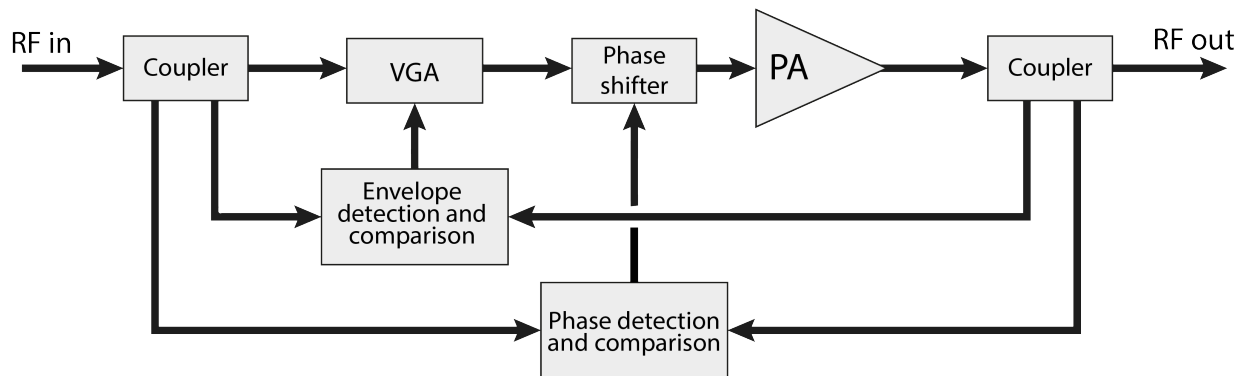
Figure 2.11: Polar loop feedback diagram

This method enables the correction of both the amplitude and phase. However, obtaining the polar coordinates is not trivial, moreover, the phase adjustment relies on analogue phase shifters which often have limited operation bandwidths. The delays on the feedback loop can lead to instability which also represents a challenge of this linearisation method.

Cartesian feedback

As previously demonstrated, the main problem with feedback is the limit on the signal's bandwidth. With Cartesian loop an attenuation of this issue can be obtained since the Cartesian coordinates have a lower bandwidth than the amplitude and phase components.

The error correction signal is applied to the in-phase (I) and in-quadrature (Q) coordinates before the modulator. A diagram of a possible implementation of this topology is depicted in figure 2.12.
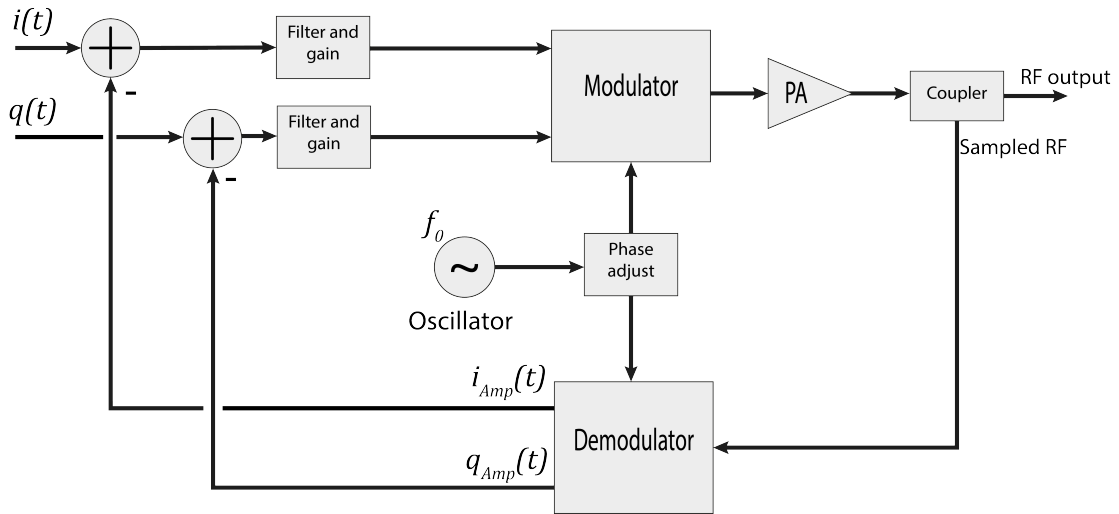
Figure 2.12: Cartesian feedback diagram

The upper signal path contains the corrected input signal, which is then filtered and adjusted to comply with the modulator requirements. The next stage consists of a modulator which converts the signal to RF to be amplified by the PA. At the output of the PA a coupler retrieves a sample of the amplified signal. This sample goes through a demodulator and is applied to the input signal correcting. Both the modulator and demodulator are controlled by the same local oscillator, however, to compensate the delays introduced by the PA, a phase adjustment is required.

Similarly to other closed loop solutions, this approach also has stability problems, which contributes to the limited bandwidth of feedback linearisation techniques. An alternative to closed loop linearisation techniques is described in the following section.

2.3.4   Pre-distortion

The third group of linearisation techniques is pre-distortion. There are two main branches within pre-distortion: digital pre-distortion and analogue pre-distortion, which are independently described in this chapter.

Despite the implementation of each one of the previously mentioned distortion methods being vastly different, both are based on the same concept.

The input signal is processed accordingly to an accurate characterisation of the PA distortion correction function before being applied to the PA. By applying the inverse function of the power amplifier to the input signal, the output signal is linearised. The improvement on linearity is strongly correlated to the accuracy of the PA inverse characteristic function.

This process is illustrated in figure 2.13.
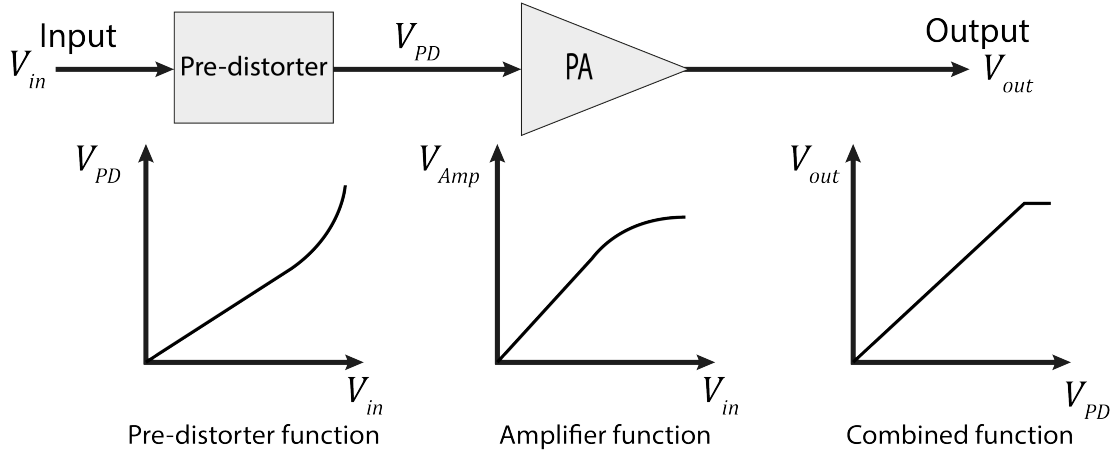
Figure 2.13: Pre-distortion diagram

The use of an accurate model of the PA's inverse characteristic to manipulate the signal before amplification mitigates the two main limitations of feedforward and feedback: the need to amplify the error signal in feedforward and the instability problems that arise in feedback.

However, using an open-loop system also has disadvantages. The inability to perform real time adjustments to the system accordingly to the operation conditions is a considerable limitation of this technique. However, adaptive loops are commonly used to update the pre-distorting function from time to time. The following sections describe the two main branches of pre-distortion, as well as the methods used to improve the linearisation results.

Digital pre-distortion

As the name suggests, digital pre-distortion is performed in the digital domain, therefore, it requires a digital-to-analogue converter (DAC) and a digital processor.

The operation of a DPD consists on the processing of the signal according to the PA's inverse transfer function, the signal is then converted to the analogue domain by the DAC.

Despite the concise explanation of the pre-distortion process, there are several challenges that elevate the design complexity of a digital pre-distorter. The processing power is one of the preeminent concerns since the PA models are complex and the signal must be promptly processed to maintain a wide bandwidth. A common processor running sequential calculations does not comply with nowadays requirements. A different architecture capable of performing concurrent operations is needed, therefore, field-programmable gate

arrays (FPGAs) and digital signal processors (DSPs) are commonly used to implement digital pre-distorters.

With a digitally implemented distortion it is possible to use complex PA models that allow the cancellation of the previously defined memory effects by taking multiple delayed inputs into account. These models are often variations of the Volterra series [14], however, this topic is not furtherly discussed here since it diverges from the subject of this work.

The mentioned features lead to a substantial improvement of linearity, which justifies the massive use of DPD in a wide range of telecommunication systems. However, the power consumption of digital pre-distorters represents a limitation with an increasing importance since the clock frequency of the FPGA is strongly correlated with their power consumption. Hence, the higher the signal's bandwidth the higher the power consumed by the pre-distorter.

Analogue pre-distortion

Contrasting with DPD, analogue pre-distortion has better efficiency at the expense of the achieved linearisation. However, with the urge to improve the efficiency and the expected modifications to the actual telecommunications systems APD may represent a viable solution to the issues at hand.

Resorting to analogue circuits to generate the required distortion functions is not as simple as coding those functions into a processor or FPGA. The complexity of implementing such circuits determines the lower accuracy of the PA models used, hence the reduction of the possible linearisation improvement. Moreover, the nonideal behaviour of hardware components plays a direct role on the achieved accuracy of the implemented analogue pre-distorter model, not being able to compete with the achieved numerical resolution that is available in digital pre-distorters.

The nature of analogue circuits determines the difficulty to tune them to different purposes. Most analogue pre-distorters are not prepared to be adjusted accordingly to different operation conditions. To better illustrate the issues and advantages of APD this section describes several possible analogue pre-distorter implementations emphasising the features of each one.

One of the most basic linearisers is the third order anti-parallel diode pre-distorter [15], illustrated in figure 2.14. Figure 2.15 depicts the interior of the intermodulation generator block which contains two diodes in an anti-parallel configuration and a resistor-capacitor (RC) circuit. The diodes are used to generate intermodulation components used to compensate the IMD introduced by the PA. The generation of this intermodulation

components is detailed hereafter.
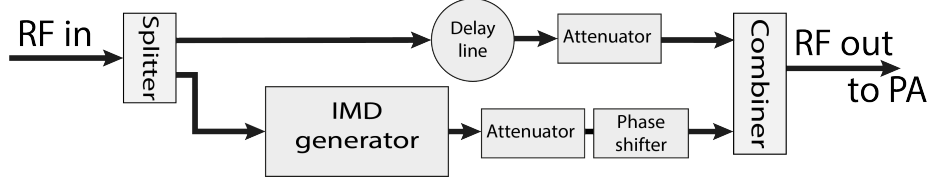
Figure 2.14: Third order analogue pre-distorter
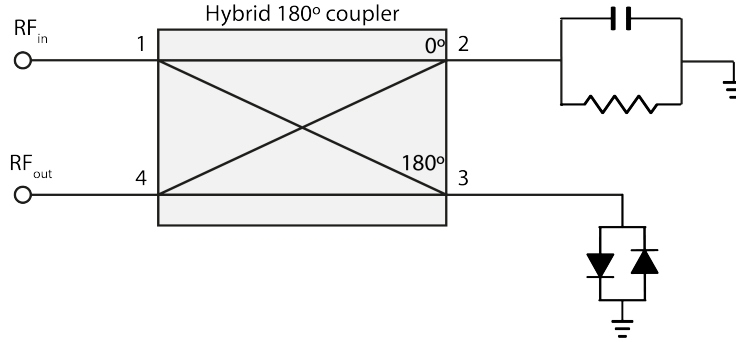
Figure 2.15: Intermodulation components generator

The IMD generation at the PA has been described in this report. The anti-parallel diode pair generates distortion in an analogous manner. By analysing the diode current-voltage equation 2.6:

$$I = I_S(e^{\frac{qV_D}{nkT}} - 1) \tag{2.6}$$

where I is the current through the diode, I_S is a scaling parameter related to the reverse bias saturation current, V_D is the voltage across the diode, k is the Boltzmann constant, q is the electronic charge, T is the absolute junction temperature and n is a factor used to model the constructive aspects of the diode. When a RF or intermediate frequency (IF) two tone signal is applied to the anti-parallel diodes third order intermodulation distortion (IMD3) is created.

Considering $\frac{q}{nkT} = K$, then the current through the diodes is given by:

$$I = I_S(e^{KV(t)} - 1) - I_S(e^{-KV(t)} - 1) \tag{2.7}$$

Using the Taylor series to solve the exponential equation:

$$I = I_S.\left[2KV(t) + \frac{[KV(t)]^3}{6} + ... + \frac{[KV(t)]^{2n+1}}{(2n+1)!} + ...\right] \tag{2.8}$$

As shown in [12], the anti-parallel diode arrangement generates mainly first and third order terms. Higher order terms have lower power levels, thus can be neglected. The first order terms, at the fundamental signal frequency, must be eliminated, which is accomplished by the RC circuit [12].

This method of pre-distortion provides a moderate linearity improvement since it cancels only the IMD3 products and the IMDs added by the PA are commonly relevant beyond the third order.

To also address the fifth order intermodulation distortion hence improving the linearisation, a more complex solution is needed. An implementation that solves this problem is the cascaded third-order pre-distorter [12] [16].

The method under discussion consists of two third order IM generators on a cascade configuration, as depicted in figure 2.16. The design is considerably similar to the one presented previously. There is a linear path which carries the original signal to the output of the pre-distorter and two nonlinear paths where the intermodulation components are generated. The linear path includes a time delay to match the signal timing with the other paths.
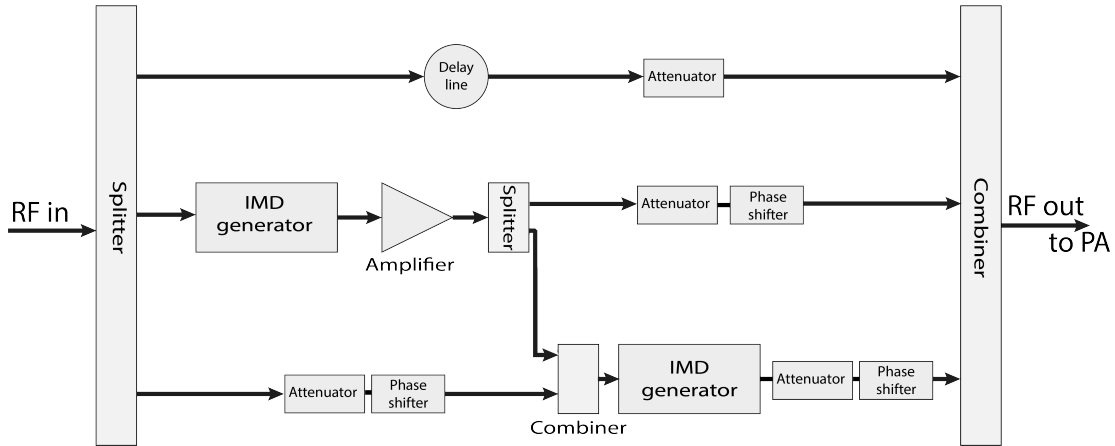
Figure 2.16: Fifth order analogue pre-distorter

The intermodulation generators are identical to the generator used in the previous design. The reason to use two is, as mentioned, due to the low level of the higher order terms at the output of the third order IMD generator. The second IMD generator uses the fundamental signal and the IMD3 to generate the fifth order intermodulation components.

The anti-parallel diode configuration of the second IMD generator creates terms at the fundamental frequency, as well as at the third and fifth order intermodulation components. The RC circuit in this block is tuned to eliminate the third order terms. The terms at the

fundamental frequency have neglectable power when compared with the signal power at the linear path, therefore, these terms do not need to be eliminated.

The pre-distorter described above, which reduces both third and fifth order IMDs provides a good improvement of linearity on the signal [12]. However, there are two problems with both analogue pre-distorters described:

- The RC circuit is tuned to one specific frequency. For signals with higher bandwidth the linearisation is degraded since the fundamental and third terms in the first and second intermodulation generators, respectively, are not perfectly and evenly cancelled across the whole bandwidth.

- The previously defined memory effects are not considered in these implementations, leading to limiting the results achieved.

To address the problems caused by the memory effects a proven solution is a multi-branch analogue pre-distorter [17]. Figure 2.17 depicts a possible implementation of this solution with three nonlinear branches and one third order intermodulation generator. Each branch contains replicas of the distortion signal delayed differently from each other.
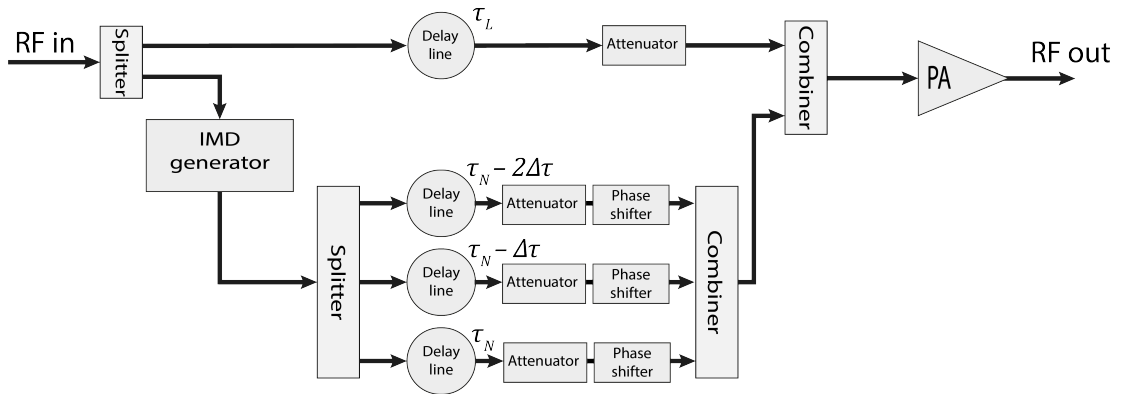
Figure 2.17: Multiple branch analogue pre-distorter

It has been proven [17] that this technique is useful when amplifying wideband signals.

2.3.5 Combination of linearisation methods

In this section, the merging of two different linearisation techniques is considered. As shown previously, each one of these techniques has limitations. To overcome such limitations, researchers began to merge the techniques, trying to convey only the advantages of each technique.

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A usual combination of linearisation methods is to combine feedback and pre-distortion. A diagram of this implementation is available in figure 2.18. The analogue pre-distorter is located outside the feedback loop to reduce the loop delay. A sample of the output signal goes through a block with the inverse gain of the PA before being compared to a delayed sample of the input signal. The error signal is then adjusted by a phase shifter and an amplifier (loop gain). The soft limit block improves stability by restraining the magnitude of the error signal [13].
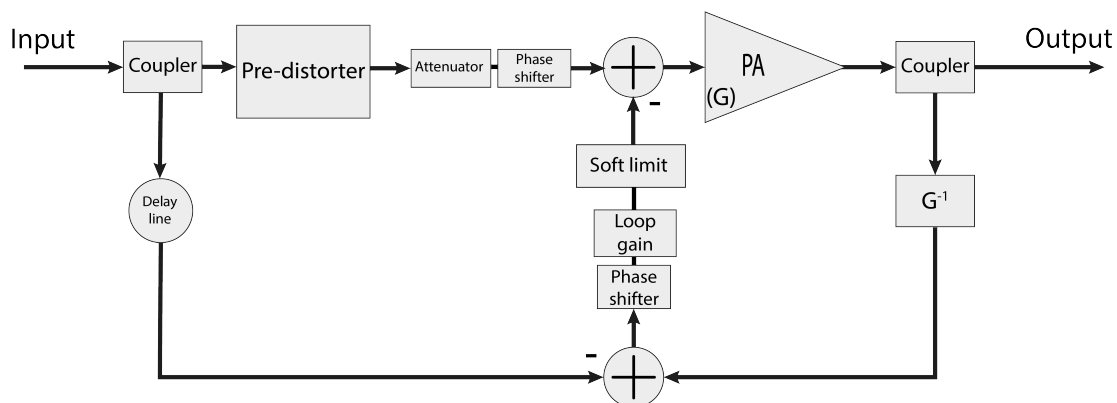
Figure 2.18: Combination of feedback with analogue pre-distortion

A different approach to the merging of feedback and APD is the adjustment of the pre-distorter functions at a much lower frequency than the frequency of the signal. The system can be tuned to the current operating conditions without limiting the bandwidth or introducing oscillations that may lead to instability.

Other solutions have been proposed, such as the merging of APD and feedforward, however this techniques commonly result in lower energy efficiency, therefore, the study of this techniques diverges from the objectives of this work.

2.3.6 Final remarks

There are many other approaches to the linearisation problem, however they can generally be divided into the three presented groups. This chapter highlighted the most common techniques used nowadays regarding each group.

The need for higher data rates, which implies wider bandwidths, as well as the pursue for better spectrum and energetic efficiency urge a constant evolution of the methods in use, therefore, innovative ideas and solutions are constantly arising.

Chapter 3

Architecture description

As the previous chapter shows, the implementation of RF-APDs has been the most widely used and explored, however, the bandwidths imposed by the 5G standard make it quite difficult to implement a useful APD since most of the implementations presented have limitations due to impedance matching, resonant circuit tuning and phase shifter circuits which, usually, only work properly in a narrow bandwidth around the centre frequency of operation.

The fact that the analogue signal processing integrated circuits (ICs), such as operational amplifiers (OP-AMPs), multipliers and others, have limited frequencies of operation, while having satisfying bandwidths, represents a critical aspect which strongly influenced the choice of the APD's architecture.

Distorting the signal at baseband resembles the principle of operation of DPD, however with analogue pre-distortion the power consumption should be reduced and the circuits should be scalable, within limits, to wider bandwidths, depending on the quality of the components and the circuit boards used.

At this stage, it is evident that in this work the implementation of a baseband analogue pre-distorter (BB-APD) is intended. However, what is yet to be defined is the architecture and the structure of such BB-APD. The analysis of possible configurations lead to the selection of two most promising architectures, which are unriddled in the following sections.

3.1 Architecture selection

3.1.1 Polar baseband analogue pre-distorter

The first considered architecture generates and applies the distortion at the baseband in terms of polar coordinates (amplitude $a(t)$ and phase $\phi(t)$), which means that the distortion is calculated and applied to the amplitude and phase components of the signal. The baseband is, usually, represented in its Cartesian form, in terms of I ($i(t)$) and Q ($q(t)$) coordinates. Therefore, the first blocks of the polar BB-APD convert the signal from Cartesian coordinates to polar ones, acording to equation 3.1:

$$\begin{cases} a(t) = \sqrt{i(t)^2 + q(t)^2} \\ \phi(t) = \arctan \frac{q(t)}{i(t)} \end{cases} \tag{3.1}$$

However, implementing 3.1 with analogue components and circuits is a subject that requires a whole section to be discussed, and since this transformation is required by both the selected architectures, this subject is approached after the architecture selection, later in this report. For the time being, the polar coordinates are considered to be available.

This analysis is only concentrated in compensating the static (i.e., nondynamic, or memoryless) behaviour of the PA. Let $f_a[\cdot]$ be the static function that maps the input amplitude signal into the PA output amplitude signal (that is the AM/AM characteristic of the PA), and $f_\phi[\cdot]$ the static function that models the phase modification in the PA output complex envelope, according to the PA input amplitude signal (the AM/PM characteristic of the PA). Then, we can define $g_a[a(t)]$ and the static function to be implemented in the APD with the objective of compensating the PA AM/AM distortion (as a function of the input amplitude signal, $a(t)$), and $g_\phi[a(t)]$ the also static function the APD should consider for compensating the PA AM/PM distortion. The relation between the PA and APD static functions that lead to perfect distortion compensation were deduced, and are presented in 3.2. In these relations, G is a constant scaling factor used to scale down the magnitude of the PA output signal, to the level of magnitude of the signals at the PA input.

$$\begin{cases} g_a[a(t)] = f_a^{-1}[Ga(t)] \\ g_\phi[a(t)] = \phi(t) - f_\phi\big[f_a^{-1}[Ga(t)]\big] \end{cases} \tag{3.2}$$

The pre-distorted polar components, produced by the $g_a[\cdot]$ and $g_\phi[\cdot]$ functions, are then applied to a vector modulator, which consists of a voltage controlled variable gain amplifier (VGA) and a voltage controlled phase shifter, which are fed by a local oscillator at the final

RF frequency or, if required, by the component limitations at some IF which would then be up-converted to RF resorting to a mixer and another local oscillator. The complete block diagram of this architecture is depicted in figure 3.1 where the local oscillator is assumed to operate at the final RF frequency.
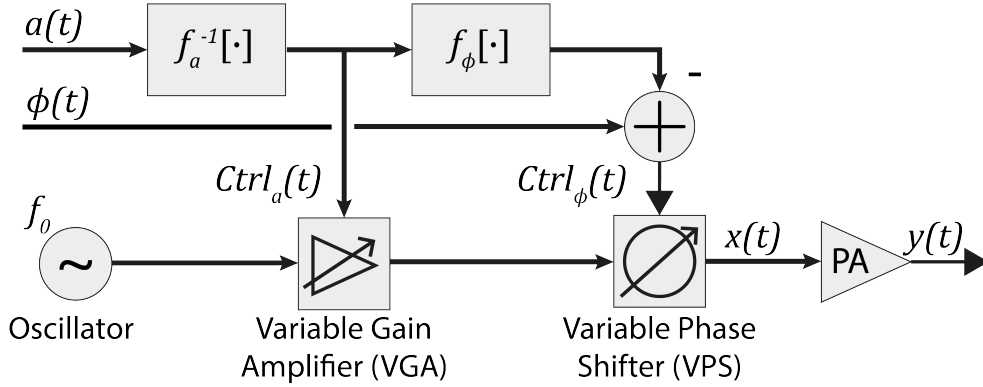
Figure 3.1: Polar analogue pre-distorter with polar modulator

After defining the architecture, it is important to consider the features of the required components. The two components which strongly limit the operation of the polar BB-APD are the phase shifter and the variable gain amplifier, restricting the frequency of operation and the bandwidth. Thus, these two components were the first to be acquired and characterized.

The available components in the market were found to be considerably expensive and with a limited range of options. Despite these limitations, to test the viability of a polar BB-APD, two VGAs and one phase shifter were purchased.

An important characteristic of the VGA is to assess is the gain flatness over a wide range of frequencies of operation, which influences the total bandwidth of the component. The test setup conceived to evaluate this characteristic, shown in 3.2, consisted of a vector signal generator (SMJ 100A) sweeping a wide range of frequencies, with a constant voltage applied to the gain control input. The expected result of this test would be an horizontal line on the vector signal analyser (FSQ3), representing a constant gain over a wide range of frequencies.
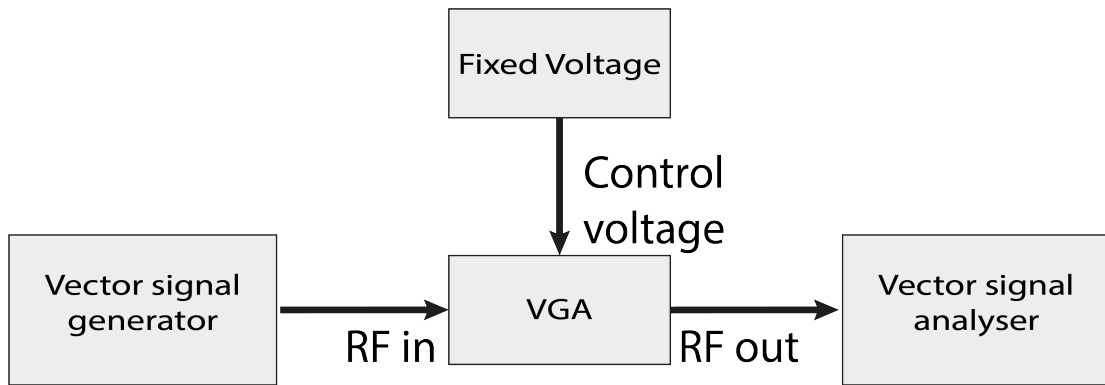
Figure 3.2: Gain over frequency test setup

The test results for both VGAs are depicted in figures 3.3 and 3.4.
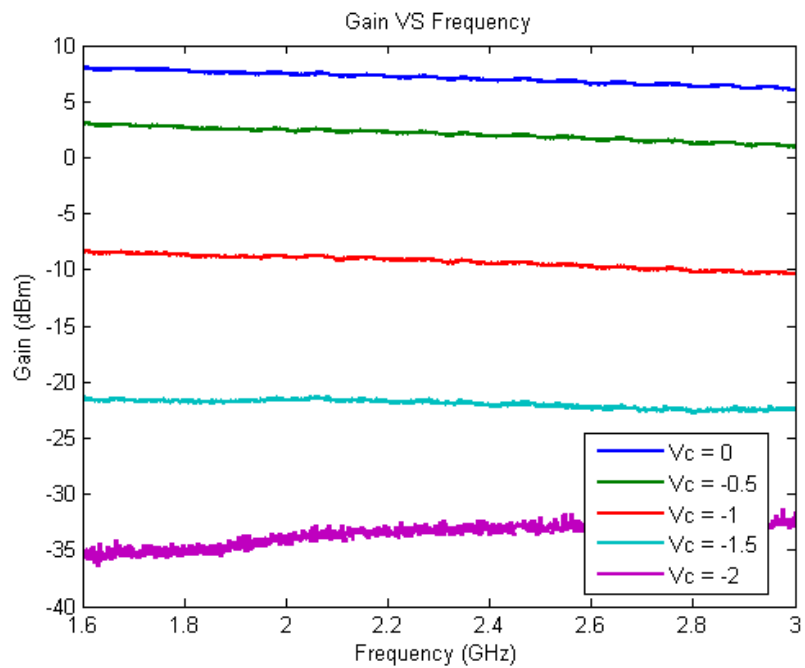
Figure 3.3: MAAM-011000 - Gain vs frequency for several control voltages
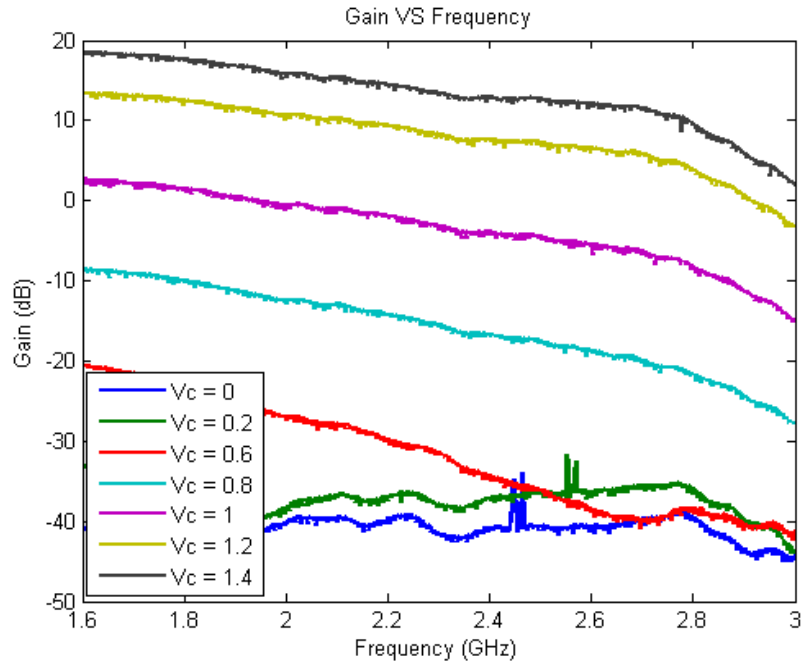
Figure 3.4: ADL5330 - Gain vs frequency for several control voltages

The MAAM-011000 performed better for the selected range of frequencies, it shows a constant gain with small variations over the frequency of operation.

As can be observed in figure 3.1, the APD architecture under analysis assumes the use of the VGA element in a nonstandard way, where the control voltage is changing at the pace of the input amplitude signal. Therefore, to characterise the bandwidth of the control signal, another test setup (depicted in 3.5) was conceived, resorting to a vector signal generation that produced a carrier at the desired frequency of operation (2.6 GHz), a vector signal analyser used as an envelope detector and a baseband signal generator which applied a sinusoidal signal to the voltage control pin of the VGA. In this simple setup, the VGA acted as an amplitude modulator. The goal of this particular test was to determine the maximum bandwidth of the VGA with respect to the voltage control signal, since this information was not clear in the component data-sheet [18].

The results of this test are presented in figures 3.6 and 3.7 for the MAAM-011100 and ADL5330, respectively. Despite having different frequencies, the samples axis of the modulated signals is normalised to facilitate the analysis of the results.

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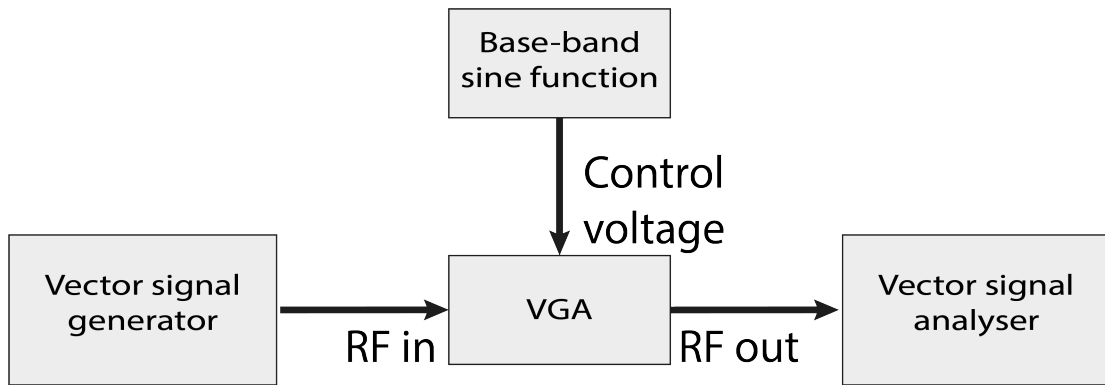
Figure 3.5: Control voltage bandwidth test setup
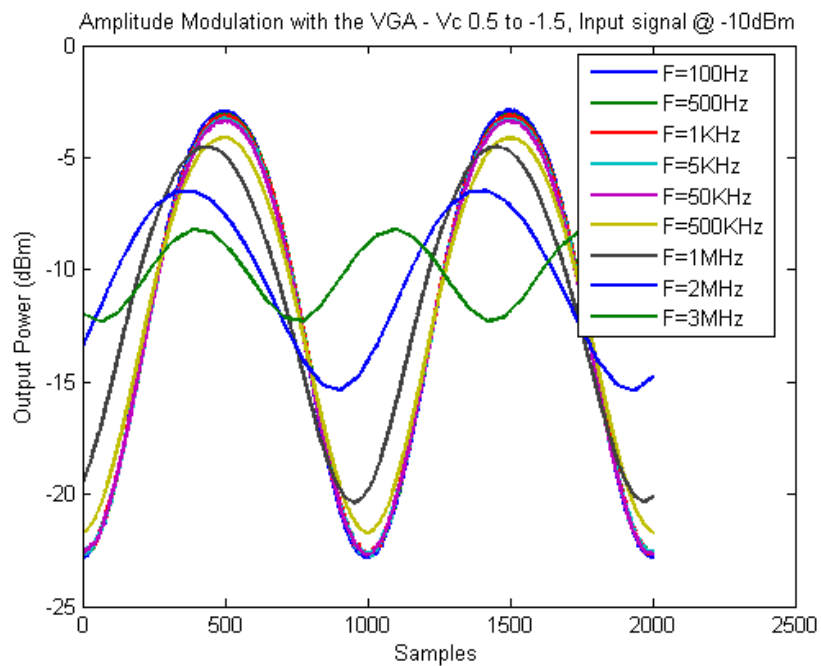
Figure 3.6: MAAM-011000 - Maximum bandwidth of the voltage control signal
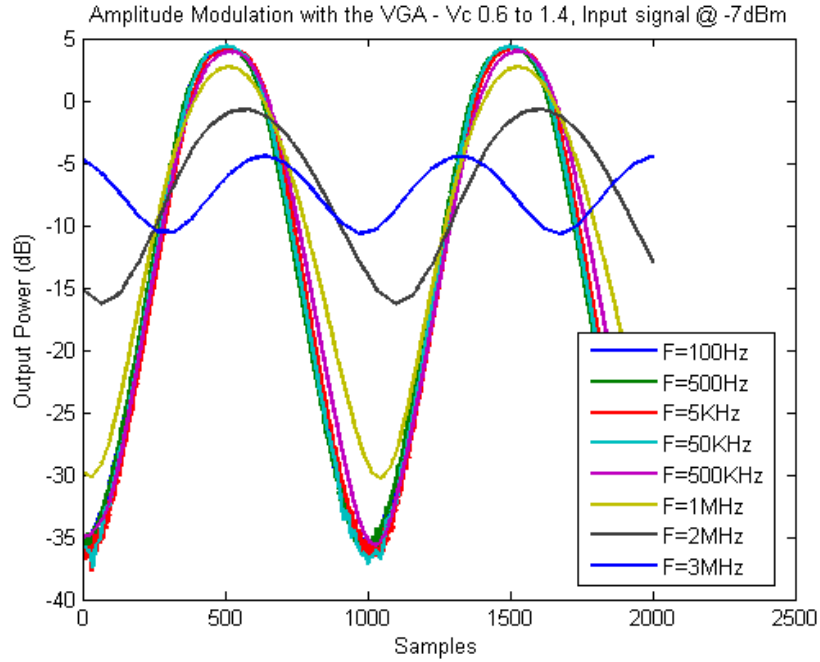
Figure 3.7: ADL5330 - Maximum bandwidth of the voltage control signal

The presented results show a very limited bandwidth for the input signal around 2 MHz. This, alone, represents a great limitation of this architecture. Additionally, there was a severe delay in the delivery of the phase shifter, which combined with the latter, determined the waiver of this architecture.

3.1.2 Cartesian baseband analogue pre-distorter

The second alternative to implement a BB-APD is to apply the distortion directly to the Cartesian components I and Q. By doing so, the necessity of a VGA and a phase shifter is suppressed, eliminating two major limitations and reducing the cost of implementation.

In this architecture, the necessity to obtain the polar coordinates prevails, since obtaining the distortion function is far more simple resorting to these coordinates. However, the distorted signal appears in the form of polar coordinates, therefore, to be modulated using an IQ modulator, it must be converted to Cartesian coordinates again.

The conversion from Cartesian to polar coordinates has been mentioned and is given

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by 3.1. The conversion from polar to Cartesian is given by the relation 3.3:

$$\begin{cases} i(t) = a(t)\cos(\phi(t)) \\ q(t) = a(t)\sin(\phi(t)) \end{cases} \tag{3.3}$$

The complete block diagram of this architecture is depicted in figure 3.8. Although it may appear more complex than the polar BB-APD, the fact that it surpasses the mentioned limitations of the polar implementation represents a strong motivation to pursue this solution.
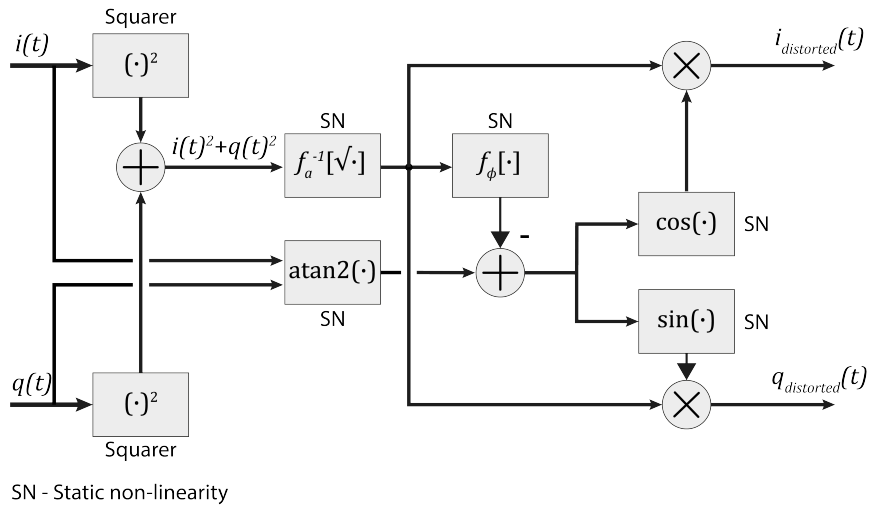
Figure 3.8: Cartesian baseband analogue pre-distorter

Each block of the figure represents an analogue circuit which needs to be planned, simulated and implemented in hardware, since the mathematical function of each block is not usually implemented resorting to analogue circuits. The maximum bandwidth which the system is supposed to support also represents a challenge, and needs to be taken into consideration along the planning of the circuits. Even though there is not a specification for a minimum bandwidth, the goal is, of course, to maximize it.

3.2 Analogue approximation of mathematical functions

Prior to designing the required circuits, it is important to have a mathematical characterization of the required functions. According to the Weierstrass approximation theorem, it is possible to approximate any given continuous function, defined in a real and limited

interval, with a polynomial function to any degree of accuracy. Therefore, polynomial approximations can be used to mathematically define the functions to implement. Moreover, the availability of analogue multipliers with wide bandwidths and the simplicity with which the approximations coefficients can be adjusted represents a great motivation to use this method of approximation.

Usually, the higher the order of the polynomial, the higher the accuracy of the approximation. However, the use of higher order polynomials has limitations.

The intended implementation of the BB-APD, in this work, is with discrete electronic elements, which means that the design can only make use of already available integrated circuits and other discrete components to implement the mathematical functions needed, limiting the number of components used, and therefore limiting the order of the polynomials.

Another issue to consider is the limitation on the approximation coefficients that can lead to saturation in the intermediate approximation signals.

Although there is a vast range of components that can be used, the discrete implementation limits the use of the translinear characteristics of analogue components, such as transistors, since the use of these properties requires the use of strongly matched components. Despite the availability of transistors in the form of matched pairs, the use of those pairs limits the range of available options. Moreover, it strongly limits the scale of the circuit, since the number of matched transistors in a package is also limited. Therefore, the use of high order approximations as presented in [19] is not a viable option. To implement higher order polynomials using two input analogue multipliers requires the use of cascaded multipliers. Considering possible delays in the different paths and the error propagation of the cascade, the error generated by such a solution is not likely to be acceptable.

Achieving a satisfying approximation with low order polynomials of a nonlinear function is only possible if such function has a behaviour that can be modelled by a low order polynomial which, in this application, is rarely the case. To overcome this problem, a possible workaround is to approximate the function with different low order polynomials in different regions, henceforth mentioned to as branch approximation.

Figure 3.9 depicts two approximations: on the left a second order polynomial approximation of the inverse AM/AM characteristic curve and on the right a branch approximation with three branches and a maximum polynomial order of two of the same curve. Maintaining the maximum order of the polynomials, a significant increase of the accuracy was achieved, proving the effectiveness of this method of approximation.
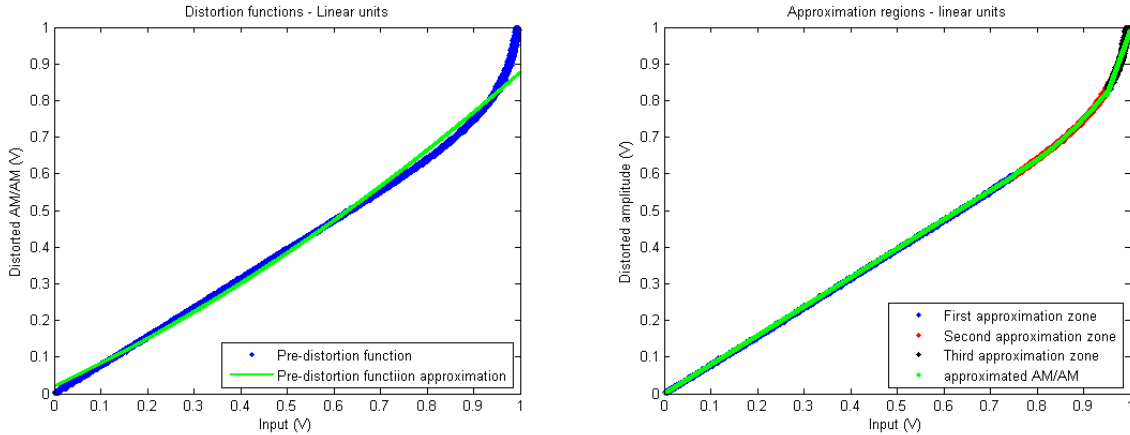
(a) Second order approximation of the inverse AM/AM characteristic

(b) Branch approximation of the inverse AM/AM characteristic

Figure 3.9: Single second order approximation vs second order branch approximation

Using branch approximations to compute the distortion comprises two other major advantages: additional degrees of freedom, and added simplicity on the adjustment of the coefficients.

The additional degrees of freedom allow a fine control of the approximation. For instance, a sixth order polynomial has six degrees of freedom (six coefficients), however, a branch approximation with two branches of second order polynomials has the same six coefficients that can be adjusted and an additional degree of freedom, the point where the switching between branches occurs, providing an additional degree of freedom to the approximation.

Beyond the additional degrees of freedom, which allow more accurate approximations, the simplicity to adjust these approximations is also an important feature of the BB-APD. Reusing the previous example, to adjust a sixth order polynomial there are six degrees of freedom that need to be adjusted simultaneously, this represents a great computational effort. A branch approximation can be adjusted only around the points where it is less accurate, and instead of having to compute a new sixth order polynomial it is only necessary to compute a new second order polynomial which is computationally less complex and therefore faster.

Despite these advantages, the branch approximation approach has a downside. It requires switching between branches which can represent a major issue. Switching between signals at high frequencies can cause peaks in the signal that leads to saturation of the components. Other problem is the switching delay, that is the time that takes to step from

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one signal to another, during which the system delivers unwanted values. Therefore, the switching needs to be as smooth and as fast as possible, even if it requires some degradation on accuracy. The branch approximation approach is, therefore, a viable option if an effort to keep the switching fast and smooth is made.

The following sections describe the planning of the analogue circuits used to approximate each one of the blocks of figure 3.8 accordingly to the previous design considerations.

3.3 Analogue implementation planning

3.3.1 Characteristic functions implementation

AM/AM block

The graphical representation of the AM/AM characteristic function can be obtained from the same PA model mentioned earlier according to the expression 3.2. The PA model to linearise includes an internal noise generator and was extracted from an existing PA available at the laboratory. Figure 3.10 depicts the inverse AM/AM characteristic function for the different amplitude values of the signal.
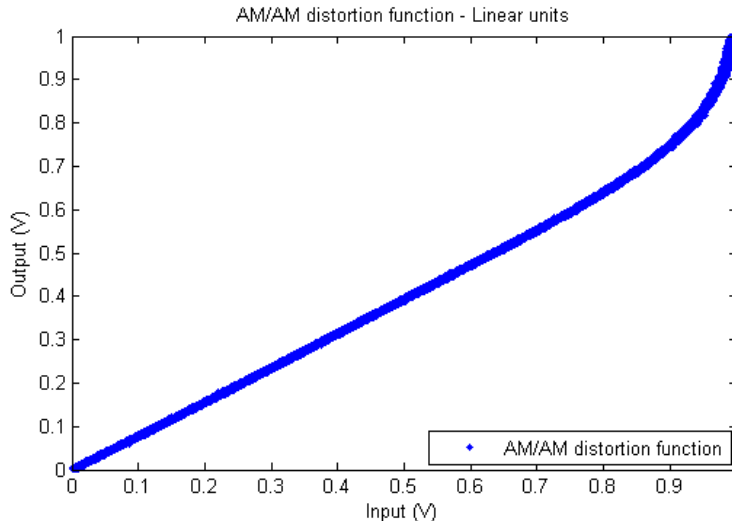
Figure 3.10: Inverse AM/AM characteristic function

As stated earlier, the amplitude values must be obtained from the I and Q components of the signal. As 3.1 shows, the amplitude is obtained with multiplications, additions and a square root operation. Additions are easily implemented in the analogue domain, resorting to OP-AMPs when adding voltages or simply connecting two nodes together when adding

currents. Analogue multiplication is also a well-studied subject and there are many ICs available that perform this operation. The square root operation, however, represents a problem due to the domain restrictions for negative values and an analogue implementation of this function is not trivial. In this particular situation, where approximations are in use, it is preferable to directly include the square root function in the approximation. In that case, the AM/AM distortion function is transformed as shown in figure 3.11.
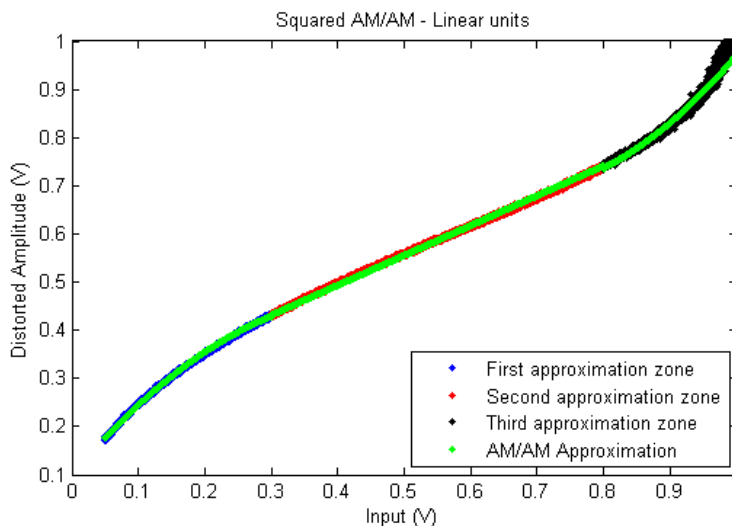
Figure 3.11: Inverse AM/AM characteristic function including the square root of the amplitude signal

The AM/AM characteristic function includes the square root function, hence the signal received by this block is the summation of the squared I and Q signals.

As the figure shows, there are two inflection points in the curve, meaning that if the approximation polynomials were to be of second order it would take at least three branches to achieve an accurate approximation. Using the *MATLAB*'s toolbox *Curve Fitting* to obtain the polynomial approximations, the results obtained are also depicted in figure 3.11.

Input voltage (V_{in}) interval	Approximation function
$[0; 0.05]$	$I_{out} = 0.795I_{in} \quad Q_{out} = 0.795Q_{in}$
$[0.05; 0.3]$	$V_{out} = -1.758V_{in}^2 + 1.625V_{in} + 0.100$
$[0.3; 0.8]$	$V_{out} = 0.620V_{in} + 0.245$
$[0.8; 1]$	$V_{out} = 2.318V_{in}^- 3.000V_{in} + 1.653$

Table 3.1: AM/AM approximation functions

The previous approximation uses four branches to obtain the distortion function, as demonstrated by table 3.1. The first branch consists only on two attenuators on both the I and Q components of the signal since the only function of the BB-APD in this region is to slightly reduce the gain of the PA to match the constant gain needed.

The second and fourth branches are quadratic and the third branch is of first order. The combination of these branches yields a satisfyingly accurate approximation, therefore, this is the pursued solution for the AM/AM characteristic block.

With the approximation method defined, the next stage is to set the guidelines for the analogue implementation. The analogue multiplications are implemented resorting to ICs available in the market. Based on the bandwidth requirements the available options were reduced to the AD835 with a 250 MHz bandwidth [20] and the ADL5391 with a bandwidth of approximately 2 GHz [21]. The decision between these components will depend on the simulation's results, which are described ahead in this report.

The second essential function is addition which, as described earlier, can be implemented with OP-AMPs. Figure 3.12 depicts a simple OP-AMP adder configuration that can be used to perform the addition operation.
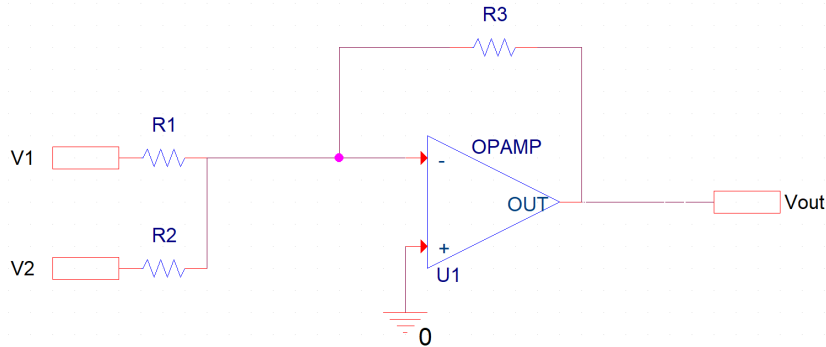
Figure 3.12: Inverting OP-AMP adder configuration

As the figure shows, the adder configuration consists only on the OP-AMP and resistors. The value of the resistors is important since it actively affects the slew rate of the OP-AMPs and can lead to current peaking according the data-sheets of some of the components [22] [23]. Thermal noise related to the resistor values is often relevant, however, the active components introduce higher noise levels than the latter. The thermal noise equation is given by 3.4 where V_n is the noise root mean square voltage, k is the Boltzmann constant, T is the absolute temperature, ΔB is total bandwidth of the signal and R is the value of

the resistor.

$$V_n = \sqrt{4kT\Delta BR} \tag{3.4}$$

As 3.4 shows, the value of the resistors should be kept on moderate values in order to limit the noise in the system. However, the passive components (resistors) have a small contribution to noise when compared with the active ones (OP-AMPs). The active components must be carefully chosen, not only due to the noise introduced in the signal by these components, but also due to bandwidth limitations and offset errors. The slew rate is also an important feature to keep the response speed of the system as fast as possible. After an analysis of the available OP-AMPs on the market, the AD8000, from *Analog Devices*, with 1.5 GHz bandwidth and a slew rate of 4100 V/μs [22] was considered a suitable component for this application. However, this OP-AMP has a current feedback topology. Current feedback OP-AMPs usually have higher slew rates, and lower offset error, however, OP-AMPs of this topology also have disadvantages, such as the low input impedance at the inverting input port which limits the configurations that can be implemented using current feedback OP-AMPs [24]. Due to this disadvantage, a voltage feedback OP-AMP was also selected. The ADA4817 is a voltage feedback low noise OP-AMP, with a bandwidth of approximately 1 GHz and a slew rate of 870 V/μs. Despite being slightly slower than the AD8000, the ADA4817 can be used where the current feedback topology represents a limitation to the circuit, for instance, when a high impedance is required on both inputs of the OP-AMP [23].

Another important operation is selecting the correct approximation branch at every instant. To implement this selection there are several viable solutions, for instance, switching based on the forward voltage of diodes, switching circuits implemented with FET, junction gate field-effect transistor (JFET) or bipolar junction transistor (BJT). Since the adjustment of the switching point is a relevant feature of the circuit, the diode based solution is not viable. Therefore, a controlled switching based on transistors is preferable, moreover, beyond allowing the adjustment of the branches, this solution also simplifies the implementation of the conditional decisions. Due to the existence of more than two branches, the decision of which branch to use is not binary, instead it requires the implementation of conditional statements such as "and", "or" and "not". Figure 3.13 depicts a possible solution to implement conditional statements using transistors.
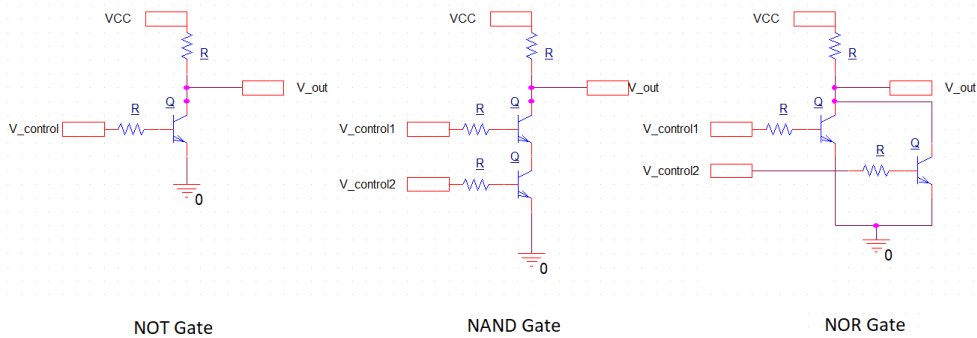
Figure 3.13: Conditional statements using transistors

Even though the transistors used in the figure are bipolar, the decision of which type to use on the implementation of the circuit is clarified in another section of this report, since the simulation results were fundamental for such decision.

The flow of the signal is, as seen above, controlled by the transistors, but the transistors need to be controlled accordingly to the signal value and a reference threshold voltage at each instant. The need to compare two voltages arises. An obvious solution to implement a comparator is to use an OP-AMP in open loop as a comparator. Even though this approach may work on applications where speed is not a primary concern, in this case the time that the OP-AMP takes to switch between levels is a crucial feature. After researching for a faster solution to compare two voltages, a particularly fast comparator IC was selected, the LMH7322 from *Texas Instruments* which has a propagation delay of 700 ps. This comparator allied with transistors with a very high transition frequency, which allows fast switching, consist in a viable solution for the branch selection process.

The complete AM/AM characteristic circuits used for the simulator and hardware implementations are illustrated and described in the respective chapters since there are crucial differences between both implementations.

AM/PM block

The AM/PM characteristic block generates a distortion correction signal that is later applied to the initial phase component of the signal. This block generates a distortion correction signal based on the amplitude of the signal, hence it has one input, the distorted amplitude signal, and one output, the phase distortion correction signal.

Figure 3.14 depicts the response of the phase component of the signal that must be corrected. The relation present in 3.2 describes the process that compensates this phase

characteristic. This process consists on determining the expected phase shift introduced by the PA with respect to the distorted amplitude signal and then subtract this value from the phase coordinate determined in the inverse tangent with two input arguments (atan2) block, as depicted in 3.8.
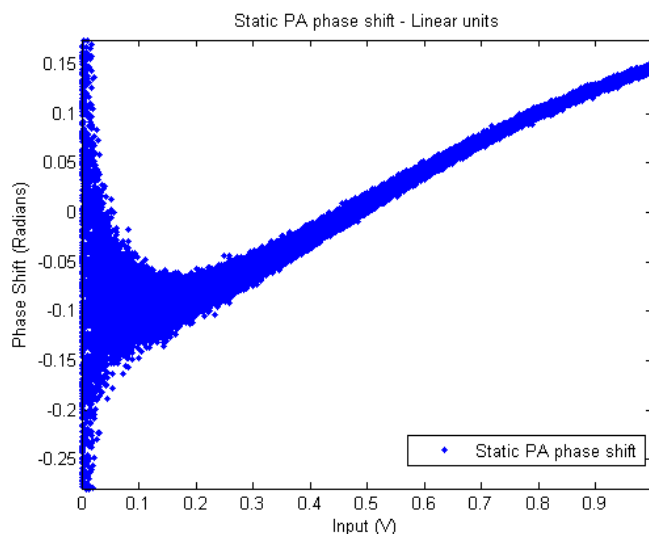
Figure 3.14: PA AM/PM characteristic

In figure 3.14 it is visible that the phase shift introduced by the PA has negative values for the lower amplitude signals, these negative values represent the propagation delay of the signal through the PA and evidently the aim of the AM/PM characteristic block is not to eliminate this delay but to correct the phase advance caused by the PA at higher amplitude values. Since this delay does not need to be considered, the phase shift function is adjusted so that the phase delay at lower amplitudes is null.

Considering the approximation of the AM/PM characteristic, the method used to approximate this function is fairly similar to the method described previously for the AM/AM characteristic. Figure 3.15 shows the different branches of approximation overlapped to the real phase characteristic curve. As stated above, for small values of amplitude the phase shift introduced by the PA is considered to be null, therefore, no phase correction is applied on the signals with amplitude bellow 0.2 V.
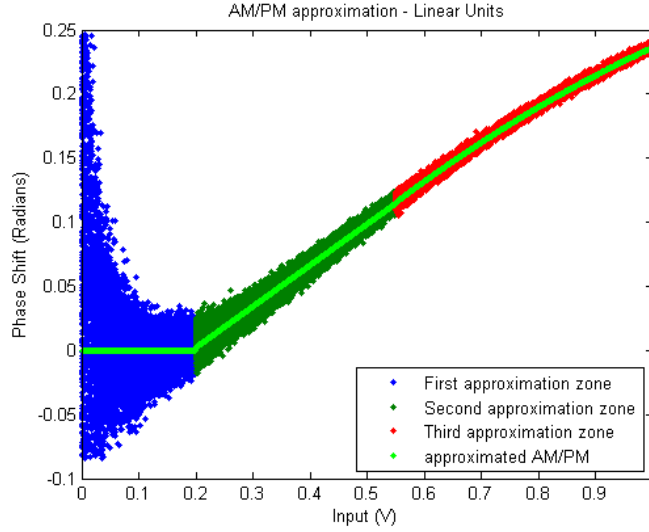
Figure 3.15: AM/PM characteristic approximation

Table 3.2 contains the approximation polynomials used to obtain the approximated curve depicted in figure 3.15. As depicted, three branches were required: one branch uses a second order polynomial and one branches resorts to a first order polynomial approximation. A third branch with null output is used for the lower amplitude values, hence two threshold values are required. Again, the analogue implementation of the circuit strongly resembles the previously described implementation of the AM/AM characteristic block. The ICs used are the same and all the branch selection process is similar, diverging only on the threshold values, which can be adjusted according to the PA's characteristics.

Input voltage (V_{in}) interval	Approximation function
$[0; 0.2]$	$V_{out} = 0$
$[0.2; 0.55]$	$V_{out} = 0.3210V_{in} - 0.062$
$[0.55; 1]$	$V_{out} = -0.1436V_{in}^2 + 0.4911V_{in} + 0.1113$

Table 3.2: AM/PM approximation functions

After obtaining the characteristic function, a simple subtraction needs to be performed to obtain the distorted phase component. An adder OP-AMP configuration can be used to implement this subtraction and obtain the distorted AM/PM.

With both the AM/AM and AM/PM components determined, the next step is to convert the signal from polar coordinates back to Cartesian coordinates. According to

expression 3.3 two more trigonometric functions (sine and cosine) must be implemented using analogue circuits, this process is described below.

3.3.2 Interface with the input signals

As illustrated in figure 3.8, the Cartesian coordinates must be converted to the polar form, the relations are described in 3.1. To obtain the amplitude signal it is possible to use two multipliers to obtain the squared Cartesian coordinates and an adder OP-AMP configuration as the one depicted in 3.12.

The phase signal requires a more complex function to be determined, the following section describes the process of obtaining the phase component.

Inverse tangent function

To introduce a distortion in the phase component of the signal it is necessary to have a signal that is related to such phase. To obtain the phase signal, the relation presented in 3.1 must be implemented using analogue components. The analogue implementation of a single arctan function by itself represents a challenge. However, the function that transforms the I and Q components in the phase component is widely known as atan2, which not only computes the value of the inverse tangent of the quotient between I and Q, but also computes the correct quadrant of the phase based on the sign of the Cartesian components.

As known, the arctan function is only defined in the first and third quadrants with discontinuities in $\pi/2$ and $-\pi/2$ and is depicted in figure 3.16. Figure 3.17 depicts the three-dimensional plot of the atan2 function. These two figures are extremely important to illustrate the complexity of the problem at hand.
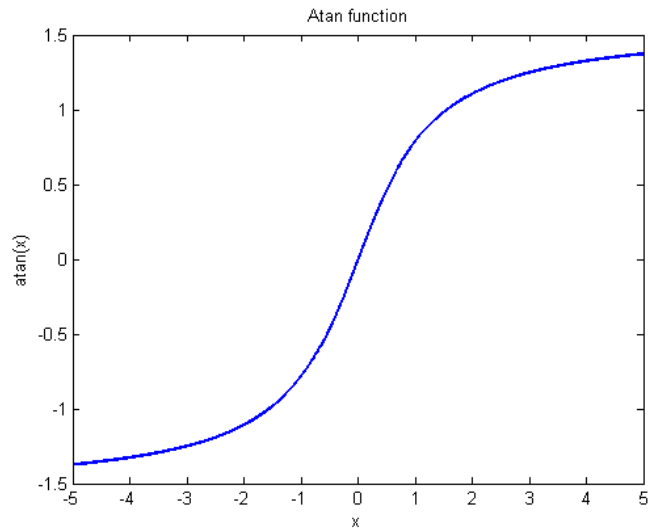
Figure 3.16: Atan representation
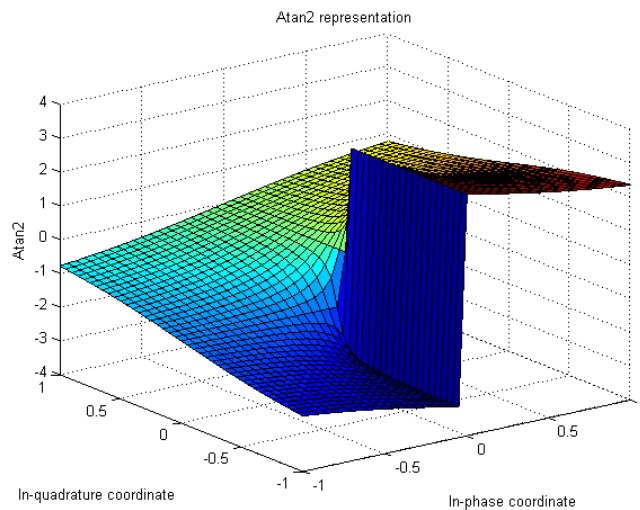
Figure 3.17: Atan2 representation

The first solution, and one that was pursued for a significant amount of time consisted in calculating the quotient of the rectified I and Q signals, then calculating the inverse tangent of that value, obtaining the phase value in the first quadrant and finally based on the sign of the I and Q components translating that value to the correct quadrant.

The inverse tangent can be obtained by using a an OP-AMP with a fixed at $G = \frac{\pi}{4}$, as demonstrated in [25], followed by a soft limiter that limits the signal to a maximum of $\frac{\pi}{2}$. The schematic of such a circuit is represented in figure 3.18.
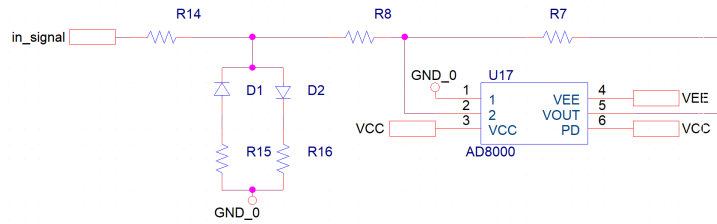
Figure 3.18: Atan approximation circuit

As stated this circuit consists of an attenuator OP-AMP preceded by a soft limiter. The soft limiter consists of two anti-parallel diodes that limit the maximum and minimum voltage between the two resistors that build up the voltage divider. The resistors from the diodes to ground soften the voltage clipping.

A practical implementation of this circuit led to the results depicted in figure 3.19. These results are exceptionally presented in this section because of the limitations of this solution, as described bellow.
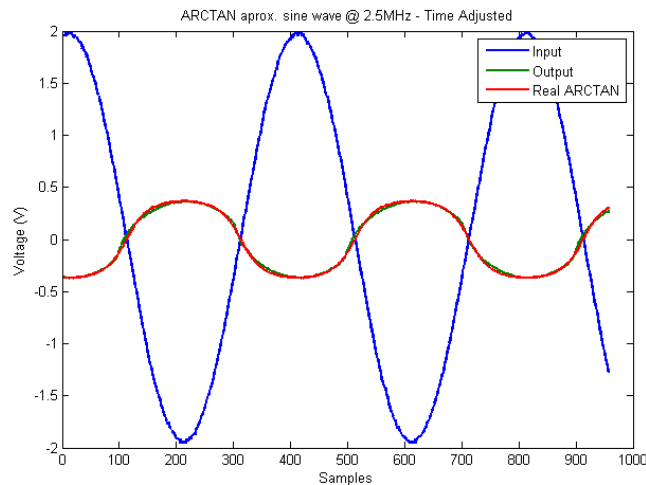
Figure 3.19: Atan approximation results

The translation of the phase values to the correct quadrant could be achieved with a decision circuit similar to the one used in the AM/AM characteristic block, which would control different offset values to be added to the calculated phase value. Table 3.3 contains a summary of the offset values and the transformations required to obtain the phase signal in the domain of $[-\pi; \pi]$ based on the sign of the I and Q coordinates.

I coordinate	Q coordinate	Quadrant	Atan2 transformation
$I > 0$	$Q > 0$	1	$\mathrm{atan}(x)$
$I < 0$	$Q > 0$	2	$\pi - \mathrm{atan}(x)$
$I < 0$	$Q < 0$	3	$-\pi + \mathrm{atan}(x)$
$I > 0$	$Q < 0$	4	$-\mathrm{atan}(x)$

Table 3.3: Offset to obtain the phase angle based on the sign of the I and Q coordinates

The following step consisted on the analogue implementation of the atan function which was accomplished using a fixed attenuator in the form of an inverting OP-AMP and a soft limiter which controlled the response of the signal near the saturation value (approximately $\pi/2$).

The signal to be fed into the atan function is the quotient of the I and Q signals as demonstrated in 3.3. To perform this quotient an analogue divider is required.

The intended implementation for this function was given in an IC's datasheet, the AD834 which is an analogue multiplier with the particularity of having current outputs [26]. However, this analogue implementation of a divider is associated with several problems:

- Due to the domain discontinuity around zero at the denominator, there are two fundamental issues that arise. Firstly, an obvious tendency to saturation at the output signal as the denominator values become closer to zero.

- The second issue is related to amplification of noise that happens when both the numerator and denominator are close to zero.

These issues combined with the fact that the divider circuit did not performed well in simulation determined the rejection of this solution.

Due to the complexity of implementing the dual input inverse tangent function and the time constrains of the project, it was not possible to reach a viable solution to this problem. Despite of having one unsolved function the remaining of the system must be tested, hence the phase signal is assumed to be available hereafter.

3.3.3 Interface with the output signals

Sine function

The sine function is a well-known trigonometric function which has been studied and implemented using distinct approaches. Implementations using the Taylor series approx-

imation have been proposed [19], however, this solution cannot be implemented using discrete component, moreover, the IC solution is not available on the market.

The reason for this void in analogue processing units and other components is undeniably related to the widely used digital processing units and the dominant digital predistortion techniques.

Even in the digital domain, the sine and cosine functions represent a challenge due to the time and complexity associated with them. Therefore, there is much literature discussing faster algorithms and approximations to implement these functions. Even though said literature is focused in digital implementations, some of the simplifications described can also be applied in the analogue domain.

A possible approximation, and one that particularly resembles the approximations implemented so far, consists on approximating the sine function using two quadratic functions. Using the tool *Curve fitting* the approximation given in 3.5 is obtained.

Since the sine function is circular, the domain to consider can be $[-\pi; \pi]$, therefore, it is important that the phase signal previously discussed is defined in the same domain. The selection of this domain yields an important advantage: the switching between branches occurs on the zero-crossing point, where both the input and the output of the sine function are zero. This can help to mitigate possible switching spikes and errors. Even though this solution (switching at the zero crossing point) was not possible in the prior approximations, it is important to make use of this property when possible.

The sine function is approximated according to 3.5. Figure 3.20 depicts the implemented approximation overlapped with the real sine function, providing a visual proof of the accuracy of this approximation.

$$\sin(x) \approx \begin{cases} 0.41x^2 + 1.27x, & if \ x < 0 \\ -0.41x^2 + 1.27x, & if \ x \geq 0 \end{cases} \tag{3.5}$$

48
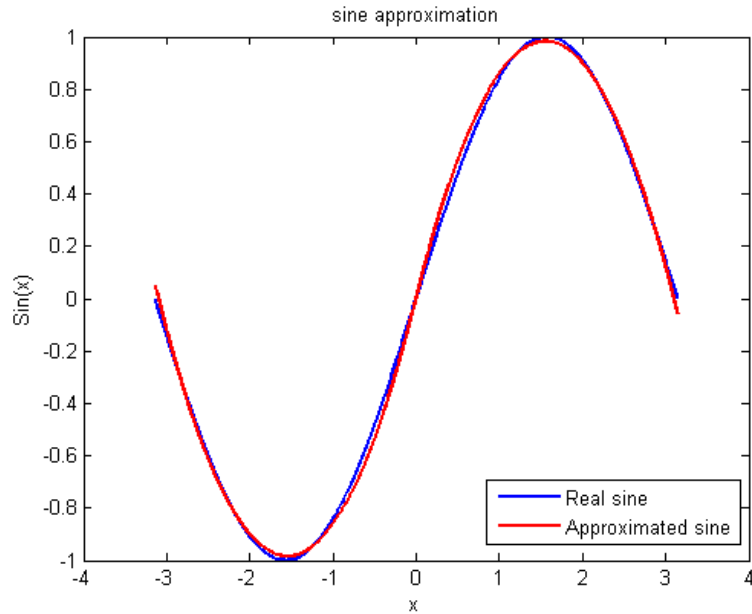
Figure 3.20: Sine approximation function

The determination of the polynomial functions is performed, as previously, using analogue multipliers and adders.

The switching in this case is binary (there are only two branches of approximation) and the threshold is located at zero, allowing a different implementation of the switching circuit, however, for simplicity reasons and to better make use of the time spent designing and simulating the previous implementation, this block uses the same switching implementation.

The complete circuit is described in the following chapter where the simulation results are also presented.

Cosine function

The tendency along this report has been to reuse as much of the work previously produced as possible. To implement the cosine function, instead of researching viable approximations or using *MATLAB*'s toolbox *Curve Fitting* to obtain new polynomial approximations, it was preferable to take advantage of the circular properties of the sine and cosine functions. Therefore, the cosine function is defined as a shifted sine accordingly to 3.6, this means that by adding an offset to the phase signal the cosine function is obtained using exactly the same approximation as the sine function. The flowchart depicted in figure 3.21 provides a better illustration of the conditional statements and the domain shifts

required.

$$\cos(x) = \sin\left(x + \frac{\pi}{2}\right) \tag{3.6}$$
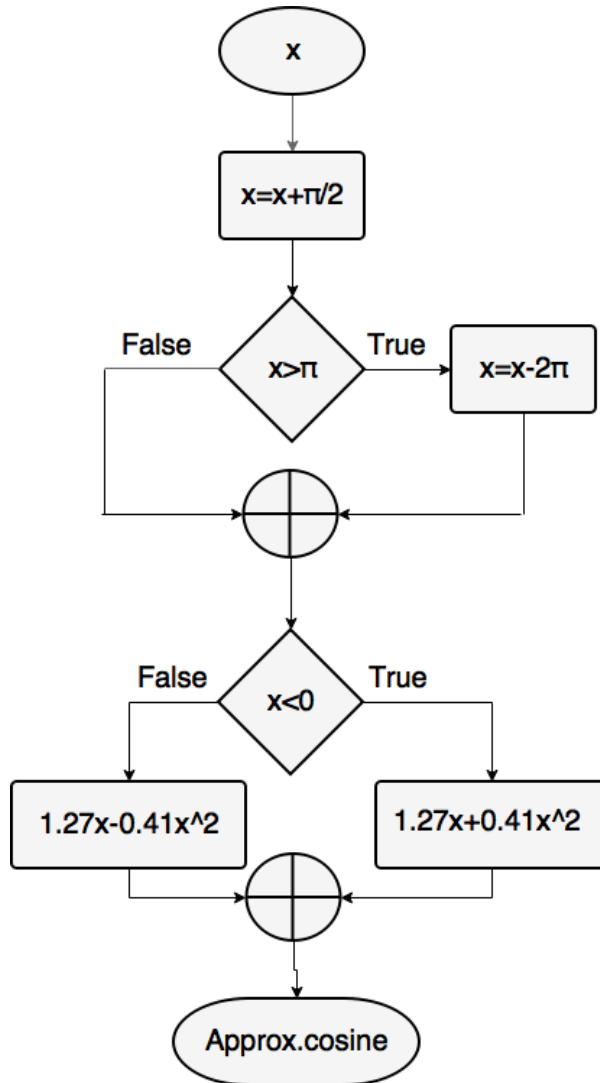
Figure 3.21: Sine to cosine transformation flowchart

The decision circuits are also implemented according to the previously described and since this chapter seeks to simply define the architecture and define guidelines for the implementation, the circuits are furtherly explored in the following chapter.

Chapter 4

Simulator Implementation

Prototyping is very costly, both monetarily and timely, especially when the components used are designed to operate at high frequencies, where the use of a breadboard is impossible and a new PCB is required for each iteration of the circuit. Moreover, it can be said that there exists a strong relation between the cost of the components and their bandwidth, which furtherly increases the cost of prototyping. It is, therefore, very important to have simulation tools that allow a prediction of the behaviour of the circuits, enabling the ability to detect bugs and solve problems in the circuit beforehand.

Each block of the BB-APD must be simulated and the results analysed carefully before a practical implementation of the circuits. This chapter describes the implementation of the planned circuits on a simulator tool, exposes the problems and drawbacks encountered and describes the process of solving or mitigating those issues.

The simulations were implemented in simulated program with integrated circuits emphasis (SPICE) using the tools from *Cadence*. This type of simulator was chosen due to the existing models of most of the components selected. Other tools such as advanced system design (ADS) could be used, however, due to the referred wide availability of simulation models and prior familiarity to the SPICE tools, the option to use the latter was made.

It is also relevant to mention that the designing process took several iterations until the final circuits were produced, however, this chapter does not present a description of all those iterations, as it would be a dense process and would not add valuable content to the report. Instead, an iteration considered to be more important is briefly mentioned and the final circuits are carefully described.

4.1 AM/AM compensation block

Maintaining the structure of the previous chapter, the first block discussed is the AM/AM compensation block. Being the first block to be designed, it was also the one which took more iterations to complete.

An important observation is that the simulation of this block considers the availability of the amplitude signal instead of the squared amplitude signal. The justification for this option are the problems with the model of the analogue multiplier described ahead. The hardware implementation of the AM/AM compensation block considers the use of the squared amplitude signal as described in the previous chapter.

4.1.1 First iteration - A current based implementation

One of the greater concerns when designing this block was the possible saturation of the internal signals. This led to the conception of a circuit based on current signals which have greater immunity to saturation. The advantages of this approach are not limited to the latter. Currents are also easier to add and subtract which is accomplished simply by connecting all the signals in a common node.

However, such an implementation would require several current mirrors, which must be implemented with strongly matched transistors, a fact that, as stated earlier, represents a great limitation in component selection process. The conversion from voltage to current requires extra OP-AMPs.

Another issue with this implementation is the complexity of the resulting circuit. Being a first iteration it can, surely, be refined.

4.1.2 Second iteration - A current-voltage mixed implementation

The dominant issue with the latter approach is the use of current mirrors, which only served to replicate a current and apply it to different paths of the circuit. As known, a voltage at one point of the circuit can be taken by simply connecting each path to the intended voltage node (assuming that impedance loading effects are minimized). By doing so, the need for the current mirrors is supressed.

The concerns with saturation, however, are enhanced when the internal signals are represented by voltages. The signals that are more likely to saturate are all the terms of the approximation polynomials due to the multiplication by a coefficient, which can lead to significantly larger signals that can ultimately saturate the components.

A viable solution is to use voltages for the majority of the signals, and currents for the ones multiplied by a coefficient. Furthermore, the signals that are multiplied by a coefficient are always part of a polynomial, which means that they are always part of an addition. Considering the inverting adder configuration of an OP-AMP, depicted in figure 3.12, there is an evident conversion from voltage to current of each term of the sum, then all the currents are added together at the common node and, finally, the resulting current is converted back to a voltage by the feedback resistor.

This simple configuration brings several advantages. The most evident is that it enables the possibility to have voltage and current signals in the same circuit. Secondly, the coefficients are determined by the values of the resistors, suppressing the need for additional active components. And finally, since the coefficients are determined by the value of the resistors, it is possible to adjust them using potentiometers or digitally controlled trimmers. The latter solves an issue that was yet to be approached, since the system needs to be reconfigurable accordingly to the operation conditions.

The circuit represented in 4.1 implements one branch of approximation with a second order polynomial expression. The squared term is obtained by the AD835 at the W pin, which receives the input signal at the X and Y inputs. The Z input adds an offset to the signal, hence is connected to ground. X1 and Y1 represent the positive inputs. X2 and Y2 represent the negative inputs.The input signal is fed into the X1 and Y2 inputs to provide the inverted square of the input signal (the inverted squared signal was required for this particular approximation).

The squared signal, the input signal and the independent voltage are added together by the inverting adder OP-AMP.
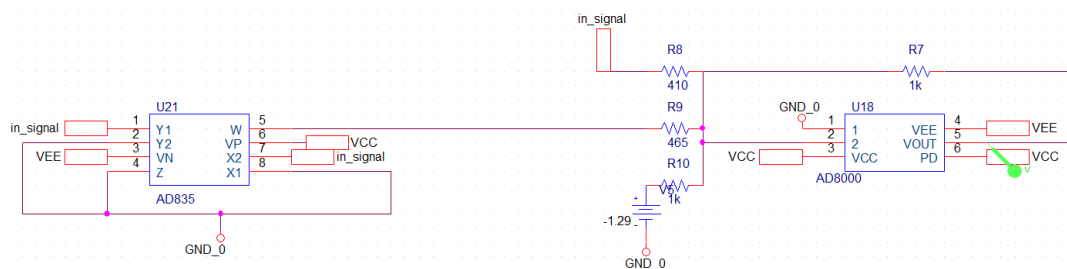
Figure 4.1: AM/AM circuit - one branch calculation circuit

Figure 4.2 shows the simulation result for a sine wave with 1 MHz frequency at the input. To prove the accuracy of the circuit, the image also contains the expected signal (obtained with *MATLAB*).
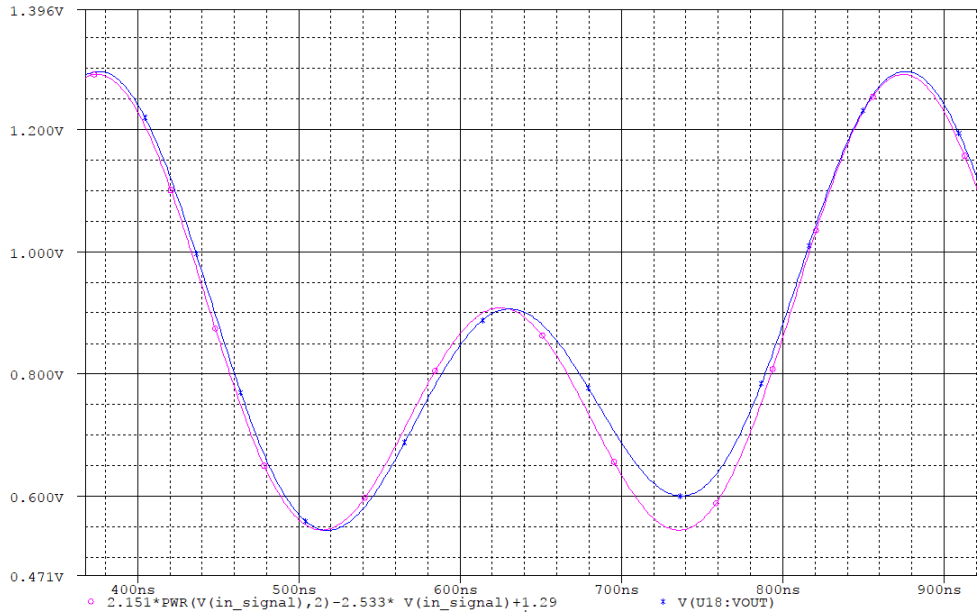
Figure 4.2: AM/AM circuit - one branch test

This simple test illustrates the viability of this solution. The multiplier model used corresponds to the AD835 which proved to work perfectly at this frequency, however, for higher frequencies this IC represents a limitation due to its group delay and pour dynamic characteristics, which deteriorate the overall approximation. Due to the different paths of the signal having different analogue components, each component needs to be as fast as possible to minimize the effects of adding signals slightly out of phase. Even though the slightly different propagation times can be compensated, the pour dynamic characteristics are difficult to improve. Another available multiplier is the ADL5391 that, accordingly to the data-sheet, has a group delay of 0.5 ns and a bandwidth of 2 GHz [21]. Unfortunately, there is not a SPICE model available for this component which prevents simulating using this component. Nevertheless, the performance of this component was verified using the evaluation board, and regardless of simulating the circuits using another multiplier, the ADL5391 is the one used in the practical implementation.

The implementation described above sets the base architecture of the AM/AM compensation block. To obtain the full design, this circuit is repeated for each branch. However, prior to describe the complete circuit, there is an important section that must be independently studied: the branch selection circuit.

To select the correct paths that must pass through the adder there are two essential components: the comparators and the switches.

To compare a signal, a simple OP-AMP in an open loop configuration can be used.

However, due to the internal circuitry of the OP-AMPs the saturation recovery time is considerable. Moreover, the voltage swing from one saturation voltage to the other depends on the slew rate. Considering the ADA4817, which has a slew rate of 870 V/μs, if the supply voltages are ±5 V, the saturation voltages are approximately ±3.5 V. The voltage swing time is approximately 8 ns. Combined with the saturation recovery time of 8 ns, the comparator would take approximately 16 ns to change the state. The switches (transistors) also take time to alter between operation states, namely from saturation to cut-off for BJT. Using an OP-AMP as a comparator would create a great limitation to the signal's bandwidth.

Using an IC design to perform comparisons yields a significant improvement on the switching times and consequently on the achievable bandwidth of operation. The LMH7322 from *Texas Instruments* is a comparator with adjustable output levels with a total propagation delay of 700 ps, representing a faster solution than the OP-AMP comparator. Despite the availability of the SPICE model of this component, it was not possible to overcome some problems that arose when trying to use it in the simulation. As an alternative, an ideal OP-AMP model was used as a comparator in the simulation.

The second essential component to implement the decision circuit is the switch. A switch can be easily implemented using a transistor. This application requires a fast and smooth switching. The speed is important to maintain the achievable bandwidth as wide as possible. Having a smooth switching means that the transitions between the on and off states have no current or voltage peaks and other irregularities, such as capacitances charging and discharging.

The selection of the transistor must take the following characteristics into consideration:

- High Transition frequency which is a good metric to evaluate the speed of the transistor;

- Small stray capacitances and inductances which influence both the speed and the switching smoothness;

- Breakdown currents and voltages appropriate for this application;

- The availability of a complementary transistor indicated by the manufacturer, which is important to guarantee a similar behaviour of the circuit regardless of the current direction;

- The availability of a SPICE model.

Based on these characteristics the BFT93 and the BFR93 were selected, these transistors have a transition frequency (f_t) of 5 GHz [27] [28] which means that the switching speeds are acceptable for the application here reported. Furthermore, the breakdown voltages and currents allow a comfortable range of the operation conditions.

The transistor is used to control the current that flows into the adder OP-AMP. The most common configuration consist on connecting the signal to the collector, the adder circuitry to the emitter and the control signal to the base of the transistor as figure 4.3 depicts.
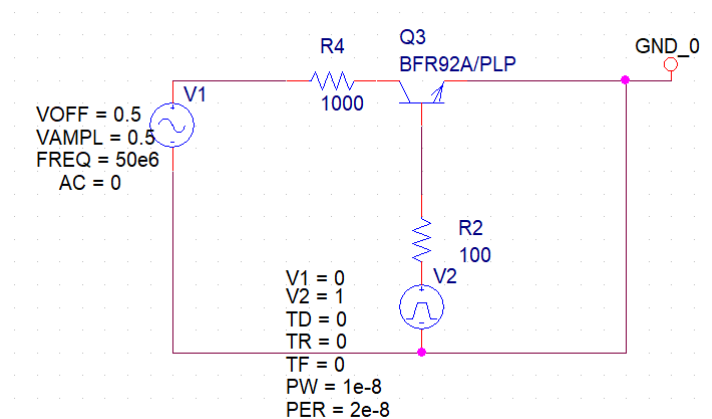
Figure 4.3: Common switching circuit

The simulation revealed some expected problems associated with this switching method. Due to the internal capacitances of the transistor, the currents observed at the emitter contain considerable peaks. These current peaks if fed into the adder circuit can easily saturate or, in the worst-case, damage the OP-AMP. It is extremely important to mitigate the current peaks.

An alternative switching configuration consists on connecting the transistor's emitter directly to ground and the collector to a point in between the first adder resistor which is, in this case, divided in two resistors. Similarly to the first switching method, the control signal is applied to the base of the transistor. The circuit is depicted in figure 4.4 which provides a better description of the configuration.
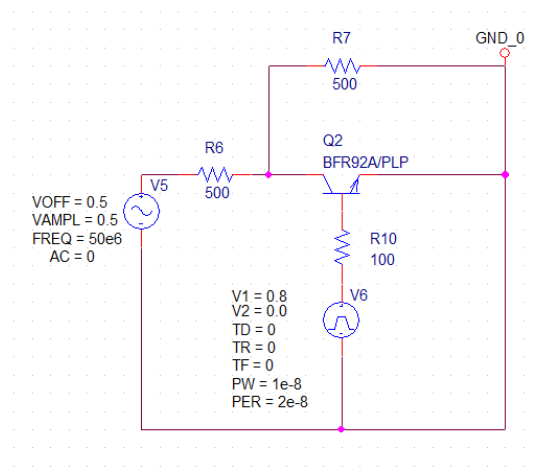
Figure 4.4: Alternative switching circuit

The voltage signal is converted to a current signal at the first resistor. If the transistor is conducting, the majority of the current flows through the transistor into ground, allowing a residual current to be fed into the adder. If the transistor is off, the two resistors are seen as a series and together determine the addition weight, in this case the polynomial coefficient.

This solution is not perfect. There is a loss in accuracy due to the residual currents that flow into the adder when the transistor is on. However, this loss in accuracy can be compensated when adjusting the coefficients.

The simulation of both configurations is presented in figure 4.5.
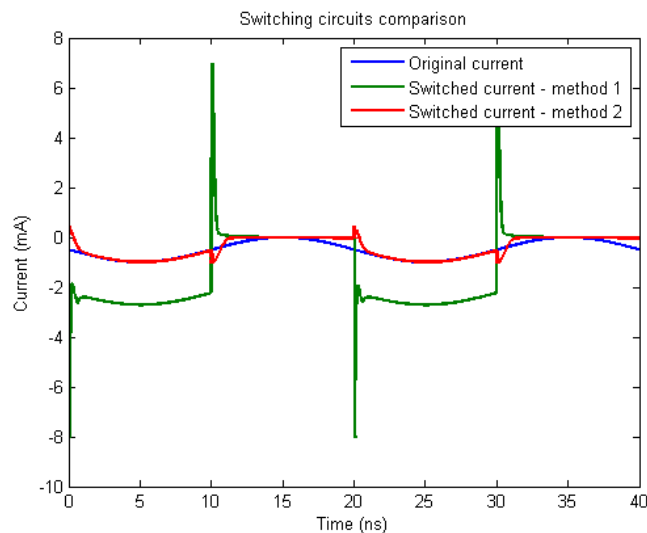
Figure 4.5: Switching circuits comparison

As shown in the figure, the current peaks are significantly smaller for the second method. Furthermore, the second method also eliminates the offset currents that flow from the transistor's base which are visible on the first method waveform.

An important note to this circuit is that the conditional control statements need to be inverted. When the transistor is on, the signal does not go into the adder. When the transistor is off, the signal goes through the adder.

The combination of the priorly described circuits results in the complete AM/AM compensation block. The complete circuit is depicted in figure 4.6. The values of the polynomial coefficients, calculated for the linearization of the static PA model described in section 2.2, are organized in table 4.1, alongside with the corresponding resistor values (R_j) calculated according to expression 4.1 and considering a value of 4700 Ω for the adder's feedback resistor (R_f). The selection of this value allows the coefficient resistors to be higher reducing the residual currents that flow into the adder when the transistor is on.

$$R_j = \frac{R_f}{Coef} \tag{4.1}$$

Branch of approximation	Order of the coefficient	Coefficient value	Calculated resistor (Ω)	Used resistor (Ω)
First	First	0.7919	5935	5900
Second	Second	2.151	2185	2180
Second	First	2.533	1850	1850
Third	First	3.477	1350	1350

Table 4.1: Coefficient resistor based on a 4700 Ω feedback resistor
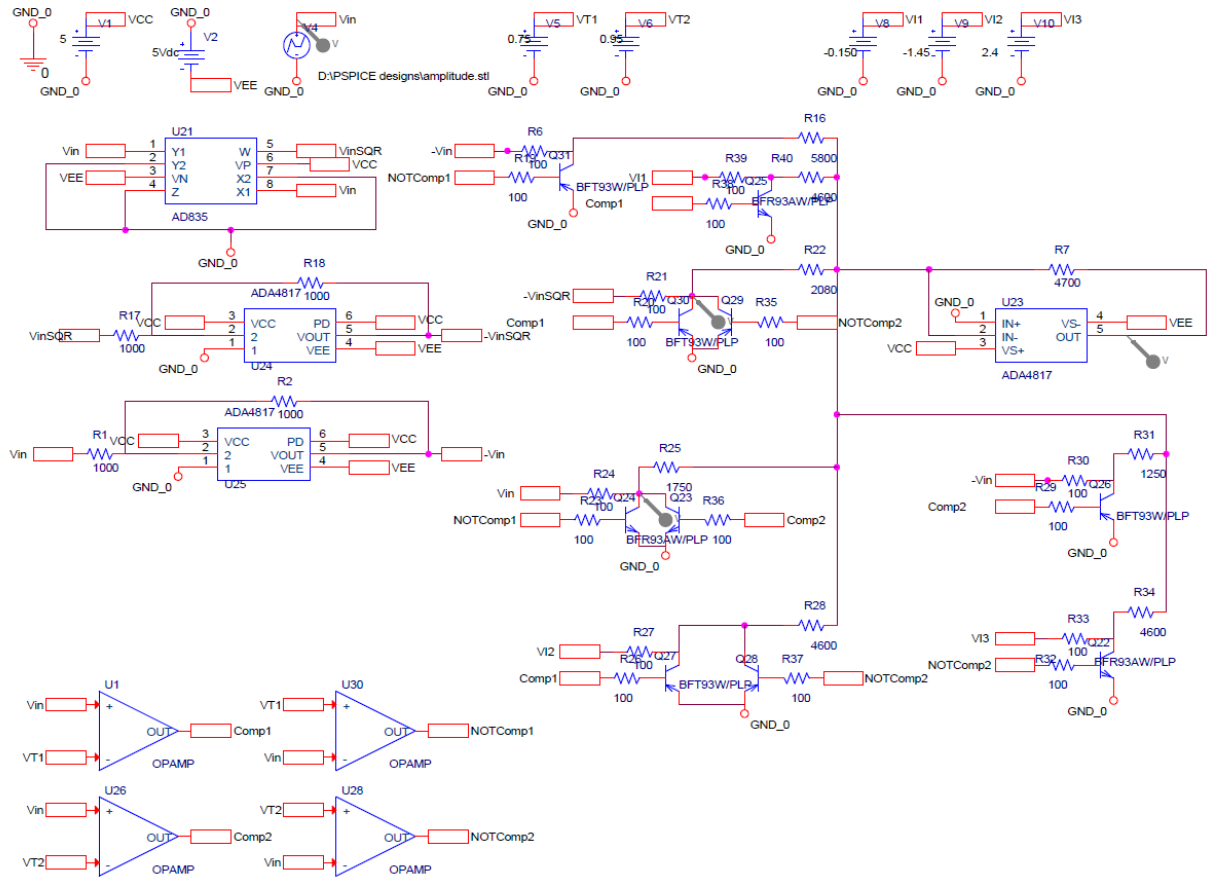
Figure 4.6: AM/AM distorter - complete circuit

As table 4.1 shows, the values of the calculated resistors are slightly different from the used ones. The values of the introduced voltages are also different from the calculated ones. These differences are due to the adjustments made to obtain the required functions. To adjust the resistors, a simulation with a direct current (dc) sweep with the values of the input signal was made. The final results are represented in figure 4.7 and are overlapped with the MATLAB polynomial approximations.

With a precise calibration achieved, the AM/AM compensation block is complete. The performance of this block is depicted in figure 4.8 where the pre-distorted signal, captured from the SPICE simulation into *MATLAB*, is applied to the PA model.
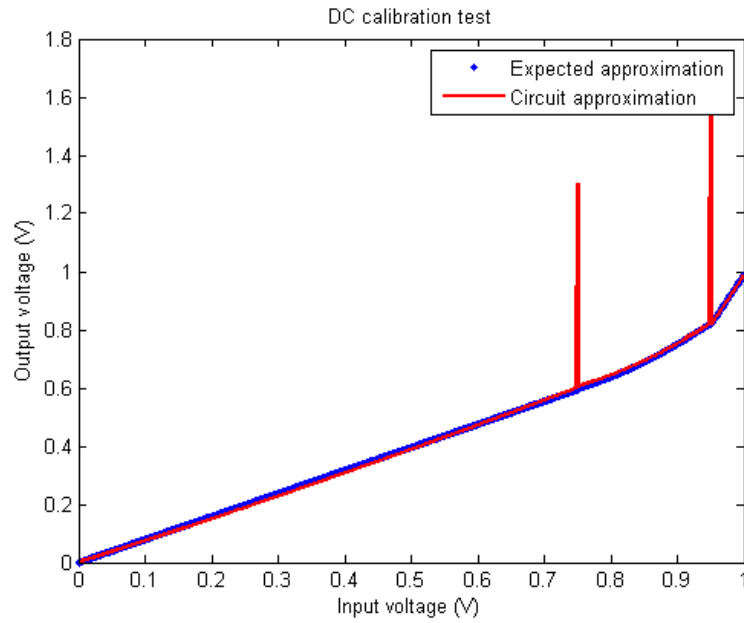
Figure 4.7: DC sweep calibration
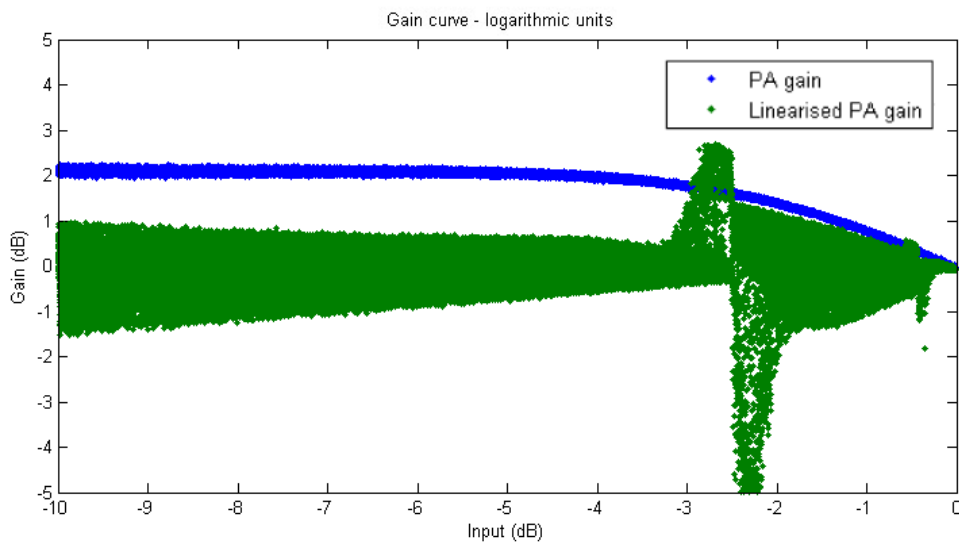
Figure 4.8: Linearised gain

There is a visible increase in the thickness of the output data cluster that is due to poor dynamic characteristics of the circuit, and arise due to the sharp edges created by the switching circuit. However, the considerably worse response in the second branch of approximation was unexpected. In that region, the gain presents a higher variation

than expected. A careful analysis of the simulation determined that the cause of this expansion of the gain curve is due to the analogue multiplier used, which has limited dynamic characteristics.

The peaks around the switching levels were expected and prove that even though the switching solution works, it represents a limitation to the overall performance of the APD.

The second branch of approximation is the only one with a second order component and the multiplier used in this simulation, the AD835, has a settling time of 20 ns [20]. The delay introduced by this IC results in an addition with slight phase differences among each signal component, leading to the deterioration of the approximations. This result determined the use of the ADL5391 in the practical implementation, which, according to the data-sheet, has a settling time of 2 ns (ten times faster than the latter) and a group delay lower than 1 ns. The use of the ADL5391 is expected to provide a considerable improvement on the linearised gain curve. Unfortunately, a SPICE model of this faster multiplier is not available, limiting the simulation results to the previously presented.

Even though the previous implementation used the ADL5391, it was considered important to have a simulated alternative circuit with proven performance.

Since the inaccuracy was proven to arise from the multiplier, a new set of polynomial approximations was determined. To avoid using multipliers, only first order polynomials were used. Table 4.2 summarises this new set of approximations as well as the threshold voltages of the new branches.

Input voltage (V_{in}) interval	Approximation function
[0; 0.8]	$V_{out} = 0.7947V_{in}$
[0.8; 0.95]	$V_{out} = 1.214V_{in} - 0.34$
[0.95; 1]	$V_{out} = 3.477V_{in} - 2.488$

Table 4.2: AM/AM linear approximation functions

The approximation results are depicted in figure 4.9. Clearly, there is a reduction in the accuracy of the approximations, however, considering the additional simplicity of the circuit and the possibility to avoid multipliers, the SPICE simulation was important.
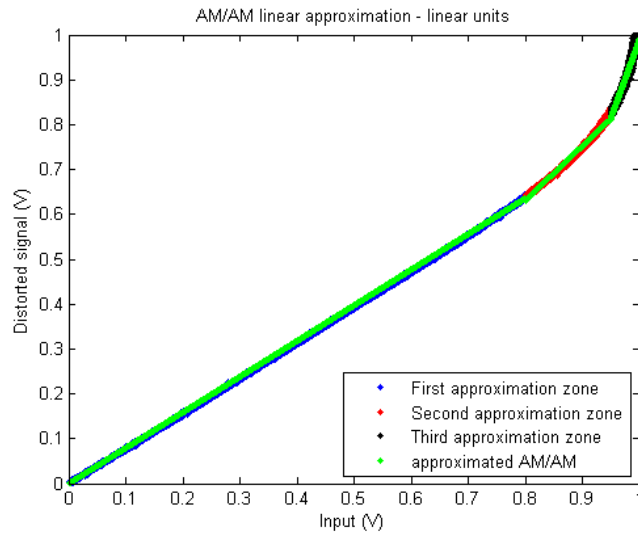
Figure 4.9: First order approximation

Figure 4.10 contains the results of the resulting linearised gain curve. The gain variations are similar in the first and third branches, however, the second branch results are considerably improved relatively to figure 4.9. The reduction of the approximation's accuracy is visible on the curvature present on the second branch of approximation. Nevertheless, this solution yields better results than the latter.
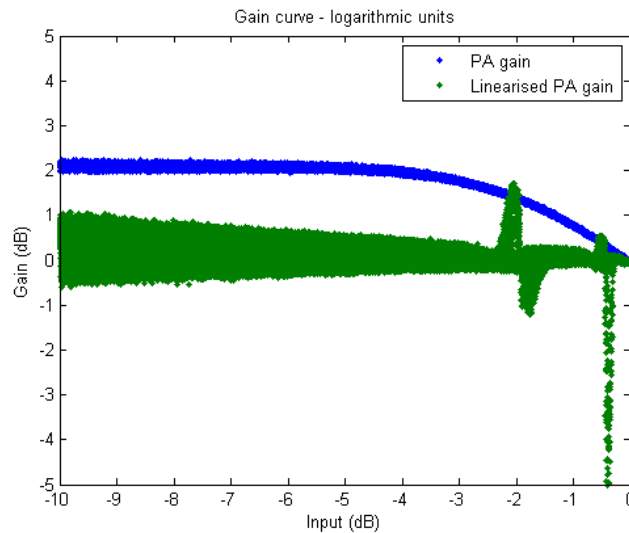
Figure 4.10: Linearised gain with first order approximations

4.2 AM/PM compensation block

The simulation of the AM/PM compensation block follows the same structure as the simulation described in the previous section. The approximations presented in chapter 3 contain second order terms, rising the same concerns as the observed in the AM/AM compensation block.

Nevertheless, to maintain a coherent structure, the simulation results with the second order terms are depicted in figure 4.11. The circuit used to simulate this block is identical to the previously illustrated for the AM/AM compensation block on figure: 4.6.

The overall description of the circuit has been detailed in this report, however, there are two important aspects that must be noted.

As shown on table 3.2, the first zone of approximation does not apply phase corrections, that is, for input powers below -14 dBW the output of the phase compensation block should be zero. It would be expected that in this branch of approximation there would be no signal going through the adder however, due to the residual currents that flow from the other signal paths and the saturation voltage of the control transistors, the output voltage in this region is not null. There are two signals present in this branch: one constant signal to compensate offsets introduced by the saturation of the transistors and one signal proportional to the input that compensates the residual currents. By introducing these two signal paths, it is possible to mitigate a considerable error and two more degrees of freedom are added to the system, improving the possibilities of adjustments according to the operation conditions.

The second important aspect is that the usual phase correction is typically low. The characterization of the PA model used in the simulations revealed a maximum phase adjustment of approximately 9°. Since the phase distortion is applied on the phase signal itself, it is necessary to have the 360° of the phase signal converted to a voltage excursion that should not be higher than 4 V. This limitation in signal excursion is imposed by the maximum operating voltages and the slew rate of the components. This means that the phase distortion signal would have a maximum excursion of 100 mV. The problem is that the noise and signal errors are set by the components and are very difficult to reduce. For instance, the ADA4817 introduces an offset error of 20 mV, which represents an unacceptable error. For this reason, the phase distortion signals are generated with three times the expected value and are later attenuated by the same factor at the addition process. The selection of a factor of three is due to the fact that this factor approximates the coefficients of the first order terms of the approximation to one, hence the distorted amplitude signal is not amplified nor attenuated, maintaining this signal as close to its original value as

possible, as shown in table 4.3.

Input voltage (V_{in}) interval	Approximation function
$[0; 0.2]$	$V_{out} = 0$
$[0.2; 0.55]$	$V_{out} = 0.963V_{in} - 0.186$
$[0.55; 1]$	$V_{out} = 0.431V_{in}^2 + 1.473V_{in} - 0.334$

Table 4.3: AM/PM approximation functions multiplied by three

After a calibration process identical to the previouslly described, the circuit was simulated. The simulation results are presented in figure 4.11. Similarly to the AM/AM compensation block, the second order terms introduce errors due to the delay present in this signal path.
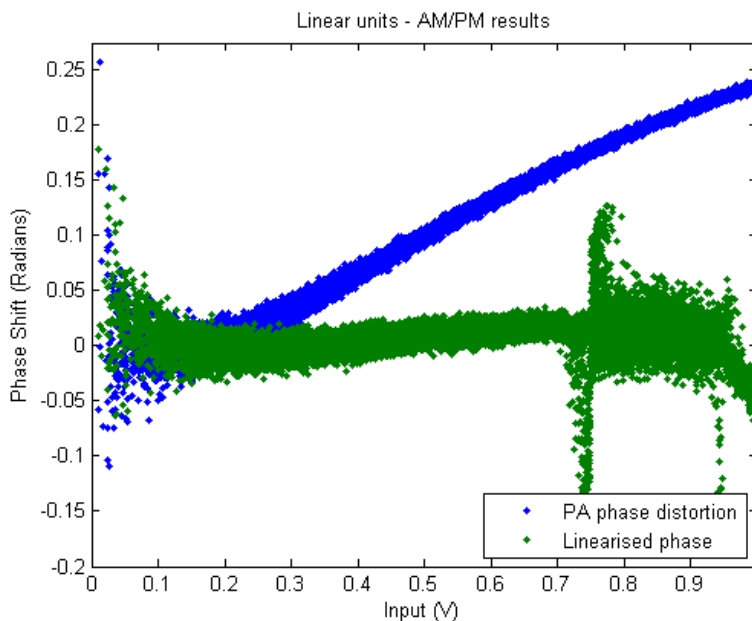
Figure 4.11: Linearised phase

An alternative solution which allows better simulation results is to obtain first order approximations of the phase characteristic function. As stated above, this procedure reduces the errors introduced by the second order terms at the expense of the approximation's accuracy. The new approximation polynomials are summarized in table 4.4. The multiplication by a factor of three is also used with these new set of approximations.

Input voltage (V_{in}) interval	Approximation function
$[0; 0.2]$	$V_{out} = 0$
$[0.2; 0.8]$	$V_{out} = 0.960V_{in} - 0.186$
$[0.8; 1]$	$V_{out} = 0.700V_{in} - 0.015$

Table 4.4: AM/PM linear approximation functions multiplied by three

The phase correction results are depicted in figure 4.12. As shown, a significant reduction of the dynamic effects was achieved. The reduction of the accuracy does not, excessively, degrades the response of the system, proving the viability of this solution.
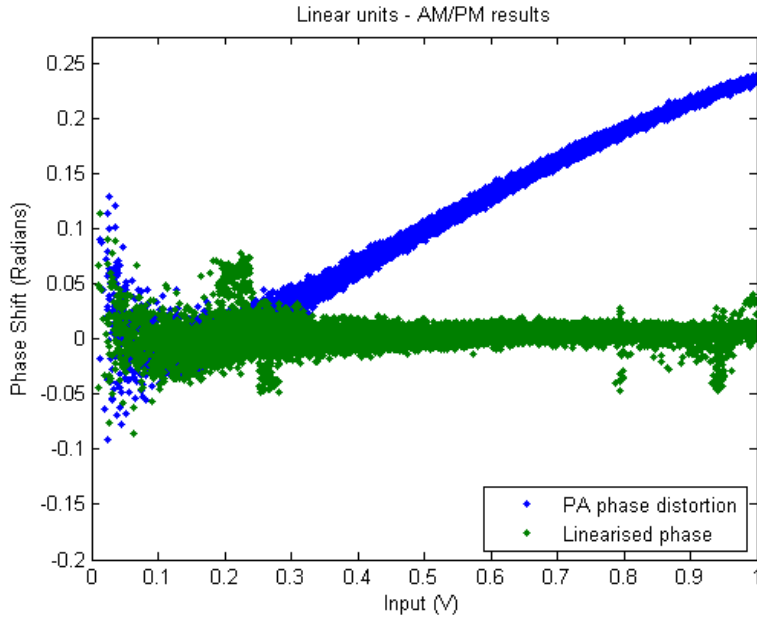
Figure 4.12: Linearised phase - Only first order approximations

An important result to assess is the frequency analysis of the complete distorted signal after amplification. The expected results of this simulation are the reduction of the sidebands introduced by the amplifier. Figures 4.13 and 4.14 depict the simulation results for a GSM four carrier signal and a LTE signal, respectively. These results derive from the second order approximation circuit and thus contain significant frequency components across the spectrum.
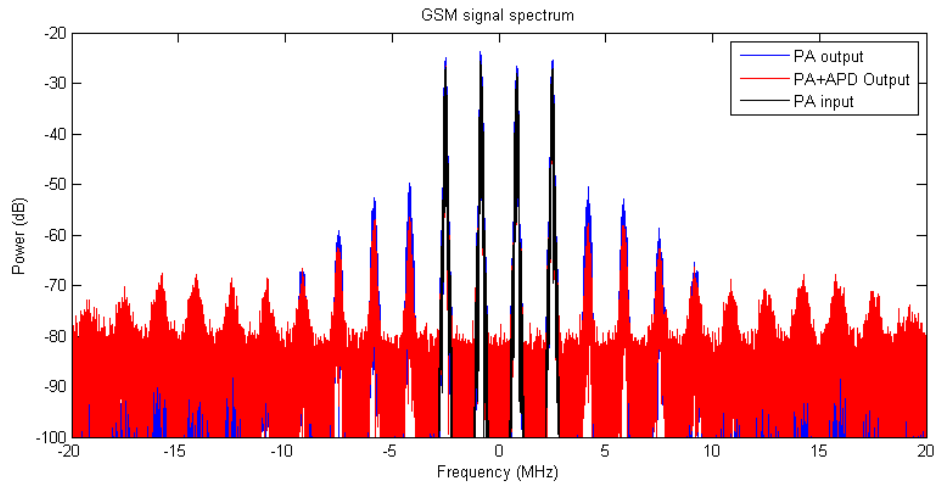
Figure 4.13: GSM signal linearisation using second order approximations
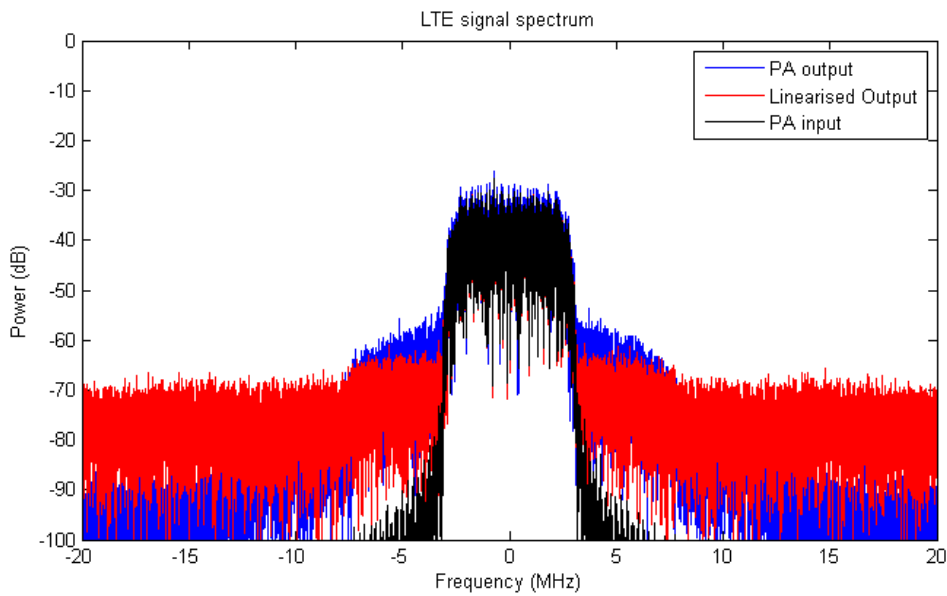
Figure 4.14: LTE signal linearisation using second order approximations

A reduction of the IMDs is visible, the third order IMD is reduced by 7 dB in the GSM signal case. The LTE signal presents a reduction of the adjacent channel power ratio (ACPR) of approximately 5 dB. Despite proving that it is possible to reduce the distortion using a BB-APD, better results could be obtained if the delays and pour dynamic characteristics in the second order path were mitigated.

Figures 4.15 and 4.16 contain the results of the same frequency analysis of the amplified

signal, using the first order polynomial approximations.
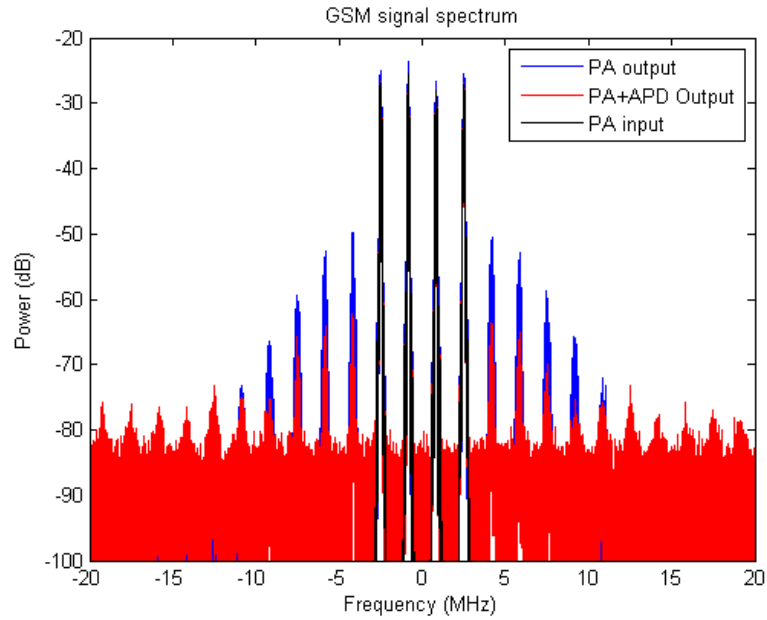
Figure 4.15: GSM signal linearisation using first order approximations
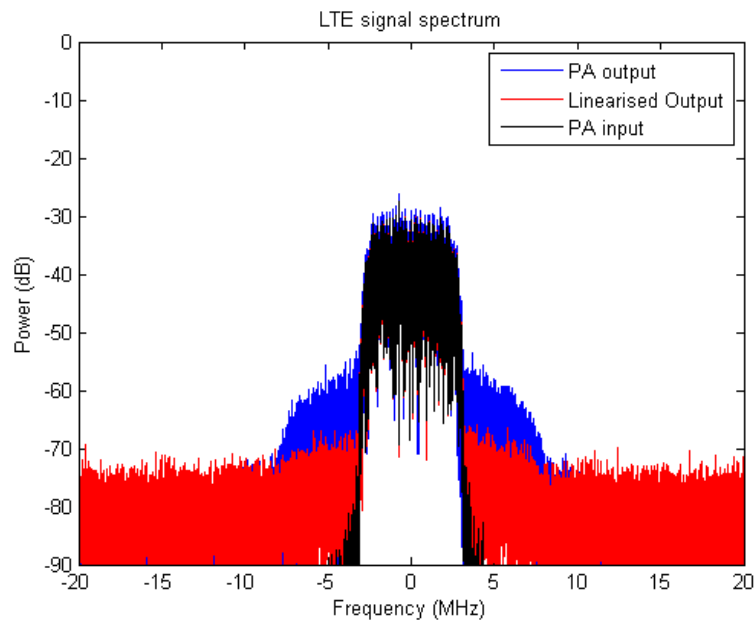
Figure 4.16: LTE signal linearisation using first order approximations

The previous figures show that despite the inferior accuracy of the approximations, the

fact that all the paths have similar propagation delays yields a better linearisation.

A 14 dB reduction of the third IMD was achieved for the GSM signal. Another interesting result is that contrasting with the previously studied third and fifth order RF analogue pre-distorters that correct the IMD components mainly up to the fifth order, this implementation provides a considerable improvement up to the ninth order IMD.

The performance of the circuit when linearising the LTE signal was similar to the previously described, with a ACPR reduction of around 10 dB. Better simulation results should be achievable with the second order approximations and using a faster analogue multiplier.

The previous results prove the performance of the solution presented in this report and justify its practical implementation which is described in the next chapter.

4.3 Sine function block

As described in the previous chapter, the sine function is implemented with second order polynomial approximations. As in the previously mentioned blocks, a switching circuit is required to implement this function.

The performance of the approximation circuit has been proven in this report, therefore, the simulations presented in this section only prove the accuracy of the approximation. Instead of using a real signal, the signal used to prove the accuracy of the solution are triangular waves, with a range equal to the input range of the block (from $-\frac{\pi}{3}$ to $\frac{\pi}{3}$). The expected output is an accurate approximation of a sine wave with the full scale of the output range selected (from -1 to 1). The frequency of the test signal is moderate due to the described problems with the analogue multipliers. At this frequency, the propagation delay of the AD835 can be neglected and the results can be considered accurate. Naturally, a practical implementation of this circuit would require a faster analogue multiplier, or a compensation, on the linear paths, of the introduced propagation delays.

The compensation of the propagation delays could be achieved by two main different methods: delay lines or a series of buffers.

Delay lines use the propagation speed of the signal to perform a delay. By designing the linear paths longer than the second order paths, small time differences can be mitigated. However, the propagation delay of the multiplier is approximately 10 ns. To fully compensate this delay using a transmission line on a flame retardant grade four (FR-4)

substract would requires a 1.4 meters long line, as shown by 4.2.

$$l = \Delta t \frac{c}{\sqrt{\varepsilon_r}} \tag{4.2}$$

where l is the length of the delay line, c is the speed of light in vacuum, Δt is the required delay, and ε_r is the relative permittivity of the substract that is 4.6.

The second option would be a series of buffers, this solution has three main drawbacks: increased noise, high cost and an incrementally fixed delay generation.

The noise introduced in the circuit by passive components, such as resistor, depends on the temperature, but complex operation of active components makes the introduced noise hard to predict.

The data-sheet often provides a prediction of the noise introduced in mV/$\sqrt{\text{Hz}}$. Beyond that, there are other factors that can degrade the signal, such as offset voltages introduced at each OP-AMP.

This method of introducing delays also represents an increase in cost, not only on the price of acquisition of each OP-AMP but also in an increased power consumption, which is an important feature of APD that cannot be undermined.

The fact that each model of OP-AMP has a fixed propagation delay, determines that a cascade of these components simply allows a multiple delay of that time.

The simulation of either of these methods does not yield valuable information, since a faster analogue multiplier is available for the practical implementation.

The simulation results are depicted in figure 4.17. The results show an accurate approximation at each of the approximations branches. A minor switching peak is also visible around the zero-crossing section of the function.
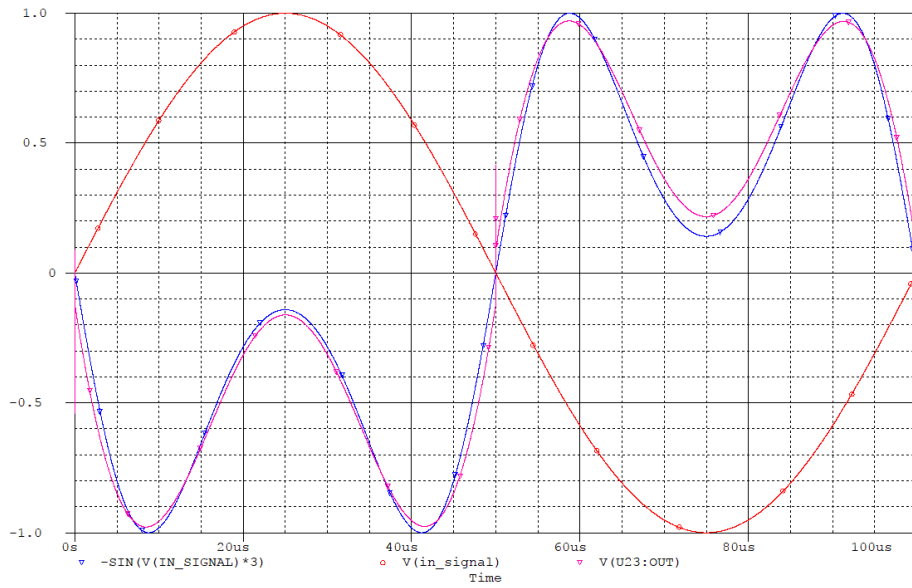
Figure 4.17: Analogue sine simulation for a sinusoidal input
(Approximation in blue; True sine in pink; Input signal in red)

Figure 4.18 contains a representation of the magnitude of the error at each instant. The figure depicts the accuracy of the proposed solution which, considering an analogue implementation, is a reasonable result.
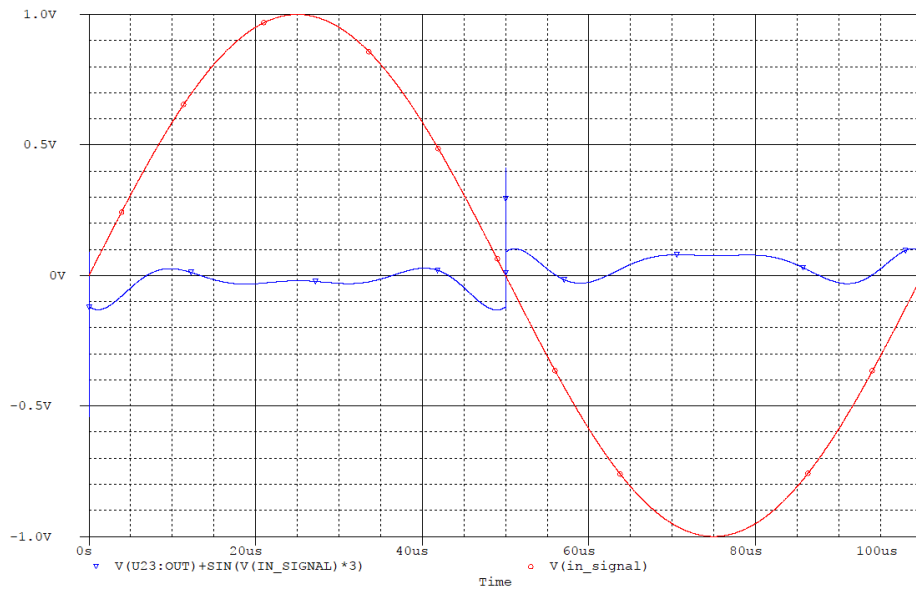
Figure 4.18: Magnitude error of the sine function approximation
(Error signal in blue; Input signal in red)

4.4   Cosine function building block

As described in chapter three, the cosine function is merely a domain shifting of the sine function, hence the accuracy of the cosine function is identical.

Due to the relatively low speed of the multipliers the simulation results of the sine function do not provide valuable information beyond the accuracy of the solution.

To characterize the cosine function, an interesting measurement would be the effects of the additional switching components at higher frequencies. However, the speed of the multiplier strongly degrades the results.

Chapter 5

Hardware Implementation

The last step of this work was the practical implementation and testing. Naturally, the practical implementation of the reported project is the integration of all the designed circuits on a board that properly accommodates all the ICs and other components. This chapter describes the process of converting the simulated circuits to the real implementation, considering all the nonideal conditions that are usually overlooked in simulations. The implemented PCBs are also described and illustrated in this chapter, as well as the results obtained.

Primarily, it is important to establish essential guidelines on the PCB design, which can help to mitigate problems related to parasitic elements, attenuation, reflection and noise and thermal issues.

5.1   Important PCB design considerations

Despite operating at baseband, the designed pre-distorter may receive signals with a span of frequencies of several megahertz in the form of I and Q components, the bandwidth of the signal significantly increases after the conversion to amplitude and phase coordinates. Moreover, there are switching operations on the circuits which require fast rise and fall times that strongly depend on the quality of the designed PCB [29].

One of the most important characteristics of any system is grounding. Depending on the types of signals and components present, there are well known rules that should be followed.

Digital signals are known to introduce noise (a voltage drop) in the ground reference rail that, despite being usually harmless to digital signals, it strongly degrades analogue signals. In a mixed signal system, it is desirable to use a star ground topology where

all the voltages are referenced to a single ground point. The path from each IC to such ground point should have low impedance and low inductance, this is achieved using a large area ground plane. The designed PCBs have the bottom layer reserved for this purpose. However, due to constrains on the fabrication process, it is only possible to produce dual layer boards, therefore, when crossed paths are strictly necessary, the ground plane is used as a second layer. Nevertheless, an effort was made to minimize these discontinuities on the ground plane.

The use of ground planes yields other benefits such as reducing the electromagnetic interference and enabling the use of transmission line techniques (microstrip lines) if required [30].

Another issue that must be considered is related to both the signal's frequency and the signal paths. It is important to analyse if the use of transmission lines is required. Since the most convenient substrate for the manufacturing process is the FR-4, the following calculations consider the use of this material, which has a relative permittivity (ε_r) of 4.6.

To investigate if the use of transmission lines is required it is essential to know the wavelength of the signal. Since the system operates at baseband and the maximum bandwidth of the test signals used so far is bellow 10 MHz, 100 MHz is a safe estimation for the bandwidth of the amplitude signal.

$$\lambda = \frac{v}{f} \quad \wedge \quad v = \frac{c}{\sqrt{\varepsilon_r}} \tag{5.1}$$

$$\lambda = 1.4m \tag{5.2}$$

The wavelength of the signal at 100 MHz is 140 cm, therefore, if the signal paths are kept below 14 cm (one order of magnitude below the total wavelength of the signal) the length of the routes on the PCB is neglectable, hence the use of transmission line models is not required. However, the cables that connect the circuit to external equipment are usually longer. Moreover, the external equipments that will be used to characterise the behaviour of the implemented circuits have terminated inputs and outputs, therefore, the inputs and outputs of each PCB require impedance matching to guarantee maximum power transfer.

There are other also important general guidelines in the design of PCBs, such as allowing an acceptable distance between signal paths, using sufficient width on the PCB routes (especially on the supply rails), and improving the heat dissipation by connecting the exposed pads of the ICs to the ground plane, when possible [22] [23].

5.2 Squarer and adder

Based in figure 3.8, the first operation to perform is the determination of the amplitude signal from the Cartesian coordinates. As explained earlier in this report, the amplitude signal is given in function of the I and Q coordinates by:

$$a(t) = \sqrt{i(t)^2 + q(i)^2} \tag{5.3}$$

The first PCB obtains the squared amplitude of the signal. The circuit consists of two input paths which are fed with the Cartesian coordinates of the baseband signal. The signals are squared by an ADL5391 and added by an OP-AMP however, the multiplier IC operates on a voltage range of 0 V to 5 V which implies that the reference voltage is at 2.5 V. An offset adjustment is required at the inputs and outputs of the multiplier. To include this offset adjustment, an extra OP-AMP is required at each input. The two extra OP-AMPs have another important function which is buffering the input signal to simplify the impedance matching required. Using the high input impedance and low capacitance of the ADA4817, the impedance matching can be achieved simply by using a 50 Ω resistor to ground.

To add the offset, the reference voltage internally generated by each multiplier was meant to be used. However, the necessity of buffering the input signal determined that the offset must be added to the inverting port of the OP-AMP, therefore, the reference voltage needs to be negative. Due to the offset error introduced by the inverting OP-AMP a potentiometer was added to the circuit to allow a fine tune of the offset voltage.

An error on the footprint of an OP-AMP prevented the soldering of this IC on the PCB. To avoid the fabrication of another board, the OP-AMP was soldered above the board. This solution is far from optimal, but since this part of the circuit contains only dc voltages, the signal path remains unaffected.

After the multiplication, the offset at each branch must be cancelled. The output OP-AMP performs both the addition of the signals and the offset cancellation. This is achieved with a noninverting adder configuration, as illustrated in the diagram of figure 5.1.
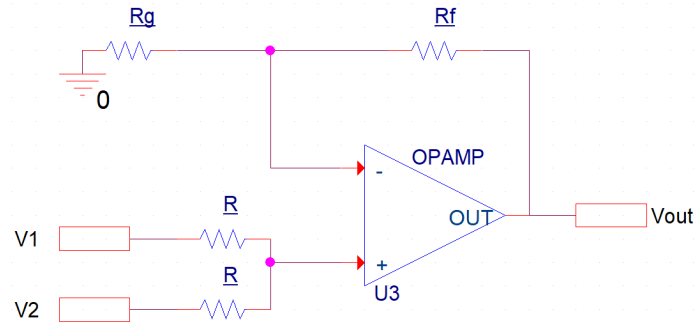
Figure 5.1: Non-inverting OPAMP adder configuration

The complete circuit diagram is presented in figure 5.2 and the designed circuit board is depicted in figure 5.3.
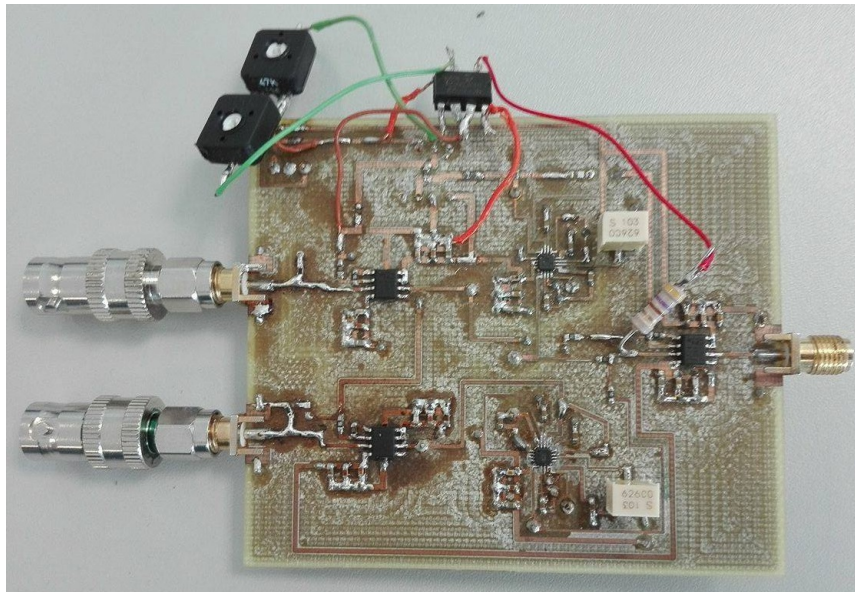
Figure 5.3: Squared amplitude calculator - Picture

The hardware implementation of this part of the system performed well. It is proved to approximate the results to the expected values. Figure 5.4 contains relative error between the calculated and experimental squared amplitude signals in the time domain. As shown, the values match the expected and can, therefore, be used to as an input interface of the BB-APD.
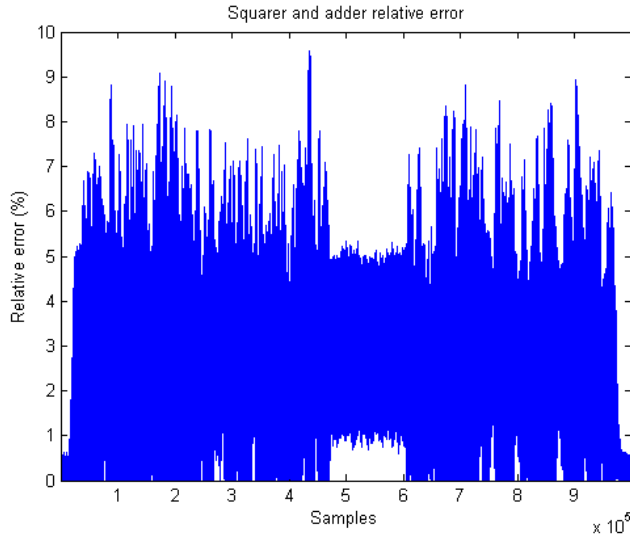
Figure 5.4: Squared amplitude calculation error

5.3 AM/AM board

5.3.1 Generation of the required signal components

With the squared amplitude signal obtained, the following stage of the system to implement is the AM/AM compensation block. The implementation of this block follows a similar structure to the one used in the simulation, however, there are some modifications due to the components used that must be addressed.

As seen with the previous block, the multiplier requires an offset adjustment. The addition of this offset to the input signal is performed by a summing OP-AMP configuration. The signal is applied to the noninverting port as well as an adjustable reference voltage. After adjusting the offset at the input of the multiplier, it is necessary to eliminate the offset at the output of that IC. This is performed by two different OP-AMPs. The use of two different summing configurations provides two samples of the multiplier's output: the first one without the offset, and the second one also without the offset but inverted relatively to the original signal. These two components are required to perform the polynomial approximations.

To implement the polynomial approximations, sensing the input signal is also required. The original input signal is buffered before being used on any other stage of the circuit. This buffering is required due to the variable loading conditions of the remaining circuit, which complicate the impedance matching. The inverted signal is obtained by applying

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the input signal to an inverting OP-AMP and the noninverted signal is obtained by a noninverting configuration.

5.3.2   Implementation of the polynomial approximations

The determination of the distorted amplitude signal is obtained precisely as described in the previous chapter. To summarize, the voltage signals are converted to currents by resistors, the value of the resistors determines the weight of each coefficient and, finally, all the currents are added by an inverting amplifier, which outputs the distorted amplitude signal in the form of a voltage. The selection of the correct branch of approximation, based on the value of the input signal, follows the same technique described in the previous chapter, where a transistor allows the current to flow into the adder circuit when it is at cut-off, or forces the current to ground when it is saturated, therefore eliminating the signal. Hence, the control logic is reversed at this stage which is relevant when implementing the control conditions. Figure 5.5 depicts the circuit that controls the current flow to the adder. For simplicity reasons, only two paths are represented: one for positive signals and other for negative signals. The V1 signal is a positive voltage signal that corresponds to a term of the polynomial approximation. The Vc1 signal is the control signal generated by the control logic described in the next subsection. V2 and Vc2 represent the equivalent part of the circuit for negative signals.
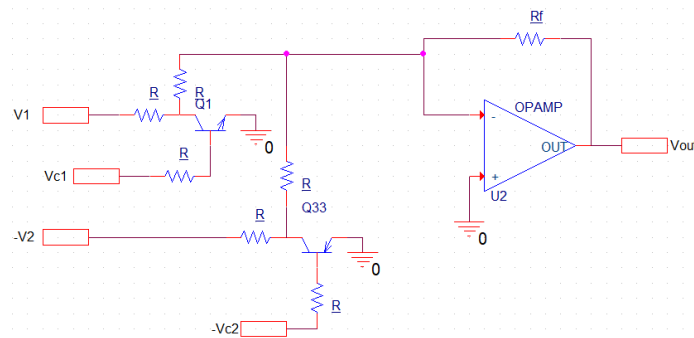

Figure 5.5: Current flow circuit

The independent terms of the polynomial approximation are emulated by independent voltage sources, that are implemented with a potentiometer followed by a buffer OP-AMP. In future implementations, such circuit could be replaced by a DAC to allow the system to be fully and automatically adjustable.

5.3.3 Implementation of the decision circuit

The part of the circuit that mostly differs from the simulation is the control circuit that determines the correct branch of approximation at each instant. A detailed explanation of this function is given in this section.

The comparators used are the LMH7322. The outputs of these ICs are limited to a 0.4 V range, that can be externally adjusted by controlling a linear voltage regulator. The current drawn by the comparator is dependent on the loading conditions, therefore, the required voltage is generated by a low noise linear regulator. Usually, the use of linear regulators is avoided due to their inefficiency, but in this particular situation both the voltage drop across the regulator and the required output current are small. Therefore, the stability and low noise of the reference voltage is worth the added power consumption. The voltage regulator used is the LT3080, which allows a continuous voltage adjustment from 0 V to 350 mV bellow the supply rail [31].

The threshold voltages are exclusively applied to the high impedance input of the comparator and are adjustable by a potentiometer (or a digitally controlled trimmer resistor). To avoid fluctuations, these voltages are buffered by an OP-AMP. Another feature of the comparators is the existence of a hysteresis input, which mitigates oscillations due to noise, when the compared voltages are similar. The adjustment of the hysteresis interval is made by a single resistor. According to the data-sheet of the LMH7322 [32], a 20 kΩ introduces a 5 mV hysteresis voltage, which is an acceptable value (0.5 % of the signal level). The introduction of an hysteresis interval degrades the quality of the switching since the comparators tend to commute at slightly different instances, enabling the appearance of undesired conjugations of events. However, the elimination of this hysteresis voltage is strongly discouraged [32], hence a small hysteresis voltage was added to reduce the oscillations caused by noise.

With the operation of the comparators described, the following stage is the interface of such comparators with the transistors that control the current flow to the output adder OP-AMP.

The switching circuit is based on BJTs that operate either on saturation or on cut-off. Signals with positive amplitudes are controlled by negative-positive-negative doped transistor (NPN) BJTs and signals with negative amplitudes are controlled by positive-negative-positive doped transistor (PNP) BJTs. The outputs of the comparators are applied to the base of the transistors and the emitters are referenced to ground, therefore, the NPN BJTs are on the saturated region when the base voltage is higher than 0.7 V and on the cut-off region if the base voltage is below the latter value. Hence, the central voltage at

the output of the comparators is set to 0.6 V, determining that the high-level of the output is 0.8 V and the low-level decision voltage is 0.4 V. These settings allow the comparators to directly control the NPN transistors. However, the PNP BJTs require control voltages below -0.7 V to operate on the saturation region, and above that value to operate at the cut-off region. To avoid the use of additional comparators, two diodes in series with a resistor are used to lower output voltages of the comparators to the required levels. Figure 5.6 depicts the circuits used to interface the comparators with the transistors.
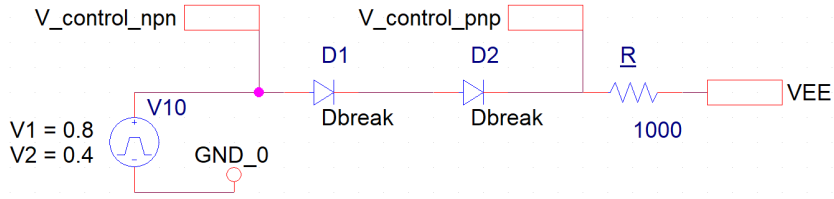
Figure 5.6: Current flow circuit

Even though the diodes are constantly on conduction, the switching circuit requires fast rise and fall times, hence high frequency diodes are used, providing low parasitic capacitances. Another important consideration is that the use of the diodes implies an additional negation to the Boolean logic that controls the signal. This control logic is detailed hereafter.

Based on the approximations presented in table 3.1, the decision circuit performs the branch selection based on three threshold voltages, accordingly to table 5.1.

Branch of approximation	Interval of voltages	Condition
First	$[0; 0.05]$	$\overline{Th_1}$
Second	$[0.05; 0.3]$	$Th_1 \cap \overline{Th_2}$
Third	$[0.3; 0.8]$	$Th_2 \cap \overline{Th_3}$
Fourth	$[0.8; 1]$	Th_3

Table 5.1: AM/AM branch selection conditions

As described above, the control logic is negated at the transistor that controls the flow of current to the adder. When the signal amplitude is negative, the use of diodes to lower the control voltage also represents a negation of the control logic, therefore it is required a careful analysis of the control conditions to implement.

The comparators provide both the true result of the comparison and its negation; hence all the required information is available. To describe the process of obtaining the

correct control conditions, three events are considered: Th_1, Th_2 and Th_3. Each of these events represents the comparison of the input signal with the respective threshold voltage. The events are considered true (high logic level) if the input voltage is higher than the threshold voltage and considered false (low logic level) otherwise. Each event represents an if statement as follows:

$$\text{If}(V_{in_j} > V_{th_j}) \tag{5.4}$$

Table 5.1 includes the required conditions for each branch of approximation to be correctly selected. Arrangements of two transistors are used to implement "and" and "or" gates as shown in figure 3.13.

The control signal path is represented in figure 5.7, which provides a visualization of the Boolean operations whom the control signals go through. This figure implements the Boolean operations required to control the second branch of approximation for both the positive and negative signals.

(a) Control path for positive signals

(b) Control path for negative signals

Figure 5.7: Single second order approximation vs second order branch approximation

The positive amplitude path starts with a logical "NAND", where the output is only zero when both inputs are low level ($\overline{Th_1}$). The output of this gate is then applied to the control transistor that, as stated, represents a "NOT" gate, hence the Boolean function of the control logic is an "AND" gate. To obtain the required control function ($Th_1 \cap \overline{Th_2}$), the inputs of the logic control system are Th_1 and $\overline{Th_2}$.

The negative amplitude path is implemented with PNP transistors, therefore the path starts with two diodes which lower the control voltage to the required range, but also constitute a negation. The following stage is an "NAND" similar to the previously mentioned

one and, finally, the current flow controller transistor emulates a "NOT" gate. The final expression of the logic control system is a "NOR" gate or, in a more appropriate form for this application, an "AND" gate with negated inputs. Hence, to obtain the control conditions expressed by $Th_1 \cap \overline{Th_2}$, the signals fed to the logic control system are $\overline{Th_1}$ and Th_1.

With one branch described, the remaining are similar, hence the repetition of this explanation for each approximation branch is redundant.

5.3.4   Complete circuit description

The circuit schematic is depicted in figures 5.8 and 5.9. Due to the size of the complete circuit diagram such division is required. Figure 5.8 depicts the leftmost part of the circuit where the input buffers and squarer are represented, as well as the the two required comparators. Figure 5.9 depicts the rightmost part of the circuit which contains the output adder and the transistors that perform the approximations branch selection.

The resulting PCB is depicted in figures 5.10 and 5.11, with the representation of the layout depicted in the first figure and the fabricated PCB result illustrated in the latter.
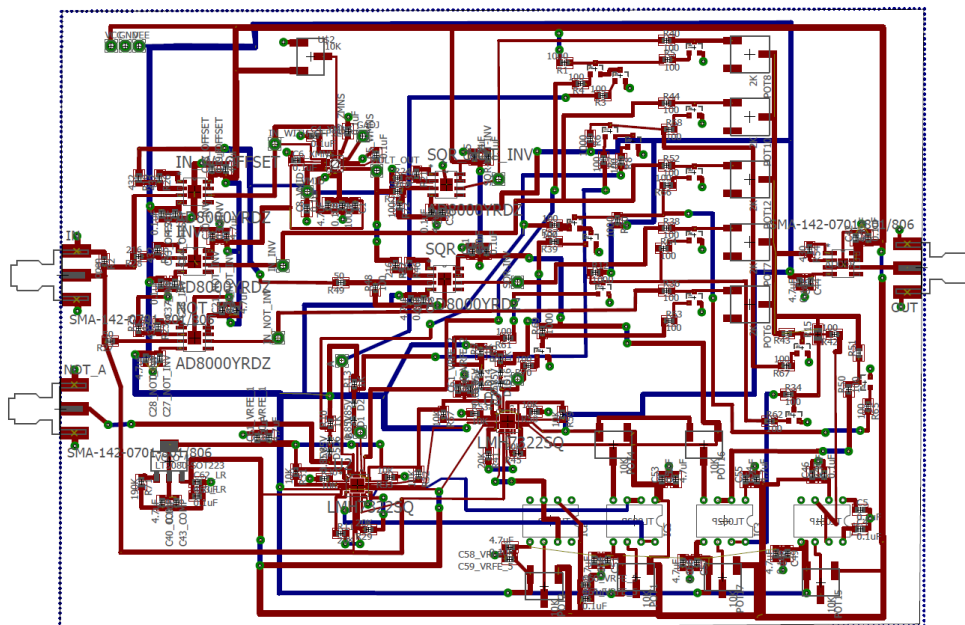

Figure 5.10: AM/AM PCB layout
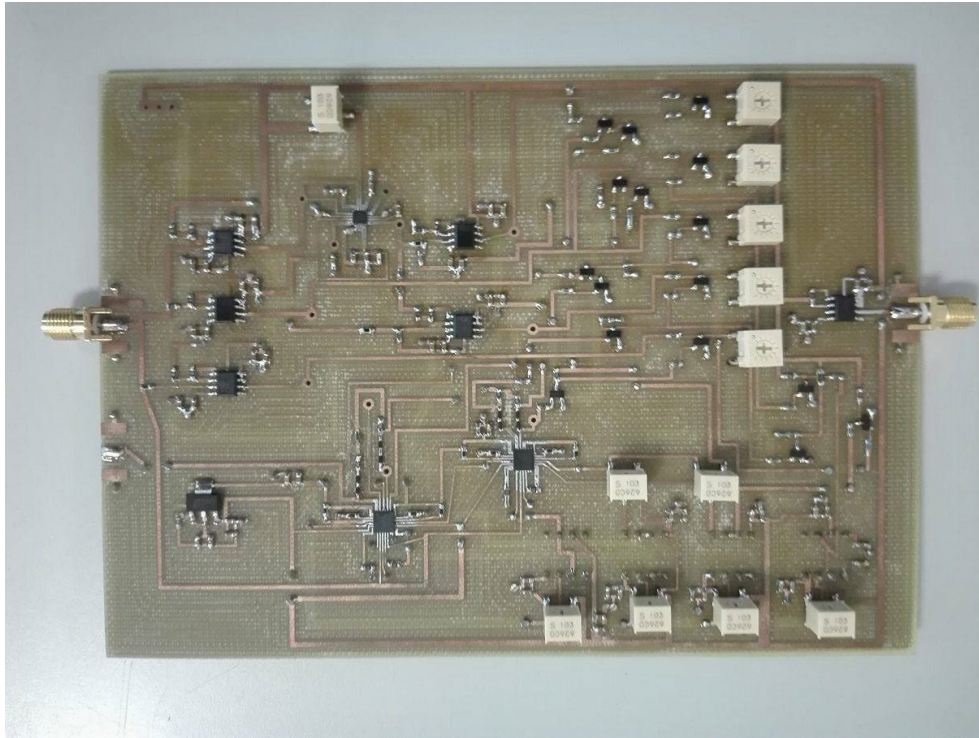(red: top layer; blue: bottom layer)

Figure 5.11: Complete AM/AM compensation circuit - Before corrections

Due to errors during the design of the PCB, the represented layouts are not final. For the system to properly function modifications were required. Due to the observed inability to adjust the introduced offsets (when testing this board in the laboratory), additional circuitry had to be introduced. This circuitry has been described and consists on potentiometers that allow an adjustment of the offset voltages, which are then buffered to improve the stability of the offset voltages.

Another misconception is related to the decision circuit where, due to a lapse in the PCB design, one condition was taken from the wrong output of the comparator. To solve this issue, two diodes and a resistor were installed to provide the correct logical input to the decision circuit. Ideally these modifications would be applied in another PCB correctly designed according to the requirements. However, due to time constrains and delays in the fabrication process, the corrections had to be made over the previously illustrated board with resort to prototyping boards where the missing components were soldered. The resulting AM/AM compensation board is depicted in figure 5.12.
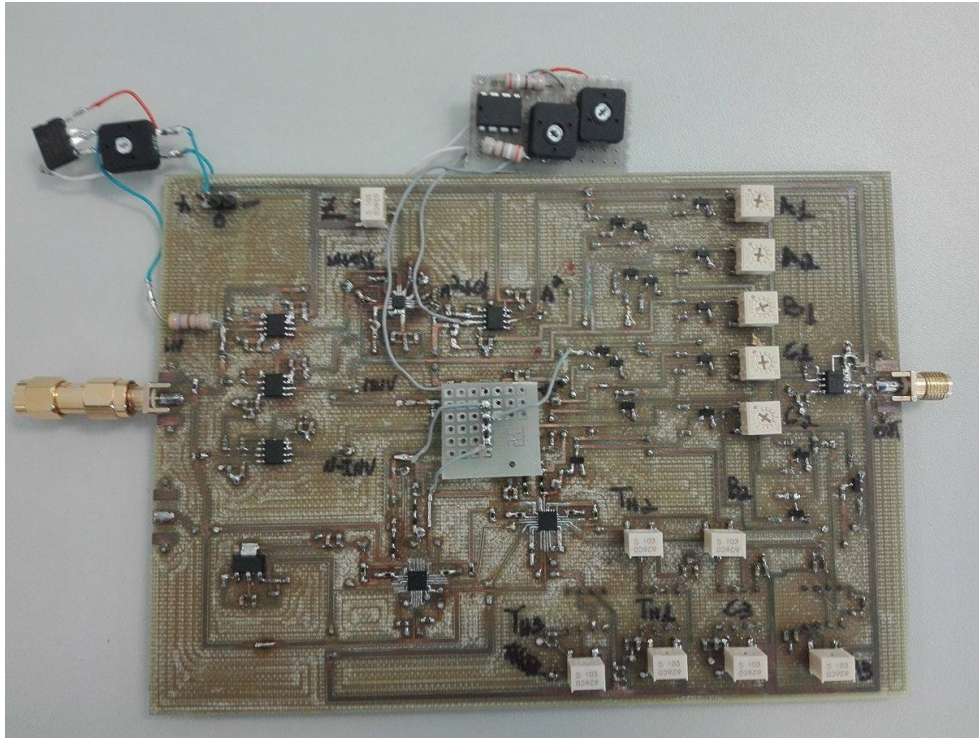
Figure 5.12: Complete AM/AM compensation circuit - Final

The majority of the required alterations only process dc, however, in this board, an output of the comparators had to be processed over the original PCB. To minimize the degradation of this signal, a small prototyping board with the required components was placed as close as possible to the respective region of the circuit (centre of the PCB), the connection wires were kept as short as possible and were carefully soldered to the PCB.

5.3.5 AM/AM results

After a simple calibration process, were the potentiometers were properly adjusted, the AM/AM compensation board performed as expected. The results of operation of this board are compared to the expected ones and depicted in figure 5.13.
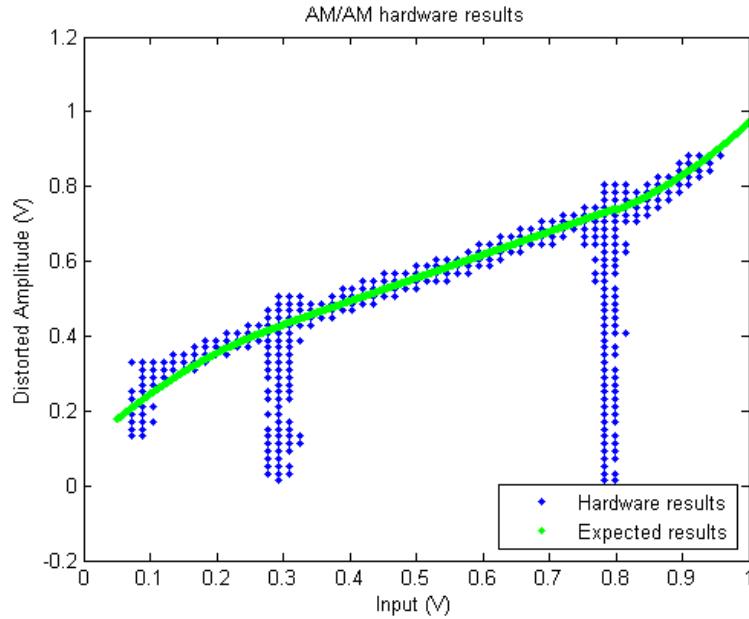
Figure 5.13: AM/AM compensation results

It is visible that near the switching thresholds there are peaks on the response of the signal. These peaks are expected to degrade the overall performance of the pre-distorter, however, it was not possible, with the available time to implement the system, to further reduce this issue. The explanation to this problem is the different switching timings for the NPN and PNP. Even though complementary transistors with a high transitory frequency (5 GHz) were chosen, there are always differences in the switching speeds due to the different carriers used in each type of transistor. PNP use holes as carriers and NPN use electrons as carriers. Electrons are known to be faster carriers, hence the observed differences in the switching times.

More relevant results of the spectrum improvement achieved are described ahead in this report, since such results require the integration of both the AM/AM and AM/PM boards.

5.4   AM/PM compensation board

The second essential function to implement the BB-APD is the AM/PM compensation generation. As described, this board receives the distorted amplitude signals and generates a phase distortion signal that is added to the original phase signal to compensate the phase advance introduced by the PA.

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Along this report, the time constrains of the project have been revealed. Ideally, the AM/PM compensation board would have been fabricated after the AM/AM board was fabricated and tested, since both boards operate on the same basic principles and, thus, design errors made on the AM/AM board and other problems could be corrected before implementing the second PCB. However, the fabrication and soldering processes are time consuming, therefore, the implementation of the AM/PM board could not be dependent on the previous PCB but had to be concurrent with the latter.

Based on the simulation results, an approximation with three linear branches yields a sufficiently accurate approximation with less components and hence a faster fabrication process. Based on those results and on the remaining time to implement the BB-APD, the decision to select a simpler architecture had to be made. Therefore, the AM/PM compensation board is constituted by three linear branches.

This added simplicity eliminates two key issues introduced by the multipliers: the need to adjust offset voltages and the heat generated by this IC.

5.4.1 Implementation of the polynomial approximations

The first order polynomial approximations are given in table 4.4. Since all the approximations are of first order, all the branches have a positive slope, hence only one OP-AMP is required at the input to invert the signal (the input signal must be inverted due to the inverting adder configuration).

The approximation is calculated by the adder OP-AMP and the weight of each path is determined by a resistor before the adder. Since this board only requires two OP-AMPs, to further simplify the design, a dual OP-AMP was used: the ADA4817-2.

To implement the independent terms, three voltages were generated by three potentiometers and buffered before being applied to the adder. Once again, these potentiometers can be replaced by digitally controlled trimmers, or the voltage source circuits can be replaced by DACs to allow a complete adjustment of the system. Even though one of the independent terms is null it is important to implement the additional degree of freedom to enable a better adjustment of the characteristic function. Furthermore, this additional degree of freedom can help mitigating errors due to leakage currents on the switching circuit.

5.4.2 Implementation of the decision circuit

The AM/PM compensation function can be approximated by three branches, therefore, only two comparators are needed. Since the LMH7322 package contains two comparators, only one IC is required.

The remaining of the decision circuit is identical to the AM/AM board. The logic expressions required, as well as their transformation to the form used in practical circuitry are summarized in table 5.2. Similarly to the previous board, the two events are defined as Th_1 and Th_2 and their Boolean values is given by the condition:

$$\text{If}(V_{in_j} > V_{th_j}) \tag{5.5}$$

Branch of approximation	Interval of voltages	Condition
First	$[0; 0.2]$	$\overline{Th_1}$
Second	$[0.2; 0.55]$	$Th_1 \cap \overline{Th_2}$
Third	$[0.55; 1]$	Th_2

Table 5.2: AM/PM branch selection conditions

5.4.3 AM/PM complete circuit diagram

The complete circuit diagram is depicted in figure 5.14. The resulting PCB layout is illustrated in figure 5.15.
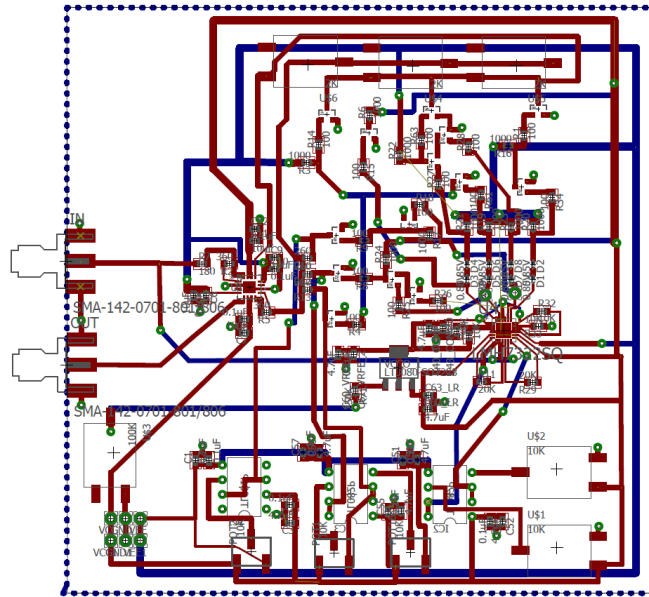
Figure 5.15: AM/PM PCB layout
(red: top layer; blue: bottom layer)

All the important PCB rules were considered during its design and routing. Figure 5.16 presents a photo of the complete PCB with all the required components soldered.
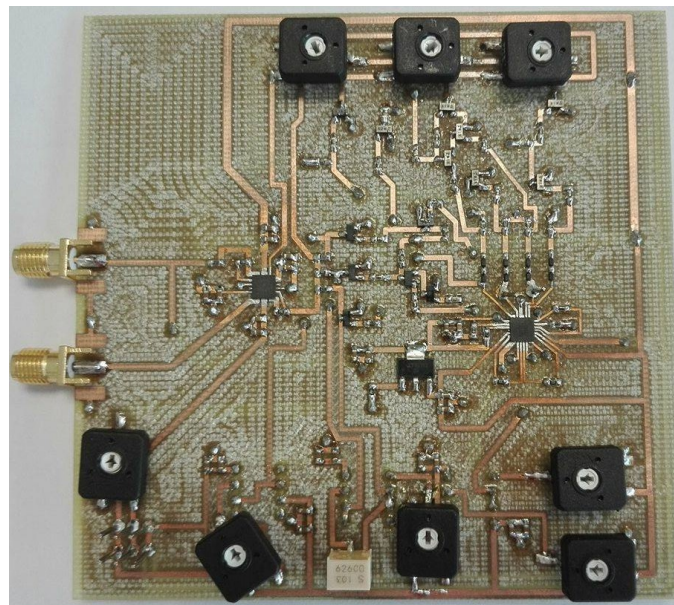

Figure 5.16: AM/PM circuit board

Contrasting with the previous board, the AM/PM PCB did not require corrections.

With the board properly functioning, the characterisation of its performance and operation was the following procedure to execute.

5.4.4 AM/PM compensation results

The performance of the AM/PM can be evaluated by the accuracy with which it approximates the necessary mathematical functions. After the calibration process, where the potentiometers were tuned to implement the necessary voltages and gains, the achieved results are depicted in figure 5.17.
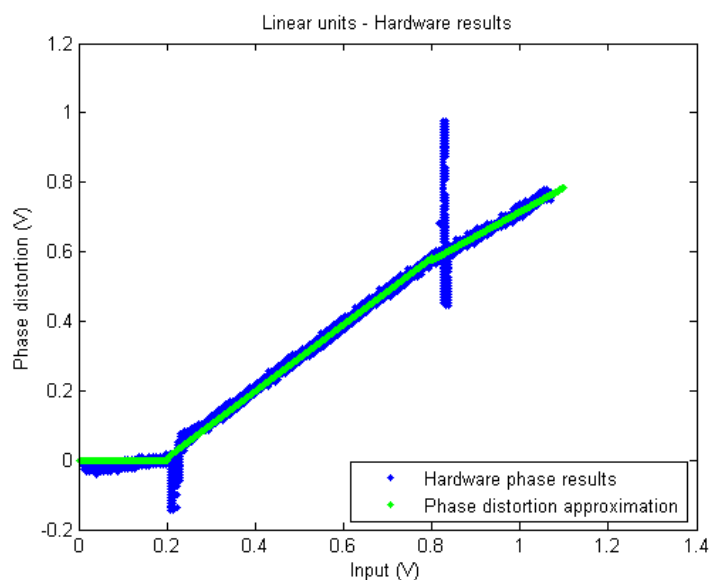

Figure 5.17: AM/PM board approximation results

As figure 5.17 depicts, the approximation functions are accurately implemented. Similarly to the AM/AM circuit results, there is an evident peaking around the voltage threshold values, where the switching occurs. This problem represents the greatest limitation of the pursued solution, however, within the time frame available, a different implementation was not possible.

Having implemented the required two characteristic curve generators, an important result to analyse is the overall IMD suppression on the frequency domain. These results are presented in the following section.

5.5 Combined board results

As explained along the report, time constrains prevented the practical implementation of all the building blocks depicted in figure 3.8. To characterise the performance of the implemented BB-APD, the squarer and adder board, which determines the squared amplitude component of the signal, receives the I and Q components and its output is applied to the AM/AM compensation board. The distorted amplitude signal is then sampled by an oscilloscope and simultaneously applied to the AM/PM board. The phase distortion signal is also sampled by an oscilloscope. The complete system test bench is depicted in figure 5.18.
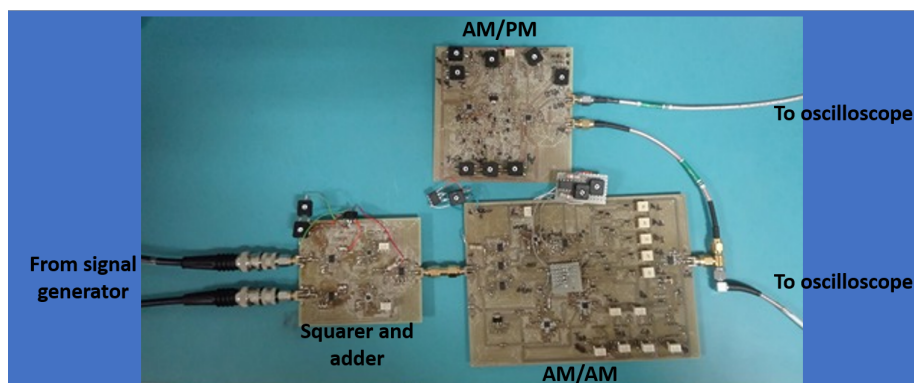

Figure 5.18: Complete system test bench

The two sampled signals are collected and processed with *MATLAB* to obtain the distorted I and Q components, which are then applied to the static PA model.

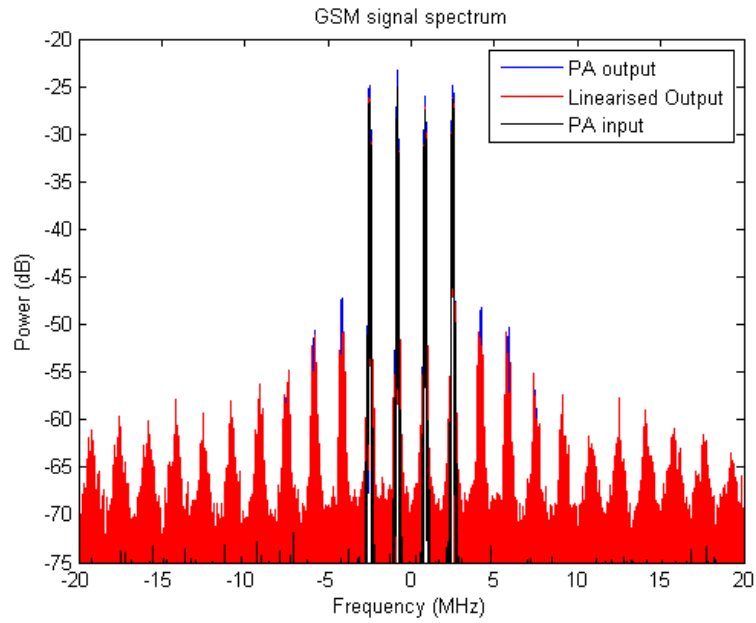The results of this procedure are depicted in figures 5.19 and 5.20.
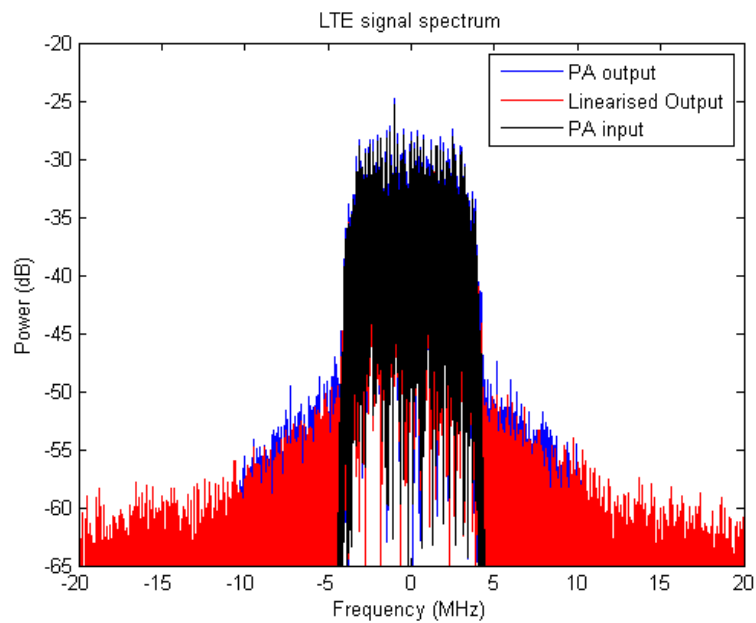
Figure 5.19: Hardware results - GSM signal

Figure 5.20: Hardware results - LTE signal

As shown, the obtained results do not meet the expectations. Contrasting with the simulation results where a 14 dB of the third order IMD improvement was achieved, the

practical implementations led to a 3 dB improvement on the third order IMD for the four-carrier GSM signal. Furthermore, the higher order IMDs are not improved and considerable frequency components appear across the spectrum. Likewise, with the LTE signal test the linearisation performance was not up to the level of that achieved in simulation. The observed ACPR improvement is approximately 2 dB.

The difference between the simulation results and the practical ones can be justified by the differences between the SPICE models and the actual practical components, which is a well known issue with simulations. Moreover, the introduction of an hysteresis voltage is responsible for a worse switching performance than the one used in simulation. However, the elimination of this hysteresis voltages results in an oscillatory behaviour near the switching regions caused by noise.
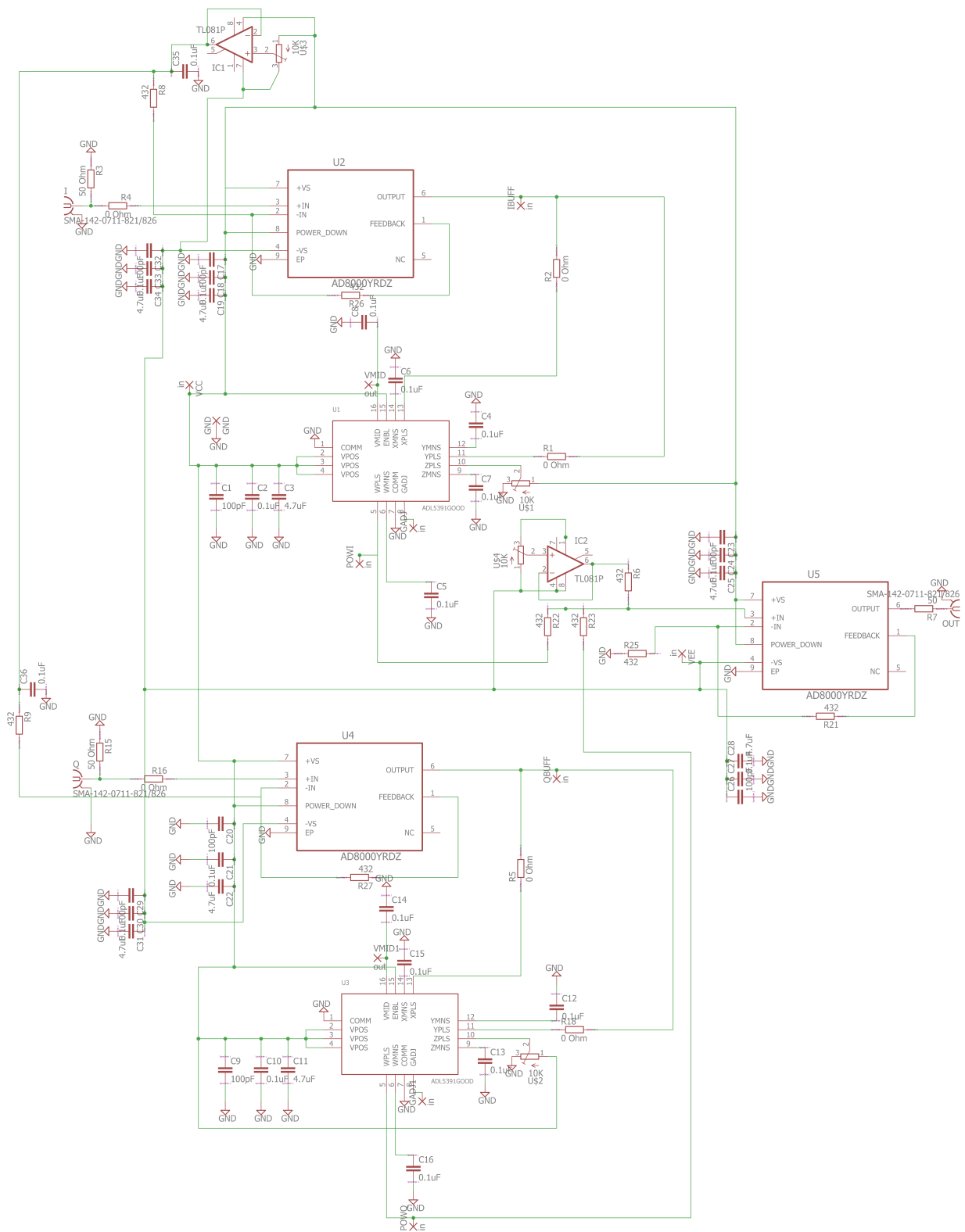
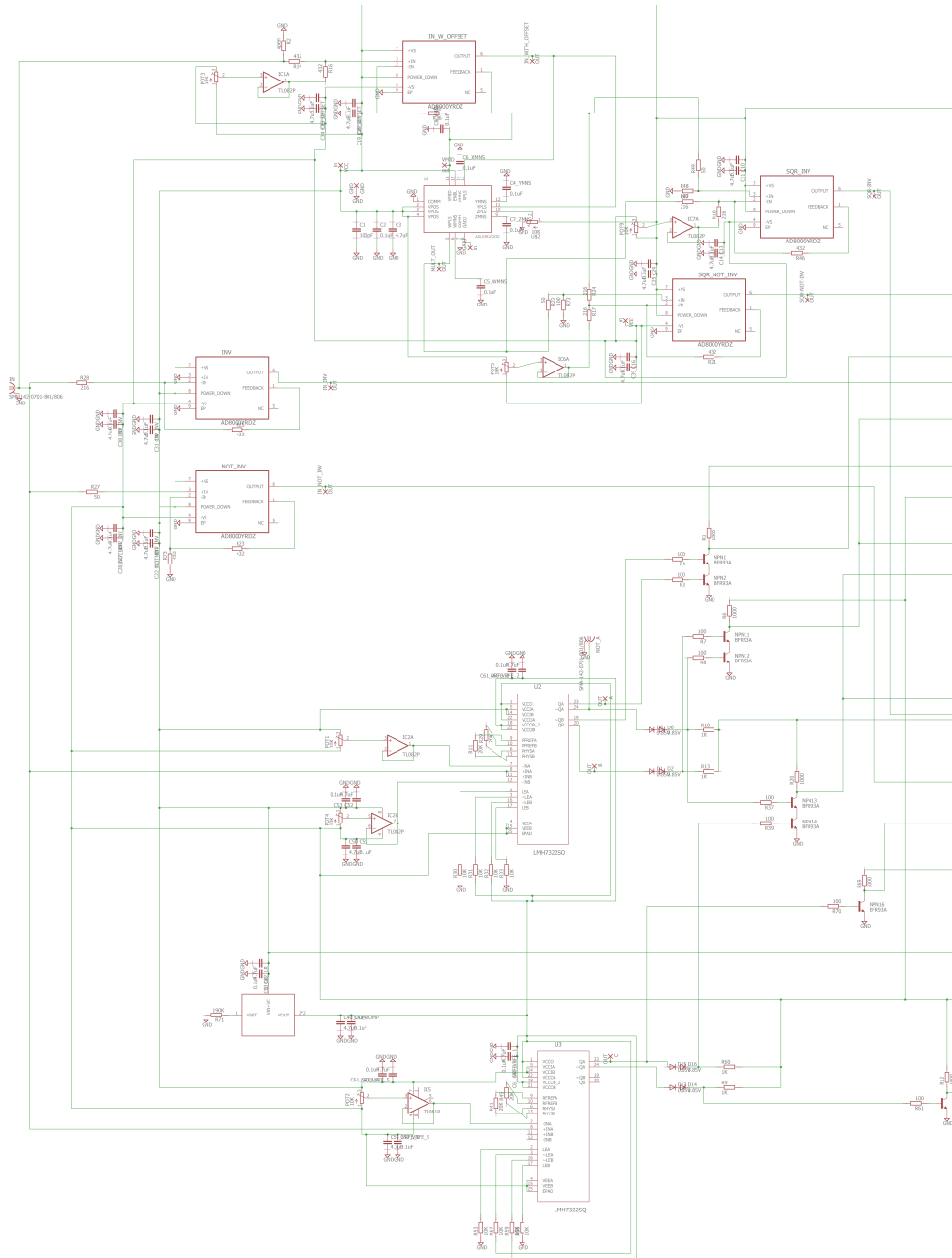Figure 5.2: Squared amplitude calculator - Circuit diagram

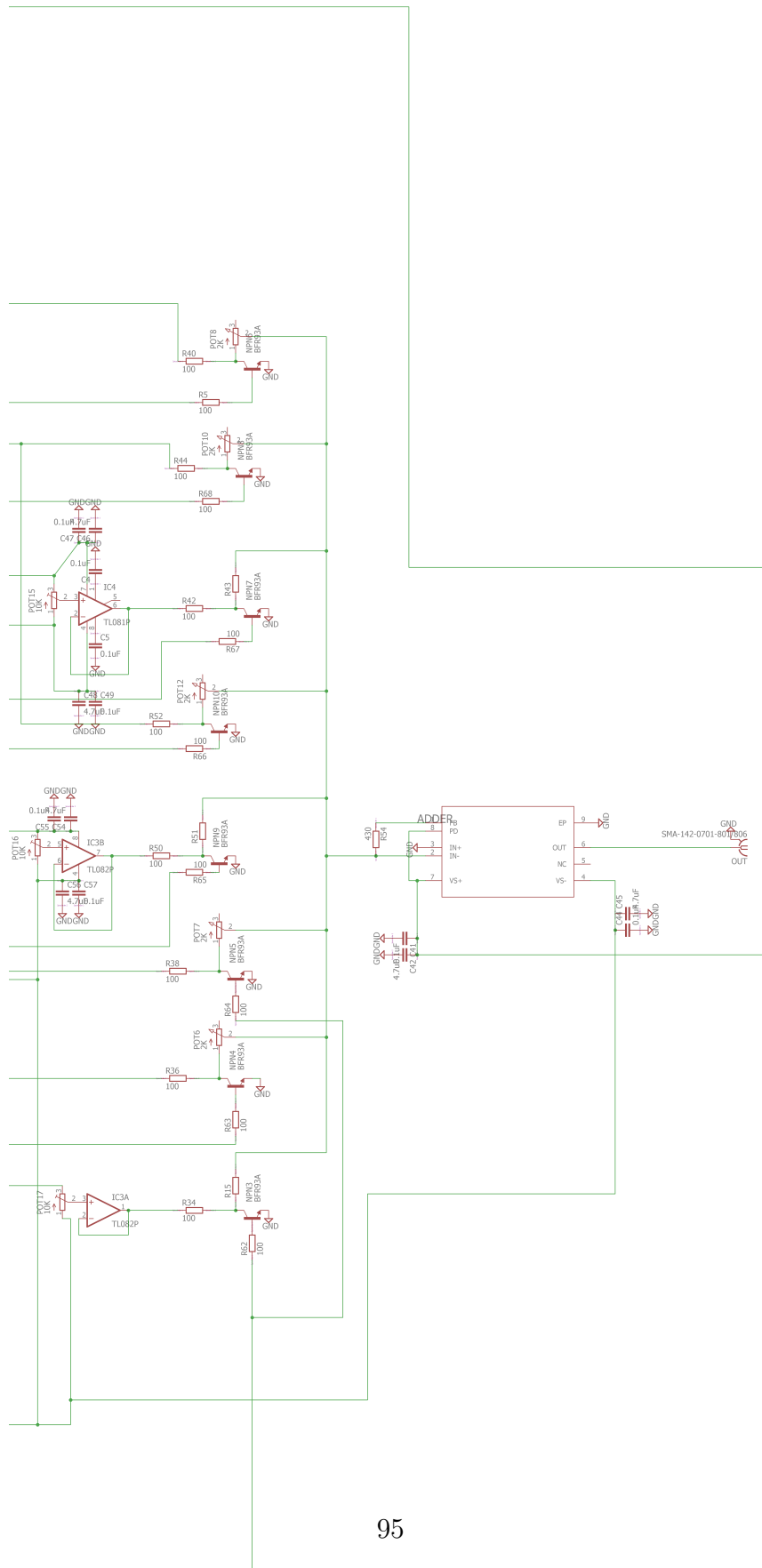Figure 5.8: AM/AM circuit schematic (leftmost part)
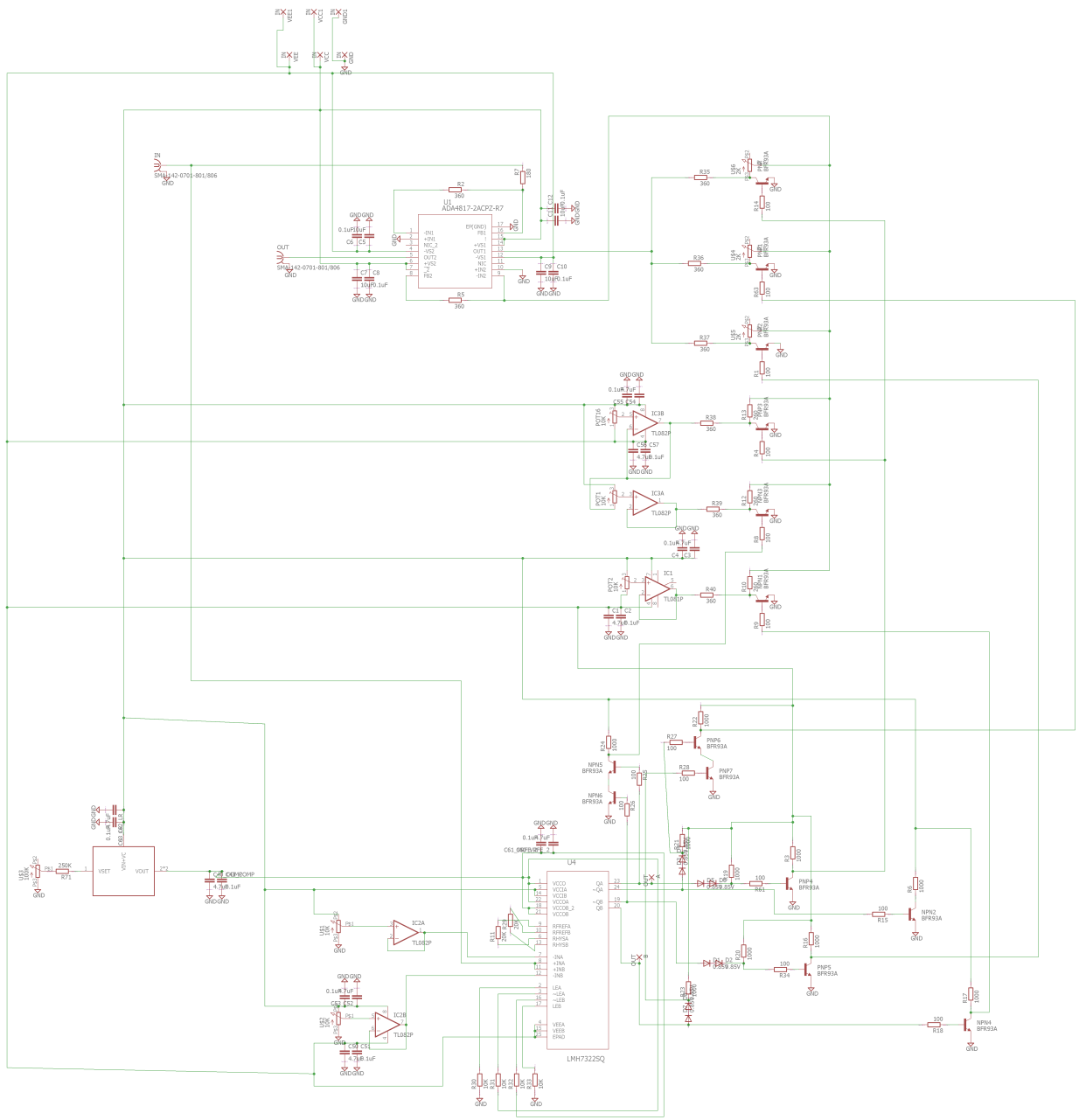
Figure 5.9: AM/AM circuit schematic (rightmost part)

Figure 5.14: AM/PM circuit schematic

Chapter 6

Conclusions and future work proposal

6.1 Conclusions

The efficiency of telecommunication systems has been a concern for many years. The improvement of the PA efficiency results in the degradation of its linearity, hence, linearisation methods have been profoundly studied. Despite the popularity of DPD this approach has strong limitations. Such limitations justify the presented study of an alternative method of pre-distortion: a baseband analogue pre-distorter.

The proposed BB-APD is implemented with resort to multiple high-speed analogue discrete components. The characteristic functions is accurately implemented using piecewise approximations. The branch selection circuitry represents the main limitation to the performance of the proposed solution.

As stated, time constrains also limited the achievement of the complete solution, which led to less accurate results due to the difficulty in matching the samples taken from each block. In fact, matching the propagation time between each block also constitutes a challenge.

The solution presented in this report yields a quality improvement of the transmitted signal in simulation where an IMD3/ACPR reduction higher than 10 dB was achieved.

A hardware implementation of this circuit was also pursued, but limited by the mentioned time constrains. Nevertheless, the AM/AM and AM/PM compensation blocks were implemented and yielded an IMD3/ACPR reduction just over 1 dB. An evident conclusion of this work is that despite the slight improvement of IMD3/ACPR, other frequency components are increased due to the switching operation and the multiple analogue ICs used, which limit the dynamic response of the circuit.

Having mentioned the benefits and limitations of the proposed work, the following

section presents suggestions of solutions to some of these limitations to be implemented in future iterations of a BB-APD.

6.2   Future work

Most of the limitations of the presented solution result from the implementation with discrete electronic components. Therefore, the pursue of an integrated solution has considerable advantages relatively to the presented work. Primarily, a carefully designed integrated implementation has fewer noise sources than a discrete one. Secondly, an integrated implementation allows the use of higher order approximations.

Another valuable improvement of the presented solution is the implementation of the piecewise approximation without binary switching, that is, implementing a decision circuit with smooth transitions between branches of approximation.

Despite the mentioned limitations, the purposed solution matches the initial objectives of this work which were to prove the viability of an analogue pre-distortion system for the next generation communication systems. Notwithstanding, much research is required and a refinement of the presented solution is needed.

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