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Modulus spectroscopy of $CaCu_3Ti_4O_{12}$ ceramics: clues to the internal barrier layer capacitance mechanism

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To date, all existing literature on the so called 'high permittivity' perovskite oxide $CaCu_3Ti_4O_{12}$ (CCTO) in the form of ceramics, single crystals and thin films show the grains (bulk) to exhibit semiconductivity with room temperature, RT, resistivity of ~10 100 Ω cm. Here we show that CCTO grains can be highly resistive with RT resistivity >1 GΩ cm when CCTO ceramics are processed at lower temperature (700 °C). With increasing processing temperature, the semiconducting CCTO phase commonly reported in the literature emerges from grain cores and grows at the expense of the insulating phase. For sintering temperatures of ~1000 1100 °C, the grains are dominated by the semiconducting phase and the insulating phase exists only as a thin layer grain shell/grain boundary region. This electrical microstructure results in the formation of the so called Internal Barrier Layer Capacitance (IBLC) or Maxwell Wagner mechanism that produces the commonly reported high effective permittivity at radio frequencies in dense ceramics. The relationship between Cu loss at elevated processing temperatures and the transformation of the grain resistivity from an insulating to semiconducting state with increasing processing temperature is also discussed.

Introduction

Extensive studies on $CaCu_3Ti_4O_{12}$ (CCTO) ceramics and single crystals over the past decade have led to a better understanding of the large and temperature-stable effective permittivity measured at radio frequencies (rf).[1–19] For CCTO ceramics, spectroscopic plots of the real component of the capacitance (C′) near room temperature (RT) exhibit a frequency-independent plateau over the range ~10–10^5 Hz. The magnitude of the plateau is a composite term, depending on the capacitance and resistance of the grain (bulk), grain boundary and/or sample-electrode nonohmic contact responses.[6,7,20] The plateau in C′ spectroscopic plots observed for dense CCTO ceramics sintered at ~1100 °C is dominated by a grain boundary or an electrode response, depending on the relative magnitude of the resistance for each response.[6,7] The ceramic processing conditions have a significant influence on the electrical properties, especially regarding the grain boundary resistivity (R_{gb}).[6] In most reports, CCTO ceramics have been sintered at 1000–1100 °C for 2–10 h with R_{gb} at RT typically exceeding 1 MΩ cm; R_{gb} is therefore much larger than the electrode responses (R_e) and the grain resistivity (R_b) which is typically <100 Ω cm at RT. In this case, the high effective permittivity (~10^{3-4}) observed at radio-frequencies is dominated by the grain boundary response and can be described as an Internal Barrier Layer Capacitance (IBLC) or Maxwell–Wagner mechanism.[6] For higher sintering temperatures and/or longer sintering periods, R_{gb} decreases significantly to be comparable to or smaller than R_e. In this case, electrode effects start to dominate the C′ rf spectrum, leading to two extrinsic responses and yet higher permittivity.[6] In CCTO single crystals, there is no grain boundary contribution and the high effective permittivity is attributed entirely to an electrode response.[8]

The relaxor-like frequency- and temperature-dependence of permittivity obtained from fixed frequency C′ measurements at higher temperatures (~400–800 K) of CCTO ceramics and single crystals also have extrinsic origins.[7] Such relaxor-like behaviour is an artefact induced by an electrode effect and an instrumental-related parasitic series inductance and resistance effect.[7]

There are several key questions regarding the electrical properties of CCTO ceramics. In particular, why are the grains semiconducting (RT resistivity ~10–100 Ωcm) and how does the electrical microstructure evolve to give the required semiconducting grains and insulating grain boundaries to obtain the Internal Barrier Layer Capacitance (IBLC) mechanism and high effective rf permittivity in dense ceramics sintered at ~1100 °C? Two models are reported in the literature to explain the electrical microstructure exhibited by CCTO ceramics. One of them is based on the comparison with other titanate-based perovskites which have semiconducting grains when sintered in reducing atmosphere and/or at high temperatures, and is related to oxygen loss with subsequent partial reduction of Ti^{4+} to Ti^{3+} ions.[21,22] R_b of dense CCTO

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ceramics sintered at 1115 °C, however, exhibits negligible dependence on the annealing oxygen partial pressure in the temperature range from 600 to 1000 °C.[11] This either suggests oxygen loss is not the main reason for the semiconductivity or oxygen diffusion is kinetically controlled for dense CCTO ceramics at the annealing temperatures.

Another model to explain the semiconductivity is based on cation nonstoichiometry.[12,13] This model suggests a small amount of Ti^{4+} ions occupy the Cu-site when Cu^{2+} ions are partially reduced to Cu^{+} ions at high temperatures. On cooling, Cu^{+} ions are reoxidised to Cu^{2+} ions and the released electrons enter the Ti 3d conduction band giving rise to the bulk semiconductivity. This model involves a reversible redox reaction between Cu^{2+} and Cu^{+} ions and is based on the premise that CuO reduces to Cu_2O in air at ~1050 °C. The reduction temperature of Cu^{2+} to Cu^{+} varies with the composition of Cu-containing compounds. For example, Sleight *et al.* report reduction of Cu^{2+} to Cu^{+} in $CuScO_{2+x}$ at 440 °C on heating in air.[23] The temperature of partial reduction of Cu^{2+} to Cu^{+} ions on heating of CCTO ceramics in air is still unknown and this model remains unverified.

The required defect level(s) to give such semiconductivity is very low (<0.01 at%),[13,21,22] which makes it very challenging to prove/disprove the models just described using common chemical (analytical) techniques. Recently, however, Schmidt *et al.*[14] used Analytical Electron Microscopy on ceramics sintered at temperatures above ~1025 °C to show a trend towards Cu-loss within individual grains with increasing sintering temperature and suggested the grains to be slightly Cu-deficient. This is in good agreement with Electron Probe Microscopic Analysis on large-grained CCTO ceramics sintered at 1115 °C with a reported average grain composition of $Ca_{0.98(2)}Cu_{2.92(2)}Ti_{4.04(2)}O_x$.[11] Schmidt *et al.*[14] also demonstrated the segregation of a Cu-rich phase out of the surfaces of unpolished CCTO ceramics sintered at ⩾1050 °C. It was suggested this secondary Cu-rich phase may exhibit high mobility, diffuse to the pellet surfaces *via* the grain boundaries and may, in part, volatilise at ~1100 °C as demonstrated by an irreversible ~1.5% mass loss detected on heating in air by thermal gravimetry.

Chemical doping studies have shown that nominal (~2 and 5 at%) replacement of Cu by Mn in the starting composition ($CaCu_{3-x}Mn_xTi_4O_{12}$, CCMTO, x = 0.06 and x = 0.15) suppresses the semiconducting grain behaviour.[12,15] This was an important discovery for two reasons. First, it allowed the dielectric properties of CCTO grains to be revealed by rf measurements on CCMTO. The relative (grain) permittivity, ε_r, of CCMTO in dense ceramics is ~90–100 at RT and rises to ~170 at 10 K. On this basis, CCMTO and therefore CCTO are similar to $CaTiO_3$. They are incipient ferroelectrics based on TiO_6 tilted perovskite structures with higher than expected relative permittivity values based on Clausius–Mossotti calculations using ion polarisability and unit cell volume. Li *et al.*[15] showed the microwave dielectric properties of CCMTO ceramics to be dependent on pellet density, with the permittivity increasing from ~35 to 93 at RT for ceramics sintered at 1025 and 1100 °C with ~65% and 95% of the theoretical density, respectively. Second, the grain response in CCMTO ceramics displayed similar levels of conductivity to that obtained from the grain boundaries in dense CCTO ceramics sintered at 1100 °C. Furthermore, the activation energy for conduction was similar in both cases, with values in the range ~0.6–0.8 eV as compared to a value of ~80 meV for the semiconducting grain response in dense CCTO ceramics sintered at 1100 °C. Similar results were obtained from Mn-doping studies on the isomorphous compound $Na_{1/2}Bi_{1/2}Cu_3Ti_4O_{12}$.[16] This has led us to suggest the composition and structure of the grain and grain boundary regions may be very similar in CCTO and there is no need to invoke a distinct and discrete grain boundary phase in CCTO-type ceramics. Both regions may be based on CCTO and that with increasing sintering temperature there is a small change in composition between the grain and grain boundaries that is sufficient to lead to the development of semiconducting and insulating regions.

In the literature, high sintering temperatures, ~1050–1150 °C, are typically employed to obtain dense CCTO ceramics from powders prepared by the conventional solid state reaction (SSR) method. Although low temperature synthetic routes have been used to prepare CCTO powders, pellets used for dielectric measurements are normally sintered at ~1000–1100 °C resulting in semiconducting grains. In this paper, we present CCTO ceramics with insulating grains by low temperature processing and demonstrate the evolution of the IBLC 'electrical microstructure' in CCTO ceramics with sintering temperature.

Experimental

Two groups of CCTO powders were prepared. One group was prepared by a conventional SSR method by calcination at 950 °C for 40 h with ball milling after every 10 h of calcination.[6] The other group was prepared by a high energy milling (HEM) method from stoichiometric quantities of precursors: $CaCO_3$, CuO and TiO_2. The reagents were mixed in ethanol with a high energy mill at 650 rpm for 10 h using Yttria Stabilised Zirconia (YSZ) media. After drying, the powder was calcined at 700 °C for 12 h in air. X-ray Diffraction (XRD) results showed no obvious evidence of any secondary phase (not shown) after this single calcination step, at relatively low temperatures and for much shorter times than required for SSR. Scanning Electron Microscopy (SEM) and Energy Dispersive Spectroscopy (EDS) results showed no appreciable contamination from YSZ media (Y and Zr content is less than 0.1 at%). CCTO pellets were sintered at 700–1100 °C for 4 h in air. The relative density of the SSR and HEM pellets increased with the sintering temperature as listed in Table 1.

High temperature Impedance Spectroscopy (IS) was performed using an HP 4192A impedance analyser in a non-inductively wound tube furnace. Subambient IS was performed using an Agilent E4980A impedance analyser in a closed-cycle

Table 1 M''_{max} and associated capacitance values for low and high temperature M'' Debye peaks in (a) SSR and (b) HEM ceramics sintered at various temperatures. Ceramic density and the M'' ratio for low and high temperature M'' peaks (final column) are also included

(a) SSR		Low temperature peak (60 K)		High temperature peak (483 K)		M''_{max} ratio
		Phase SC		Phase R		
T (°C)	Density	M''_{max} (F $^{-1}$ cm)	C (F cm $^{-1}$)	M''_{max} (F $^{-1}$ cm)	C (F cm $^{-1}$)	Phase SC/Phase R
800	62%	11.2×10^{10}	4.5 p	8.9×10^{10}	5.6 p	1.25
900	66%	10.0×10^{10}	5.0 p	2.3×10^{10}	21.7 p	4.35
1000	87%	3.9×10^{10}	12.8 p	1.8×10^{9}	0.28 n	21.7
1100	94%	3.7×10^{10}	13.5 p	8.1×10^{8}	0.62 n	45.7
(b) HEM		Low temperature peak (100 K)		High temperature peak (523 K)		M''_{max} ratio
		Phase SC		Phase R		
T (°C)	Density	M''_{max} (F $^{-1}$ cm)	C (F cm $^{-1}$)	M''_{max} (F $^{-1}$ cm)	C (F cm $^{-1}$)	Phase SC/Phase R
700	57%			14.0×10^{10}	3.6 p	0
800	61%	4.0×10^{9}	0.13 n	12.2×10^{10}	4.1 p	0.03
900	72%	1.4×10^{10}	35.7 p	5.6×10^{10}	8.9 p	0.25
1100	92%	5.1×10^{10}	9.8 p	3.7×10^{8}	1.40 n	137.8

He refrigerator (Oxford Instruments Ltd., UK). Sputtered Au electrodes were applied to the ceramics. IS data were corrected for sample geometry and analysed using the commercial software package ZView (Version 2.9c, Scribner Associates Inc., USA).

Results and discussion

C′ spectroscopic plots at RT for samples sintered at different temperatures, Fig. 1, reveal immediately the significant effect of sintering temperature on the electrical properties. Regardless of the powder preparation method, the commonly observed plateau with a high associated capacitance of ~1 nF cm $^{-1}$ for CCTO ceramics sintered at 1100 °C decreases by about three orders of magnitude to 2–3 pF cm $^{-1}$ for samples sintered at 700–800 °C. Based on the brickwork layer model, the high capacitance is consistent with a grain boundary response, whereas the capacitance of ~2–3 pF cm $^{-1}$ suggests a bulk response. Such a dramatic decrease of capacitance can't be explained by changes in ceramic density and must therefore be related to changes in grain and/or grain boundary resistivity. These changes are presumably associated with changes in composition induced by high temperature ceramic processing.

Spectroscopic plots of the imaginary component of the electric modulus, M'', are an excellent method to probe the grain response in electrically heterogeneous ceramics such as CCTO. For a homogeneous ceramic or a single crystal, a single, large M'' Debye peak should be present from which the relative permittivity and grain resistivity of the bulk phase (or crystal) can be calculated using the peak height and relaxation frequency. The M'' peak height is inversely proportional to relative permittivity ($M'' = 1/(2\varepsilon_r)$). Often relative M'' (absolute value of M'' divided by ε_0, where ε_0 is the permittivity of free space) is presented. It follows that $M''/\varepsilon_0 = 1/(2\varepsilon_0\varepsilon_r) = 1/(2C)$ and C is capacitance corrected after pellet geometry (pellet thickness/area). C can be therefore calculated from the M'' peak maximum, M_{max}, using the relationship $C = 1/$

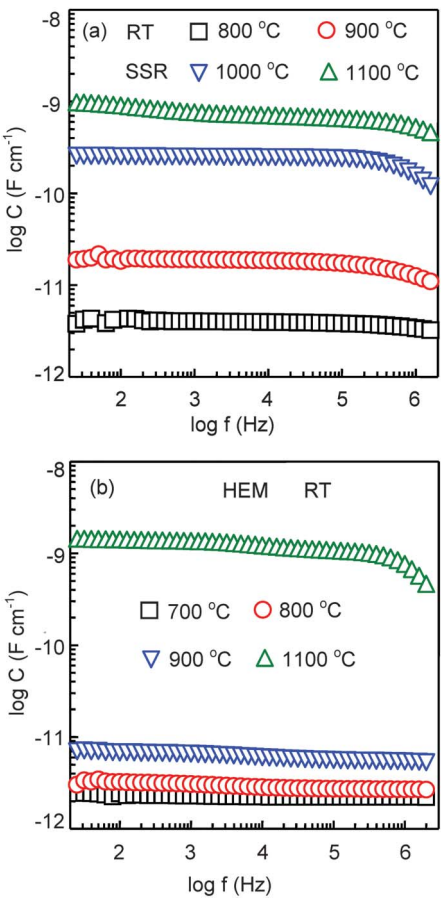

Fig. 1 C′ spectroscopic plots at room temperature for CCTO ceramics sintered at different temperatures using (a) SSR powder, and (b) HEM powder.

$(2M''_{max})$.[24,25] At the M'' peak maximum, the relationship $\omega_{max}RC = 1$ holds, where $\omega_{max} = 2\pi f_{max}$ and f is the applied frequency in Hz. Consequently, $f_{max} = 1/(2\pi RC) = 1/(2\pi\rho\varepsilon_0\varepsilon_r)$, where ρ is resistivity, ε_0 is permittivity of free space, 8.854×10^{-14} F cm^{-1} and ε_r is the relative permittivity. f_{max} is a geometry-independent parameter and therefore allows direct comparison of the bulk response for ceramics with different relative density. For single crystals of CCTO, the relative permittivity ε_r rises from ~100 at RT to ~170 at ~10 K and due to the inverse relationship between M''_{max} and ε_r, M''_{max} should decrease from $\sim 5 \times 10^{10}$ to $\sim 2\text{–}3 \times 10^{10}$ F^{-1} cm on cooling from RT to 10 K.[8] Due to the semiconducting nature of the single crystals which are grown from high temperature, $R_b \sim 10\text{–}15$ Ω cm at RT, M''_{max} occurs at a frequency above the limit of impedance spectroscopy instrumentation (~2–10 MHz) and subambient measurements are required to observe the M'' peak within the measured IS frequency range.

The C' spectroscopic plots in Fig. 1 are somewhat inconclusive about the prevailing bulk or grain boundary contributions for SSR samples sintered at intermediate temperatures (800–900 °C). Further evidence was therefore obtained on combining M'' spectroscopic plots obtained above RT and under cryogenic conditions.

For SSR ceramics sintered at 800 °C, M'' spectroscopic plots reveal the presence of two M'' peaks with similar M''_{max} values, Fig. 2 (a) and (b). One peak occurs at temperatures below ~100 K, for example $M''_{max} \sim 11.2 \times 10^{10}$ F^{-1} cm with $f_{max} \sim 100$ kHz at 60 K, Fig. 2 (a) and the other at temperatures above ~450 K, for example $M''_{max} \sim 8.9 \times 10^{10}$ F^{-1} cm with $f_{max} \sim 10$ kHz at 483 K, Fig. 2 (b). These M''_{max} values correspond to associated C values of 4.5 and 5.6 pF cm^{-1}, respectively and are therefore consistent with bulk-type responses, albeit with lower than expected C values. Using the relationship $\omega RC = 1$ at the M'' peak maxima in Fig. 2 the low temperature peak is associated with a semiconducting bulk-type component (Fig. 2 (a)) with $R_b \sim 330$ kΩ cm at 60 K and the high temperature peak is associated with a resistive bulk-type component (Fig. 2 (b) and (c)) with $R_b \sim 3$ MΩ cm at 483 K. The resistive phase associated with the high temperature peak will be referred to as phase R and the semiconducting phase associated with the low temperature peak as phase SC. Thus, these modulus spectroscopic results provide unique information on the effects of processing conditions that are below the detection limits of other methods of analytical, microstructural or structural characterisation. The temperature dependence of $1/R_b$ and f_{max} for each phase obey the Arrhenius law with an activation energy, E_a, for conduction of ~0.7 eV and ~0.06 eV for the R and SC phases, respectively (not shown).

SSR ceramics sintered at higher temperatures reveal an insightful trend towards the development of the IBLC for CCTO ceramics sintered at temperatures ~1100 °C. f_{max}

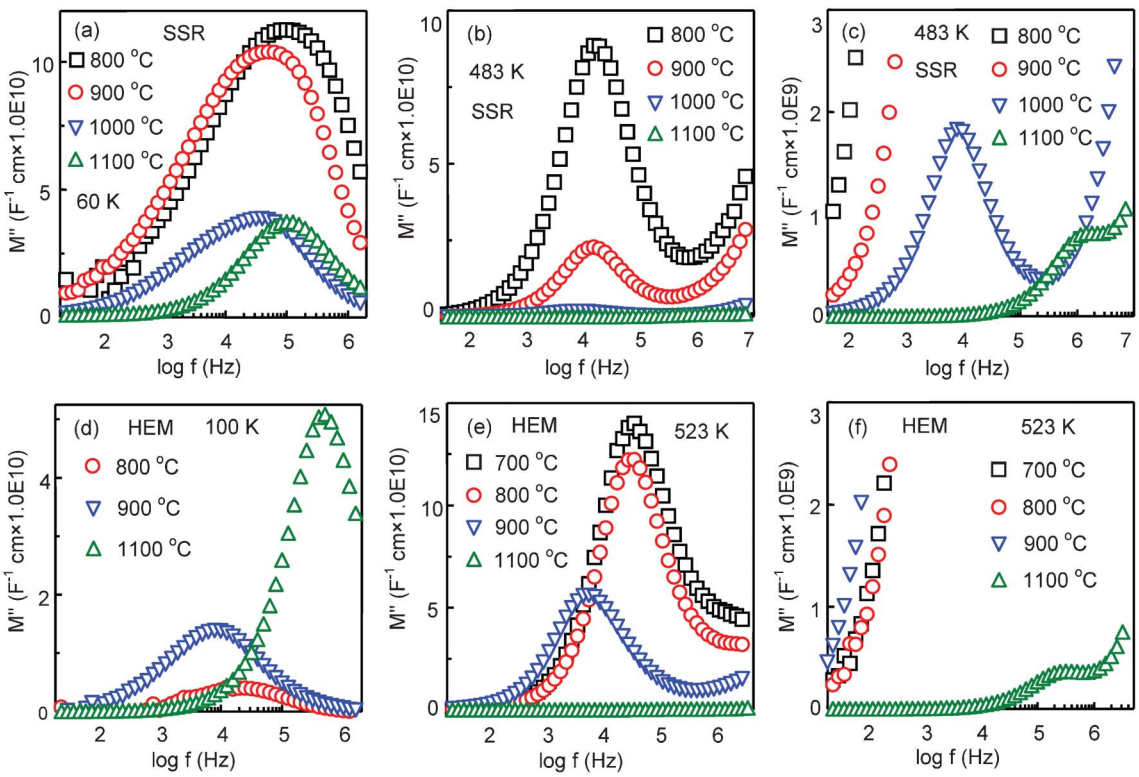

Fig. 2 M'' spectroscopic plots at (a) 60 K, (b) 483 K and (c) expanded scale of (b) for CCTO ceramics sintered at different temperatures using SSR powder, and M'' spectroscopic plots at (d) 100 K, (e) 523 K and (f) expanded scale of (e) for CCTO ceramics sintered at different temperatures using HEM powder. Relative M'' (absolute value of M'' divided by ε_0, where ε_0 is the permittivity of free space) is presented. Capacitance corrected after pellet geometry (pellet thickness/area), C, can be estimated from the M'' peak maximum using the relationship $C = 1/(2M''_{max})$.

associated with the low temperature peak (phase SC) at 60 K remains unchanged for all SSR ceramics sintered between 800 and 1100 °C, however M''_{max} decreases in magnitude by a factor of three with increasing sintering temperature with a value of $\sim 3.7 \times 10^{10}$ F $^{-1}$ cm for samples sintered at 1100 °C, Table 1. The corresponding C of ~ 13.5 pF cm $^{-1}$ ($\varepsilon \sim 153$) is consistent with the ε_r expected for single crystal CCTO and the permittivity of the bulk response from dense ceramics of CCTO, as reported elsewhere.[6] The similarity in f_{max} values for phase SC indicates ρ and ε_r to be similar in all samples but the change in M''_{max} as listed in Table 1 indicates a change in the SC volume fraction on increasing the sintering temperature from 800 to 1100 °C.

In contrast, dramatic changes are observed in the magnitude and f_{max} of the high temperature M'' peak associated with phase R, see Fig. 2 (b) and (c) and Table 1. In this case, on increasing the sintering temperature from 800 to 1000 °C, f_{max} does not change significantly but M''_{max} decreases in magnitude by a factor of ~ 45 from $\sim 8.9 \times 10^{10}$ to $\sim 1.8 \times 10^9$ F cm $^{-1}$, see Fig. 2 (b) and (c), respectively (please note the expanded scale of Fig. 2 (c) compared to 2 (b)). This corresponds to a substantial increase in the associated C from ~ 5.6 pF cm $^{-1}$ to ~ 0.3 nF cm $^{-1}$ for phase R, Table 1. Such a high C is consistent with a typical thin layer response, indicating the volume fraction of phase R decreases dramatically with sintering temperature. For SSR ceramics sintered at 1100 °C, M''_{max} decreases by a further factor of two with an associated $C \sim 0.6$ nF cm $^{-1}$ and in this case f_{max} increases significantly by ~ 2 orders of magnitude, Fig. 2 (c). This indicates a significant change in ρ (and therefore composition) of phase R for samples sintered at 1100 °C.

It is desirable to obtain volume fractions of the SC and R phases using the relative ratio of M''_{max} for each phase. Samples sintered at low temperatures exhibit low density with fine grains (<5 μm) and poorly-defined grain boundaries. These ''neck-like'' boundary regions between the grains can be considered to have the same/similar composition as the bulk material but with a smaller cross sectional area, as revealed by SEM (not shown). This type of ceramic microstructure makes it challenging to obtain a quantitative relationship between M''_{max} and volume fraction using the brick work layer model (a model is being developed by Finite Element simulations and will be reported in the future). Nevertheless, at this stage, assuming ε_r for phase SC and R is similar, the relative ratio of phase R to SC within each ceramic can be assessed qualitatively by comparing the M''_{max} values of the high (483 K) and low temperature (60 K) peaks, final column Table 1. An increase in the M''_{max} ratio of phase SC to phase R suggests there is a significant increase in the volume fraction of phase SC with increasing sintering temperature. There are errors in this analysis due to the temperature-dependence of C for CCTO due to its incipient ferroelectric behaviour and also because of the porosity and non-ideal Debye peak shape of the various M'' peaks due to electrical heterogeneity within the ceramics. Nevertheless, the errors associated with the above factors are much smaller than the estimated change in volume fraction of the two phases on increasing the sintering temperature. For example, ε_r for CCTO single crystals changes by less than a factor of 2 between 10 and 300 K and this is much smaller than the order of magnitude change in height of the M'' peak associated with phase R on increasing the sintering temperature from 800 to 1100 °C, Fig. 2 (b) and (c).

Samples using HEM powders show a similar trend with the relative ratio of phase SC/R increasing with sintering temperature, Table 1. Significantly, for HEM powders sintered at 700 °C there was no obvious peak in the low temperature M'' spectroscopic plots indicating an absence of phase SC in these samples. However, an M'' peak associated with phase SC was present for samples sintered at $\geqslant 800$ °C, Fig. 2 (d) and the associated C of ~ 9.8 pF cm $^{-1}$ ($\varepsilon \sim 111$) at 100 K for samples sintered at 1100 °C is in agreement with that expected for ε_r of single crystals and dense ceramics of CCTO. There is a dramatic increase in f_{max} from ~ 10 kHz to 1 MHz for phase SC on increasing the sintering temperature from 900 to 1100 °C, Fig. 2 (d). This indicates a significant decrease in ρ and therefore composition of phase SC for HEM powders sintered at 1100 °C. The trend in the high temperature M'' spectra for phase R is similar to that observed for SSR ceramics. For HEM samples sintered at 700–900 °C, C from M'' spectroscopic plots at 523 K is in the range ~ 3.6–8.9 pF cm $^{-1}$, Fig. 2 (e), suggesting phase R has a bulk-type response. The M'' peak height of HEM ceramics sintered at 1100 °C decreases by a factor of ~ 380 to $\sim 3.7 \times 10^8$ F $^{-1}$ cm, Fig. 2 (f) corresponding to $C \sim 1.4$ nF cm $^{-1}$, suggesting phase R becomes a thin layer-type phase, Table 1. The higher ratio of phase SC/R at lower sintering temperatures for SSR samples is because this method requires high calcination temperatures (>950 °C) to obtain phase-pure CCTO and this temperature is sufficient to partially transform phase R to phase SC prior to sintering of SSR ceramics. The higher impact during milling and better homogeneity of the precursors by the HEM method permits a substantial decrease in the calcination temperature (to 700 °C) required to obtain phase-pure CCTO powder and this restricts the formation of phase SC and only phase R is present in ceramics sintered at 700 °C.

Arrhenius-type plots of f_{max} for phase R and SC in samples sintered at 900 and 1100 °C are shown in Fig. 3. f_{max} is a geometry-independent parameter that is determined by the resistivity and permittivity of the phase. The temperature dependence of permittivity is typically much smaller than that of resistivity. E_a from such plots therefore reflects mainly the behaviour of resistivity. E_a for phase R and SC from the various ceramics are in the range ~ 0.60 to 0.86 eV and 40 to 80 meV, respectively. These E_a values are consistent with that of grain boundary and grain regions reported in the literature for dense ceramics of CCTO sintered at ~ 1100 °C.[5] The variation in magnitude of f_{max} and E_a values for phase SC from HEM and SSR ceramics indicates the sensitivity of IS to detect small compositional changes in this phase with the processing temperature.

These IS results draw a general picture of the evolution of the IBLC 'electrical microstructure' in CCTO ceramics with

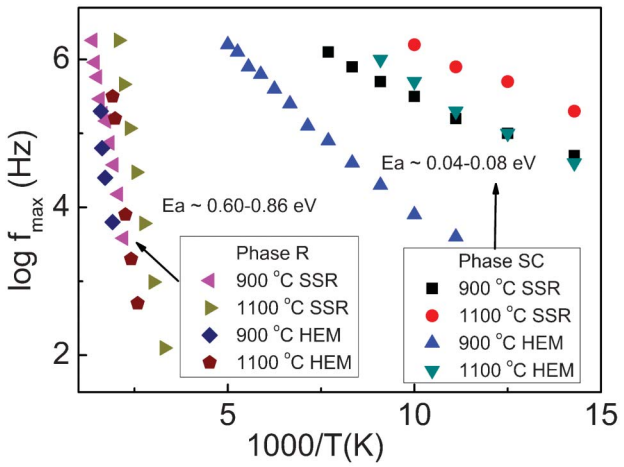

Fig. 3 Arrhenius type plots of f_{max} from M'' spectroscopic plots for both insulating phase R and semiconducting phase SC in CCTO ceramics sintered at 900 and 1100 °C using SSR and HEM powders.

sintering temperature. The distribution of phases R and SC in CCTO ceramics is proposed to be an intra-granular, core–shell type distribution, as there is no appreciable difference in the IS response before and after polishing CCTO pellets (see Fig. 3c in ref. 6) to suggest macroscopic compositional heterogeneity throughout the ceramic (outer insulating skin and inner conducting core regions of a pellet) plays a significant role. Core–shell type compositional heterogeneity within grains has been widely observed in other titanate-based perovskites such as $BaTiO_3$.[24,25] The HEM CCTO ceramics sintered at 700 °C are electrically homogeneous. Both the grains and "neck-like" grain boundary regions consist only of insulating phase R (resistivity > 1 GΩ cm and $f_{max} < 10$ Hz at RT) and, therefore, only one electrical-active response is observed by IS. With increasing sintering temperature, the conducting phase SC emerges and grows from the (inner) core part of grains at the expense of phase R, giving rise to another M'' peak at higher frequency in the modulus plot. The conducting SC phase exhibits resistivity < 1 kΩ cm and f_{max} > 10 MHz at RT. The volume fraction of the grain shell and "neck-like" grain boundary regions containing phase R decreases until the grain shell and "neck-like" grain boundary regions become a resistive thin-layer that can be considered as a well-defined grain boundary region. Ceramics sintered at 1100 °C therefore effectively consist of semiconducting (SC) grains and resistive (R) grain boundaries.

We postulate the change in resistivity of the respective phases is influenced by the Cu-loss mechanism reported recently by Schmidt *et al.*[14] with phase SC being Cu-deficient with respect to phase R. Although the oxygen-loss mechanism may also be present, it appears that diffusion of copper from within the grains towards the grain boundaries may be responsible for the evolution of the semiconducting (SC) phase with increasing processing temperatures. The resistive phase R of CCTO can be prepared by low temperature processing, *e.g.* HEM where the Cu-loss mechanism is suppressed or retained in the Cu-rich outer (shell) grain/grain boundary regions in ceramics processed at high temperatures. Single crystals of CCTO grown from high temperature methods are semiconducting with $R_b \sim 10$ to 15 Ω cm at RT and are therefore composed of phase SC.

For CCTO ceramics sintered at high temperatures (~1100 °C), the grain composition is off stoichiometry (due to Cu and/or oxygen loss) and becomes semiconducting; however, the main grain boundary insulating R phase (apart from possible isolated CuO/Cu_2O phases) may have a composition close to stoichiometric CCTO for two possible reasons: a) diffusion of Cu from the grain to grain boundary regions resulting in no Cu loss in the grain boundary regions, and, b) no significant oxygen loss in the grain boundary regions when sintered in air, presumably due to fast oxygen diffusion along grain boundaries on cooling from the sintering temperature.

The conduction mechanisms in insulating phase R and semiconducting phase SC remain unclear at this stage. Thermoelectric power measurements on ceramics sintered at 1000–1100 °C show CCTO to be an n-type semiconductor.[13,17] In these samples, phase SC is the bulk phase and this suggests it exhibits n-type semiconductivity. To date there have been no transport studies on low temperature sintered CCTO ceramics that primarily consist of insulating phase R and therefore the type of charge carrier in phase R is unknown. Further studies on the pO_2 dependence of the conductivity of phase R in ceramics in combination with thermoelectric power measurements, Transmission Electron Microscopy (TEM) and Electron Energy Loss Spectroscopy (EELS) measurements are currently ongoing to resolve the conduction mechanisms in these CCTO-type phases.

Conclusions

The evolution of grain resistivity and 'electrical microstructure' in CCTO ceramics with sintering temperature (from 700 to 1100 °C) was recorded using Modulus Spectroscopic plots from Impedance Spectroscopy data. Ceramics sintered at 700 °C consist of insulating grains with RT resistivity > 1 GΩ cm. With increasing sintering temperature the insulating grains transform to semiconducting grains and exhibit much smaller RT resistivity (by at least six orders of magnitude when sintered at 1100 °C). The volume fraction of the insulating and semiconducting phases change with the sintering temperature to give the semiconducting grains and insulating grain boundaries required for the Internal Barrier Layer Capacitance (IBLC) mechanism responsible for the high effective permittivity at radio frequencies in dense ceramics. Such a transformation from insulating phase into semiconducting phase and the evolution of the IBLC mechanism are linked to the diffusion and eventual volatilisation of copper at elevated processing temperatures.

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