Universidade de Aveiro
2014

Departamento de Electrónica, Telecomunicações e Informática

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Funcionalidades de Encaminhamento Ótico de Pacotes

All-Optical Routing Functionalities

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Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Eletrotécnica, realizada sob a orientação científica do Doutor António Luís Jesus Teixeira, Professor Associado do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro e do Doutor Paulo Sérgio de Brito André, Professor Associado no Departamento de Engenharia Eletrotécnica e de Computadores do Instituto Superior Técnico da Universidade de Lisboa.

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agradecimentos/ acknowledgments

Firstly, I would like to express my gratitude to Professor Dr. António Teixeira for giving me the opportunity to be a member of his research group and for his invaluable advice, guidance and constant encouragement during the elaboration of this thesis.

I would like also to thank Professor Dr. Paulo André for taking active interest in the progress of my thesis.

I am also extremely grateful to the partners of EU NoE EURO-FOS project for giving me all the facilities and invaluable support. Special thanks to Professor Dr. Hercules Avramoupoulos, Dr. Christos Kouloumentas, Dr. Alexandros Maziotis and Dr. Marios Bougioukos for the warm reception in my one-week stay at the photonic lab of the National Technical University of Athens, in Greece.

I am also extremely grateful to Dr. Tanay Chattopadhyay for his many fruitful discussions, collaborative research and, especially, friendship.

I would like also to thank my colleagues of IT optical group for being always willing to help and create such friendly environment, making my time there more enjoyable, in particular Dr. Ana Rocha, Eng. Ali Shahpari, Dr. Berta Neto, Dr. Giorgia Parca, Dr. Rogério Dionisio and Eng. Vitor Ribeiro.

I acknowledge Ministério da Educação and Instituto de Telecomunicações (IT) for the amazing working conditions.

On a more private note, I would like to thank all my family, especially Daniel for having faith in me and encouraging me throughout this project, and particularly in the last few months of my thesis writing.
Last, but not least, for my beautiful baby Duarte, you are trully my best achievement accomplished during this PhD work.

palavras-chave

Portas lógicas óticas, flip-flops óticos, encaminhamento ótico de pacotes, interferómetro Mach-Zehnder, amplificadores óticos semicondutores, processamento ótico de sinal, memórias óticas, modulação cruzada de fase.

Resumo

As soluções totalmente óticas para a comutação e encaminhamento de pacotes de tráfego são cruciais para a realização de uma rede verdadeiramente transparente. Para atender às exigências crescentes de maior largura de banda, tais redes de comutação de pacotes óticos exigem a implementação de funções digitais na camada física. Este cenário estimulou-nos a investigar e a desenvolver memórias totalmente óticas, focando-nos principalmente na implementação de flip-flops óticos síncronos, cujo estado de comutação é accionado por um sinal de relógio.

Esta tese também apresenta novas soluções para implementar portas lógicas óticas, visto estas serem um elemento fundamental para o desenvolvimento de funcionalidades complexas de processamento.

A maioria dos esquemas propostos neste trabalho são baseados em estruturas interferométricas activas Mach-Zehnder (SOA-MZI) devido às suas características intrínsecas, nomeadamente, razão de extinção elevada bem como elevada capacidade de integração.

A implementação experimental de um sistema de encaminhamento de pacotes totalmente ótico foi realizada usando cascatas de SOA-MZIs. O impacto da potência residual, devido à comutação não ideal dos SOA-MZIs, foi também analisado.

Keywords

All-optical logic gates, all-optical flip-flops, all-optical packet routing, Mach-Zehnder interferometer, semiconductor optical amplifier, all-optical signal processing, optical storage, cross phase modulation.

Abstract

All-optical solutions for switching and routing packet-based traffic are crucial for realizing a truly transparent network. To meet the increasing requirements for higher bandwidth, such optical packet switched networks may require the implementation of digital functions in the physical layer. This scenario stimulated us to research and develop innovative high-speed all-optical storage memories, focusing mainly on bistables whose state switching is triggered by a pulsed clock signal. In clocked devices, a synchronization signal is responsible for controlling the enabling of the bistable.

This thesis also presents novel solutions to implement optical logic gates, which are basic building blocks of any processing system and a fundamental element for the development of complex processing functionalities.

Most of the proposed schemes developed in this work are based on SOA-MZI structures due to their inherent characteristics such as, high extinction ratio, high operation speed, high integration capability and compactness.

We addressed the experimental implementation of an all-optical packet routing scheme, with contention resolution capability, using interconnected SOA-MZIs. The impact on the system performance of the reminiscent power of the blocked packets, from the non ideal switching performed by the SOA-MZIs, was also assessed.

To my family

Contents

List of acronyms

AOFF	All-Optical Flip-Flop
BER	Bit Error Rate
BPF	Band Pass Filter
CLK	Clock
CW	Continuous Wave
EDFA	Erbium Doped Fiber Amplifier
O/E/O	Optical-Electrical-Optical
ER	Extinction Ratio
FWM	Four-Wave Mixing
HNLF	Highly Non-Linear Fiber
MZI	Mach-Zehnder interferometer
SOA-MZI	Mach-Zehnder Interferometer with Semiconductor Optical Amplifiers
MZM	Mach-Zehnder Modulator
NOLM	Non-Linear Optical Loop Mirror
NRZ	Non-Return-to-Zero
OCDMA	Optical Code Division Multiple Access
PC	Polarization Controller
PRBS	Pseudo-Random Bit Sequence
PS	Phase Shifter
RSOA	Reflective Semiconductor Optical Amplifier
RZ	Return-to-Zero
SOA	Semiconductor Optical Amplifier
VOA	Variable Optical Attenuator

WDM	Wavelength Division Multiplexing
XGM	Cross Gain Modulation
XPM	Cross Phase Modulation

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Chapter 1

Introduction

The exponential growth of internet traffic and new internet-based services (such as video on demand, voice over IP, video teleconference and multimedia services) have been the major driving forces for the increasing demand of transmission bandwidth over the last years. This is making network operators looking for optical approaches in order to allow higher transmission rates, maintaining the efficiency of the network.

All-optical devices can provide data format transparency, higher-speed processing, smaller foot-print and, expectably, lower power consumptions, compared to their electronic counterparts [1]. The optical-electrical-optical (O/E/O) conversions required for routing information between electronic circuits and the optical transmission medium impose a severe bottleneck, which limits the data bit rate and the traffic capacity that can be processed [2]. Today, the current maximum bandwidth obtained by electronic processing is typically around 40 Gb/s, while the maximum capacity of optical transport within a fiber has exceeded 20 Tb/s, which shows the limited speed of electronic processing [3]. An increase in the optical packet bit rate will increase the difficulty in using electronic devices. Indeed, routing a high number of packets per second through the several layers of electronics in a router, can cause router congestion and exceed the performance of electronics and the ability to efficiently handle with the high level of heat generated [4]. Therefore, is desirable that switching and routing can be carried out directly over the optical domain. Such optical packet switch networks require the implementation of digital functions in the physical layer, namely all-optical logic gates and all-optical flip-flops.

All-optical logic gates are crucial devices in optical networks because they can execute essential signal processing functions such as switching, regeneration and header recognition processing in photonic switching nodes. All-optical gates are capable to perform Boolean logic operations at high data bit rate and, in recent years, considerable research has been done mainly due to technology advances in monolithic and hybrid integration. In [5] and [6], a NOT logic gate is demonstrated

based on a semiconductor optical amplifier assisted Sagnac interferometer and by using a single optical directional coupler configuration, respectively. In [7], an optical NOT gate with variable threshold is implemented using dual wavelength injection locking. In [8], is proposed an all-optical XOR gate with optical feedback using highly Ge-doped nonlinear fiber and a terahertz optical asymmetric demultiplexer, whereas in [9] an optical logic AND gate is implemented based on a nonlinear optical loop mirror (NOLM). Others approaches use an electroabsorption modulator (EAM) [10] or exploit the nonlinearity of semiconductor optical amplifiers such as cross gain modulation (XGM) of SOA based devices [11] and [12] or are based on four-wave mixing phenomenon [13].

A basic building block of any router, electrical or optical, is the memory circuit. It is essential for storing, temporarily, the header information of a packet and for solving the contention problem that occurs when several packets arrive for the same port, at the same time. Using fiber delay lines (FDLs), as an optical buffer to store optical packets, it is possible to prevent packet loss in a switch. When packets arrive at the same time, they are routed to different FDLs, with delay equivalent to the packet length, and the collision can be avoided. However, this technology doesn´t allow neither long-term storage nor random access at an arbitrary timing. Another problem is that FDLs introduce losses that increase with its size [14].

One of the most important optical devices for buffering decisions in next generation photonic transmission systems is the optical flip-flop. This device has at least two stable states and its operation principle is based on hysteresis phenomena, in which is possible to obtain multiple states under the same input conditions. In general, hysteresis can be achieved by a combination of a feedback mechanism and a nonlinear effect. In a conventional flip-flop, the bistability operation is performed in the ‘S-shaped’ hysteretic region, and the output state is distinguished by the different output power while in the optical memory, the state can be distinguished by different output wavelengths [15]. An optical bistable is a sequential device therefore its outputs not only depend of the input values in a considered instant, but also depend of information from a previous state, so it can be used as a one-bit optical memory.

Different technologies have been proposed to implement all-optical flip-flops such as the use of SOA based Mach-Zehnder interferometer (SOA-MZI) with a feedback loop [16], two coupled fiber ring lasers [17] or two coupled SOA-MZI [18]. Among these approaches, the ones that use active interferometric devices have attracted increasing attention because they require low energy to operate, have high compactness and extinction ratio (ER), as well the potential for further optical integration. Exploiting the non-linear effects of active Mach-Zehnder interferometer has enabled the demonstration of most of the novel techniques proposed in this PhD work.

Clocked flips-flops are some of the most used elements in digital very-large-scale integration (VLSI) systems, but scaling CMOS sequential logic is extremely difficult, namely due to the power consumed of their leakage currents. Therefore, it is so important to find high-speed and low-power optical clocked flip-flops capable to overcome the limitations of CMOS technology. In the last years, most of the research of optical flip-flops has been done considering mainly the asynchronous operation, where any change of information in the flip-flop inputs is transmitted, immediately, to the output according to the truth table. However, in some cases the inputs can suffer unwanted variations and if we are using asynchronous devices, we can be storing unwanted information. The dynamic operation of an asynchronous bistable device can be changed by providing an additional synchronization input (CLK), in order to control the enable of the flip-flop, making it sensitive or not to the values present at its inputs. Most of our work regarding flip-flops is concentrated on devices operating synchronously.

Besides all the known applications that an optical bistable device can fulfill namely, as clock dividers, optical counters and shift registers, optical flip-flops are essential building blocks for implementing all-optical packet routing configurations such as the one shown in Figure 1.

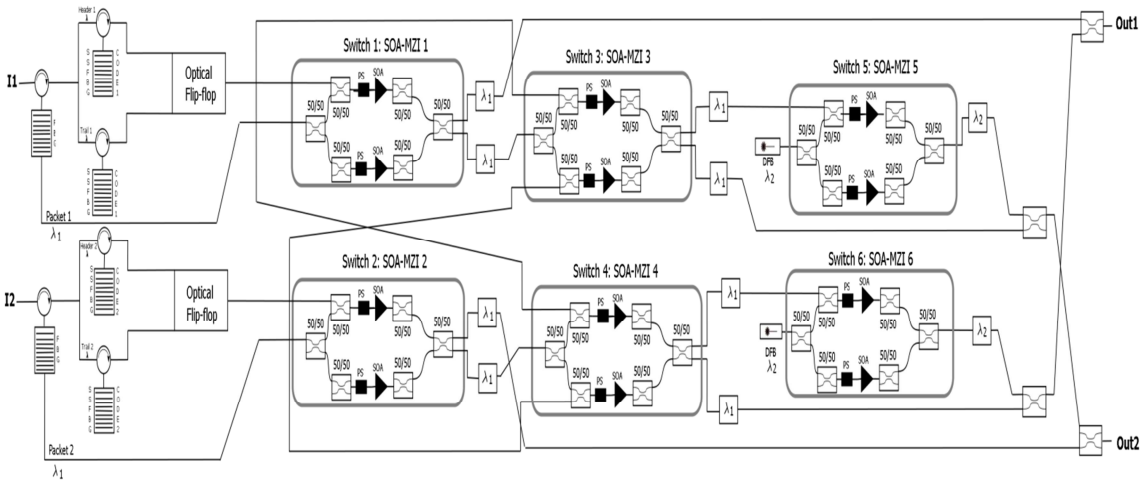

Figure 1- Schematic of an all-optical router.

Figure 1 comprises four main building blocks: the all-optical header/label processing block, the optical buffer unit, the switching stage based on SOA-MZI switches and the collision detection/solver block.

The first functional block performs header processing recognition in the optical domain through autocorrelation. Here, optical code division multiple access (OCDMA) codes are used to encode the packet addresses and sent in a separate wavelength band (out of band signalling). Employing the OCDMA labelling scheme, the routing information is encoded by scrambling the label with a

specific OCDM code, which may be viewed as a local address [19]. The address recognition unit consists in a well-matched decoder with time reversed impulse response compared to the encoded signal. The fact that optical code processing can be realized in the optical domain provides the possibility to overcome speed limitations due to optical/electrical conversions required in header processing and enhance the energy efficiency of the routing nodes. The proper autocorrelation function of the matching pair is pursued, in order to provide the triggering signal for buffering elements of the routing node. Concerning the management of the spectral addressing band, the encoding process allocates a distinct spectral band compared to the band devoted to data transmission. The second block consists of all-optical flip-flops for holding temporary the packet duration. The third building block of the all-optical packet router consists of two parallel SOA-MZI structures (first SOA-MZI stage of Figure 1) and based on the information coming from the flip-flop output, it switches the optical packets through cross phase modulation (XPM), which results in an interference process, that can be constructive or destructive. Finally, the collision detector and solver blocks are implemented based also on hybrid integrated SOA-MZIs. If both optical packets are routed to the same output port, at the same time, collision is detected by the second SOA-MZI stage of Figure 1 (SOA-MZI3 and SOA-MZI4) and then avoided by the collision solver block based on wavelength conversion.

Others photonic routing schemes have been also designed and experimentally validated. In [20], is proposed a photonic routing system that performs on-the-fly contention resolution between 40 Gb/s packets of the same wavelength whereas in [21] asynchronous packets are routed by combining packet detection, space switching and self-resetting latches.

1.1 Thesis motivation and outline

As described in the previous section, with the continuously growth of Internet traffic, it is necessary to develop new techniques and devices capable to support the huge bandwidth required by the future services, with scalability and flexibility. This scenario stimulates us to research and develop innovative high-speed photonics solutions, such as all-flip-flops and logic gates, for the effective operation of transparent optical networks. Some of the research results presented in this work were performed under the EU NoE EURO-FOS project consortium and it was performed mainly in the facilities of Instituto de Telecomunicações (IT) in Aveiro, and during a one-week stay at the photonic lab of the National Technical University of Athens, in Greece. The following

chapters present an analysis and novel concepts of some of the main building blocks of all-optical packet routing schemes. This thesis is constituted by five chapters, organized as follows.

Chapter 1 provides a brief background about photonic transmission systems and devices, and describes the organization of the thesis as well as its main scientific contributions to the state-of-art.

Chapter 2 focuses on the design and operation principle behind all-optical logic gates, since they are a fundamental element for the development of complex processing functionalities. Two novel optical logic gates configurations, capable to perform different logic operations, are presented and described. The first method is experimentally and numerically demonstrated and uses, simultaneously, both output ports of an active interferometer. The second configuration is based on a single Mach-Zehnder interferometer, with controlled phase modulators, and performs different Boolean logic operations without changing setup design. The non-linear behavior of a SOA-MZI is also described regarding gain and phase dynamics, since it is the base of most of the applications studied and proposed throughout this PhD work. An all-optical logic XOR gate based on a SOA-MZI, is also compared in terms of the way the incoming signal is injected (co or counter propagation) via numerical simulations and experimentally.

Chapter 3 presents an overview of the state of the art on all-optical flip-flops, discussing their basic designs and theoretical concepts. We appraised, quantitatively, in terms of commuting speed, switching energy and integration capability some of the most relevant experimental AOFF implementations and the obtained results demonstrate the suitability of them in next generation communication systems. In this chapter, we also proposed four new all-optical flip-flop configurations, experimentally and by means of simulation, focusing mainly in bistables whose state switching is triggered by a pulsed clock signal.

Chapter 4 addresses the technical solution of the contention problem that can arise from packets aiming the same switch port but, firstly, an overview of some of the most preeminent all-optical routing designs, with particular relevance for the ones using SOA-MZI structures, is outlined. The reminiscent power of the blocked packets, due to the non ideal switching performed by the SOA-MZIs, is analyzed in every stage of the routing configuration and the performance transmission is experimentally evaluated through BER measurements and extinction ratio analysis.

Chapter 5 overviews the developed work, summarizes the main conclusions, and presents suggestions for future work.

1.2 Main contributions

The main contributions of this work can be summarized as follows:

- Development and experimental demonstration of four optical Boolean operations based on a single SOA-MZI, using simultaneously both output ports.

- Investigation of an all-optical logic XOR gate and assessment of its performance in co and counter propagation schemes.

- Development and validation through numerical simulation of an optical configuration that provides 16 optical logic operations, using a single MZI with controlled phase modulators in each arm, without changing the setup scheme.

- Proposal and experimental implementation of all-optical S-R and D type clocked flip-flops, using SOA-MZI structures.

- Proposal and performance demonstration, through numerical simulations, of an all-optical S-R flip-flop using two gain-clamped RSOAs.

- Proposal and theoretical analysis of an all-optical clocked D flip-flop using a single SOA assisted symmetric MZI.

- Identification and experimental demonstration how the reminiscent power of blocked packets from non ideal SOA-MZIs can affect the data performance transmission.

1.3 List of publications

The work accomplished during the elaboration of this PhD work resulted in 13 papers published/ submitted in internationally peer reviewed journals and 16 international conference proceedings. The publications are listed below.

1.3.1 Journal Articles

[J1] C. Reis, T. Chattopadhyay, P.S. André, A. Teixeira, "Single Mach-Zehnder interferometer based Boolean logic gates", *Applied Optics*, Vol. 51, no. 36, pp. 8693 - 8701, December 2012.

[J2] C. Reis, T. Chattopadhyay, G. Parca, R. Dionísio, P. André, A. Teixeira, " All-optical multifunctional logic operations using simultaneously both interferometric output ports in a symmetric SOA-MZI", submitted to *Optics and Laser Technology*.

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[J5] C. Reis, A. Maziotis, C. Kouloumentas, C. Stamatiadis, N. Calabretta, P.S. André, R.P. Dionísio, B. Neto, H.J.S Dorren, H.Avromopoulos, A.T. Teixeira, "All-Optical Clocked D Flip-Flop Memory using a Hybrid Integrated S-R Latch", *Microwave Optical Technology Letters*, Vol. 53, no.6, pp.1201-1204, June 2011.

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[J8] T. Chattopadhyay, C. Reis, P.S. André, A. Teixeira, "Theoretical analysis of all-optical clocked D flip-flop using a single SOA assisted symmetric MZI", *Optics Communications*, Vol. 285, no. -, pp. 2266 - 2275, April 2012.

[J9] C. Reis, G. Parca, M. Bougioukos, A. Maziotis, S.Pinna, H. Brahmi,G. Giannoulis P.André, N. Calabretta, V. Vercesi, G. Berrettini, C. Kouloumentas, A. Bogoni, T. Chattopadhyay, D. Erasme, H. Avramoupoulos, A. Teixeira, "Experimental analysis of an all-optical packet routing", *IEEE/OSA Journal of Optical Communications and Networking*, Vol. 6, No. 7, pp. 629–634, July 2014.

[J10] B. Neto, C. Reis, R.P. Dionísio, J. Ferreira, J. Lázaro, G. Tosi-Beleffi, A.N. Pinto, R. N. Nogueira, A.T. Teixeira, P.S. André, "Assessment and mitigation of EDFA gain transients in hybrid WDM/TDM PON in the presence of packet based traffic", *IET Optoelectronics, SPECIAL ISSUE ON Next Generation Optical Access*, Vol. 4, No. 6, pp. 219 - 225, December 2010.

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1.3.2 International Conferences

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Chapter 2

Optical logic gates

In the last few years, optical logic gates have been widely investigated in order to overcome the speed limitation of electrical signal processors. All-optical gates can be used in a variety of signal processing applications, such as optical bit pattern recognition, optical time division demultiplexing, optical bit-error rate monitoring, optical label swapping as well as in optical binary adders and optical counter [22, 24].

Several approaches have been proposed up-to-date to demonstrate different optical logic operations and mostly are based on highly nonlinear optical fibers (HNLFs), on microring or on nonlinear effects in semiconductors optical amplifiers (SOAs), integrated or not in interferometric structures. The HNLF-based logic gates exploit the Kerr effect of silica, through a response in few femtosecond range however, despite the significant advances in fabrication technology, HNLFs still present severe limitations when integration is required. In general, optical logic gates based on the nonlinear effects in SOAs, such as cross-gain modulation (XGM), cross-phase modulation (XPM), four wave mixing (FWM) and cross polarization modulation have been preferred mainly due to their high potential for photonic integration and cascadability, high gain of SOAs and strong change of the refractive index. However, they present speed limitation and latency, primarily due to the slowly recovery time of the SOAs. Operation speed can be increased with the integration of SOAs in interferometer structures, especially in Mach-Zehnder interferometers.

Semiconductor optical amplifiers in Mach-Zehnder interferometers (SOA-MZI) are the key devices for the majority of the all-optical processing functionalities studied and proposed in this PhD thesis, therefore a characterization of this device will be made in this work.

This chapter, based on journals [J1], [J2], [J6] and conferences [C1], [C2], [C3], [C4], starts with the presentation of the operation principle of the SOA-MZI and explains the steps to balance the interferometer so it can work properly. In Section 2.2, we propose and experimentally demonstrate a configuration based on a single hybrid integrated SOA-MZI switch capable to carry

out different logic operations at the same time, using simultaneously both output ports of the interferometer. In this section, we also perform a comparison study of an all-optical logic XOR gate based on a SOA-MZI, implemented in co and counter propagation way. In Section 2.3, we present a novel scheme that performs 16-Boolean logic operations based on a single Mach-Zehnder interferometer with controlled phase modulators, using the same design. The novel configurations proposed in this chapter present very low complexity and suggest high integration potential. Finally, in section 2.4, a summary of the research topics discussed in this chapter is drawn.

2.1 Mach-Zehnder interferometer structures with semiconductor optical amplifiers (SOA-MZI)

SOA-MZIs are widely used in many optical applications since they perform a variety of optical functions such as, on-off keying (OOK) and multi-format optical signals regeneration, wavelength conversion, all-optical switching, high-speed logical processing and, more recently, optical contention resolution. The SOA-MZI is an element that provides high extinction ratio, high operation speed, requires low switching energies to operate and have high integration capability and compactness.

2.1.1 Operation principle of SOA-MZI

In this PhD work, we propose optical circuits mostly based on the symmetrical hybrid integrated SOA-MZI shown in Figure 2, where each arm incorporates one Semiconductor Optical Amplifier (SOA1 or SOA2) and one Phase Shifter (PS1 or PS2).

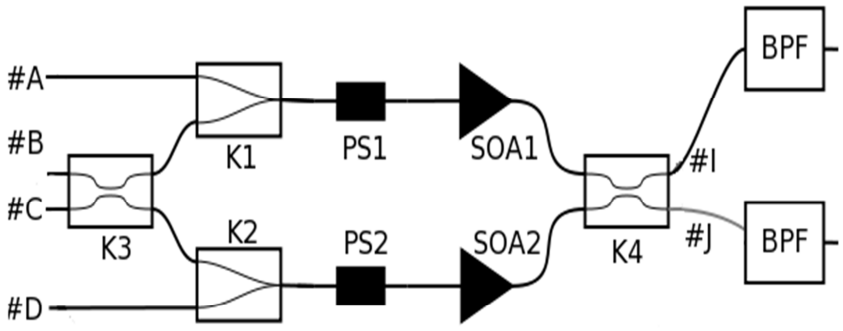


Figure 2 - Schematic of an all-optical SOA-MZI switch.

Although it is possible to operate active interferometer structures with discrete components, monolithic or hybrid integration allows longer term stability. K3 and K4 are couplers of the SOA-MZI based switch for dividing and combining the incoming data entering at ports #B or/and #C. The power at the interferometric outputs (#I and #J) is a result of an interference process occurring in coupler K4. The electromagnetic fields at this coupler will define the conditions for the output measurements [26].

The SOA-MZI operation principle is based on cross phase modulation effect and relies on the dependency of the refractive index on the carrier density in the active region of the SOA. A control signal that depletes the carrier density will modulate the refractive index and thereby result in a phase modulation of the incoming data coupled into the SOA-MZI. For example, if one control signal is injected into one of the MZI input ports (#A or #D), through the directional couplers K1 or K2, it will deplete the carriers density of the corresponding SOA. When the SOA is under gain saturation, the refractive index will change as a consequence of the gain saturation variations and a phase difference is created in the signals being amplified. In this case, the incoming data flow out to the respective bar output ports. However, if the control signals are launched simultaneously into ports #A and #D, SOA1 and SOA2 will have the same carrier density, so will not suffer a change in their refractive index and thereby the incoming data will exit from the respective output cross-ports. The same happens when there is no control signals applied into the SOA-MZI switch.

The band pass filters (BPF), placed at the output ports, are used to recover the incoming data and to block the control signals.

2.1.2 Balancing the SOA-MZI

In this subsection, is explained the balancing process that is realized each time an experiment using active interferometers - SOA-MZI – is implemented.

Due to very small changes in motherboard fabrication there is a very small effective path length difference in each arm of the MZI, which causes a small phase change and slightly unbalance the MZI. Similar effects are also seen in the SOAs contained in each arm of the MZI. Therefore, when we are using SOA-MZI structures it is very important to firstly balance the interferometer to get it to work properly. The SOA-MZI is balanced when a maximum extinction ratio (ER) between the interferometer output ports is achieved.

For the balancing process of a SOA-MZI, we use the experimental setup depicted in Figure 3. Firstly, we connect a continuous wave signal (CW) into port #B of the device, followed by a polarization controller (PC), and then set the power to a typical value, for example 1 dBm, with a

variable optical attenuator (VOA). Since the device is optically symmetric, the CW signal can also be coupled to one of the following SOA-MZI ports: #C, #I or #J. Then, we monitored the output power at port #I and #J with two power meters (PM). Note that is also possible to measure simultaneously the output power at both ports using a single power meter but, in this case, an optical switch connected at ports #I and #J is needed.

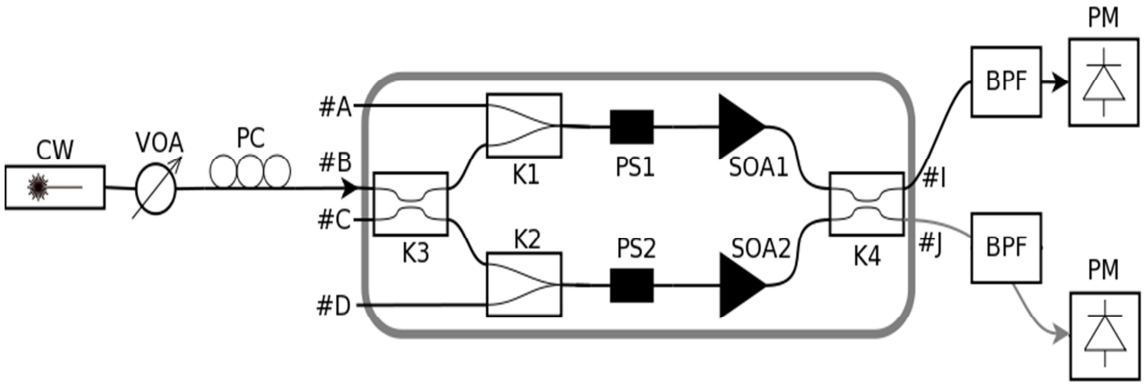


Figure 3 - Experimental setup to balance the SOA-MZI.

When the Peltier controller is powered on and the temperature of the device is stabilized (26º C), we set the bias current of both SOAs to an equal value, adjust the input CW polarization and apply a voltage to one or both phase shifters to obtain a minimum power value on the destructive MZI output (port #I) and a maximum power at the constructive port (Port #J). In the end, normally a small detuning on the SOA bias current and in the input power is needed in order to improve the ER, but at every change, we need to re-adjust the voltage of the phase shifters and the input polarization.

In order to obtain the maximum extinction ratio (ER) between the output ports, tunable filters are placed at the MZI output ports to improve the balancing results.

In Figure 4, we vary from 150 mA to 540 mA the bias current of SOA1 (ISOA1), maintaining constant the bias current of SOA2 (ISOA2=200 mA). The mean power of the incoming signal, injected into port #B of the SOA-MZI was increased from -8 dBm (in Figure 4 (a)) to 8 dBm (in Figure 4 (b)). These experimental results highlight the fact that by changing the operational parameters, the interference process suffers considerable changes. We can see clearly that in Figure 4 (b), even without input CW polarization and phase shifters adjustments, a better operational point was achieved. It is also noticeable that in Figure 4 (b), at certain moment, the constructive output port converts in the destructive port, and vice versa, only by changing some system parameters and not by injecting a control signal into SOA-MZI.

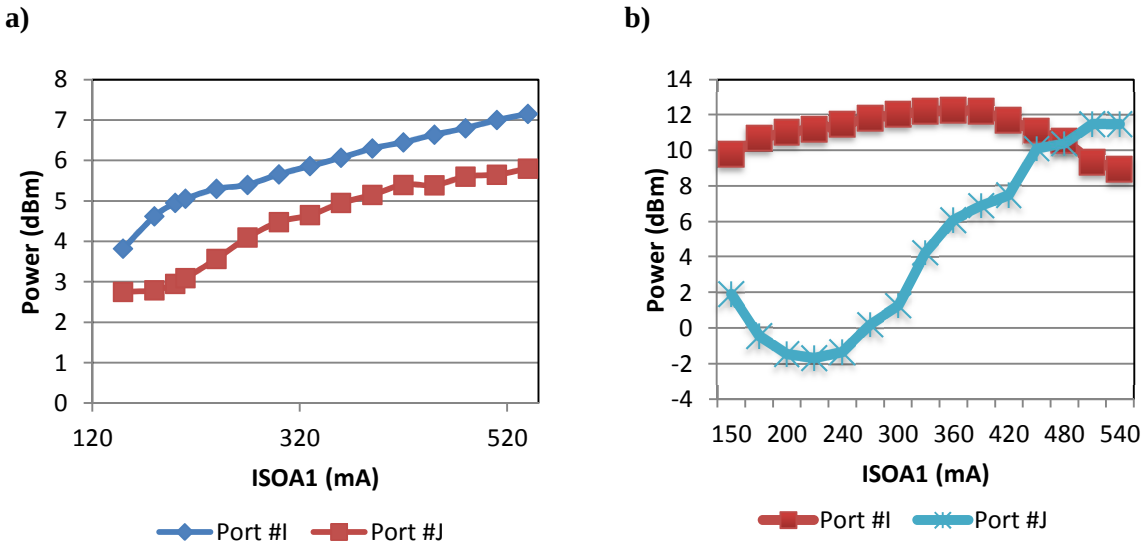


Figure 4 – (a) SOA-MZI interference at the output ports with P_{CW}= -8 dBm. (b) SOA-MZI interference at the output ports with P_{CW}= 8 dBm. Lines are visual guides.

2.2 All-optical logic operations using a symmetric SOA-MZI

Logical operation using a single SOA-MZI switch is an attractive technology due to the small device size, low power consumption and complexity. Depending on the signals applied into its input ports, a single SOA-MZI switch is capable to carry out different logic operations at the same time, using simultaneously both output ports of the SOA-MZI. Traditional logic gates have a single output, but if we take advantage of the two output ports of the SOA-MZI based interferometric switch as logical outputs, it is possible to obtain multi output logic functions. Using this concept, we proposed a novel all-optical configuration capable to carry out four logic operations, using simultaneously both output ports of the SOA-MZI. The performance of such architecture is assessed measuring the obtained extinction ratio (ER) for each Boolean function. The proposed circuit is simulated and experimentally demonstrated, using NRZ-OOK modulated signals driven at 10 Gb/s.

2.2.1 Operation principle

Four Boolean operations (AND, Transposed INHIBITION, EQUIVALENCE, INVERTER) can be performed depending of the signals applied into the input ports #a, #b and #c of the

interferometric structure illustrated in Figure 5. At the output ports #I and #J, optical band pass filters are placed in order to recover the signal injected into port #b.

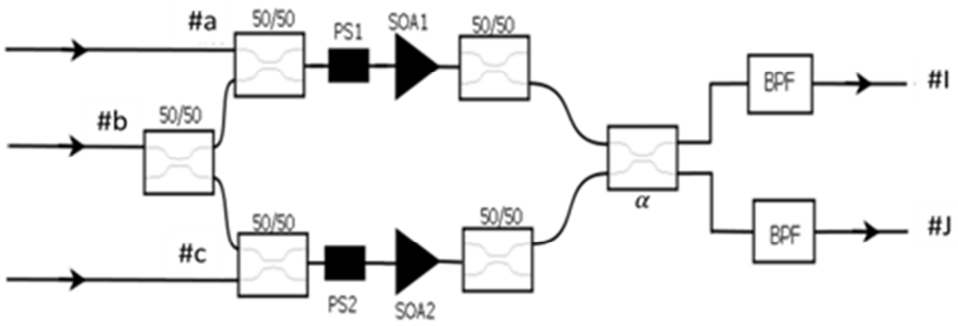


Figure 5 - Schematic diagram of the proposed all-optical circuit based on a single SOA-MZI. BPF: Band pass filter, PS: Phase shifter, SOA: Semiconductor optical amplifier. The input ports of the SOA-MZI are #a, #b, #c and the output ports are #I, #J.

Table 1 represents the truth table of the proposed circuit and from this table it is possible to obtain the logical expression at the output ports. Therefore, the Boolean equations at the interferometric output ports, expressed in the disjunctive canonical form, are given by

$$\begin{aligned} I &= a \cdot b \cdot \bar{c} + \bar{a} \cdot b \cdot c \\ J &= \bar{a} \cdot b \cdot \bar{c} + a \cdot b \cdot c \end{aligned} \tag{2.1}$$

Where the symbols '$\cdot$' and '$\bar{}$' indicate logical 'AND' and 'INVERTER/NOT' expression, respectively. Equations (2.1) are already in their simplified form, so it is not necessary to use Karnaugh maps or apply Boolean algebra to obtain a simpler solution.

Consider two modulated signals X=[10010000] and Y=[00010010], at the same wavelength, and a continuous signal at a different wavelength. If signals X and Y are injected, respectively, at port #a and port #b of the SOA-MZI switch (no signal at port #c), according to equation (2.1) the logical expressions at the output ports can be written as

$$\begin{aligned} I &= X \cdot Y \cdot \bar{0} + \bar{X} \cdot Y \cdot 0 = X \cdot Y \\ J &= \bar{X} \cdot Y \cdot \bar{0} + X \cdot Y \cdot 0 = \bar{X} \cdot Y \end{aligned} \tag{2.2}$$

which correspond to the logic ‘AND’ and ‘Transposed INHIBITION’ operations between the two modulated optical beams. Also, based on this case, an ‘EQUIVALENCE’ and ‘NOT’ logic operations can be obtained, simultaneously, at port #I and port #J of the SOA-MZI if the signal X is launched at port #a and the continuous signal at port #b.

In this situation, the logic equations at the interferometric output ports are

$$I = X \cdot 1 \cdot \bar{0} + \overline{X} \cdot 1 \cdot 0 = X \qquad (2.3)$$
$$J = \overline{X} \cdot 1 \cdot \overline{0} + X \cdot 1 \cdot 0 = \overline{X}$$

Table 1: Truth table of the proposed all-optical circuit. #a, #b, #c: interferometric input ports; #I, #J: interferometric output ports.

Expected logic levels					**Experimental static power measurements (dBm)**	
Inputs			**Outputs**			
a	**b**	**c**	**I**	**J**	**I**	**J**
0	0	0	0	0	-12,2	-12,2
0	0	1	0	0	-12,1	-13,7
0	1	0	0	1	-10,4	9,1
0	1	1	1	0	7,5	-8,7
1	0	0	0	0	-13,7	-12,2
1	0	1	0	0	-13,7	-12,4
1	1	0	1	0	7,9	-8,2
1	1	1	0	1	-11,2	2,4

On the other hand, if signal Y is injected at port #c while at port #b we maintain the continuous wave signal, the logical expressions at the output ports #I and #J can be written according to equation (2.1) as

$$I = 0 \cdot 1 \cdot \overline{Y} + \overline{0} \cdot 1 \cdot Y = Y$$
$$J = \overline{0} \cdot 1 \cdot \overline{Y} + 0 \cdot 1 \cdot Y = \overline{Y} \quad (2.4)$$

From these two latter cases, we can conclude that if a control signal is injected at port #a or port #c of the SOA-MZI, the two even parts of the continuous wave signal (injected at port #b) will propagate through the two MZI arms and will suffer different gains and phase shifts, leading to the unbalance of the SOA-MZI. In these cases, the modulation of the refractive index will not be the same ($n_{SOA1} \neq n_{SOA2}$) and the light in the upper arm of the MZI will present a different velocity than the lower arm; hence a replica of the control signal appear at port #I (EQUIVALENCE operation), and its complementary at port #J (NOT operation). This technique to implement the NOT operation is designed with a very simple logic circuit since it is performed using only two optical signals (one modulated and another continuous), contrary to the NOT implementations that uses three optical signals. In section 3.2, using also two optical signals, we implemented a NOT gate based on cross gain modulation in a SOA to realize our all-optical D synchronous flip-flop. To perform the XGM based NOT gate, a modulated signal (with λ1) was injected in a SOA and modulated the gain of the amplifier due to its saturation. We coupled to the modulated signal a continuous wave (with λ2), which was modulated by the gain variation of the SOA, and at the output of the SOA, a band pass filter to eliminate the signal with wavelength λ1. The advantage of this technique lies in its simplicity, polarization independence and insensitivity to the wavelength of the modulated data (provided it is within the SOA gain bandwidth). However, presents some disadvantages such as a decreased extinction ratio for up-converted signals and pattern effects of the SOA due to the slow recovery time [27].

2.2.2 Black box static model

Our logic configuration is characterized experimentally in terms of non-ideal splitting factors and SOA1, 2 gains, following the method adopted in [26].

The measurements of SOA-MZI output power as function of input power and SOA current is made considering the two arms separately, using forward propagation, from input #a to output #I, with SOA2 disabled and, similarly, from input #c to output #J, with SOA1 disabled. The trends of the SOA output power vs. SOA current and input power are found and the obtained curves are shown in Figure 6(a) and Figure 6 (b). It is worth noting that this characterization is referred to the

overall path on which the signal propagates, so it takes into account losses and any other kind of asymmetry of the device.

The power at the output of the SOA-MZI (#I and #J) is a result of an interference process occurring in coupler α. The electromagnetic fields at the two inputs of this coupler will define the conditions for the outputs measured. So, specifically, when used as an amplitude modulator, one important factor to take into consideration is the ER of the output signal. For example, through SOAs input power/current variation, the power distribution on the SOA-MZI arms can be further changed, leading to the consequent variation of the interference conditions on output couplers.

a) b)

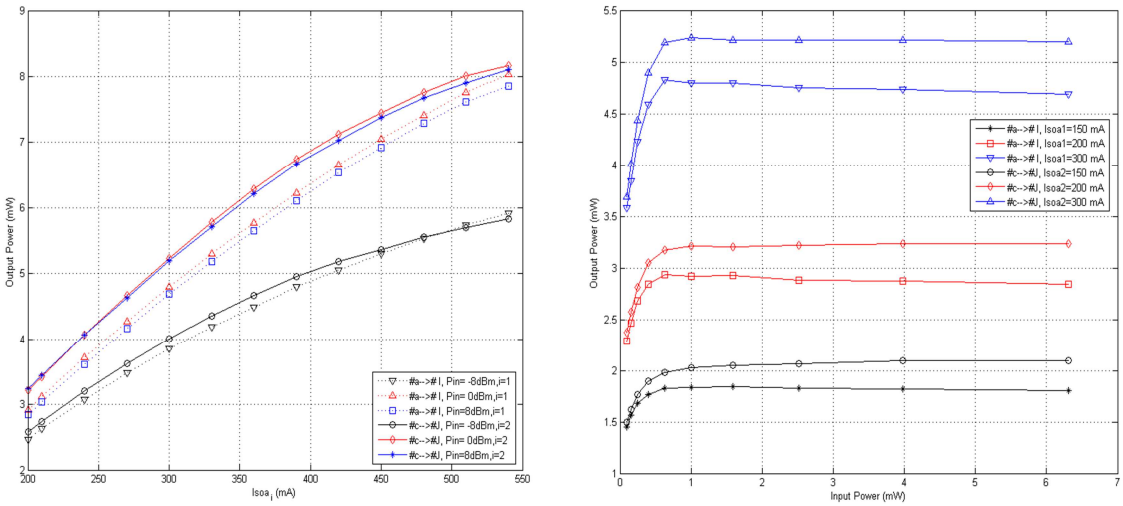


Figure 6 - #I and #J output power as function of (a) SOA_1, SOA_2 current variation and (b) #a, #c input power. Lines are visual guides.

Moreover, a phase shift on SOAs output signals is induced due to the dependence of SOAs refractive index on carrier density.

We model the working characteristic for a SOA-MZI, in order to describe how physical parameters actually control the interference depth, thus providing a tool for operational point optimization, which for example can be used for maximizing ER.

The output powers P_I (port #I) and P_J (port #J) are indirectly computed as a function of the SOAs' total input power level and SOAs' bias current (Isoa) through SOA 1,2 gain curves reported in Figure 6.

In Table 2, all the 3-bit words obtained combining the 0-1 levels on the inputs #a, #b, #c are considered and identified through the index i=1,…8.

Table 2: Possible input combinations.

Input	*i =1*	*i =2*	*i =3*	*i =4*	*i =5*	*i =6*	*i =7*	*i =8*
#a	*0*	*0*	*1*	*1*	*0*	*0*	*1*	*1*
#b	*1*	*1*	*1*	*1*	*0*	*0*	*0*	*0*
#c	*0*	*1*	*0*	*1*	*0*	*1*	*0*	*1*

A black box model, representing the relation between #I and #J output power as function of input power on port #b, obtained from interferometric structure principles considering the couplers yield, path differences and non-ideality, is given by [26]:

$$\begin{aligned} P_{I_i} &= (1-\alpha)P_{1b_i} + \alpha P_{2b_i} - \sqrt{P_{1b_i} P_{2b_i}}\,\sin(\Delta\phi_i + s_{1_i}) \\ P_{J_i} &= \alpha P_{1b_i} + (1-\alpha)P_{2b_i} + \sqrt{P_{1b_i} P_{2b_i}}\,\sin(\Delta\phi_i + s_{2_i}) \\ \Delta\phi_i &= \Delta\phi_{a_i} - \Delta\phi_{c_i} + \Delta\phi_{b_0} = kP_a - kP_c + \frac{\pi}{2} \end{aligned} \tag{2.5}$$

Where α is the splitting factor of the last coupler evaluated experimentally. P_{1bi} and P_{2bi} are the power levels on λ_b at the input of the rightmost coupler in Figure 5. $\Delta\phi_i$ is the phase difference between the two arms, which depends on the individual phase shift induced by the input #a on upper arm $\Delta\phi_{a_i}$, input #c on lower arm $\Delta\phi_{c_i}$ and input #b $\Delta\phi_{b_0}$ on both arms. The first two are considered linear with the respective input power, because of the linear relation between SOA induced phase and carrier density, through refractive index variation, taking into account that the SOAs' current was kept constant. The last phase shift is considered constant at the value $\frac{\pi}{2}$ due to the initial balancing operation. The other internal couplers yield, path length differences between the upper and lower arms, the SOA carrier density variations and non-ideality of the tested architecture, are taken into account through further phase delays s_{1i} and s_{2i}.

The SOA-MZI black box static model provides a general frame of how parameters control the interference depth, thus providing a tool for operational point optimization, which for example can be used for maximize the ER.

The parameters' values of the black box model, α estimated experimentally and the others through MATLAB, are reported in Table 3 and used for the final validation, carried out considering the measured output powers P_I and P_J, with $Isoa_1$ and $Isoa_2$ constant at 240 mA.

Table 3: Parameters extracted from the model fittings and used in the final validation.

α	k	$\Delta\phi_{b_0}$	s_{1_i}	s_{2_i}
0.51	*6,3x10³*	$\frac{\pi}{2}$ *rad*	$-1 \div 2$ *rad*	$-1 \div 2$ *rad*

After balancing the SOA-MZI, the basic switching operation is performed injecting a signal on port #a or #c: this will produce the interference inversion so that the injected signal will be forwarded through port #I, while the power on port #J is minimized.

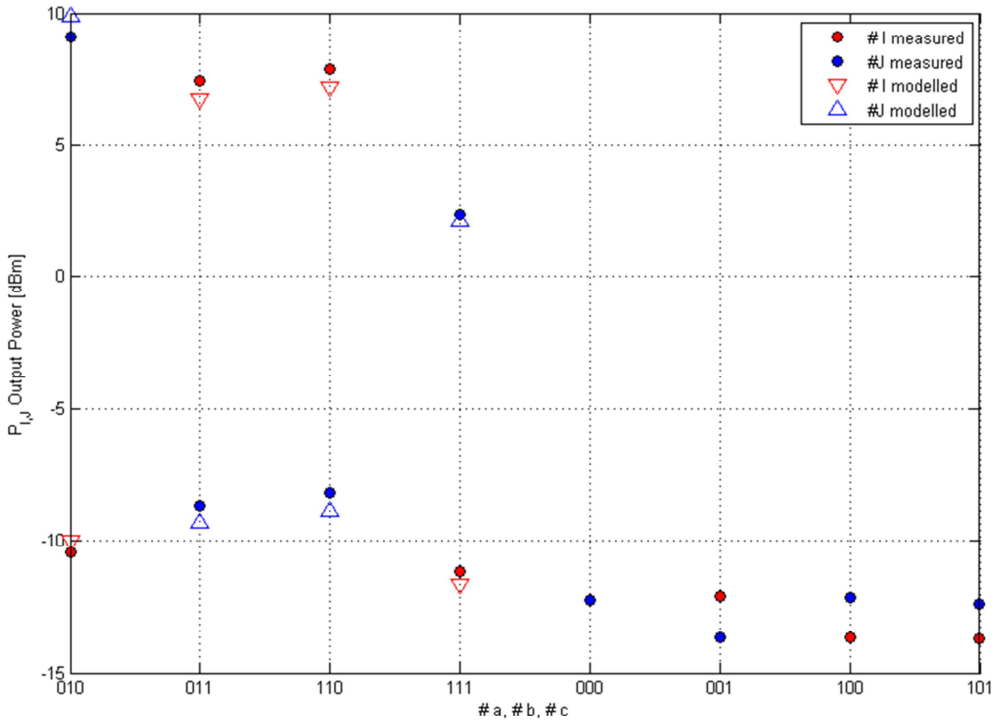
In order to verify the logical operations, we use MATLAB environment and the black box model. At the output ports we measured the power levels corresponding to the expected logic operation on the wavelength of the signal injected in #b input, λ_b . Thus, in all the cases where port #b is set to zero, no wavelength conversion was performed.

In Figure 7, we present the comparison among the obtained experimental static power measurements shown in Table 1 and the modeled output power levels. Through the static black box model, it is possible to find a good matching with the correct output levels, applying the optimization of all the parameters that affect the output interference, exactly as it happens experimentally when the maximum ER between the port #I and #J has to be achieved.

The ER optimization is strictly dependent on each inputs combination, due to the different XGM/XPM effect induced by the two SOAs. The 4th case (input combination=111), illustrated in Figure 7, explains how the power levels and the ER are reduced in practice because of the gains saturation and the presence of the three inputs a#, b#, c# set at logical level 1.

The interference depth can be maximized in theory and in practice through adjustments of the phase shifters contribution; in our formulation for the static model we included their contributions in the parameters $s_{1_i}$and s_{2_i}.

For all these reasons, the ER maximization in practice is obviously achieved differently for each case. This is why, for example, cases 2 (input combination=011) and 3 (input combination=110) are slightly different in power levels and ER, although the input configuration is the same, except for injecting signal at input #c in case 2 and at input #a in case 3.



#a	#b	#c	#I	#J
X	Y	-	$X \cdot Y$	$\bar{X} \cdot Y$
X	CW	-	X	$\bar{X}$
-	CW	Y	Y	$\bar{Y}$

$$\#I = a \cdot \mathrm{b} \cdot \bar{c} + \bar{a} \cdot \mathrm{b} \cdot c$$

$$\#J = \bar{a} \cdot \mathrm{b} \cdot \bar{c} + a \cdot \mathrm{b} \cdot c$$

Figure 7 - Comparison between measured and modeled output power levels versus #a, #b, #c input logic levels (level 0→0 mW; level 1→ 0.5 mW).

2.2.3 Experimental results

To experimentally demonstrate these different logic functions using both interferometric output ports of the SOA-MZI, we implemented the setups depicted in Figure 8. They consist of two DFB lasers peaking at 1549.32 nm and 1547.72 nm, followed by polarizations controllers to adjust the input polarization. The laser at 1549.32 nm is externally modulated by a Mach–Zehnder operating at 10 Gbit/s, with an ER of 11 dB, amplified by an Erbium Doped Fiber Amplifier (IPG-EAD-500-C3-W) and then split into two equal parts using a 3 dB coupler. The control data sequence is equal to X=[10010000] and is produced by a BERT pattern generator (Agilent N4901B). Different data

patterns, launched into the SOA-MZI ports (CIP 100G-2R2-ORP), are obtained by delaying the X signal, using an optical delay line.

The signal at 1547.72 nm works in continuous wave (CW), and its power is adjusted by a variable optical attenuator (VOA).

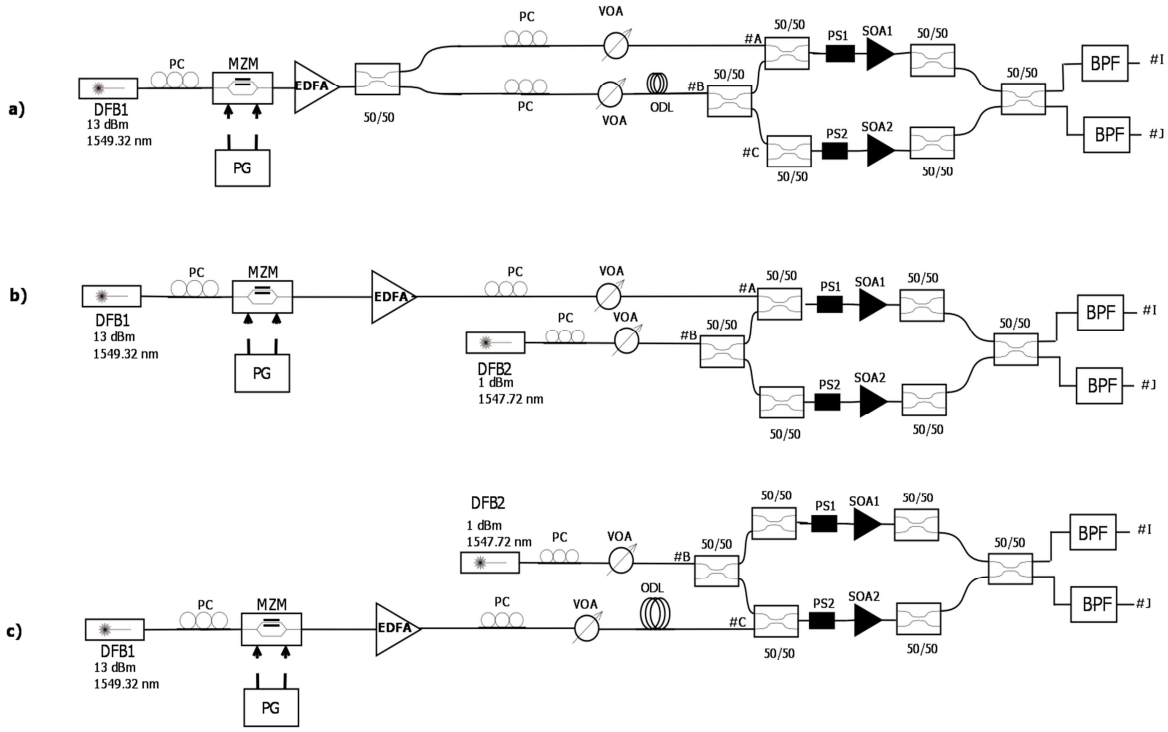


Figure 8 - Experimental setups: a) to obtain $I = X \cdot Y$ and $J = \overline{X} \cdot Y$; b) to obtain $I = X$ and $J = \overline{X}$; c) to obtain $I = Y$ and $J = \overline{Y}$.

The output signals are obtained using a filter with a 25 GHz bandwidth (X-tract Net Test), centered at the wavelength of the signal injected in port #b of the SOA-MZI.

A PIN (HP-11982A), with responsivity of 0.7 A/W, and an oscilloscope (Agilent Infinium 86100A) are used to analyze the temporal evolution of the different all-optical logic operations.

Initially, the SOA-MZI is balanced by acting on the SOAs gain and on the voltage of the phase shifters, so that in the absence of modulated control signals, the continuous wave signal injected in port #b could experience a complete destructive interference at port #I.

From the experimental setup depicted in Figure 8(a), we obtain the results of the all-optical AND gate operation shown in Figure 9. In this case, the modulated signals X and Y are respectively launched into port #a and port #b and, at the interferometric output ports, we obtain

simultaneously the logical functions $I = X \cdot Y$ and $J = \overline{X} \cdot Y$. The measured ER for these two all-optical logic functions was 12.4 dB and 12.2 dB at port #I and port #J, respectively.

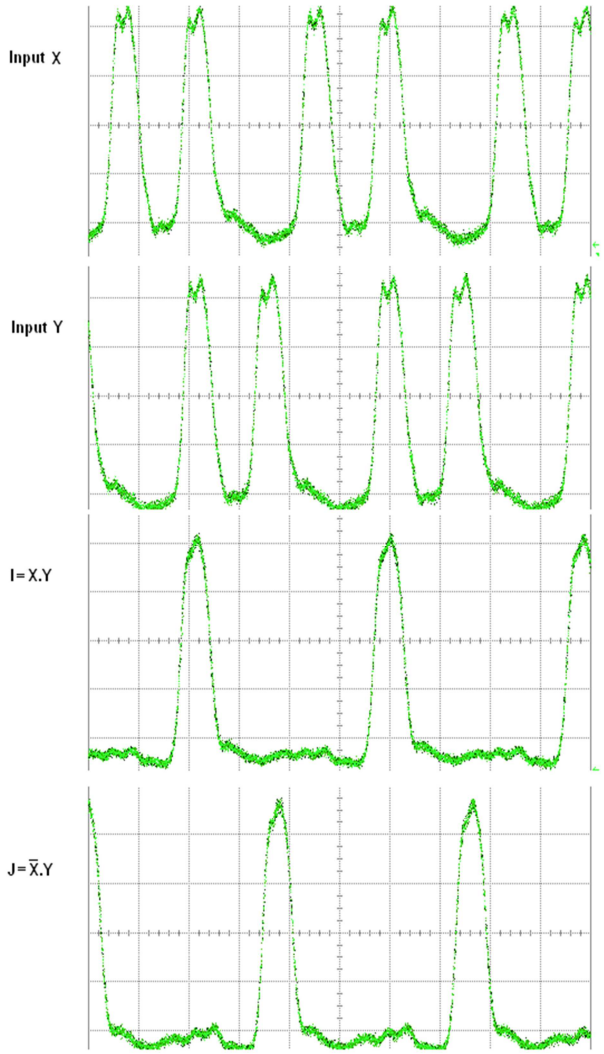


Figure 9 - Experimental time domain traces obtained for Boolean functions $I = X \cdot Y$ and $J = \overline{X} \cdot Y$. Horizontal scale is 200ps/div and Y axis represents optical power in arbitrary units.

In Figure 8 (b) and Figure 8 (c), the CW signal is injected at port #b of the SOA-MZI, and the control modulated signals X and Y are, respectively, injected at port #a in Figure 8 b) and at port #c in Figure 8 c) in order to obtain the NOT operation and its complementary. Figure 10 shows the results of the all-optical NOT logical gate operation and its complementary: the left figure shows the results when the control signal X is injected in port #a of the SOA-MZI and the right figure when the control signal Y is injected at port #c. The ER for each of these logic

functions was also experimentally analyzed and when the control signal X is injected we obtained 10.5 dB at port #I and 14 dB at port #J; when the control signal Y is injected we obtained 10 dB at port #I and 11.8 dB at port #J.

The experimental results show, in general, extinction ratio values higher than 10 dB, which proves the potential of using both output ports of the SOA-MZI to obtain, simultaneously AND/Transposed INHIBITION and EQUIVALENCE/INVERTER logic functions.

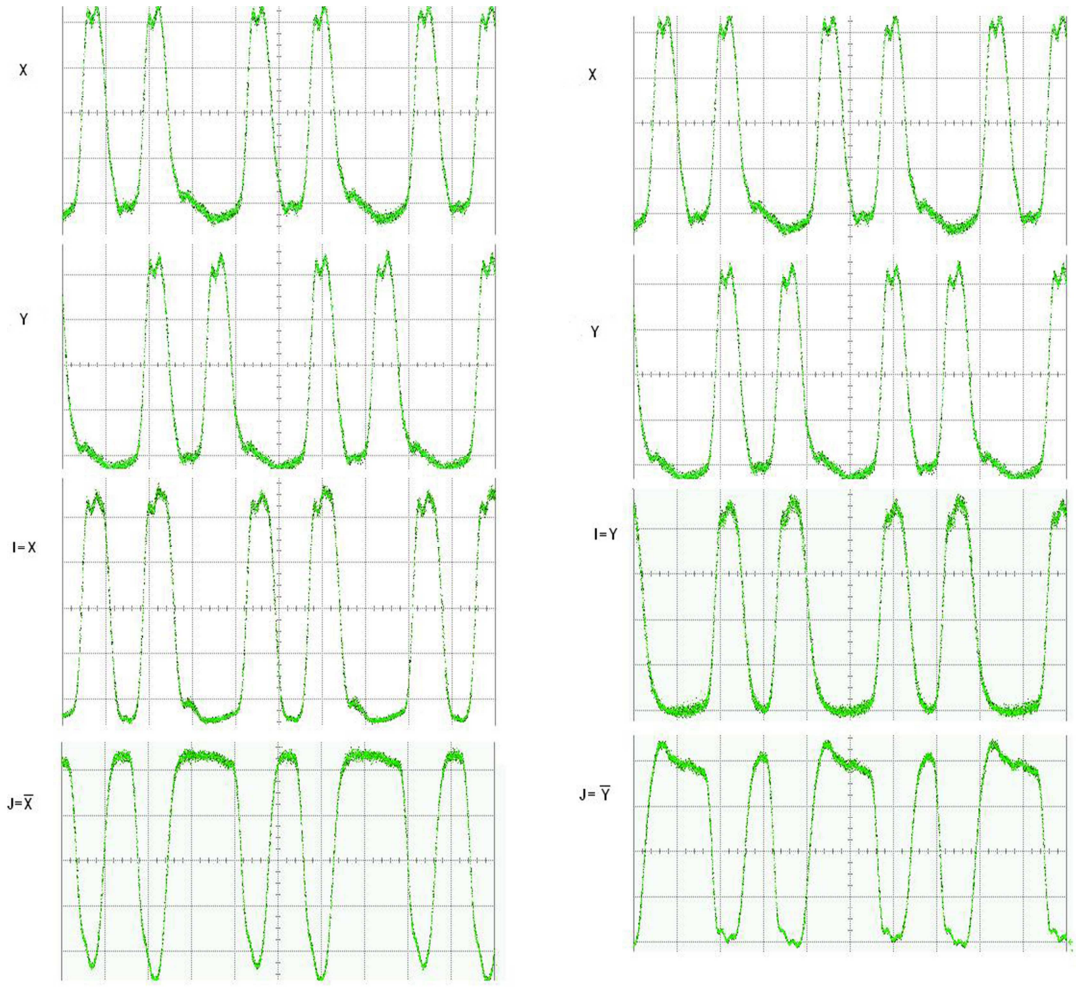


Figure 10 - Experimental time domain traces obtained for Boolean functions: on the left $I = X$ and $J = \overline{X}$; on the right $I = Y$ and $J = \overline{Y}$. Horizontal scale is 200ps/div and Y axis represents optical power in arbitrary units.

2.2.4 All-optical XOR using a co and counter propagation schemes

It was also implemented an all-optical logic XOR gate based on a hybrid integrated SOA-MZI, using NRZ modulated signals driven at 10 Gbit/s.

Two logic XOR schemes, depicted in Figure 11, are implemented in co and counter propagation, and the results obtained, experimentally and from simulation (using Virtual Photonics Inc. Software (VPI)), are compared.

For the co-propagation scheme, the incoming signal, a continuous wave (CW) lasing at 1546.12nm and with 0 dBm average power, is launched into port #B and the XOR signal is recovered at port #I, using a filter with a 25 GHz bandwidth and centered at the incoming signal wavelength.

The counter-propagation scheme uses the same incoming signal but it is launched into port #I of the SOA-MZI. In this case, the output is now at port #B. For this counter-propagation setup, an isolator is placed between the EDFA and the 3 dB coupler.

Both control data signals, peaking at 1549.32 nm, are launched into the SOA-MZI (CIP 40G-2R2-ORP) port #A and port #D through an optical delay line, a variable optical attenuator and a polarization controller to adjust and synchronize the signals. Different data patterns are obtained by delaying signals at port #A and port #D.

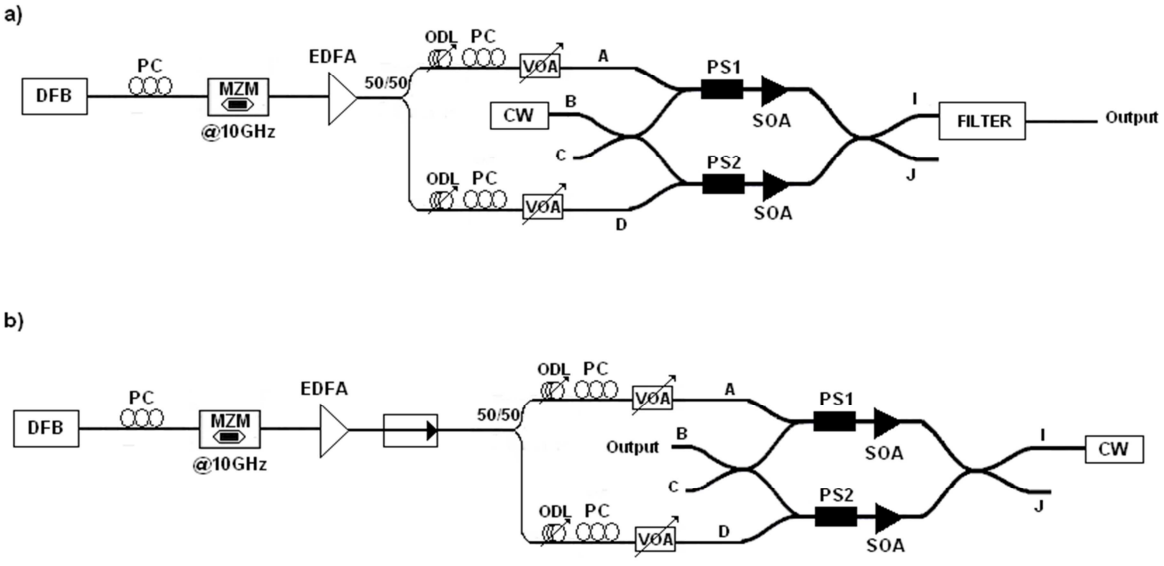


Figure 11 - Experimental setup a) co-propagation scheme b) counter-propagation scheme. DFB: distributed-feedback laser; PC: polarization controller; MZM: Mach-Zehnder modulator; EDFA: erbium doped fiber amplifier; ODL: optical delay line; VOA: variable optical attenuator; CW: continuous wave; SOA: semiconductor optical amplifier; PS: phase shifter.

By adjusting the optical powers and the bias currents of the SOAs, the incoming signal can interfere either constructively or destructively at the output of the interferometer, directly performing the logic XOR operation of the two input data signals.

Figure 12 illustrates the control data input signals injected into the arms A and D of the SOA-MZI, each with 2 dBm mean power, and the corresponding XOR gate output, at 10 Gbit/s. The results obtained experimentally are in agreement with the operation principle of an XOR gate, since the output is at the logical level '0' only when both of the inputs signals have the same value.

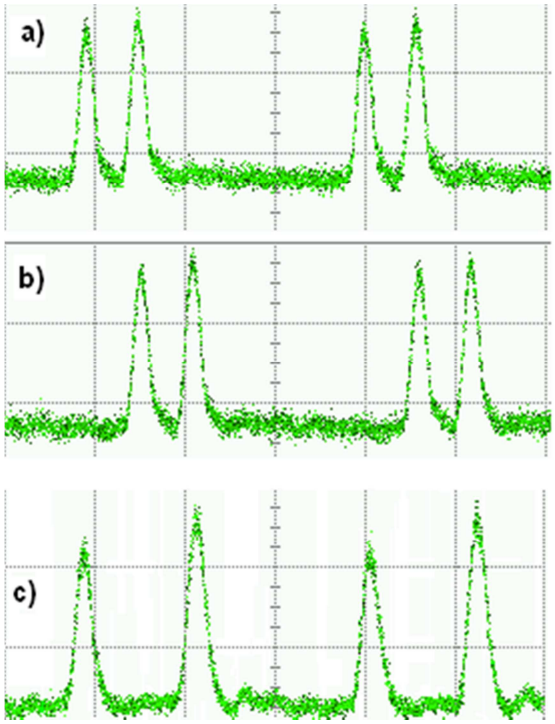


Figure 12 - XOR output. Vertical scale is arbitrary and horizontal scale is 500 ps/div.

Simulation of both systems depicted in Figure 11 is done using the VPI Software. The SOA parameters are based on the parameters used in [28] and they are illustrated in Table 4.

Table 4: Parameters used in simulation for the SOA-MZI XOR gate.

Parameter	Value	Unit
Injection Current	0.2	A
Length	4.25×10^{-4}	M
Width	1.5×10^{-6}	M
Height	1×10^{-7}	M
Optic Confinement	0.2	
Internal Losses	2×10^{-9}	m^{-1}
Differential Gain	1.5×10^{-20}	m^2
Carrier Density Transp.	1.5×10^{-12}	m^{-3}
Index To Gain Coupl.	5	
Linear Recombination	5×10^{7}	s^{-1}
Bimolecular Recombination	1×10^{-16}	m^3s^{-1}
Auger Recombination	7.5×10^{-41}	m^6s^{-1}
Initial Carrier Density	1×10^{-12}	m^{-3}

Figure 13 presents the performance of all-optical XOR gates with the variation of the input power of the NRZ data signals from 0 to 4 dBm, maintaining at the same power the CW control signal (0 dBm).

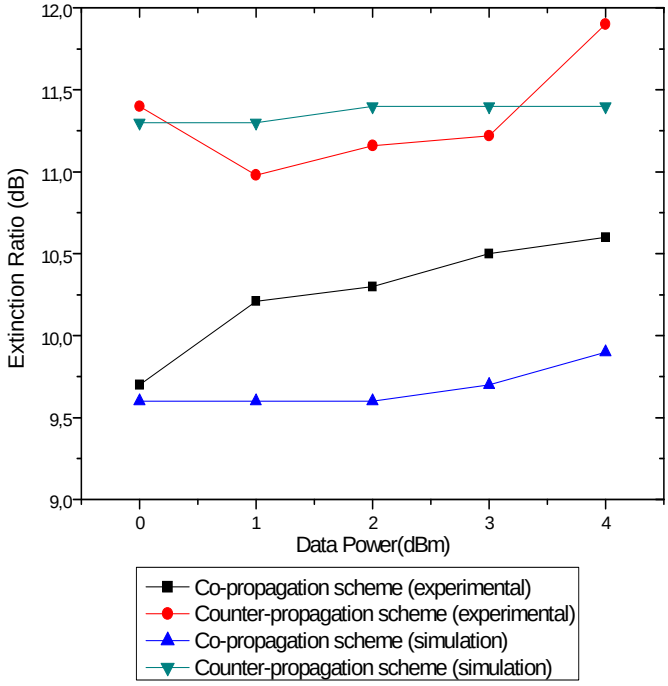


Figure 13 - Performance of all-optical XOR gate Vs Input data signal.

For both co and counter-propagation scheme, the performance of the XOR gate is almost independent of the input power, since the power variation of the two data signals involved in the comparison is the same. However, the counter-propagation scheme shows a better performance, with a slight improvement on the extinction ratio, ranging from 0.72 dB to 1.64 dB. We can also conclude that the simulation results are in good agreement with the experimental measurements.

2.3. Boolean Optical Logic Gates using a Single Mach-Zehnder Interferometer

In an attempt to overcome the speed limitation and latency of the SOAs due to their slowly recovery time, we present a novel configuration that provides 16 optical logic operations, using a single MZI with controlled phase modulators in each arm, without changing the setup scheme. Conventional logical circuits are designed with one output, so each logic operation can only be realized once at a time. This means that the output port can present the '0' logic level, i.e., no light, although the circuit is fed with light signal at its inputs. Data loss can be prevented if is designed a circuit with two outputs, in which one is the complement of the other. The proposed scheme uses both interferometric output ports of the MZI, so every input data can reach any of the ports, with no data loss [29],[30]. Since both output ports are complementary, for the same operational conditions we can obtain, simultaneously, two different optical logic gates.

Figure 14 depicts the proposed configuration of the 16-Boolean optical logic circuit and it consists of a single MZI, with a programmable phase modulator (PM) in each arm.

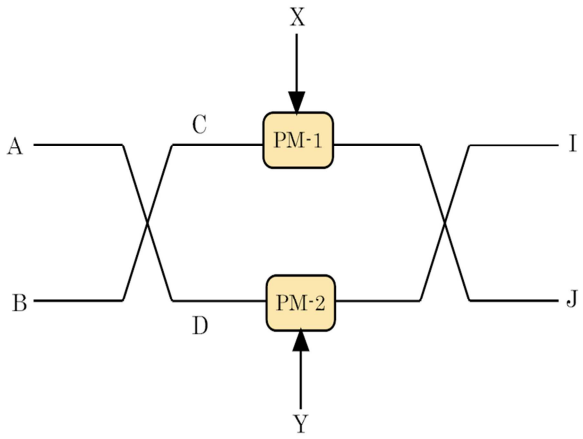


Figure 14 - Schematic diagram of proposed MZI based 16-logical operation circuit. PM: phase modulator.

The operating principle can be explained as follows. When an optical signal is launched into port #A, its power is distributed, equally, through both MZI arms, by the input 3-dB coupler, with a phase shift of $\pi/2$. Then, the signals experiment an optical phase change in response to an applied voltage, provided by the controlled phase modulators placed in each MZI arm. The input signals X and Y will program the phase modulators, in order to control the phase change in the arms of the interferometer. The phase modulators are mostly based on the electro-optic effect, in which an electrical field is applied to an electro-optic element, creating a change in its refractive index.

Finally, when the optical signals arise at the output 3-dB coupler, they will suffer another phase shift of $\pi/2$ and, at the MZI output ports, different output levels are obtained. Therefore, since the 3-dB couplers of the MZI introduce always the same phase shift, the sixteen logic circuits are obtained by simply adjusting the voltage of the controlled phase modulators in the setup, in order to get the desired optical phase change in the MZI arms.

Next, the mathematical model of the proposed circuit is presented and is also described the operational conditions to implement 16 logical operations.

2.3.1. Theoretical model and 16-logic operation cases

Considering that the path length of the two arms of the interferometer is the same (L), and that both signals present the same wavelength (λ), the MZI arms have a phase difference $\Delta\theta$ that can be described by

$$\Delta\theta = \frac{2L\pi}{\lambda}(n_1 - n_2) = \frac{2L\pi}{\lambda}\Delta n = \theta_1 - \theta_2 \tag{2.6}$$

Assuming that the scattering matrix (also called propagation matrix) of a 2x2 guided-wave coupler is given by

$$\begin{bmatrix} \sqrt{1-\varepsilon} & j\sqrt{\varepsilon} \\ j\sqrt{\varepsilon} & \sqrt{1-\varepsilon} \end{bmatrix} \tag{2.7}$$

Then, according to the latter expression, the output fields intensities of the ideal 3-dB input coupler (50/50 coupling ratio, i.e, ε = 0.5) can be calculated as

$$\begin{bmatrix} E_C \\ E_D \end{bmatrix} = \begin{bmatrix} \frac{1}{\sqrt{2}} & j\frac{1}{\sqrt{2}} \\ j\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \cdot \begin{bmatrix} E_A \\ E_B \end{bmatrix} \tag{2.8}$$

Considering that the propagation matrix of a phase shifter is given by [31]

$$\begin{bmatrix} e^{j\frac{\Delta\theta}{2}} & 0 \\ 0 & e^{-j\frac{\Delta\theta}{2}} \end{bmatrix} \tag{2.9}$$

Then the transfer matrix of a MZI can be defined as

$$\begin{bmatrix} \frac{1}{\sqrt{2}} & j\frac{1}{\sqrt{2}} \\ j\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \cdot \begin{bmatrix} e^{j\frac{\Delta\theta}{2}} & 0 \\ 0 & e^{-j\frac{\Delta\theta}{2}} \end{bmatrix} \cdot \begin{bmatrix} \frac{1}{\sqrt{2}} & j\frac{1}{\sqrt{2}} \\ j\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{2.10}$$

Note that the output coupler has also 50/50 coupling factor.

Equation (2.10) can be re-written as

$$\begin{bmatrix} \frac{1}{2}e^{j\frac{\Delta\theta}{2}} - \frac{1}{2}e^{-j\frac{\Delta\theta}{2}} & j\frac{1}{2}e^{j\frac{\Delta\theta}{2}} + j\frac{1}{2}e^{-j\frac{\Delta\theta}{2}} \\ j\frac{1}{2}e^{j\frac{\Delta\theta}{2}} + j\frac{1}{2}e^{-j\frac{\Delta\theta}{2}} & -\frac{1}{2}e^{j\frac{\Delta\theta}{2}} + \frac{1}{2}e^{-j\frac{\Delta\theta}{2}} \end{bmatrix} \tag{2.11}$$

Knowing that $e^{j\frac{\Delta\theta}{2}} = \cos\frac{\Delta\theta}{2} + j\sin\frac{\Delta\theta}{2}$, equation (2.11) can be simplify and the electric fields of the output of the interferometer can be calculated as

$$\begin{bmatrix} E_I \\ E_J \end{bmatrix} = \begin{bmatrix} j\sin\frac{\Delta\theta}{2} & j\cos\frac{\Delta\theta}{2} \\ j\cos\frac{\Delta\theta}{2} & -j\sin\frac{\Delta\theta}{2} \end{bmatrix} \cdot \begin{bmatrix} E_A \\ E_B \end{bmatrix} \tag{2.12}$$

In the absence of an optical signal in port #B, the output powers can be found by:

$$\begin{aligned} P_I &= E_I \cdot E_I^* = \sin^2\left(\frac{\Delta\theta}{2}\right) P_A \\ P_J &= E_J \cdot E_J^* = \cos^2\left(\frac{\Delta\theta}{2}\right) P_A \end{aligned} \tag{2.13}$$

From these equations we can plot the normalized output powers P_I and P_J with $\Delta\theta$, as illustrated in Figure 15(a). From this graph we can conclude that, at $\Delta\theta = 180^0$, P_I is maximum and P_J is minimum. At $\Delta\theta = 90^0$, $P_I = P_J = 0.5$, showing that is possible to vary the output power with $\Delta\theta$.

Hence, the crosstalk at the different MZI ports also varies, as illustrated in Figure 15(b). Crosstalk is defined by the ratio of the powers at the non-targeted port (P_{nt}) and targeted port (P_t) of the MZI, i.e.

$$XT = 10\log\left(\frac{P_{nt}}{P_t}\right) \tag{2.14}$$

In an optical device, to increase the performance the crosstalk effect should be minimum. With our proposed configuration, we can create different output powers and crosstalk by applying different phases to the phase modulators.

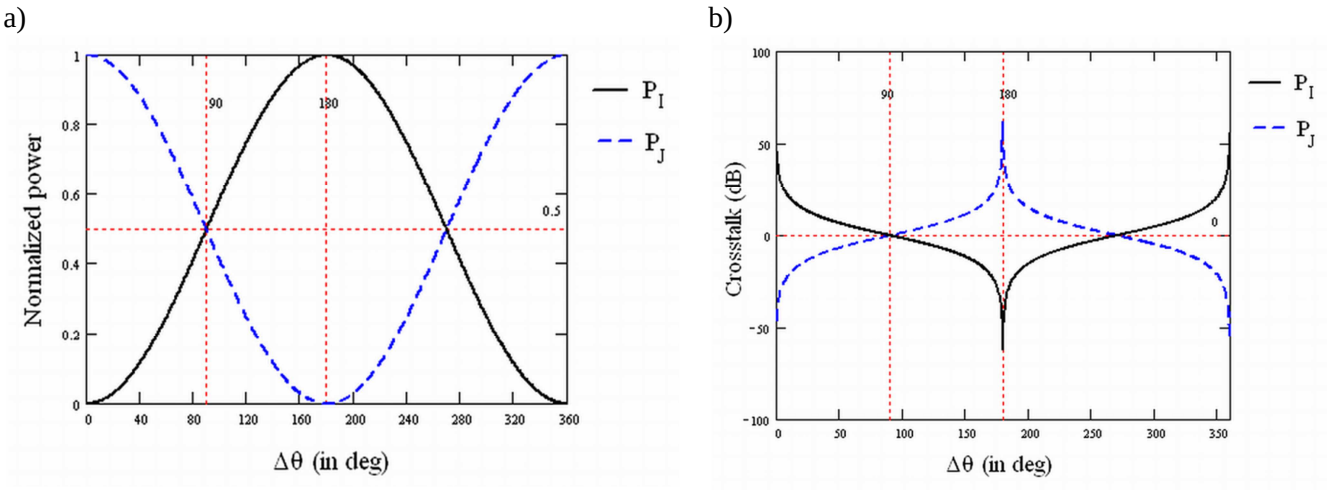


Figure 15 – (a) Variation of normalized output power (a.u.) with Δθ (in degree). (b) Variation of crosstalk (in dB) with Δθ (in degree).

For logical operation, it is not always required that the '0' logic level has a very low (nearly zero) optical power. In fact, we can adjust it by a threshold level, in which above this level we have the logic level '1' and below the logic level '0'. So, we consider a power range between 0.75 - 1 as logic '1' state and 0 - 0.25 as logic '0' state.

The proposed logic circuit, shown Figure 14, uses a very simple concept, and is capable to perform different optical logic gates based on the phase difference between the two arms of a Mach-Zehnder interferometer. The data input signals X and Y will program the phase modulators, in order to control the phase change in the arms of the interferometer.

The operational conditions to implement an AND/NAND optical gate are demonstrated in Table **5**. When X or Y are equal to 1, the phase modulators introduce, respectively, an additional 300º and 60º in upper and down MZI arm; otherwise no additional phase shift is added. The powers at the output ports, P_I and P_J, presented in Table 5, are obtained by solving equation (2.13).

Table 5: Optical AND/NAND logic gate.

X	Y	θ_1	θ_2	$\Delta\theta$	P_I	P_J
0	*0*	*0*	*0*	*0*	*0*	*1*
0	*1*	*0*	*60º*	*-60º*	*0.25*P_A	*0.75*P_A
1	*0*	*300º*	*0*	*300º*	*0.25*P_A	*0.75*P_A
1	*1*	*300º*	*60º*	*240º*	*0.75*P_A	*0.25*P_A

Considering P_A equal to 1 a.u., when (X:Y) are (0:0); (0:1); (1:0) and (1:1), the powers at port #I are, respectively, 0; 0.25 a.u.; 0.25 a.u. and 0.75 a.u., which correspond to the output logic levels 0;0;0;1. Thus, the output port #I only have the logical value '1' when the input signals (X:Y) are simultaneously equal to 1. This correspond to the AND logical operation (XY). Since both output ports are complementary, for the same operational conditions we also obtain, simultaneously, at the output port #J, the NAND logic circuit.

All the possible 16-optical logic gates that can be implemented with the proposed configuration are illustrated in Table 6, and they are performed based on the same operating principle described in AND/NAND optical gate. So, by changing the phase at the two arms of a Mach-Zehnder interferometer (θ_1 and θ_2), it is possible to obtain different logic functions at the MZI output ports, port #I and port #J.

Table 6: 16-Boolean optical gates using a single MZI.

Logic Gate	θ_1	θ_2	Output Port	Output power when input signal X:Y			
				0:0	0:1	1:0	1:1
XY (AND)	300º	60º	Port I	0	0.25	0.25	0.75
$\overline{X}+\overline{Y}$ (NAND)	300º	60º	Port J	1	0.75	0.75	0.25
$X\overline{Y}$	120º	60º	Port I	0	0.25	0.75	0.25
$\overline{X}+Y$	120º	60º	Port J	1	0.75	0.25	0.75
$\overline{X}Y$	60º	120º	Port I	0	0.75	0.25	0.25
$X+\overline{Y}$	60º	120º	Port J	1	0.25	0.75	0.75
$X\oplus Y$ (XOR)	180º	180º	Port I	0	1	1	0
$\overline{X\oplus Y}$ (XNOR)	180º	180º	Port J	1	0	0	1
0 (False)	60º	60º	Port I	0	0.25	0.25	0
1 (True)	60º	60º	Port J	1	0.75	0.75	1
X	240º	60º	Port I	0	0.25	0.75	1
$\overline{X}$	240º	60º	Port J	1	0.75	0.25	0
Y	60º	240º	Port I	0	0.75	0.25	1
$\overline{Y}$	60º	240º	Port J	1	0.25	0.75	0
$X+Y$ (OR)	240º	120º	Port I	0	0.75	0.75	0.75
$\overline{X}\overline{Y}$ (NOR)	240º	120º	Port J	1	0.25	0.25	0.25

2.3.2 Simulation results for each logic gate

In order to analyze the proposed optical logic circuit, presented in Figure 14, under different phase conditions, without changing the setup design, we simulate the system shown in Figure 16, using the Optisystem® 7.0 software. Each optical logic gate is obtained by properly setting the voltage in each phase modulator, in order to get the appropriate phase change that implements the desired logic operation. The input signals X and Y will control the phase modulators, and the data sequences used are X = [0011] and Y = [0101].

At the outputs ports of the MZI, we also introduce two attenuators, adjusted with same attenuation in both arms, in order to set the maximum power at 1mW.

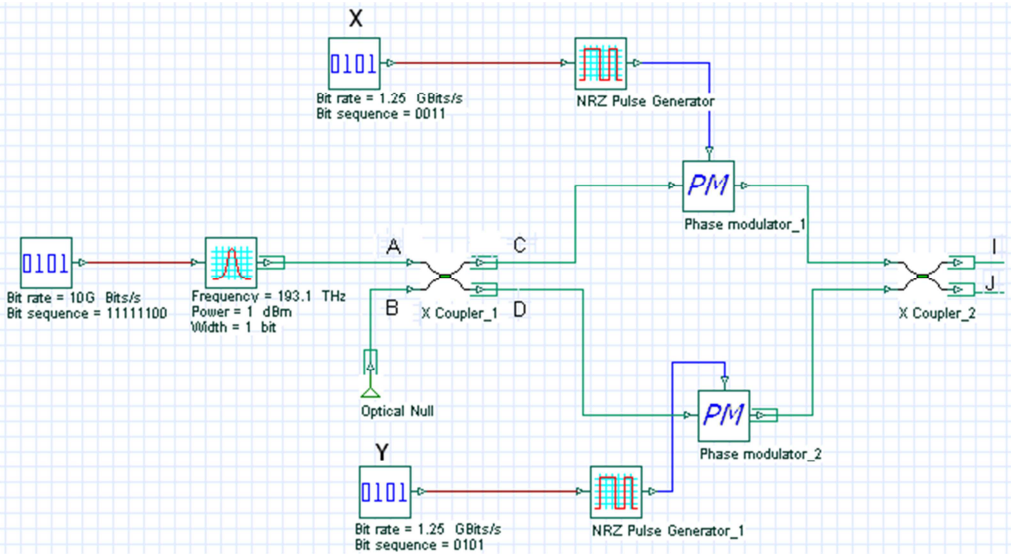


Figure 16 - Proposed configuration of the optical 16-Boolean logic circuit based on a single MZI.

Figure 17 shows the graphs of simulated data measured from output ports #I and #J, for each logic gate. These results demonstrate that the optical pulse, injected into port #A will suffer a constructive or destructive interference, depending of the phase difference between the two MZI arms. The phase change is obtained using phase modulators controlled by the input data signals, X and Y. Therefore, the different logic operations are obtained as a result of a combination of the chosen inputs.

The simulated results presented in Figure 17 also show that the estimated output powers, PI and PJ from Table 6, obtained using the theoretical model (equation 2.13), are in good agreement with the simulated measured curves, which validates our concept.

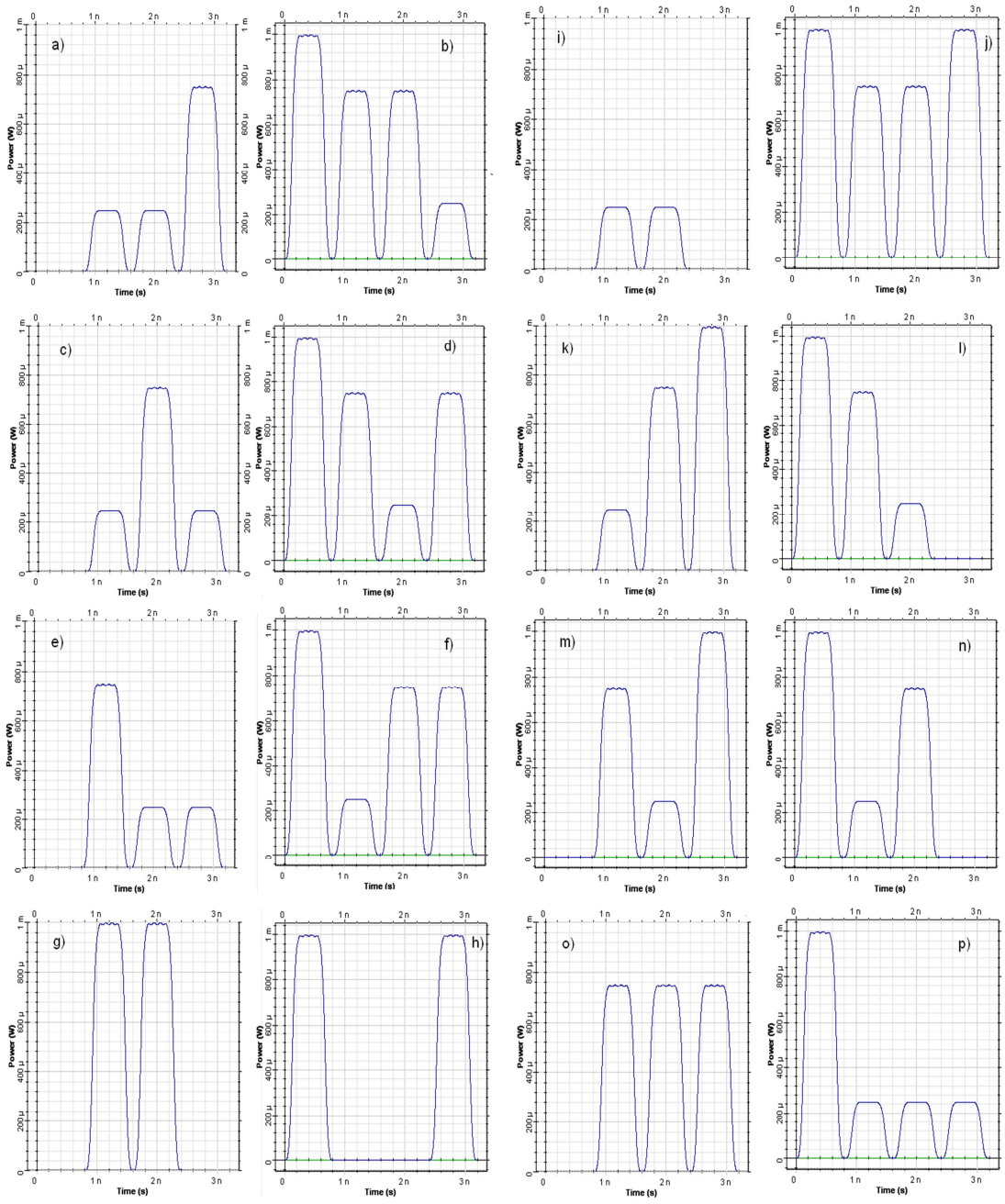


Figure 17 - Simulated curves for each logic gate. a) $XY(AND)$; b) $\overline{X} + \overline{Y}$ ($NAND$); c) $X\overline{Y}$; d) $\overline{X} + Y$; e) $\overline{X}Y$; f) $X + \overline{Y}$; g) $X \oplus Y(XOR)$; h) $\overline{X \oplus Y}$ ($XNOR$); i) $0(False)$; j) $1(True)$; k) X; l) $\overline{X}$; m) Y; n) $\overline{Y}$; o) $X + Y(OR)$; p) $\overline{X}\,\overline{Y}(NOR)$.

We considered values between 0.75 - 1 as the logic 'high' state and values between 0 - 0.25, as the logic 'low' state. However, it is possible to reduce the variation of the 'high' output levels and suppress the 'low' logic levels shown in Figure 17, using optical thresholding schemes. The thresholder function can also improve the extinction ratio values of different logic gates. In this context, an optical thresholder scheme [32] (shown in Figure 18) is connected by an Erbium Doped Fiber Amplifers (EDFA) to each one of the MZI output ports #I and #J of Figure 16, in order to investigate the performance of each logic gate. The gain of both EDFAs is set to 20 dB and the parameters of the two thresholders are the same. Both attenuators have an attenuation of 5 dB in order to guarantee asymmetrical losses. The HNLFs used have low dispersion slope, a fiber length of 0.4km and a nonlinear refractive index of $2.6\times10^{-18}\,\mathrm{m^2/W}$. However, their wavelengths are slightly different: $HNLF_1$ wavelength is 1565nm and $HNLF_2$ wavelength is 1566.6 nm. At both thresholder output ports, an optical band pass filter is placed with a bandwidth of 10 GHz.

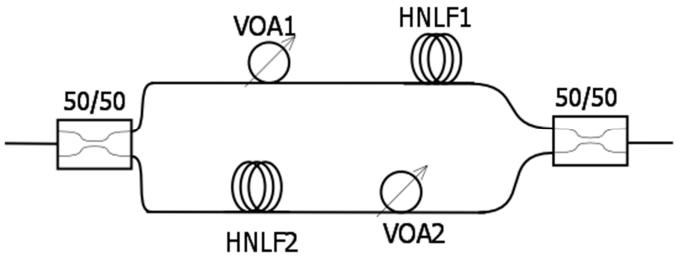


Figure 18 - Schematic diagram of the optical thresholder circuit.

Figure 19 shows the simulation results obtained, for each optical logic gate, after the thresholder function is introduced. It is possible to observe an almost complete suppression of the 0 pulses and, although an undesired peak is presented, the 1 output pulses are almost equalized. Therefore, the two logic levels '0' and '1' are well defined.

The system performance is assessed with the calculation of the extinction ratio (ER) values for each Boolean gate, before and after the thresholder function. In a simple MZI, the ER is given by [33]

$$ER = 10\log\left(\frac{P_{avg}^{1}}{P_{avg}^{0}}\right) \tag{2.14}$$

Where P_{avg}^{1} and P_{avg}^{0} are the average values of the peak power level when the output has the logic value 'HIGH' (1) and 'LOW' (0).

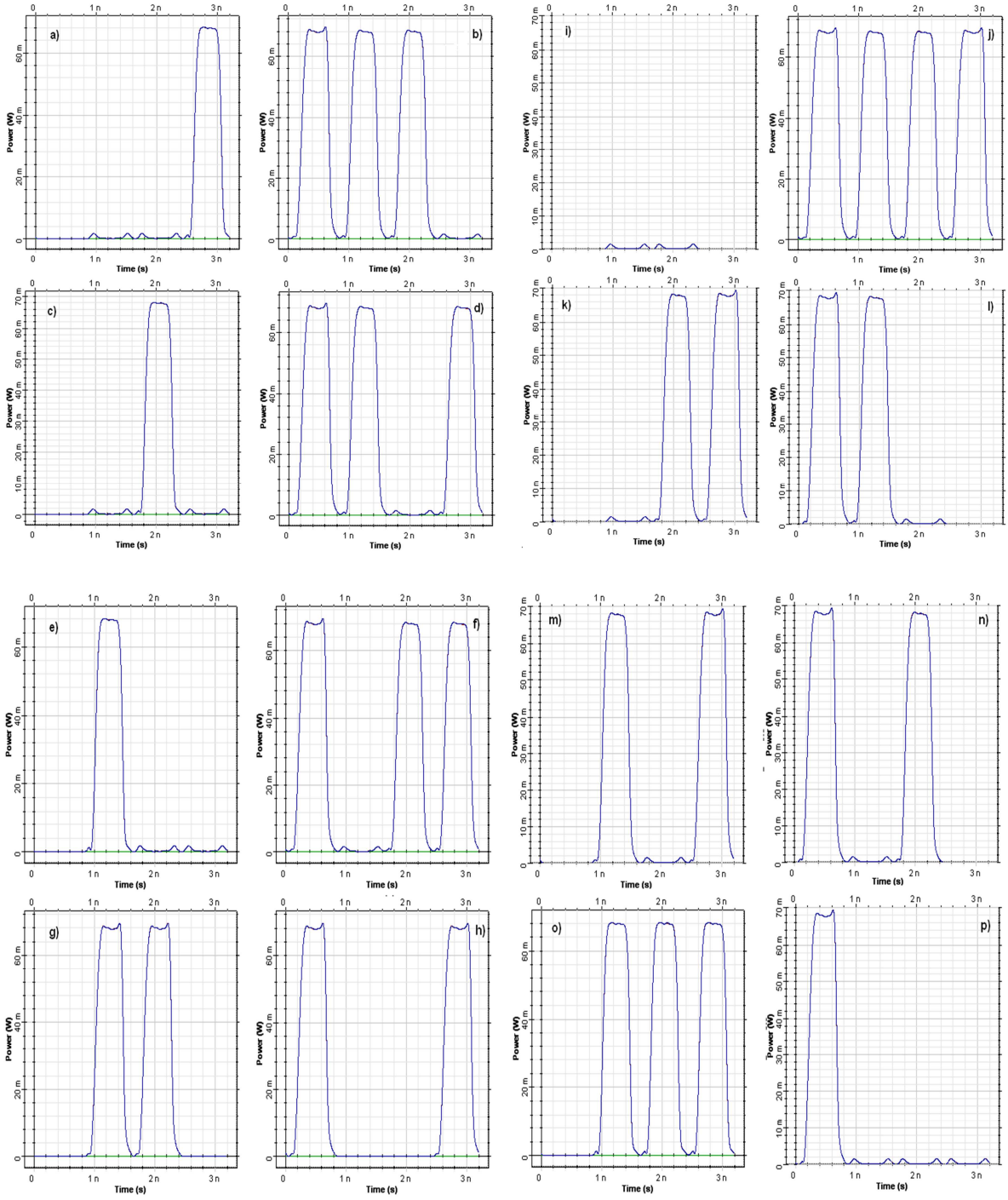


Figure 19 - Simulated curves for each logic gate after thresholder function. a) $XY\,(AND)$; b) $\overline{X}+\overline{Y}\,(NAND)$; c) $X\overline{Y}$; d) $\overline{X}+Y$; e) $\overline{X}Y$; f) $X+\overline{Y}$; g) $X\oplus Y(XOR)$;h) $\overline{X\oplus Y}\,(XNOR)$; i) $0(False)$; j) $1(True)$; k) X ; l) $\overline{X}$; m) Y; n) $\overline{Y}$; o) $X+Y(OR)$; p) $\overline{X}\,\overline{Y}(NOR)$.

In Table 7, is possible to observe that after using a thresholder circuit, the simulated ER increased for almost all the cases. The exception cases are the ones that before the thresholder circuit presented already only two optical powers. Namely, comparing the functions XOR/XNOR in Figure 17 and Figure 19, it can be seen that the simulated curve in Figure 19, has undesired peaks, which degrades slightly the signal and consequently the ER value. However, for these cases, the thresholder function is not needed since the ER achieved is superior to 10 dB. For all the other cases, we observed a significantly improvement in the ER values after introducing the thresholder circuit, since it almost suppresses completely the '0' levels and leads to a stabilization of the '1' logic level. Also from equation (2.14), it can be easily said that ER before using a thresholder should be lower than the values obtained after thresholders. Because before using a thresholder circuit, the 'Logic-1' and 'Logic-0' levels vary from 0.75 to 1 and from 0 to 0.25, respectively. Hence the low difference of $\left|P_{avg}^{1} - P_{avg}^{0}\right|$ results in a smaller ER. After using thresholders, the 'Logic-1' and 'Logic-0' levels have almost the same values, which can be seen in Figure 19. As a result, ER improves.

Table 7: Extinction Ratio before and after the thresholder circuit.

Logic functions (I/J)	Before Thresholder		After Thresholder	
	I	J	I	J
XY (AND) / $\overline{X}+\overline{Y}$ (NAND)	4.23 dB	4.68 dB	15,0 dB	15.3 dB
$X\overline{Y}$ / $\overline{X}+Y$	3.75 dB	4.24 dB	14,0 dB	15.1 dB
$\overline{X}Y$ / $X+\overline{Y}$	4.03 dB	3.98 dB	14.4 dB	14.2 dB
$X \oplus Y$ (XOR) / $\overline{X \oplus Y}$ (XNOR)	16.99 dB	16.99 dB	14.9 dB	14.9 dB
0 (False) / 1 (True)	11.3 dB	13.85 dB	9.7 dB	14.6 dB
X / $\overline{X}$	4.24 dB	4.36 dB	15,0 dB	15,0 dB
Y / $\overline{Y}$	4.29 dB	4.27 dB	15.1 dB	15.1 dB
$\overline{X}\overline{Y}$ (NOR) / $X+Y$ (OR)	13.22 dB	7.12 dB	14.9 dB	14.1 dB

2.3.3 Complex circuit using the MZI based logic unit

The proposed circuit differs from the traditional ones, since we find a logic function ($f(x,y)$) and its inverse simultaneously from a single optical light input. Here, two variables *x* and *y* behave like control signals of the circuit. Hence, any data entered in the circuit will reach any of the output ports. The block diagram of the proposed scheme is shown in Figure 20(a). Using this single unit block, we can design a more complex circuit, as shown in Figure 20(b).

a) b)

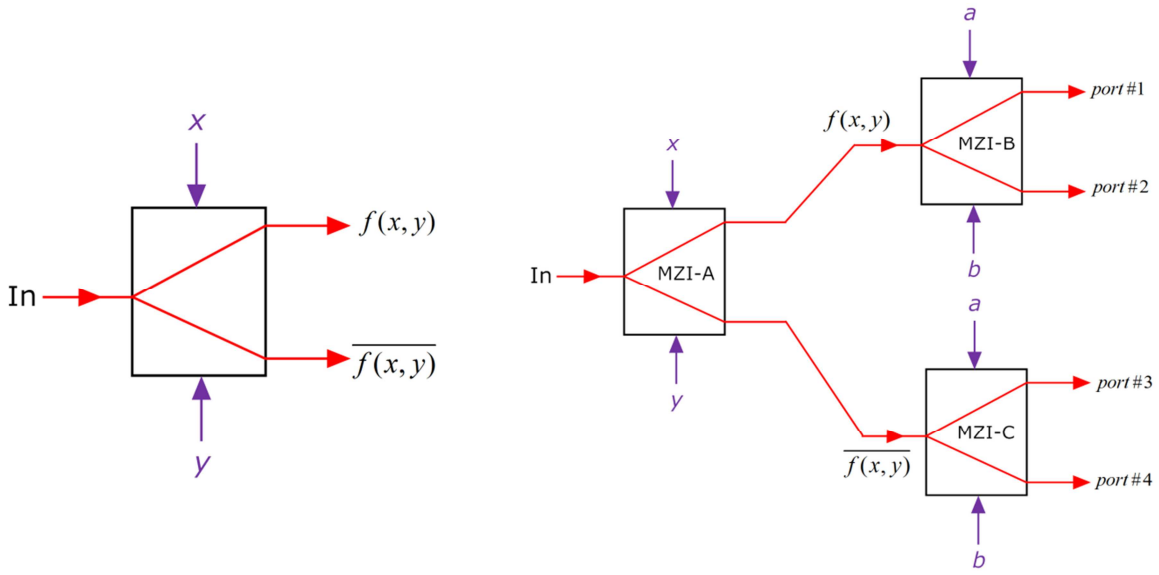


Figure 20 – (a) Block diagram of our proposed MZI based logic unit. (b) Complex logic circuit using three cascaded MZI.

By cascading these blocks, the operation performance will not be affected and no errors will occur at the output. This complex circuit has one optical data input and four optical outputs and it consists of three cascaded MZIs (MZI-A, MZI-B and MZI-C). The logical expressions at the outputs of this complex circuit can be expressed as:

$$LE|_{\#1} = [f(x,y)] \cdot [f(a,b)] \tag{2.15}$$

$$LE|_{\#2} = [f(x,y)] \cdot [\overline{f(a,b)}] \tag{2.16}$$

$$LE|_{\#3} = [\overline{f(x,y)}] \cdot [f(a,b)] \tag{2.17}$$

$$LE|_{\#4} = [\overline{f(x,y)}] \cdot [\overline{f(a,b)}] \tag{2.18}$$

Where $LE_{|\#n}$ indicates the logical expression at output port #n, with n=1,…, 4. The symbols ‘ $\bar{}$ ’ and ‘ · ’ represent binary ‘INVERSE’ and ‘AND’ expressions, respectively.

In this complex logical circuit, optical data and control signal conversion is not permitted i.e. data and control signals are distinguishable. The control signals create a phase difference in the circuit, which allows optical data to be directed to the selective output port.

To explain the operation of the complex circuit, consider firstly that all MZIs are set to θ_1=300º and θ_2=60º. So, if we apply at the control inputs x = [0011], y = [0101], a = [1110] and b = [1000] then, the logical expressions at the outputs ($LE_{|\#n}$) can be obtained by solving equations (2.15) to (2.18). In Table 8 (first row), the theoretical values obtained for the first case are presented.

Table 8: Inputs and outputs for all ports of complex circuit of Figure 20(b).

MZI-A				MZI-B				MZI-C				Port# 1	Port# 2	Port# 3	Port# 4
x	y	θ_1	θ_2	a	b	θ_1	θ_2	a	b	θ_1	θ_2				
(0011)	(0101)	300°	60°	(1110)	(1000)	300°	60°	(1110)	(1000)	300°	60°	(0000)	(0001)	(1000)	(0110)
		300°	60°			120°	60°			120°	60°	(0000)	(0001)	(0110)	(1000)
		120°	60°			180°	180°			180°	180°	(0010)	(0000)	(0100)	(1001)

The simulation results, shown in Figure 21 (case-I) prove that the theoretical results are in good agreement with the simulated measured curves. Other cases are also studied, based on the same operating principle described above, and the results are shown in Table 8 and Figure 21 (case-II and case-III), respectively.

At the outputs ports of the complex circuit, we introduce attenuators, adjusted with same attenuation in all ports, in order to set the maximum power at 1mW.

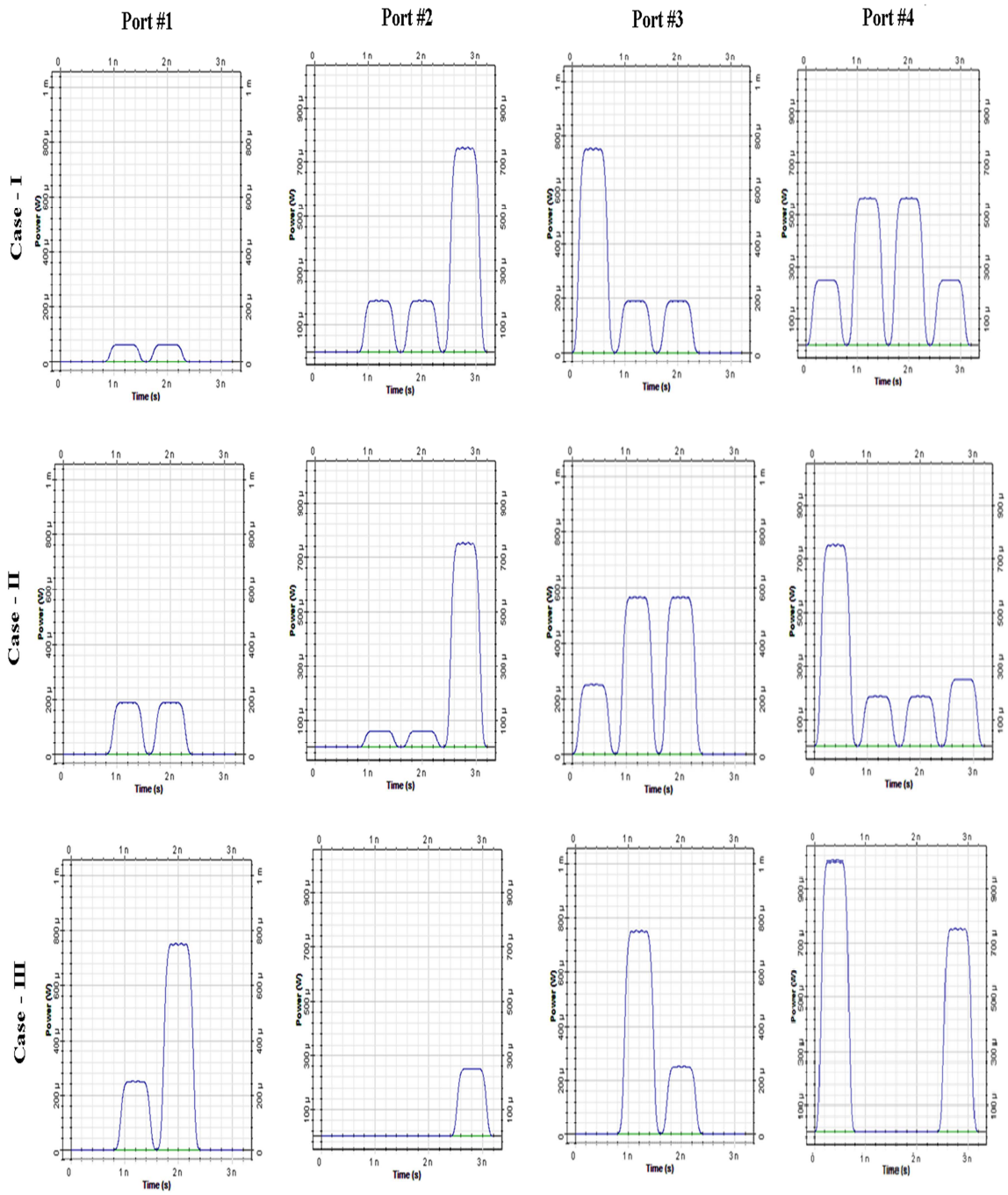


Figure 21 - Simulatated waveform of the proposed complex circuit shown in Figure 8(b).

2.4 Conclusions

In the last few years, the exponential growth of network traffic motivated the development of ultrafast signal processing in the optical domain. In this context, all-optical logic gates are essential

devices since they can execute complex optical processing functions, from binary address and header recognition to optical time division demultiplexing, which demonstrates their importance in a wide range of applicability.

In this chapter, the non-linear behavior of the SOA-MZI device has been studied and characterized since it is the foundation of most of the all-optical applications proposed and studied throughout this PhD work.

In this chapter we also proposed and demonstrated two novel methods to obtain all-optical logic gates.

The first method demonstrates four all-optical logic operations, using simultaneously both output ports of a SOA-MZI. The four logical functions are AND / transposed INHIBITION and EQUIVALENCE / INVERTER. The experimental and simulation results confirmed that the proposed configuration switch operates according to its truth table. The extinction ratio measurements also demonstrated the suitability of the proposed circuit for all-optical logic gates implementation. The potential of integration makes the proposed scheme attractive to perform optical signal processing operations in next generation photonic transmission systems.

The second proposed scheme performs 16-Boolean logic operations based on a single Mach-Zehnder interferometer, using the same design. We showed that through optical phase changes in MZI branches, using controlled phase modulators, is possible to successfully demonstrate different logic operations. Also we showed that the proposed scheme can be used to build successfully a complex logic circuit. We have explained the operation principle of our concept and assessed its performance against several operational criteria, through numerical simulation, which allowed to theoretically confirm our model.

We also assessed the behavior of an all-optical logic XOR gate based on a SOA-MZI in terms of the way the incoming signal is injected (co or counter propagation). We conclude that for both co- and counter-propagation schemes, the performance of the XOR gate is almost independent of the input power, since the power variation of the two data signals involved in the comparison is the same. However, the counter-propagation scheme showed a better performance, with a slightly improvement on the extinction ratio.

Chapter 3

All-optical flip-flops

An optical flip-flop (AOFF) is a one-bit memory and is a key building block in next generation photonic transmission systems since it can fulfill many optical signal processing functions. Examples of such functions are: as storage of the header information of a packet, while the payload of the packet is routed to the output port [34], as basic building blocks of optical shift registers [35] and optical counters [36], in threshold functions and self-routing [37], in optical contention resolution schemes, as regenerative memory elements [38], among others.

In the last few years, there has been an intensive research on optical flip-flops as it is demonstrated in Figure 22, which displays the annual citations on the IEEE Xplore for papers with index terms referring optical flip-flops. This research interest can be explained mainly due to technology advances in monolithic and hybrid integration, and the need for a high-speed and low-power memory.

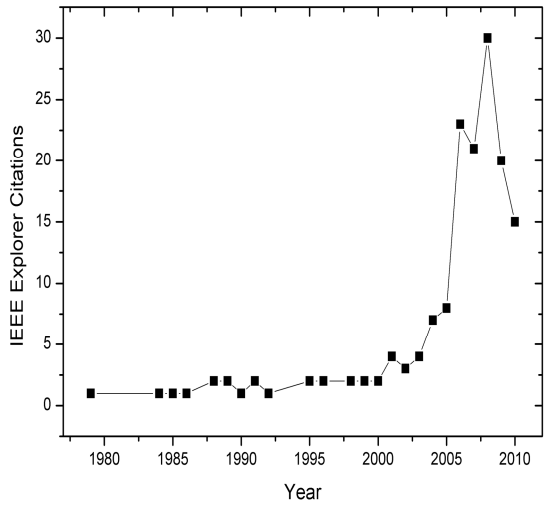


Figure 22- IEEE Xplore annual citations with index terms referring to optical flip-flops. The lines are visual guides.

To implement an AOFF is necessary to use an element that presents a bistable behavior. In this kind of elements, hysteresis phenomena occur. Hysteresis is the tendency of a material or system to maintain its properties in the absence of a stimulus that generated them. In a hysteretic

cycle, the output level depends on the previous state of the device which results in a curve with the form of a loop. Depending of its previous state and for the same input value, the output of the device presents two possible states of operation. Therefore, the outputs of an AOFF not only depend of the input values in a considered instant, but also depend of the information from the previous states.

Two conditions are required to implement an optical bistable device:

- nonlinearity (two types of nonlinear optical elements can be used: dispersive nonlinear elements, for which the refractive index is a function of the optical intensity. Elements based on the Kerr effect such Mach- Zehnder interferometers are examples of dispersive elements; or dissipative nonlinear elements, for which the absorption coefficient depends of the optical intensity. In an absorptive element, a saturable absorber has an absorption coefficient which is a non-linear function of density of photons. The cavity is setup for resonance: at small intensities, the absorption due to the element is high and the output is low and as the intensity is increase beyond intensity of threshold, the absorption rapidly decreases and the output goes high;
- feedback (by using fiber Bragg gratings, mirrors or feedback loops, for example).

In a conventional flip-flop, the bistability operation is performed in the `S-shaped' hysteretic region and the output state is distinguished by the different output power. In an optical memory, the state can be distinguished by different output wavelengths [15]. This fact led to an increase research study on all-optical flip-flops.

This chapter, based on the publications [J3], [J4], [J5], [J7], [J8] and conferences [C5], [C6], [C7], presents an overview of the state of the art of all-optical flip-flops technologies, and their possible experimental implementation solutions, for a variety of applications in optical signal processing. A performance comparison of the up-to-date all-optical flip-flops design schemes is then evaluated based on experimental results. The experimental and theoretical implementations of the all-optical flip-flops developed in this thesis are described in section 3.2. The experimental work of all-optical clocked flip-flops presented in the latter section were performed under the EU NoE EURO-FOS project consortium and carried out in the optical communications laboratory of the National Technical University of Athens – School of Electrical and Computer Engineering, Greece.

Finally, in section 3.3, the topics discussed in this chapter are concluded.

3.1 State-of-Art of All-Optical Flip-Flops

In the last few years, several approaches to implement all-optical flip-flops have been proposed and studied [39]. These different technologies are discussed, in more detail, below.

3.1.1 Asynchronous AOFF schemes

In [40] and [41], a Set-Reset (S-R) AOFF is implemented based on a single SOA-MZI, with an external feedback loop. The flip-flop state is determined as a function of the phase shift between the two arms of the interferometer. So, when a reset signal is injected, the SOA-MZI is unbalanced and the AOFF output is at a low logical level; on the other hand, when the SOA-MZI is balanced, the AOFF output is in the high logical level. In Figure 23, the AOFF circuit block diagram is depicted. The output power of this flip-flop can be adjusted by modifying the feedback loop coupling factor (r) and, by increasing the energy of set/reset pulses, the flip-flop response delay can be reduced. Switching times in order of ns were achieved**.**

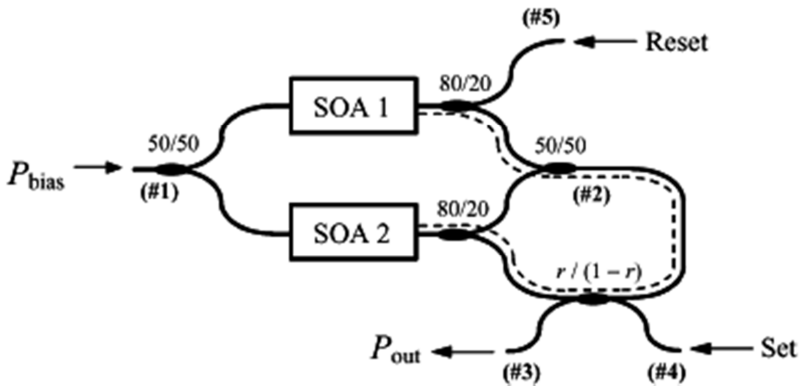


Figure 23 - All-optical S-R flip-flop based on a single SOA-MZI [41].

In [42], a slightly different S-R AOFF architecture, using a single SOA-MZI, is experimentally assessed and it is based on the theoretical analysis demonstrated in [41]. The operation principle of this scheme relies on adding a feedback loop to an optical exclusive-OR gate, in order to maintain bistability. Initially, with no input pulse, the device delivers no signal. When a pulse is launch into the set input, the output switches from the OFF to the ON state (Set (1) XOR Reset (0) = 1). A reset pulse allows to go back to the OFF state since the result of Set (1) XOR Reset (1) = 0. This configuration is wavelength independent but power sensitive. The required width of set and reset

pulses to switch between states depends on the length of the loop, therefore as the feedback loop increases, a higher energy of set and reset is needed.

To overcome the limitations of the scheme proposed in [40], a multiple forward-control S-R AOFF configuration is presented in [43]. This all-optical flip-flop, shown in Figure 24, is also based on a symmetric SOA-MZI with a feedback loop but uses multiple forward set/reset signals. As a result, this AOFF overcomes the feedback-loop delay, making it appropriate for high-speed applications.

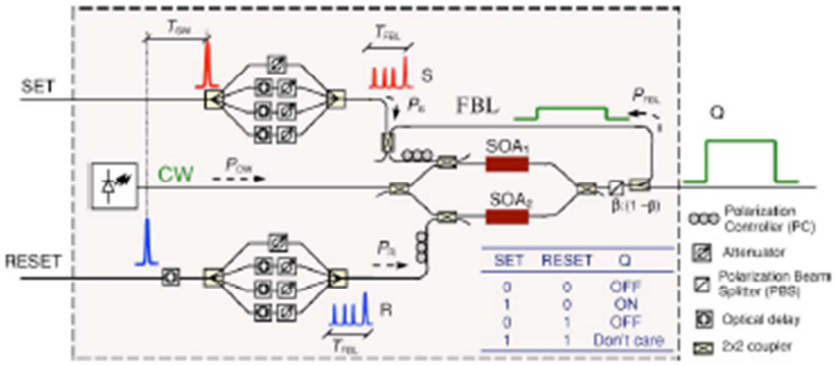


Figure 24 - Architecture for the S-R optical flip-flop using a single SOA-MZI and multiple forward signals [43].

In [18], an S-R all-optical flip-flop is demonstrated using two coupled SOA-MZI and its operation principle is based on the gain quenching effect, in which the signal output from the dominant laser (master) suppresses the other laser (slave), through gain saturation of the SOA. Figure 25 illustrates this optical flip-flop architecture. In state 1, the SOA-MZI 1 is the master and suppresses the output from SOA-MZI 2 (slave). In this case, the output of the flip-flop is a continuous wave operating at λ1. In the same way, in state 2 the SOA-MZI 2 output suppresses the output from SOA-MZI 1 and now λ2 is dominant. So, controlling the level of the output signal in one of the SOA-MZIs, it is possible to suppress the other one. The two possible operation states can be switched by injecting set/reset pulses into the SOA-MZI that is currently dominant.

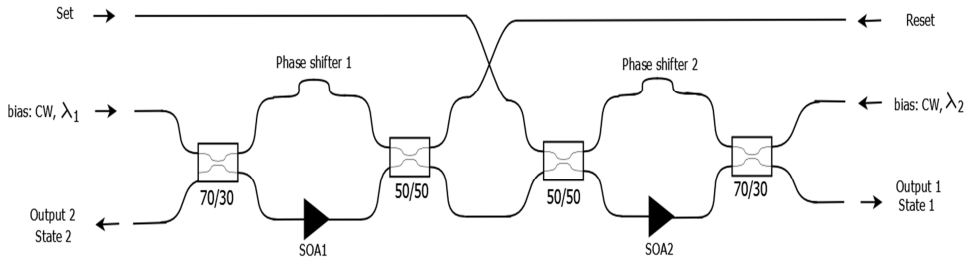


Figure 25 - All-optical S-R flip-flop based on two coupled SOA-MZI.

In [44] and [17], two all-optical S-R flip-flops are proposed based also on the gain quenching concept. In [44], the AOFF is implemented using two coupled ring lasers and an arrayed waveguide grating (AWG), acting as the frequency selective element of each cavity. Each ring laser has its own gain element (SOA) and the light propagates bidirectionally in the ring. Its operation principle is shown in Figure 26. In state 1, light from a laser A flows in counterclockwise direction and saturates the gain element of a laser B, suppressing laser B from lasing. In this situation, the light from the dominant laser (laser A) is sent to an output by the AWG. Thus, the AWG ensure isolation between the device input and output. In the same way, in state 2, only laser B is lasing, suppressing laser A from lasing. Thus, only one of the lasers can be lasing at a time, due of the fact that the dominant laser suppresses the other laser through gain saturation. Lasing in the master can be turned off by injecting external optical pulses, changing in this way the state of the system. The cavity length of this AOFF scheme is about 4.5 mm, which cause speed limitation.

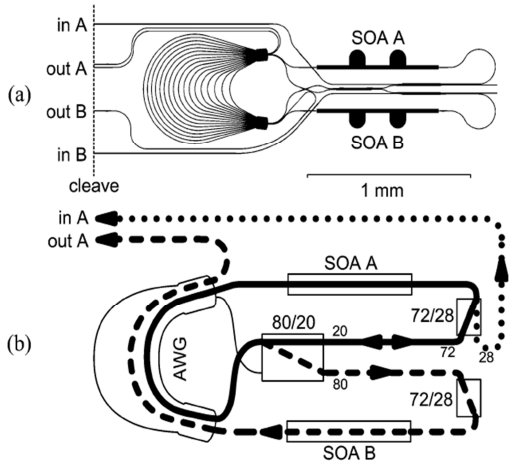


Figure 26 - a) Mask layout for two-state multiwavelength laser. b) Operation of device showing laser A suppressing lasing in laser B. SOA: semiconductor optical amplifier; AWG: arrayed waveguide grating [44].

In Figure 27, is presented the AOFF proposed by [17], which consists of two coupled SOA fiber ring laser, operating at λ_1 and λ_2. Each ring laser is composed of a SOA, which acts as a gain element, an isolator to ensure a unidirectional propagation of the light in the ring and a band pass filter (BPF) as the wavelength selective element. The operation principle can be explained as follows: when the set signal is injected, it will pass through couplers E, B and D, respectively, which suppresses ring 2 due of SOA2 saturation, setting the flip-flop to state 1. On the other hand, injecting optical pulses in the Reset port, the output light of ring 2 suppresses the emission of ring 1. In this case, the flip-flop output is a continuous wave operating at λ_2 and presenting the logic

level “0”. The switching between states can be realized by the injection of an external light at the wavelength of the cavity that is not lasing.

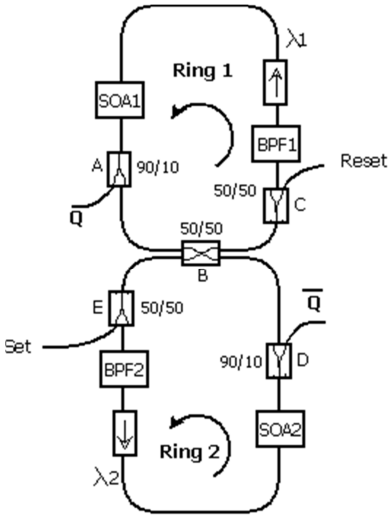


Figure 27 - All-optical S-R flip-flop based on SOA fiber ring lasers.

The flip-flop configuration proposed in [45] is very similar to the flip-flop scheme presented in [17]. The main difference is that in [17] each ring laser has its own SOA and a coupler is used to couple the two ring lasers whereas in [45] the AOFF consists of two ring lasers with a feedback loop, operating at different wavelengths, and sharing the same active element, as shown in Figure 28. The bistability of this configuration is caused by the feedback of a fraction of the lasing light into the laser, through an optical loop mirror implemented by a 3 dB coupler.

In [46], an AOFF is proposed based on a Mach-Zehnder interferometer bistable laser diode (MZI-BLD), with distributed Bragg reflectors (DBRs) at two interferometric ports, to obtain single-mode laser operation. Its operation principle is based on XGM and saturable absorption parts. The latter flip-flop configuration overcomes the issues of multimode interference BLD (MMI-BLD) flip-flop scheme proposed in [47], since the two cross-coupled lasing modes have, theoretically, 100% spatial overlap, which allows a strong interaction between the two modes and the optical input signals.

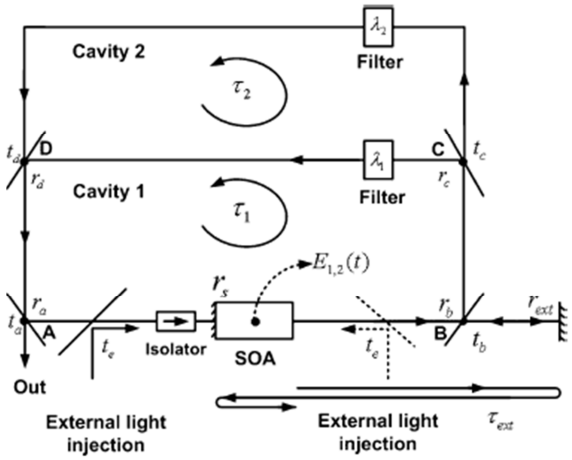


Figure 28 - All-optical S-R flip-flop based on SOA fiber ring lasers sharing a SOA [45].

The AOFF proposed in [48] and depicted in Figure 29 consists of two coupled injection locked single-mode Fabry-Perot laser diode (FP-LD). The slave FP-LD is a commercially available laser and the master FP-LD is designed with a built-in external cavity, operating in single longitudinal mode, with a high side mode suppression ratio. When a control light has a power higher than the locking threshold, the slave FP-LD is injection locked and holds its state even if the input power decrease to a value lowered than the initial threshold.

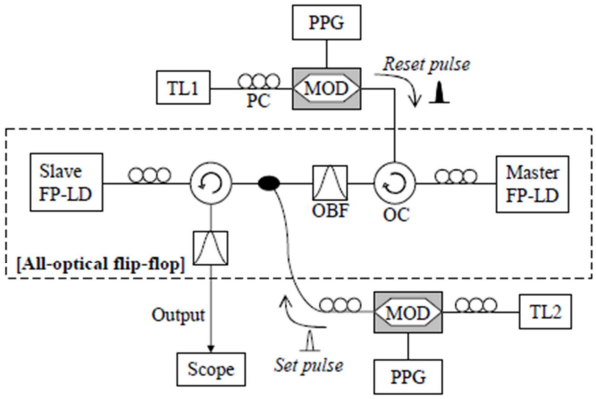


Figure 29 - All-optical S-R flip-flop based on the bistability of injection locked Fabry-Perot laser diode [48].

In [49], an AOFF is demonstrated using a single distributed feedback (DFB) laser diode, operating with a CW signal to obtain optical bistability (Figure 30). If the CW signal is injected in the laser diode, it is possible to observe two states, for the same power, due to the spatial hole

burning effect. In one of the states, when the laser is lasing, an external light will suffer a small amplification, due to the gain clamping, and its influence will be almost negligible on the laser light. In the other state, when the DFB laser is turn off, the external signal will experience a high amplification, which results in a strong non-uniform distribution of the carriers. Thus, if a reset signal is injected into the DFB laser, at the same side of the CW signal, it will turn off the laser, causing a non-uniform carrier distribution. By injecting a set pulse in the other side of the DFB laser, the uniformity of the carrier distribution is restored, and the laser starts lasing. To prevent interaction with the DFB grating, the wavelength of the external set/reset pulses should not be close to the lasing wavelength.

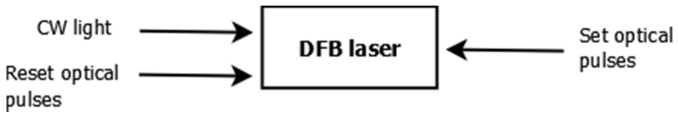


Figure 30 - Schematic diagram of an optical flip-flop based a DFB laser [49].

In [50] and [51], AOFFs are demonstrated based on single and coupled micro-ring lasers, respectively. In a micro-ring laser typically exists two lasing modes, based on the direction that laser light propagates - clockwise (CLKW) or counterclockwise (CCLKW) and depending on the bias current, different operating regimes can occur. Also, ideally, the CLKW mode is not coupled to the CCLKW mode and vice-versa. The AOFF configuration proposed in [50] is depicted in Figure 31. It has racetrack cavity geometry and it is produced in a InGaAs/InGaA1As/InP MQW material. The AOFF exhibits bistability between the counter-propagation cavity modes that can be switched by external optical pulses. It has four inputs/outputs ports that are all-active, and can be use to inject or extract optical signals.

In [51], two micro-ring lasers coupled by a waveguide are presented and this AOFF configuration has two stable states. In state 1, CLKW light from a ring laser 1 is injected into a ring laser 2 and will suffer a significant amplification if the resonant frequencies of both lasers are close. If sufficient light is injected into laser 2, its gain will decrease below threshold, which suppresses its oscillations, forcing the light to propagate only in the CLKW direction. Injecting an optical pulse, close to the lasing wavelength, in the waveguide that connects the ring-lasers, set both lasers in the CLKW or CCLKW direction.

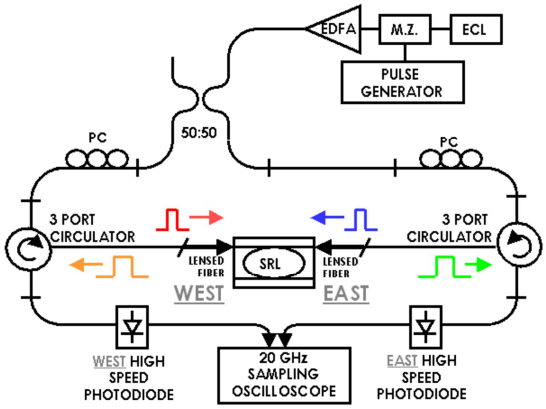


Figure 31 - Scheme of an optical S-Rflip-flop based on single micro-ring laser [50].

In [52], an electrically pumped AOFF based on a single microdisk laser is demonstrated and its schematic diagram is shown in Figure 32. The production of bistable AOFF is based on a heterogeneous integration of InP-based devices onto a silicon-on-insulator, and the high refractive index contrast in the InP membranes allows to reduce the device size. The bistability of this configuration is caused by a weak coupling between the CLKW and CCLKW whispering gallery modes (WGMs) and by the presence of a high non-linear gain. Switching occurs between predominant clockwise and counter clockwise lasers modes, through injection of short optical pulses.

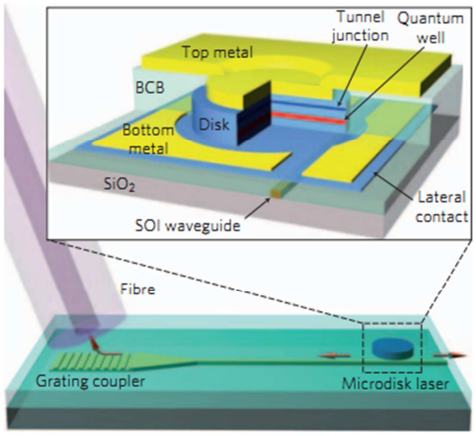


Figure 32 - Schematic diagram of optical flip-flop memory on a silicon chip [52].

An AOFF is proposed in [53], exploiting the polarization bistability in a 1.55 µm vertical-cavity surface-emitting laser (VCSEL). A VCSEL has a square mesa structure, with circular transverse geometry and presents bistable polarization switching between 0° and 90° linear polarization. If a Set pulse of 0° polarization is injected into the polarization bistable VCSEL and exceeds the polarization-switching threshold, the lasing polarization state of VCSEL is switched from 90° to 0°,

and maintains this state until a Reset pulse of 90° polarization occurs. In this case, the polarization state of the VCSEL switches from 0° to 90°. An AOFF operating at 0.98 µm, also based on VCSEL, is demonstrated in [54], and compared with the latter AOFF, it needs lower energies to switch between the two states and allow faster switching times.

3.1.2 Synchronous AOFF schemes

The dynamic operation of an asynchronous bistable device can be changed by providing an additional input (CLK), in order to ensure that only when clock signal is enable (CLK=1), the information at the inputs is transferred to the output of the flip-flop. Otherwise, the information presents at the inputs do not produces effects on the output. Therefore, the clock signal acts as a control input for the latching switch.

Some of the research results shown in this subsection were performed under the EU NoE EURO-FOS project consortium, in which we also collaborated and gave origin to our experimental work of all-optical clocked flip-flops, presented in section 3.2.

In [55], clocked all-optical S-R, D and T flip-flops, whose state switching is triggered by a pulsed clock, are demonstrated. The core components of all the clocked flip-flops, proposed in [55], are the optical S-R bistable based on coupled SOA fibre ring lasers [17] and all-optical logic gates [56]. The Boolean functions, between the input pulsed clock and control signals, are carried out by exploiting four wave mixing (FWM) and cross gain modulation (XGM) nonlinear effects in SOA. The clocked S-R flip-flop setup is shown in Figure 33. It consists of two AND gates and the coupled SOA fibre ring laser flip-flop [17]. The “AND 1” and “AND 2” outputs are connected to the “Set” and “Reset” ports, respectively, in order to achieve clocked functionality. If the clock signal and the set/reset optical signals are simultaneously ‘1’, the FWM phenomenon occurs. However, if the set/reset signals are equal to ‘0’, the FWM effect is not generated and no light flows out from the AND gates.

The setup of the clocked D flip-flop is reported in Figure 34. The “AND 1” gate performs the AND function between the clock and the input signal D. The other gate, “AND 2”, carries out the AND function between the clock and inverted D ($\overline{D}$).

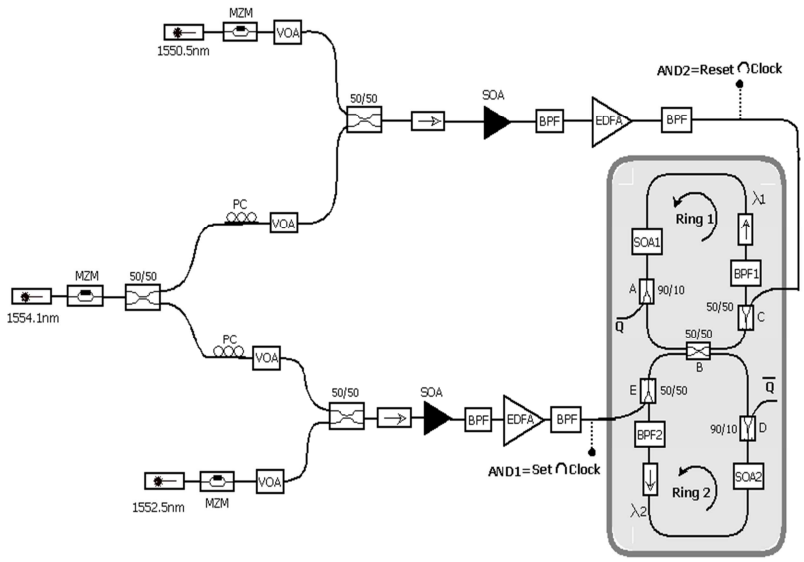


Figure 33 - Scheme of the optical clocked S-R flip-flop based on two coupled SOA ring lasers.

Since the clock signal is amplified when the input signal is at the low level, a light comes out from the AND between the clock signal and $\overline{D}$; otherwise the carriers density of the SOA will be depleted and the clock input signal will be not amplified, due of XGM effect. When the clock signal and the data input signal (D) are simultaneously '1', the FWM phenomenon occurs.

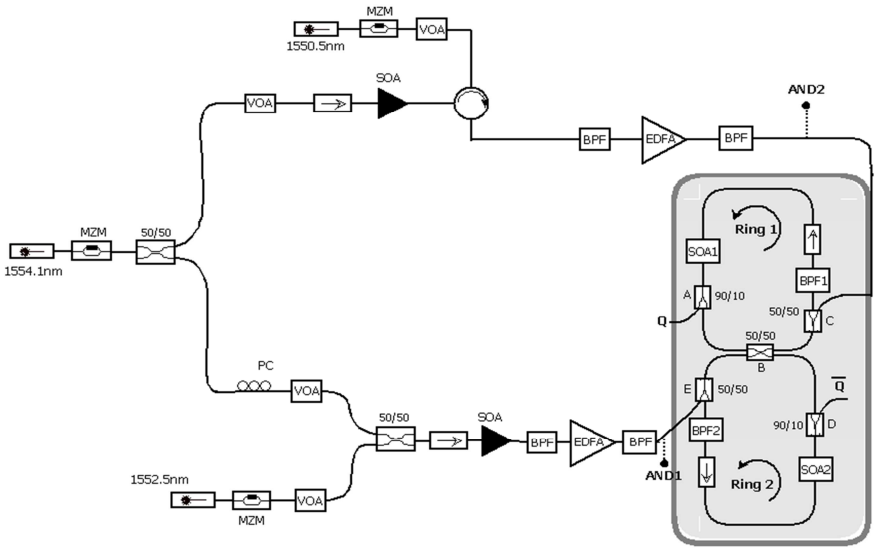


Figure 34 - Scheme of the optical clocked D flip-flop based on two coupled SOA ring lasers.

The logic circuit for the all-optical clocked T flip-flop, proposed by [55], is shown in Figure 35

and consists of three logic gates and one S-R latch, based on two fibre ring lasers. Unlike the previously described S-R and D flip-flops, in the T flip-flop a feedback of the output Q is launched into its inputs. The "AND 1" logic gate carried out the AND function between the clock and T signal, whereas "AND 2" performs AND function between the "AND 1" output ($CLK \bigcap T$) and the feedback Q. The other logic gate, "AND 3", performs the AND function between $CLK \bigcap T$ and inverted Q.

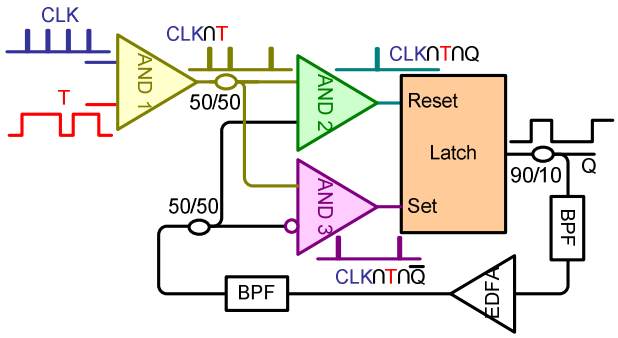


Figure 35 - Logic circuits for all-optical clocked T flip-flop [55].

In [57], an all-optical clocked delay flip-flop is proposed, using a single terahertz asymmetric demultiplexer (TOAD) based switch, and its schematic diagram is shown in Figure 36. The clock (CLK) and input D signals are selected as two orthogonally polarized lights. CLK is introduced to the TOAD loop with a polarizing beam splitter (PBS) and it is rejected by another PBS such that no unwanted data can pass to the output. When D = 1, the light enters into the TOAD loop through the 50:50 coupler (from port P1) and split into two equal parts (CW and CCW). In that situation, when CLK is ON, the SOA changes its index of refraction. As a result, two counter propagating data signals will experience different gain saturation profiles. Therefore, cross phase modulation takes places when they recombine at the 50:50 coupler, and a $-\pi$ phase change is introduce between them and data is transmitted to the output Q. This condition is called 'SET'. Partially silvered mirror (PSM, placed between the path P2 and the output) reflects some portion (nearly the same power of input D) of the output data into the loop. In the meantime, the gain of SOA tries to recover. When CLK is OFF, then the reflected data enters to the TOAD loop through port P2. This is treated as incoming data. As clock is absent, CW and CCW pulses pass through the SOA at different time, but with almost the same gain. Hence, the phase difference between them becomes almost equal to zero and data is reflected towards the source i.e. to P2 port. In that case, the data is locked. This cannot be changed, regardless the information at the D input. After one CLK pulse, clock becomes 'zero' and the TOAD itself behaves like a loop mirror i.e. data will come to the

reflected port. Only they are amplified by the SOA. Thus, output pulse power is higher than input D. When CLK is ON and D =0, the data is reflected toward the transmitted port (P1). So, no data is found at output *Q*. This condition is called 'RESET', and no light can be reflected by PSM. This condition maintains the same, even if D = 1 (then, light enters into the TOAD through P1 port and comes again to the incoming port P1, as no clock is present at that time).

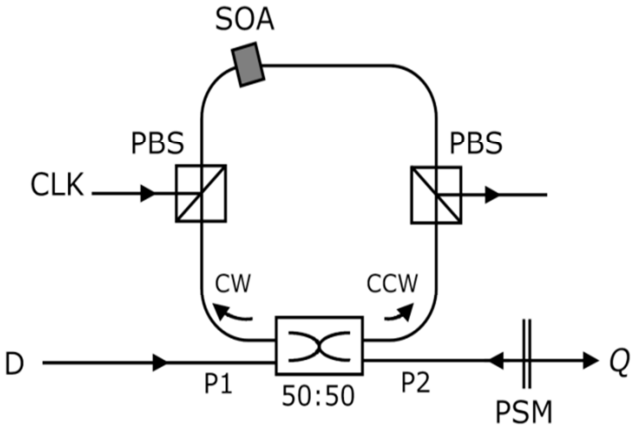


Figure 36 - Physical model of the all-optical clocked D flip-flop using a single TOAD.

The optical clocked S-R flip-flop configuration, proposed in [58], is based on a SOA-MZI, with distributed Bragg reflectors (DBRs) at two interferometric ports, to obtain single-mode laser operation. Figure 37 depicts the Mach-Zehnder interferometer bistable laser diode (MZI-BLD), working with an external synchronization signal Its operation principle is based on cross gain modulation (XGM) and saturable absorption parts. Like the flip-flop implementation proposed in [46], the MZI-BLD-based clocked flip-flop is composed by two cross-coupled modes, with a perfect spatial overlap. Mode 1 occurs in the right upper port and the left lower port of the active interferometer. On the other hand, mode 2 is between the left upper port and the right lower port. The left output is switched ON with the set optical pulses, throughout all the clock pulse period, and maintain its high state until a reset optical pulse occurs. In that situation, when mode 2 starts lasing, it obtains optical gain at SOAs section, in both MZI arms, which suppresses mode 1 from lasing. Switching from mode 2 to mode 1 occurs when a set pulse is injected at the left lower interferometer port, on the high logical level of the clock signal. Therefore, switching occurs only when a clock pulse arrives, according to the set and reset information at that time.

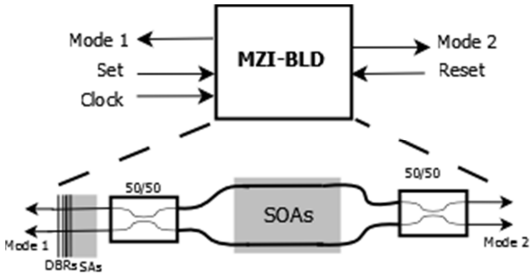


Figure 37 - Logic circuit for the all-optical clocked S-R flip-flop based on MZI-BLD.

3.1.3 Applications of AOFF in all-optical signal processing

All-optical signal processing is expected to overcome the limitations of electrical signal processing and to lead optical communications to the next level. Therefore, it is essential to develop all-optical sequential devices which allow an effective improvement of the all-optical processing capabilities of future networks.

In the last few years, considerable research has been done using AOFFs as basic building blocks of several photonic schemes to perform a variety of optical signal processing functions that requires memory. This subsection will provide an overview of some of the most important all-optical flip-flop applications performed, experimentally, in all-optical signal processing systems.

3.1.3.1 All-optical binary counter

An all-optical binary counter can be used for header recognizing and payload processing in optical packet-switching networks, besides working as a finite-state machine in optical computing. In [59], a two-bit all-optical counter is proposed, presenting parallel output. The experimental setup is shown in Figure 38. The scheme is composed by two identical stages realized each one by an optical S-R flip-flop [17] and an optical AND logic gate based on FWM in SOA. Each stage has 3 ports: the input clock, the output (Qi) and the carry signal. The latches output Q_1 and Q_2, represent, respectively, the less significant bit (LSB) and most significant bit (MSB) of the counter output. In order to carry out two-bit counting operations, the two stages are cascaded by using the "Carry 1" signal coming from stage 1, as input for the second stage. Extension to N-bit counting can be performed by cascading N stages.

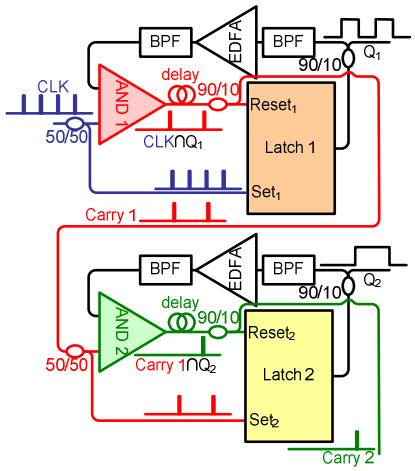


Figure 38 - Logic circuits for all-optical binary counter [59].

In Figure 39, an all-optical two-bit counting is demonstrated, at speeds of 120 kHz. By analysing Figure 39, it is possible to observe that each time a clock pulse comes in, Q2Q1 is incremented by 1, from 00 to 01, 10, and 11, finally returning to 00. Performance evaluation in terms of Q factor confirms the effectiveness of the proposed scheme in cascaded configurations.

Besides counting two-bit sequences, the proposed scheme can also be used as a ½ optical frequency divider (obtained using only one flip-flop) or ¼ optical frequency divider (using both cascaded flip-flops).

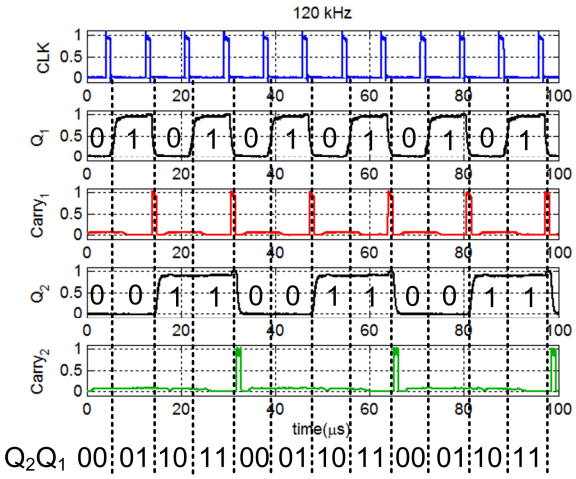


Figure 39 - All-optical two-bit binary counting at 120 kHz.

3.1.3.2 All-optical shift register

A shift register is a device capable of retaining information in the form of a binary number, i.e., the register can store a binary word. In addition of being used as temporary memory, an optical shift register also have the ability to make successive shifts to the left or to the right. An optical shift register scheme is demonstrated in [35], which consists of an optical converter in combination with two cascaded AOFFs. The principle of operation of the proposed optical shift register is shown in Figure 40. The intensity modulated input data is transformed by the optical converter into wavelength encoded data and, subsequently, injected into the port 'In_1' of $AOFF_1$, which is cascaded with $AOFF_2$. Each AOFF is based on two ring lasers, with a single active element and a feedback arm [45]. The two cascaded AOFFs are controlled by optical clock pulses that are required to clear the states of the optical flip-flops. The output from $AOFF_1$ then sets the new state of $AOFF_2$. After this operation, the delayed clock pulse is injected into the port 'In_2' of $AOFF_1$ and subsequently clears its state. The signal encoded in wavelength that outputs from the optical converter then sets the new state of $AOFF_1$. Thus a compete 'shift' function has been realized.

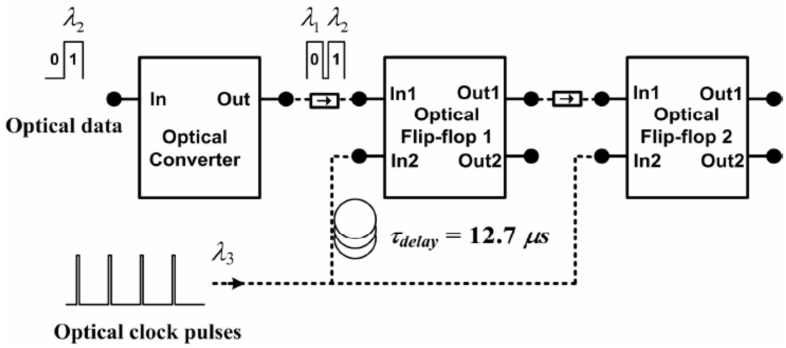


Figure 40 - Optical shift register scheme [35].

Figure 41 shows the binary 01010011 signal being shifted along the circuit. The three outputs are filtered using an optical filter with a central wavelength of λ_2, and it is shown in

Figure 41 that both optical flip-flops keep their initial states until they are cleared by the strong clock pulses. This is because the optical power injected into each optical flip-flop via the port 'In_1' is below the threshold power and the optical flip-flops can only be cleared by a well-timed clock pulse injected via the port 'In_2'. The optical power of the clock signal is split into two parts and 50% of the power is directly injected into the port 'In_2' of $AOFF_2$ to clear this memory. After 4 μs (the duration of the clock pulse), the output of $AOFF_1$ sets the new state of the $AOFF_2$. This procedure is repeated for $AOFF_1$ using the other 50% of the power of the clock pulse, delayed by

12.7 μs. The new state of $AOFF_1$ is then set by the output of the optical converter, which leads to the completion of the 'shift' function.

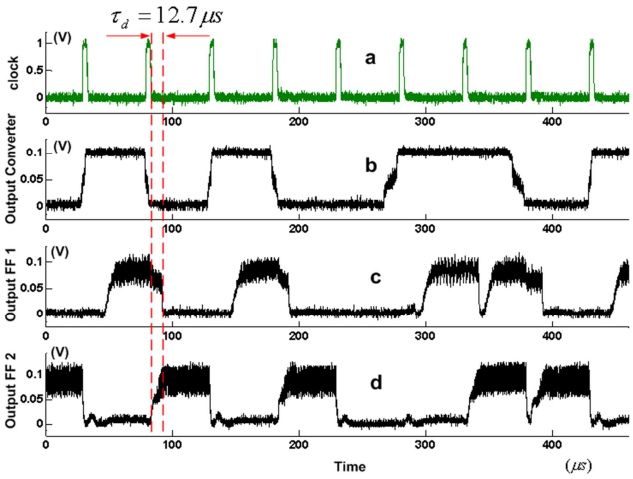


Figure 41 - Results for shifting of the binary sequence 01010011. (a): The 20 kHz clock signal. (b) The output of the optical converter. (c) The output of optical flip-flop 1. (d) The output of optical flip-flop 2. All the signals in panels (b), (c) and (d) are filtered by a filter with a center wavelength of λ2 [35].

3.1.3.3 All-optical random access memory

An optical memory is required to store the optical signal while several processing functionalities are performed. The first all-optical static RAM cell, with true random access read/write functionality, is demonstrated in [60], and is based on the hybrid integrated optical flip-flop proposed in [18], in combination with two additional semiconductor optical amplifiers (SOAs). This optical RAM memory can be used for asynchronous and variable-length data packet processing and, if integrated in a memory RAM bank, can avoid the contention of packets.

Figure 42 depicts the configuration of the optical static RAM cell. The optical flip-flop serves as the single-bit memory element utilizing the wavelength dimension and the coupling mechanism between the two SOA-MZIs for determining the memory content, whereas the two SOAs operate as XGM switches, controlling access to the flip-flop configuration. The ON-OFF of both SOAS depend of the value present at the inverted access bit (Port A).

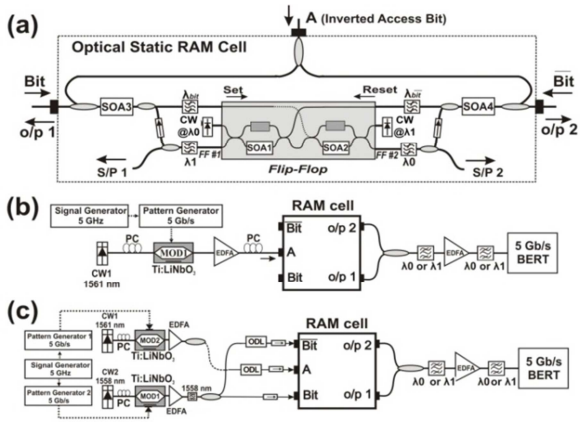


Figure 42 - (a) Layout of the optical static RAM cell. (b) Read mode experimental setup. (c) Write mode experimental setup [60].

Error-free read and write functionality with true random access properties at 5 Gb/s were demonstrated directly in the optical domain (Figure 43).

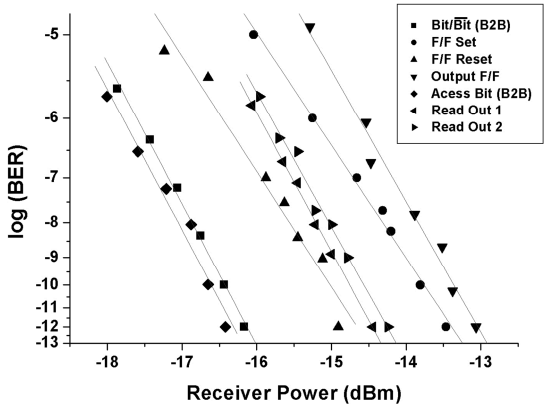


Figure 43 - BER measurements at 5Gb/s for read and write mode operation [60].

3.1.3.4 All-optical square-wave clock generation

Optical square-wave clock signals are essential in all-optical synchronous systems and they can be very attractive for the integration of different devices into a photonic integrated circuit. In [61], an optical square-wave generation is demonstrated using an all-optical optical flip-flop, based on a bistable resonant-type SOA (RT-SOA), and a traveling-wave SOA (TW-SOA). The proposed optical-clock generation scheme operates as shown in

Figure **44**. The square-wave optical clock is created by sequentially bringing the optical power above and below the switching thresholds of the bistable hysteresis, and is obtained after the TW-SOA block, although it is present before and after the RT-SOA.

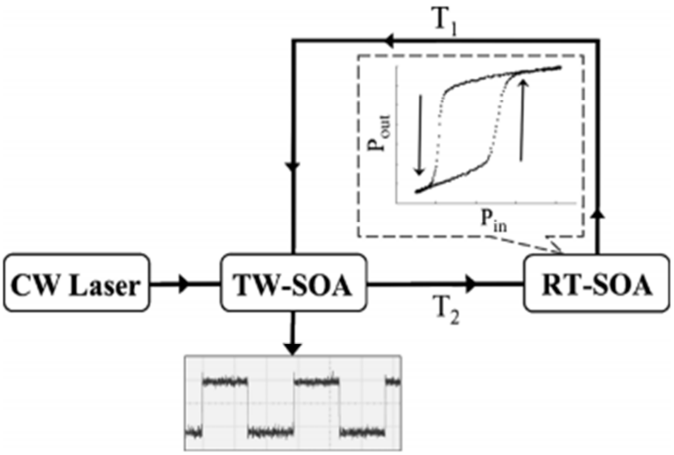


Figure 44 - All optical square-wave clock generation. Inset figure show the hysteresis loop of the RT-SOA [61].

Figure 45 shows the experimental time domain traces of the optical square-wave clock signal, for a span of 1 ms. A rise time of 560 ps and a fall time of 740 ps are obtained. The active elements, used to generate the optical clock signal, are electrically driven only with DC currents.

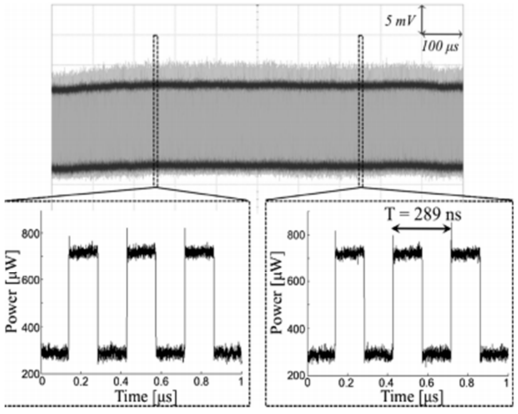


Figure 45 - Optical square-wave clock generation. Insets show the details of the square-wave regions over 1µs windows of the optical clock [61].

3.1.4 Performance comparison between different AOFF techniques

We collected and characterized in terms of commuting speed, switching energy and integration capability some of the most relevant experimental implementations of all-optical flip-flops.

Table 9 presents our comparative study of the different technologies proposed for the implementation of AOFFs and their performances were evaluated based on experimental results. Besides the figures of merit presented in this table, other parameters could also be used to assess the performance of the different AOFF configurations, such as tunability, set reset wavelength dependence, polarization dependence, insertion losses, among others.

Since the output of clocked flip-flops are mainly determined by the S-R latch state, in [55] the authors of the optical clocked flip-flops, based on SOA ring lasers, ignored the influence of the other elements of the proposed schemes. Therefore, the performance of these optical clocked flip-flops was evaluated considering the results obtained in the asynchronous S-R latch. This scheme needs isolators to ensure the unidirectional propagation of the light in the rings, and the total length of each ring laser is few tens of meters, which limits the operation speed of these optical flip-flops. Photonic integration could improve the switching performance of these bistable devices, however with today's technology optical isolators smaller than 0.8 mm are difficult to obtain. A key indicator of the performance of AOFFs is the extinction ratio and, ideally, it should be a high value. The compared AOFF technologies present extinction ratio values in order of 10 dB (dynamic measurements), which are still suitable in optical signal processing.

The influence of set/reset pulse energies needed to change the flip-flop state and their relation with the feedback loop of some AOFF schemes were also investigated. Values in order of fJ are already possible to obtain.

As a summary, Table 9 indicates that the optical one-bit memories presented in this section require, in general, low energies to operate, without compromising state integrity, and have potential high operation speed, making them suitable for future optical packet switching networks. They also present, in general, photonic integration capability, which allow high density packaging

Table 9: Comparison between different all-optical flip-flops techniques. A: asynchronous; S: synchronous; DM: dynamic measurement; SM: static measurement CR: Contrast ratio.

Technology	**Type**	**Extinction Ratio**	**Switching Times**	**Switching Energies**	**Hybrid Integration**	**Monolithic Integration**	**Discrete fibre device**
AOFF based on coupled SOA-MZI	A S-R [18]	>10 dB DM	< 200 ps	< 1 pJ	✓		
AOFF based on coupled SOA ring lasers	A S-R [17]	40 dB SM	≤ 1µs	≤20 nJ			✓
	S S-R [55]	40 dB SM	≤ 1µs	≤20 nJ			✓
	S D [55]	40 dB SM	≤ 1µs	≤20 nJ			✓
	S J-K [55]	40 dB SM	≤ 1µs	≤20 nJ			✓
	S T [55]	40 dB SM	≤ 1µs	≤20 nJ			✓
AOFF based on coupled SOA ring lasers, with AWG	A S-R [44]	35 dB SM	≤ 1ns	< 10 pJ		✓	
AOFF based on MZI-BLD	A S-R [46]	>14.4dB DM	< 320 ps	≤ 67 pJ		✓	
	S S-R [58]	9 dB DM	≤ 300 ps	< 30 fJ		✓	
AOFF based on MMI-BLD	A S-R [47]	16 dB DM	≤ 470 ps	~260 pJ		✓	
AOFF based on a single SOA-MZI	A S-R [41]	11 dB DM	≤ 66 ns	< 235 pJ			✓

Technology	**Type**	**Extinction Ratio**	**Switching Times**	**Switching Energies**	**Hybrid Integration**	**Monolithic Integration**	**Discrete fibre device**
AOFF based on a SOA-MZI, with a coupler inside the feedback loop	A S-R [42]	13.6 dB DM	≤ 29 ps	< 0.5 nJ			✓
AOFF based on coupled FP-LD	A S-R [48]	7 dB CR	~ 50 ps	< 119 fJ			✓
AOFF based on single DFB	A S-R [49]	12dB DM	≤ 75 ps	≤ 190 fJ		✓	
AOFF based on a single micro-ring laser	A S-R [50]	>20 dB SM	<190 ps	4 fJ		✓	
AOFF based on coupled micro-ring lasers	A S-R [51]	> 8 dB DM	< 20 ps	~5,5 fJ	✓		
AOFF based micro-disk laser	A S-R [52]	11 dB DM	60 ps	1,8 fJ		✓	
AOFF based VCSEL	A S-R [53]	-	~ 300 ps	10 fJ		✓	

3.2 Experimental and theoretical demonstration of all-optical flip-flops

In subsection 3.1.2, we presented an overview of clocked AOFF configurations, but most of the optical bistable devices reported in the literature are still asynchronous, and any change of information in the inputs is transmitted, immediately, to the output of the flip-flop, according to its truth table. However, in some cases, the flip-flop' inputs can suffer unwanted variations and if we are using asynchronous devices, we can be storing unwanted information. Therefore, it is interesting that a higher priority input exists to be responsible for controlling the enabling of the latch, making the bistable sensitive or not to the values at the inputs.

In this section, we proposed and experimentally demonstrated two synchronous bistable schemes based on two coupled SOA-MZIs and additional combinational logic circuits. To our best knowledge, these were the first demonstration of all-optical clocked flip-flops, using SOA-MZI structures. In this section, we also proposed and demonstrated, through numerical simulations, the performance of two novel schemes: an all-optical S-R flip-flop using two gain-clamped Reflective Semiconductor Optical Amplifiers (RSOAs) and an all-optical clocked D flip-flop based on a single SOA assisted symmetric MZI.

3.2.1 All-Optical S-R Flip-Flops Techniques

3.2.1.1 All-optical clocked S-R flip-flop based on two coupled SOA-MZI

We implemented an optical synchronous S-R flip-flop based on active interferometric devices, which consists of a latch S-R and two AND gates to enable the flip-flop by the clock signal. Figure 46 presents the experimental scheme of our proposed all-optical clocked S-R flip-flop. Since all building blocks are based on hybrid SOA-MZIs, this technology has the potential for fast switching speeds, high extinction ratios and photonic integration.

The main component of the optical clocked S-R flip-flop scheme, shown in Figure 46, is the S-R latch [18], which consists of two coupled SOA-MZI, powered by two continuous wave (CW) signals, at different wavelengths. The latch operation principle is based on the gain quenching concept: when MZI1 suppresses the output from MZI2 it becomes dominant and the latch emits a signal at 1554.75 nm; due of system symmetry, when the MZI2 suppresses the output from MZI1, the latter one becomes the slave, and 1550.26 nm dominates the output.

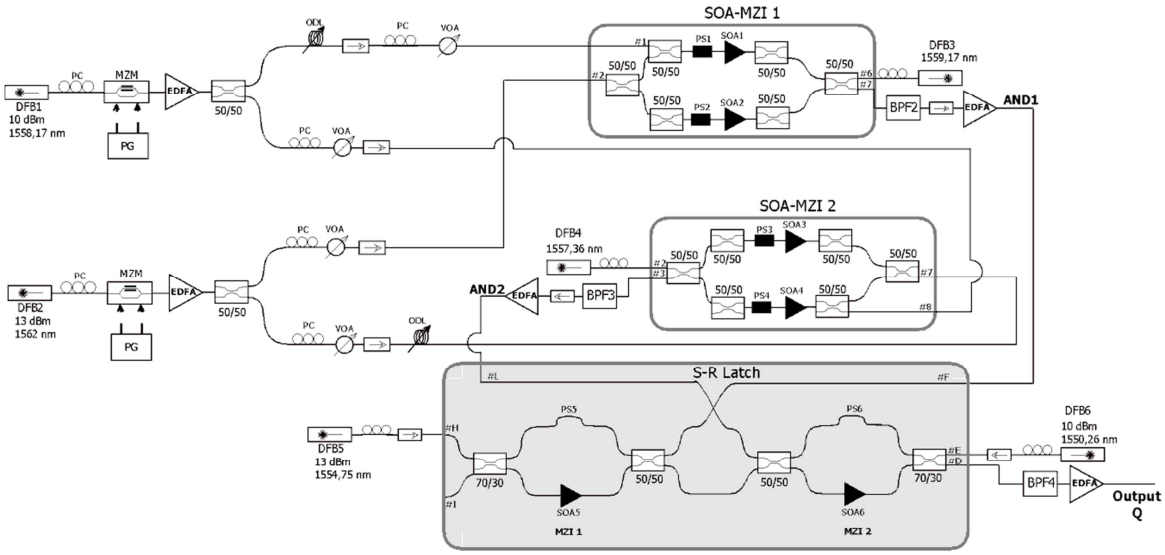


Figure 46 - Experimental scheme of the optical clocked S-R flip-flop. DFB: distributed-feedback laser; PC: polarization controller; MZM: Mach-Zehnder modulator; EDFA: Erbium Doped Fiber Amplifier; ODL: optical delay line; CW: continuous wave laser; BPF: band pass filter; VOA: variable optical attenuator; SOA: semiconductor optical amplifier; PS: phase shifter; PG: pattern generator.

The experimental setup of the optical S-R latch is illustrated in Figure 47 and its dynamic operation is experimentally demonstrated in Figure 48, by toggling the state of the latch through the injection of set and reset optical pulses.

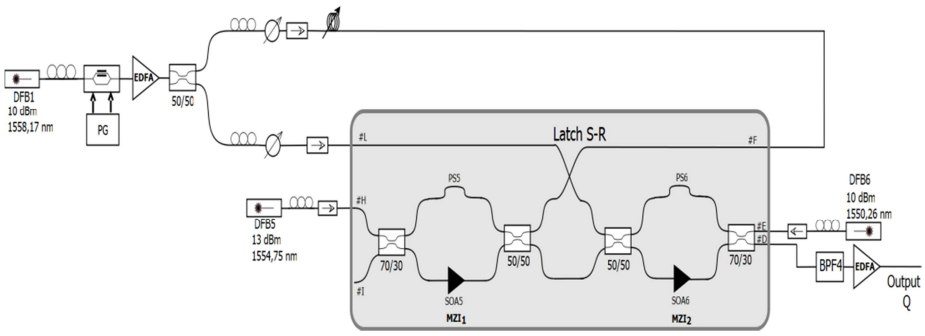


Figure 47 - Experimental optical asynchronous S-R latch scheme based on two coupled SOA-MZI.

The set and reset optical pulses are generated by an external cavity laser peaking at 1558.17 nm, followed by a polarization controller and a Mach-Zehnder external modulator. The NRZ-OOK data signal, generated by an Anritsu MP 1763C, is then amplified by an Erbium Doped Fiber Amplifier (EDFA), split into two equal parts using a 3 dB coupler and then delayed by 11,6ns to obtain different set and reset patterns.

The experimental results, depicted in Figure 48 show that a change of information in the latch inputs is transmitted, immediately, to the output, according to the S-R latch' truth table. The rise

and fall times are 1.029 ns and 857 ps, respectively, and these results are limited mainly due to the recovery time of the SOAs.

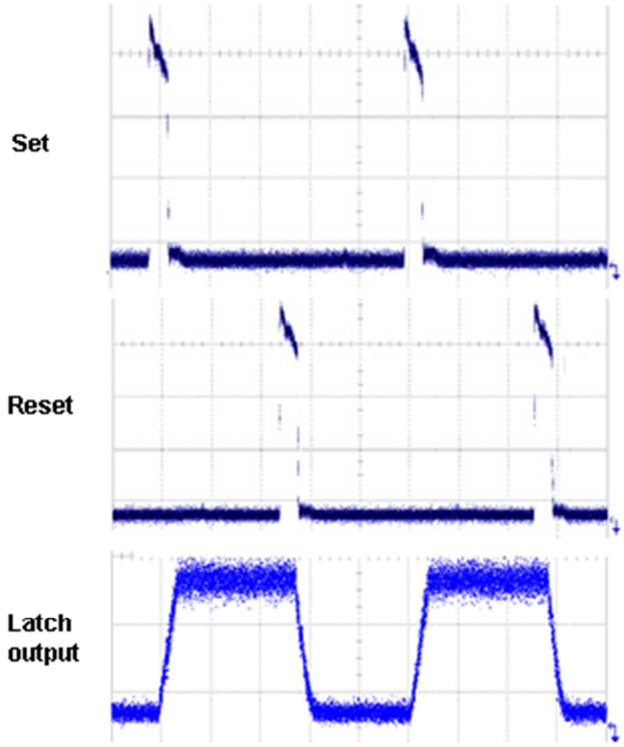


Figure 48 - Experimental results for asynchronous S-R latch. The vertical scale is arbitrary and the horizontal scale is 5ns/div.

Contrary to the described S-R latch operation, the optical clocked S-R flip-flop, shown in Figure 46, allows to control the way the information at set/reset inputs is stored, by working with a synchronization signal (CLK). To implement this all-optical clocked S-R flip-flop scheme, two SOA-based Mach–Zehnder interferometer devices, acting as AND logic gates, are used to enable the S-R latch by the logical level of the clock signal. So, for the cases that the clock signal is in its high level (CLK=1), the information at the inputs is transmitted to its outputs. On the contrary, if CLK=0, the flip-flop maintains its previous state, regardless the binary input data.

Both optical AND gates are implemented in a co-propagation configuration. The SOA-MZI 1 performs the Boolean AND logic operation between the reset and the clock signals. On the other hand, SOA-MZI 2 performs the AND function between the set signal and the clock signal. The clock signal is generated by an external cavity laser, peaking at 1562 nm, with 13 dBm of optical power. The set and reset input signals are the same as the ones used to test the asynchronous S-R latch.

Figure 49 illustrates that the all-optical clocked S-R flip-flop switches between two states, by

injecting optical pulses into the MZI that is currently dominant, allowing the other MZI to become dominant only when a clock pulse arrives, otherwise the flip-flop maintains its previous value. Depending on the flip-flop state, the bistable device emits a signal at 1554.75 nm or at 1550.26 nm.

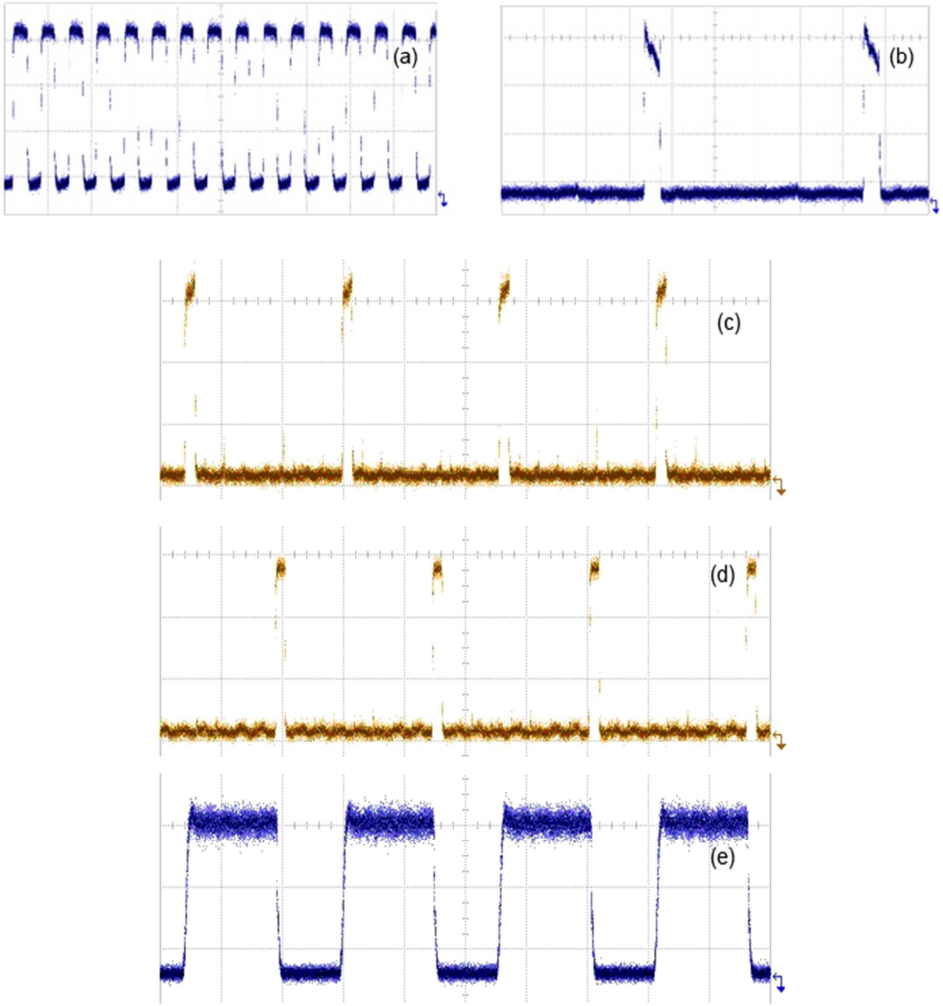


Figure 49 - Experimental results: a) clock signal; b) reset signal; c) AND2 optical gate (Set∩Clock); d) AND1 optical gate (Reset∩Clock); e) optical clocked S-R Flip-Flop output The vertical scale is arbitrary and the horizontal scale is 5ns/div for a) b) figures and 10 ns/div for c)d)e).

Although all the building blocks of our synchronous S-R flip-flop are based on hybrid integrated SOA-MZIs, the interconnection between the blocks and in the feedback loop were, experimentally, implemented using discrete fiber pigtailed, which affects the switching behavior. Anyway, we achieved a switching speed of 430 ps and 420 ps for rise time and the fall time, respectively. However, a complete integration would enhance the performance and reduce the device size. We also analyzed the performance of this flip-flop and 18 dB of extinction ratio was obtained.

3.2.1.2 All-optical S-R flip-flop based on two gain-clamped Reflective Semiconductor Optical Amplifiers (RSOAs)

We demonstrated the operation of a novel all-optical S-R flip-flop scheme based on two coupled lasers, with high photonic integration capability.

Figure 50 illustrates the simulation setup of the proposed all-optical S-R flip-flop memory. This AOFF works as follows: both set and reset signals propagate in the same wavelength λ3. When the set signal is in its high level, the laser beam, centered in λ1, generated by the reflections between the Fiber Bragg Grating (FBG) centered in λ1 and RSOA1, has its power attenuated by XGM effect. Besides, the laser beam generated by the reflections between the FBG centered in λ2 and RSOA2, goes to an high level due to the low level of λ1 (due to the effect of XGM, also) and at the output we have the laser beam λ2 at an high level and the laser beam λ1 at a low level. When the set comes again to the low level, both set and reset are in the '0' level and the AOFF maintains its present state which means that we have the laser beam λ2 at an high level and the laser beam λ1 at a low level. When the reset goes to a high level, the process is inverted and, due to XGM, the λ2 laser beam goes to a low level and the λ1 goes to a high level.

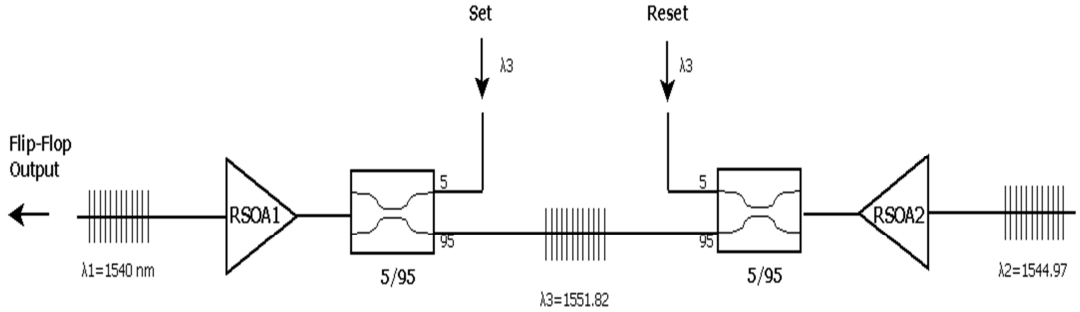


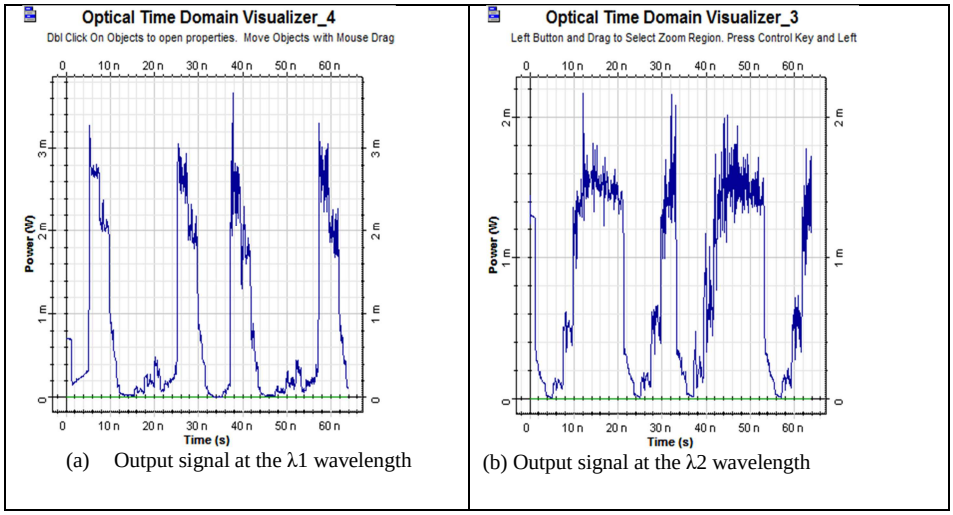
Figure 50 - Simulation setup of the all-optical S-R flip-flop based on two coupled lasers.

In Table 10 the RSOA and simulation parameters are shown. The most distinguishable fact is that the FBG reflectivity is higher than the RSOA reflectivity, in order to have the highest value possible for the energy inside the Fabry-Perot cavity. Simulations results show that a FBG reflectivity of 40% is the optimum value.

Table 10: RSOA and simulation parameters

RSOA and simulation parameters		Unit
Input Facet Reflectivity	0.00005	
Output Facet Reflectivity	0.1	
Active Length (Lx)	0.001	m
Taper Length (Ly)	0.0001	m
Active Area	1e-13	m^2
Optical confinement factor	0.45	
Recombination coefficient A	3.6e8	s^{-1}
Recombination coefficient B	6.5e-16	m^3 / s
Recombination coefficient C	2e-41	m^6 / s
Differential Gain	4e-20	m^2
Carrier density at transparency	9e23	m^{-3}
Index of refraction (η_{eq})	3.22	
$\frac{dn_{eq}}{dN}$	3e-27	m^{-3}
λ1 and λ2 FBGs reflectivity	0.4	
λ3 FBG reflectivity	0.99	

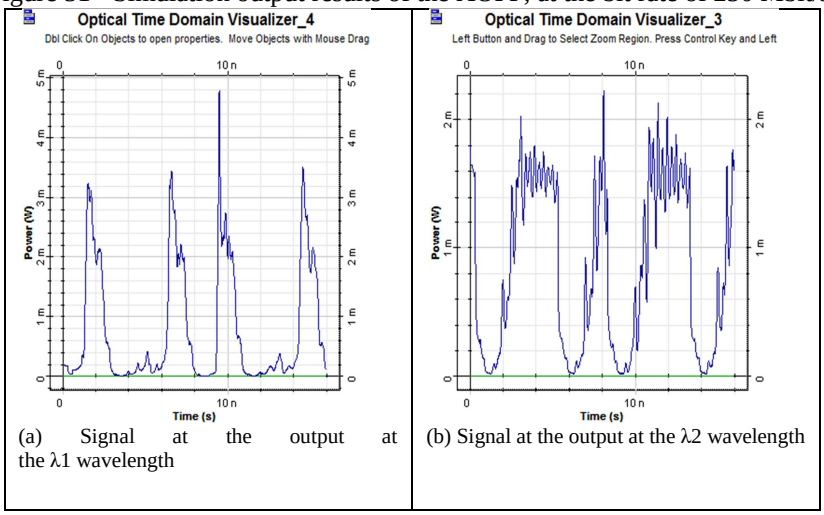
In Figure 51 and Figure 52 the results for the AOFF output are shown. We see a clear toggle, between the λ1 and the λ2 wavelength, showing a correct operation for the AOFF even for challengeable bit rates, like 1 Gbit/s. Although some undesired peaks appear, we expect to smooth the signal by including a filter at the output of the AOFF.



(a) Output signal at the λ1 wavelength

(b) Output signal at the λ2 wavelength

Figure 51 - Simulation output results of the AOFF, at the bit rate of 250 Mbit/s.



(a) Signal at the output at the λ1 wavelength

(b) Signal at the output at the λ2 wavelength

Figure 52- Simulation output results of the AOFF at the bit rate of 1Gbit/s.

We also can conclude, by analyzing Figure 51 and Figure 52, that the rise and fall times are in the nanoseconds/subnanoseconds range.

The flip-flop configuration proposed in [15] presents a similar operation principle, however, with a cavity of 7 meters long, the device is not integrable to the chip-level, something that is solved with a our solution, which presents a cavity with some millimeters. Also we do not use two lasers to control the set and reset operation, only one laser, centered in λ3, is needed, and an optical delay line, to delay the signal between the set and reset operation. A simpler approach is achieved with our solution, using only three FBGs, instead of four. Therefore, we reduce the complexity by using fewer components.

3.2.2 All-Optical clocked D Flip-Flops Techniques

An optical S-R flip-flop has a forbidden state that occurs when both set and reset inputs are at the high state (‘1’). In that situation, it is not possible to predict, theoretically, the flip-flop output.

The optical D flip-flop is an adaptation of the optical S-R flip-flop and can be implemented using a transparent S-R latch. Since the optical D flip-flop only has one data input, the D signal is launched into the S port of the latch and the complement of the D input into to the R input port. Therefore, at the input latch ports are only possible the following combinations: S=0 and R=1 (when D=0) or S=1 and R=0 (when D=1) removing, in that way, the S=R=0 and the delicate condition S=R=1.

An optical clocked D type flip-flop only changes its logical state when the clock signal is in the high level. If the clock signal is low when a transition in the D input occurs, the output Q will only toggle at the next clock pulse

The operation principle of the optical clocked D flip-flop is summarized in Table 11.

Table 11: Truth table of the optical clocked D flip-flop.

CLK	D	Q
1	0	0
1	1	1
0	X	Last Q

3.2.2.1 All-optical clocked D flip-flop based on coupled SOA-MZI

Like the optical clocked S-R flip-flop based on two coupled SOA-MZI, shown in subsection 3.2.1.1, the logic level obtained in the output of our proposed and experimentally demonstrated optical clocked D flip-flop is determined by the dominant wavelength laser.

The experimental setup is depicted in Figure 53.

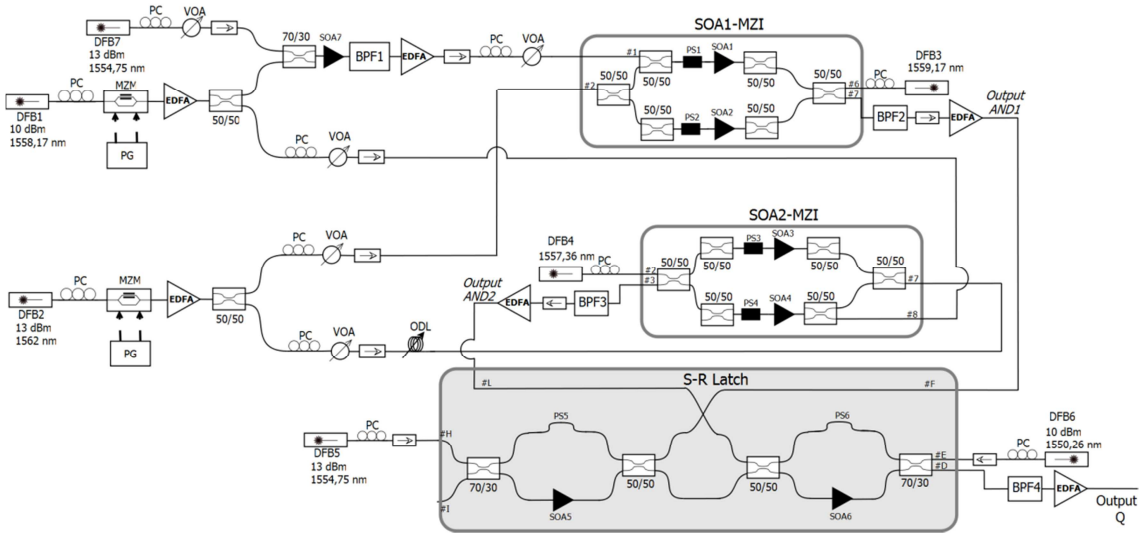


Figure 53 - Experimental scheme of the optical clocked D flip-flop based on two coupled SOA-MZI.

Since the optical clocked D flip-flop only has one input data, a NOT gate, implemented with one SOA, is needed to realize the complementary signal. To carry out the optical NOT logic operation, based on cross gain modulation (XGM) in a SOA, the NRZ signal at 1558.17 nm is coupled to a continuous wave signal, centered at 1554.75 nm. Then, is injected into SOA_7, which will modulate the gain of the amplifier due to its saturation. Since a co-propagation scheme is used to implement the NOT gate, a band pass filter (BPF_1) is introduced, at the output of the SOA_7, to eliminate the modulated signal wavelength. In order to prevent the degradation of the inverted signal quality, the translation was made from longer to shorter wavelength.

Two AND gates are used as the control signals of the S-R latch in order to maintain the flip-flop' previous state, in the absence of the clock signal, independently of the D input information at that moment. Both AND gates are implemented using SOA-MZI structures that are previously balanced in order to obtain the maximum extinction ratio possible between the interferometric outputs. By acting in the polarization controllers, on the SOAs gains and by applying voltage to the phase shifters, SOA_1-MZI and SOA_2-MZI were balanced, showing an ER of 36 dB and 25 dB, respectively.

After balancing the SOA-MZI structures, the clock signal, peaking at 1562 nm, with 13 dBm of optical power, is split by a 3 dB coupler and then launched into the ports of SOA_1-MZI and SOA_2-MZI. Due to the nonlinear phase rotation of the SOAs in an interferometer, the logic AND functions are carried out between the clock signal and the inputs data signals. Since both AND gates are implemented in a co-propagation configuration, the wavelength of the data signal and the clock signal are enough separated in order to avoid undesired crosstalk and nonlinear effects such

as four wave mixing (FWM).

The dynamic operation of the synchronous D flip-flop is experimentally demonstrated by toggling the state of the flip-flop through the injection of optical pulses.

Figure 54 illustrates the time domain traces of the clock, D input and Q flip-flop output signals. The input D signal has a repetition rate of 40 MHz, with a pulse width of 2 ns while clock signal has a repetition rate of 300 MHz, with a pulse width of 1.67 ns.

The experimental performance analysis shows that if a change of information occurs in the data input, when the clock is at its low state, the Q output will maintain its last value, switching only at the next clock pulse. The experimental results are in good agreement with the operation principle of the flip-flop shown in the D truth table.

We achieved a switching speed of 290 ps and 379 ps for rise time and the fall time, respectively. We also made an evaluation performance of the proposed clocked D flip-flop and an extinction ratio of 12,5 dB was obtained.

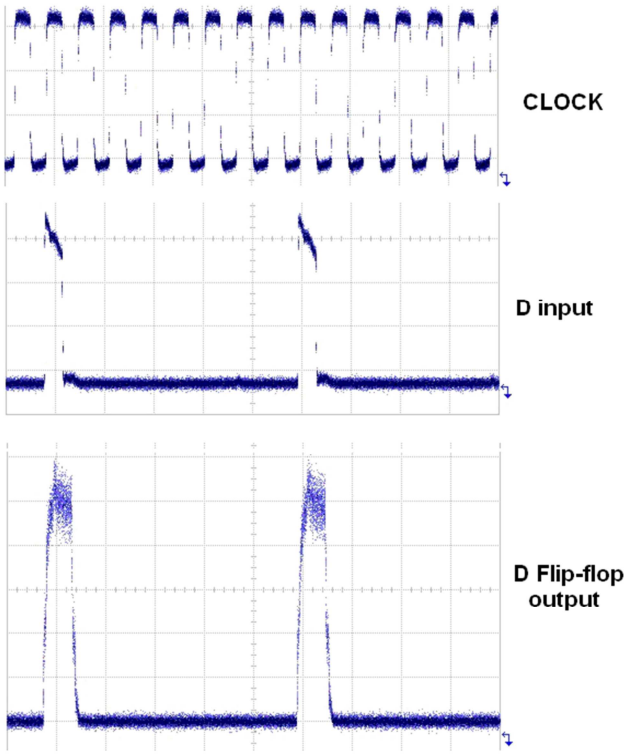


Figure 54 - Optical clocked D flip-flop operation. The vertical scale is arbitrary and the horizontal scale is 5ns/div.

3.2.2.2 All-optical clocked D flip-flop using a single SOA assisted symmetric MZI

We proposed and numerically demonstrated an all-optical clocked D flip-flop scheme capable to control the timing when the information is stored. The bistability of the proposed configuration, illustrated in Figure 55, is caused by an external feedback loop between the output Q and the inputs, and due to the interferometric structure of this flip-flop configuration, its operation principle relies on the dependency of the refractive index on the carrier density of the SOA. The loop has an optical delay line (ODL) and an optical attenuator (ATT), in order to synchronize and to equalize the power of the input data signals that enter in the circuit from interferometric ports #B and #C. The objective of the feedback loop is to maintain the flip-flop's previous state, in the absence of the clock input signal. The feedback loop length should be such that the data can reach to the port #C of the MZI when the gain recovery of the SOA takes place, otherwise the optical data can reach to the unwanted port, due to crosstalk.

The SOA-MZI used in the numerical simulations is a uniformly symmetric device, with the exactly same optical path on both MZI arms.

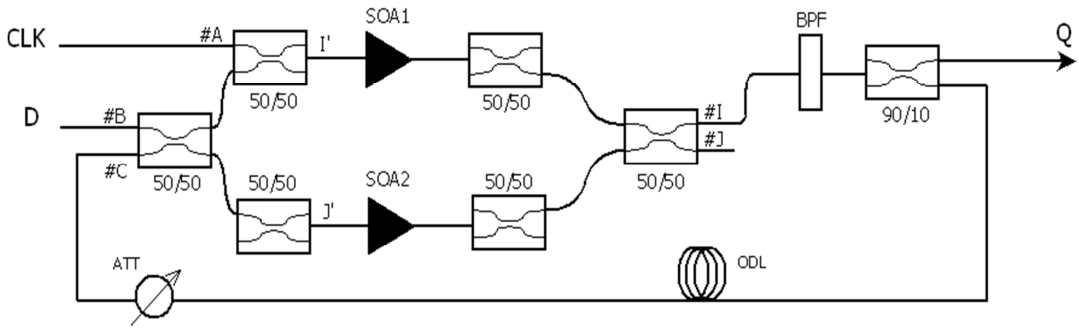


Figure 55 - Schematic representation of the all-optical D flip-flop based on a single SOA-MZI. D: incoming signal; CLK: clock signal; Q: flip-flop output; ODL: optical delay line; ATT: optical attenuator; BPF: band pass filter. The input ports of the MZI are A, B.

The power at the flip-flop output Q (port #I) is a result of an interference process, that can be constructive or destructive, depending on the internal phase condition of the interferometer. So, when the control signal (CLK) is 'ON', the data of the input port (D) reaches to its corresponding bar-port (port #I). On the other hand, if CLK = OFF then the incoming signal emerges at its cross-port (port #J).

A. Theoretical model and operation cases

Some assumptions were considered for the theoretical model of the clocked D flip-flop based on a symmetric SOA-MZI switch, namely that the incoming signal (D) should not affect the SOA gain dynamics. So, the incoming signal was selected ten times smaller than the control (CLK) pulse. The gain and group-velocity dispersion were neglected, which is practically satisfied for pulse-width in the pico-second range. This essentially means that the incoming and clock signals travel through SOA at same speed, so their transit times are equal. In [62], it was demonstrated that ASE becomes too high and influence the gain saturation only for SOAs longer than 1500μm. Since the energy of the control pulse was less than 1 pJ, with a very narrow pulse-width, the two-photon absorption (TPA) and ultrafast nonlinear reflection (UNR) were also neglected [63]. Furthermore, the SOA small signal gain, internal loss and saturation energy were assumed to be wavelength independent and hence the same for both control and incoming signal, otherwise we would need to use the second order polynomial of the gain spectrum [57], which would increase the model complexity.

The saturation energy and unsaturated single-pass amplifier gain of the SOA can be expressed as [64, 65]:

$$E_{sat} = \frac{\hbar \omega_0 wd}{a_N \Gamma} \tag{3.1}$$

$$G_0 = \exp\left[g_0 L - \alpha_D L\right] \tag{3.2}$$

$$g_0 = \Gamma a_N N_{tr}\left(\frac{I\tau_e}{qwdLN_{tr}} - 1\right) \tag{3.3}$$

where, E_{sat} is the saturation energy of the SOA, G_0 the unsaturated single-pass amplifier gain, Γ the confinement factor, a_N the differential gain, N_{tr} the carrier density at transparency, *q* the charge of a electron, *w* and *d* are, respectively, the width and the depth of the active region of SOA, *L* is the active length of SOA, α_D the internal loss of the waveguide and $\omega_0$the frequency. $\hbar = h/2\pi$, where h is the Plank constant.

When an optical pulse passes through a SOA, it is amplified and can be defined as [66]

$$P_{out}(t) = P_{in}(t) \cdot \exp\left[h(t)\right] \tag{3.4}$$

where, $P_{in}(t)$ and $P_{out}(t)$ are the power and phase of the input and output pulse, respectively.

From the following differential equation [66]

$$\frac{dh(t)}{dt} = \frac{g_0 L - h(t)}{\tau_e} - \frac{P_{in}(t)}{E_{sat}}\left\{\exp\left[h(t)\right] - 1\right\} \tag{3.5}$$

$h(t)$ can be calculated as

$$h(t) = -\ln\left[1 - \left(1 - \frac{1}{G_0}\right)\exp\left(-\frac{E_{cp}(t)}{E_{sat}}\right)\right] \tag{3.6}$$

When a clock pulse (CLK) is injected into the SOA assisted symmetric MZI switch, it saturates the SOA at time t_s and changes its index of refraction. The gain of the SOA decreases rapidly as

$$G(t) = \exp\left[h(t)\right] \tag{3.7}$$

The energy fraction contained in the leading edge of the pulse until the $t' \le t$ is given by

$$E_{cp}(t) = \int_{-\infty}^{t} P_{cp}(t')\, dt' \tag{3.8}$$

By definition $E_{cp}\left(t \to \infty\right) = E_c$ = total energy of the control pulse. After a while, the gain recovers due to injection of carriers and can be obtained from the gain recovery formula [67]

$$G(t) = G_0\left[\frac{G(t_s)}{G_0}\right]^{\exp\left[-\left(t - t_s\right)/\tau_e\right]} \quad ; \quad t \ge t_s \tag{3.9}$$

where, τ_e is the gain recovery time.

When a periodic pulse train is injected into the SOA, there is no time for the recovery of the gain to G_0. Instead, it only recovers to a lower gain, G_l [68]. Hence, equation (3.7) takes the following form

$$G(t)=\left\{1-\left(1-1/G_l\right)\exp\left[-E_{cp}(t)/E_{sat}\right]\right\}^{-1} \tag{3.10}$$

Considering a Gaussian pulse $P_{cp}(t)=\frac{E_c}{\sigma\sqrt{\pi}}\exp\left(-\frac{t^2}{\sigma^2}\right)$ as the clock signal and σ related to full width at half maximum (FWHM) by $T_{FWHM}\approx 1.665\sigma$ then we can write

$$E_{cp}(t)=\frac{E_c}{2}\left[1+erf\left(\frac{t}{\sigma}\right)\right] \tag{3.11}$$

where, *erf*(.) is the error function.

The SOA saturation time is $t_s \approx T_{FWHM}$, then 99% of the pulse transmits through the SOA. So, from equation (3.10) we obtain

$$G_f = G(t_s)=\frac{G_l}{G_l-\left(G_l-1\right)\exp\left(-E_c/E_{sat}\right)} \tag{3.12}$$

At the next bit period (ξ), SOA gain does not reach to G_0, but only G_l. So,

$$G_l = G(\xi)=G_0\left[\frac{G_f}{G_0}\right]^{\exp\left\{-\left(\xi-T_{FWHM}\right)/\tau_e\right\}} \tag{3.13}$$

For the next pulse, the gain starts to decrease again and the same process is repeated. The output power at bar-port (□) and cross-port (×) can be expressed as

$$P_{□}(t)=\frac{P_{in}(t)}{4}\cdot\left\{G_1(t)+G_2(t)-2\sqrt{G_1(t)\cdot G_2(t)}\cdot\cos\left(\Delta\varphi\right)\right\} \tag{3.14}$$

$$P_{\times}(t)=\frac{P_{in}(t)}{4}\cdot\left\{G_1(t)+G_2(t)+2\sqrt{G_1(t)\cdot G_2(t)}\cdot\cos\left(\Delta\varphi\right)\right\} \tag{3.15}$$

where $G_1(t)$ and $G_2(t)$ are the gain of SOA_1 and SOA_2, respectively, at the time t and $\Delta\varphi = -\frac{\alpha}{2}\cdot\ln\left(\frac{G_1}{G_2}\right)$, where α is line-width enhancement factor. Therefore, after they recombine at the

input coupler, the $\Delta\varphi \approx \pi$ and data will exit from the bar port (□). At same time, the power at the cross port = $P_x(t) \approx 0$.

In the absence of the clock signal (*CLK=OFF*), the incoming signal enters into the two arms of the MZI, propagates through both SOA at the same time, and experience almost the same unsaturated amplifier gain G_0. Therefore, the incoming signal passes through the 3dB output coupler with $\Delta\varphi \approx 0$ (as $G_1 \approx G_2$). So expression for $P_{□}(t) \approx 0$ and $P_x(t) \neq 0$.

The D flip-flop output (Q) has two possible states: one is its current state (Q_{n+1}) and the other is its previous state (Q_n). Depending on the different input conditions, the output state Q_{n+1} can be expressed as:

$$P_{Q_{n+1}}(t)\Big|_{\substack{D=CLK=1\\Q_n=0}} = \left(0.9P_{□}(t)\Big|_{Input=D}\right)_{HIGH} \tag{3.16}$$

$$P_{Q_{n+1}}(t)\Big|_{\substack{D=CLK=1\\Q_n=1}} = \left(0.9P_{□}(t)\Big|_{Input=D}\right)_{HIGH} + \left(0.9P_{\times}(t)\Big|_{Input=Q_n}\right)_{LOW} \tag{3.17}$$

$$P_{Q_{n+1}}(t)\Big|_{\substack{D=1,\ CLK=0\\Q_n=1}} = \left(0.9P_{□}(t)\Big|_{Input=D}\right)_{LOW} + \left(0.9P_{\times}(t)\Big|_{Input=Q_n}\right)_{HIGH} \tag{3.18}$$

$$P_{Q_{n+1}}(t)\Big|_{\substack{D=CLK=0\\Q_n=1}} = \left(0.9P_{\times}(t)\Big|_{Input=Q_n}\right)_{HIGH} \tag{3.19}$$

$$P_{Q_{n+1}}(t)\Big|_{\substack{D=0,\ CLK=0\\Q_n=0}} = P_{Q_{n+1}}(t)\Big|_{\substack{D=0,\ CLK=1\\Q_n=0}} = 0 \tag{3.20}$$

$$P_{Q_{n+1}}(t)\Big|_{\substack{D=1,\ CLK=0\\Q_n=0}} = \left(0.9P_{□}(t)\Big|_{Input=D}\right)_{LOW} \tag{3.21}$$

$$P_{Q_{n+1}}(t)\Big|_{\substack{D=0,\ CLK=1\\Q_n=1}} = \left(0.9P_{\times}(t)\Big|_{Input=Q_n}\right)_{LOW} \tag{3.22}$$

Note that the 0,9 factor present in the above formulas is due to the 90/10 coupler of the flip-flop setup. Therefore, only 90% of the power is obtained at the D output port; the others 10% are launched into the feedback loop.

During the operation of the optical clocked D flip-flop, $2^3 = 8$ possible situations can occur.

The possible operation cases of the proposed flip-flop are depicted in Figure 56, and will be discussed, in more detail, below.

CASE-I: *CLK=D=1 and Q_n=0*

Let us consider a strong control signal (CLK) injected, through an optical 2x1 combiner, in the port #A of the SOA-MZI. This signal modulates the gain of the SOA_1, which induces a modulation of its refractive index. If the incoming signal (D) is launched into port #B, half of its power appears at each output of the input coupler, with a phase shift of $\frac{\pi}{2}$. However, due to the presence of the control signal, the two even parts of the incoming signal will suffer different gains and phase shifts, which lead to the unbalance of the SOA-MZI. In this case, the modulation of the refractive index are not the same ($n_1 \neq n_2$), therefore the light in the upper arm of the MZI presents a different velocity than the lower arm; hence the incoming optical pulse emerges at port #I, as illustrated in Figure 56 (a). Therefore, in this case, the flip-flop output is Q = '1'.

CASE-II: *CLK=D=1 and Q_n=1*

If, however, in the previous state, the flip-flop output presented the logical value '1', an optical pulse will travel in the feedback loop and will arrive at port #C of the interferometer, at same time of the incoming optical pulse. Again, due to the presence of the control signal, the two even parts of both signals will experience different gains and phase shifts. Therefore, the optical incoming pulse and the optical pulse from the feedback loop (last Q) will reach their bar-ports, as it is shown in Figure 56 (b). Therefore, in this particular case, the flip-flop's next state will be the logical value '1'.

CASE-III: *CLK=0 and D=Q_n=1*

In the absence of a clock pulse and $D=Q_n=1$, a '1' logical level will arrive to interferometer port #C, at the same time of D optical pulse. Both input signals are split equally, with a phase shift of $\frac{\pi}{2}$, by the input 3-dB coupler.

The outputs of the 3 dB input coupler (coupling ratio=0.5) are given by:

$$\begin{bmatrix} E_{I'} \\ E_{J'} \end{bmatrix} = \begin{bmatrix} \frac{E_B}{\sqrt{2}} + j\frac{E_C}{\sqrt{2}} \\ j\frac{E_B}{\sqrt{2}} + \frac{E_C}{\sqrt{2}} \end{bmatrix} \quad ;\left(j = \sqrt{-1}\right) \tag{3.23}$$

After passing through the input coupler, the signals propagate into the two MZI arms, where they will be evenly amplified by the SOAs. Since the modulation of the refractive index are the same (n_1=n_2), both signals will be affected by the same phase and gain, and no additional phase shift between the two MZI arms is added. Therefore, we can simplify this system analysis, by neglecting the gain and phase contribution provided by the SOAs (since this contribution are the same for both arms).

When the signals arise at the output 3-dB coupler, they will suffer another phase shit of $\frac{\pi}{2}$, and the optical output fields can be calculated by:

$$\begin{bmatrix} E_I \\ E_J \end{bmatrix} = \begin{bmatrix} \frac{E_{I'}}{\sqrt{2}} + j\frac{E_{J'}}{\sqrt{2}} \\ j\frac{E_{I'}}{\sqrt{2}} + \frac{E_{J'}}{\sqrt{2}} \end{bmatrix} \equiv \begin{bmatrix} E_I \\ E_J \end{bmatrix} = \begin{bmatrix} jE_C \\ jE_B \end{bmatrix} \tag{3.24}$$

The output powers can be found by:

$$\begin{aligned} P_I &= E_C \cdot E_C^* = jE_C \cdot (-jE_C) = E_C^2 = P_{Q_n} \\ P_J &= E_B \cdot E_B^* = jE_B \cdot (-jE_B) = E_B^2 = P_D \end{aligned} \tag{3.25}$$

where the superscript * means the complex conjugate. Therefore, when CLK=0 and D= Q_n=1, the D flip-flop holds the information of its last output state, as it is shown in Figure 56 (c).

CASE-IV: *D=CLK=0 and Q_n=1*

In the absence of other input signals, if in the previous state Q_n=1, then a '1' logical level will travel in the feedback loop and will arrive to port #C of the interferometer. After passing through the input coupler, the signal is split in two equal parts and half of the input power appears at each output of the coupler, with a phase shift of $\frac{\pi}{2}$.

$$\begin{bmatrix} E_{I'} \\ E_{J'} \end{bmatrix} = \begin{bmatrix} j\frac{E_C}{\sqrt{2}} \\ \frac{E_C}{\sqrt{2}} \end{bmatrix} \tag{3.26}$$

The signals travel through the nonlinear media (SOAs) and deplete the carrier density, modulating the refractive index. Since both parts of the signal experiments the same gains and phases (G_1=G_2), the signals are equally amplified and recombine at the output coupler, where experiments another $\frac{\pi}{2}$ phase shift. Since the phase and gain, provided by the SOAs are the same for both arms, again no additional phase shift between the two MZI arms is added, so the system can be calculated as

$$\begin{bmatrix} E_I \\ E_j \end{bmatrix} = \begin{bmatrix} jE_C \\ 0 \end{bmatrix} \tag{3.27}$$

For this case, the output powers can be defined as:

$$\begin{aligned} P_I &= E_C^2 = P_{Q_n} \\ P_J &= 0 \end{aligned} \tag{3.28}$$

which means that the output of D flip-flop maintains its previous state when, in the absence of other input signals, the last value of the flip-flop output is ‘1’. This situation is illustrated in Figure 56 (d).

CASE-V: *CLK=1; D=0 and Q_n=1*

When a strong control pulse (CLK) is injected again into the interferometer, it arises at SOA_1, reducing its carrier density, hence the refractive index of SOA_1 changes. In this situation, if in the previous state Q_n=1, this optical pulse will be split in two, after passing through the 3 dB coupler, and will suffer different gains and phase shifts in each of the interferometer arms. Therefore, when the clock is in its high state, it saturates the upper SOA and the signal in the upper arm is not amplified, which means that no optical power is obtained at the flip-flop output (port #I), and the

pulse from the previous state emerge, at the next state, in its bar port, as illustrated in Figure 56 (e). In this case, the flip-flop changes its states from '1' to '0'.

CASE-VI: *CLK=1; D=0 and Q_n=0*

This condition, illustrated in Figure 56 (f), occurs when only a clock pulse is injected into the SOA-MZI. Since the filter block the clock pulse, no optical power will be obtained at the D flip-flop output.

CASE-VII: *CLK=D= Q_n=0*

In this case, it is clear that if no light is injected at the interferometer inputs, no optical signal can be obtained at the interferometer outputs. So, the D flip-flop output presents the logic value '0'.

CASE-VIII: *D=1 and CLK= Q_n=0*

When only an incoming pulse (D) is injected into port #B of the input coupler, its power is distributed, equally, through both SOA-MZI arms, but with a phase shift of $\frac{\pi}{2}$ between the two branches of the interferometer.

$$\begin{bmatrix} E_{I'} \\ E_{J'} \end{bmatrix} = \begin{bmatrix} \frac{E_B}{\sqrt{2}} \\ j\frac{E_B}{\sqrt{2}} \end{bmatrix} \tag{3.29}$$

In the MZI, the two even parts of the incoming signal pass through the two SOAs, where they modulate, equally, the carrier density and thereby the refractive index. Since the length path of the MZI arms and SOA's phase shifts and gains are identical (G1=G2), no additional phase shift is added in the MZI arms because the light velocity, propagating in both MZI arms, is the same. Therefore, both parts of the incoming signal will be evenly amplified and will recombine at the output of the interferometer destructively (port #I) and constructively (port #J). In this situation, the SOA-MZI is balanced.

$$\begin{bmatrix} E_I \\ E_J \end{bmatrix} = \begin{bmatrix} 0 \\ jE_B \end{bmatrix} \tag{3.30}$$

The output powers are then given by:

$$P_I = 0 \qquad (3.31)$$
$$P_J = E_B \cdot E_B^* = jE_B \cdot (-jE_B) = E_B^2 = P_D$$

where the superscript * means the complex conjugate. Therefore, in this case, no optical signal is obtained at the D flip-flop output. i.e., in the absence of a clock pulse, the output does not change even if in D input is applied logic '1'.

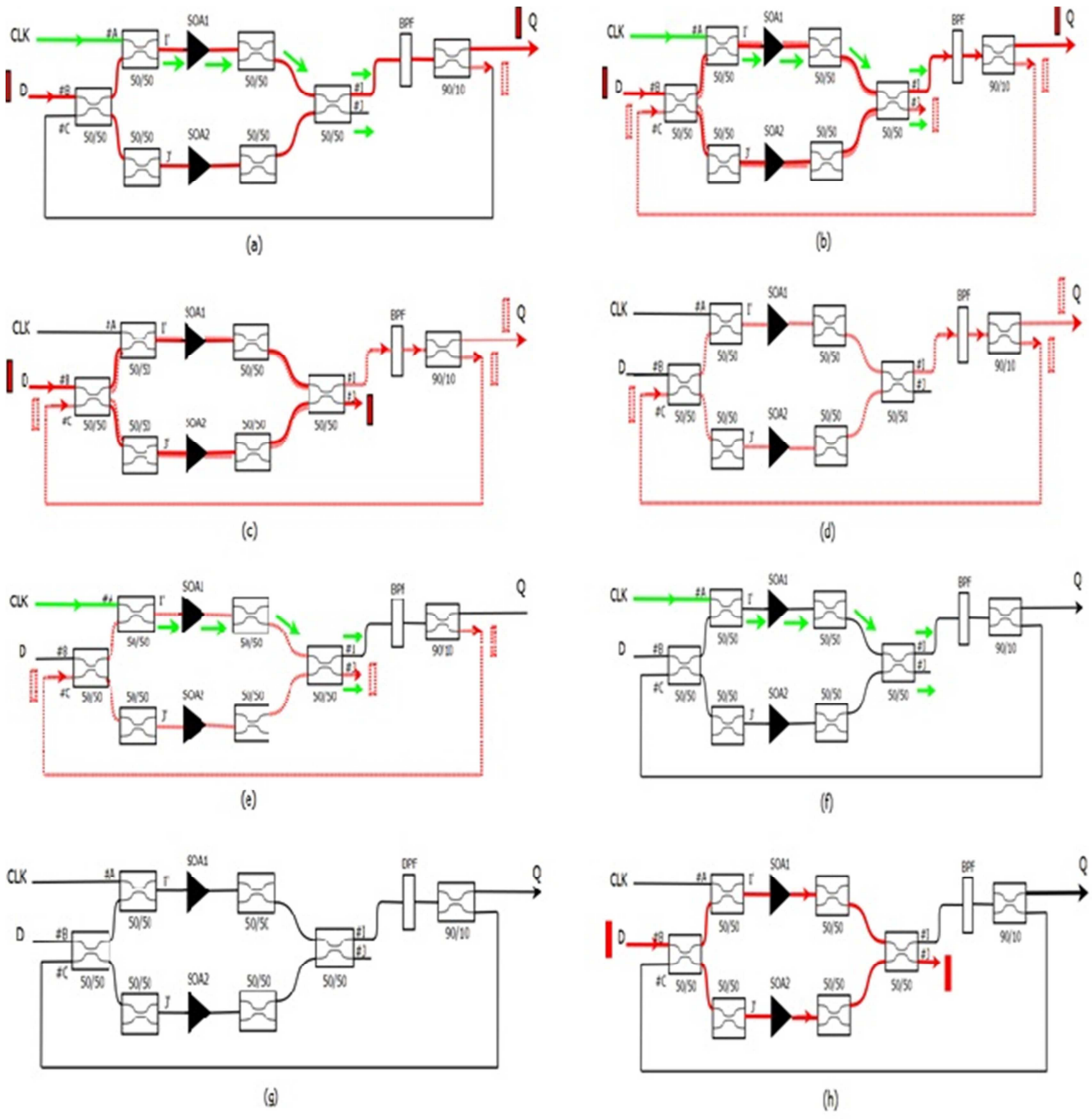


Figure 56 - Power distribution, along the interferometer arms, for different cases. (a) Case-I: D = 1, CLK = 1, Qn = 0, (b) Case-II: D = 1, CLK = 1, Qn = 1, (c) Case-III: D = 1, CLK = 0, Qn = 1, (d) Case-IV: D = 0, CLK = 0, Qn = 1, (e) Case-V: D = 0, CLK = 1, Qn = 1, (f) Case-VI: D = 0, CLK = 1, Qn = 0, (g) Case-VII: D = 0, CLK = 0, Qn = 0, (h) Case-VIII: D = 1, CLK = 0, Qn = 0.

B. Simulation results

A simulation study of the all-optical clocked D flip-flop was carried out at 50 Gb/s, using the parameters summarized in Table 12 [57, 62], of a bulk InGaAsP-SOA operating in 1500 nm spectral region.

Table 12: Parameters used in simulation.

Parameters	Symbol	Value
Injection current of SOA	I	600 mA
Confinement factor	Γ	0.48
Differential gain	a_N	3.3×10^{-20} m^2
Line-width enhancement factor of SOA	α	6.5
Carrier density at transparency	N_{tr}	1.0×10^{24} m^{-3}
Width of the active region of SOA	w	0.7 μm
Depth of the active region of SOA	d	220 m
Active length of SOA	L	150 μm
Internal loss of the wave guide	α_D	2700 m^{-1}
Wave length of light	λ_0	1500 nm
Gain recovery time	τ_e	20 ps
Unsaturated single-pass amplifier gain	G_0	23.14 dB
Clock pulse energy	E_c	15 fJ
Full width at half maximum of control pulse	σ	2 ps
Incoming pulse power		0.2 mW

The dynamic operation of the all-optical clocked D flip-flop was numerically demonstrated by toggling the state of the flip-flop, through the injection of optical pulses. Figure 57 presents the time domain traces obtained for the clocked D flip-flop and it is very noticeable that the

information at the D flip-flop input is transferred to the Q output, only when the clock signal is enabled; otherwise maintains its previous state.

We assessed the performance of this flip-flop configuration and an E.R. = 10.792 dB was obtained. Switching speeds of around 33 ps and 6 ps were achieved for rise time and fall time, respectively. The rising time is higher than the falling time because, after the decrease of the gain of SOA1, the gain increases slowly to its recovery value.

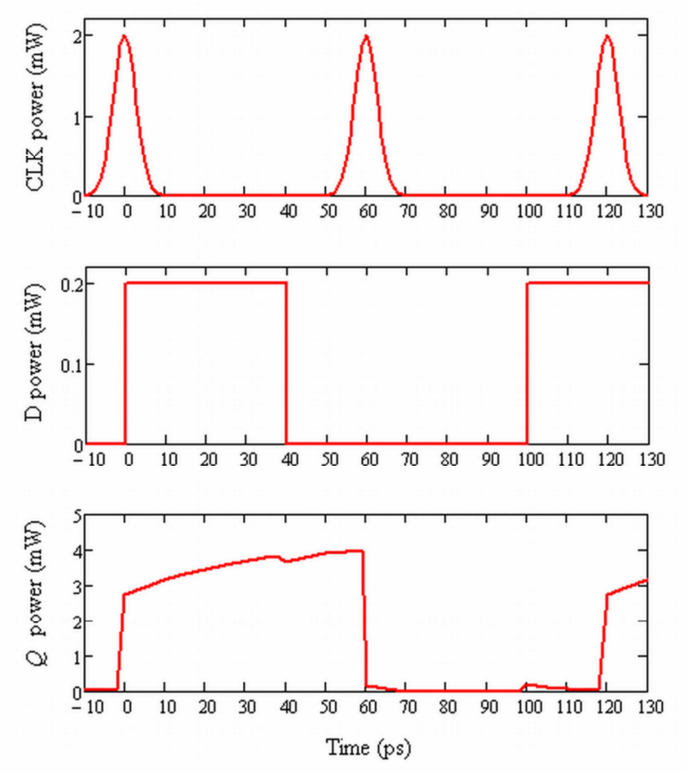


Figure 57 - Simulated output of SOA-MZI based all-optical clocked D flip-flop.

C. Feedback loop calibration

In this flip-flop, the feedback loop is a very important feature since it maintains the flip-flop's previous state, in the absence of the clock input signal. In this section, we try to make a calibration of the length of the feedback loop by showing the effect on the output waveforms, for different loop lengths. Let us consider that the feedback loop length is *L*. So after emission from port#I, the data will reach to the MZI port#C after the time $\tau = L/\upsilon$, where υ is the velocity of light inside the fiber.

When data (D signal) enters through port#B, at time $t_{0,}$ it emits through port#I (if control pulse is 'ON') at time $(t_0 + t_{MZI})$, where t_{MZI} is the time taken through the MZI switch (t_{MZI} is very small). After time 'τ', one part of that signal enters again into the switch through port#C and if the control pulse is 'OFF' then, the data emerges again from port#I after the time $(t_0 + 2t_{MZI} + \tau)$.

The flip-flop properties of the proposed circuit depend on some important aspects, such as:

a. When data arrives at port#C through the feedback loop, the D signal can be present or not.
b. At that time the gain of the SOA_1 recovers or not.
c. The loop length delay time (τ) can be small or large.

As it is shown in Figure 58, we realize numerical simulations to find out the output waveform of the all-optical flip-flop, for different τ. We chose all the possible cases for D and CLK pulse applied, i.e. D=CLK = 1 (at 0 ps in time scale); D=CLK = 0 (at ~0-to-220 ps in time scale); D=1, CLK = 0 (at ~220-to-300 ps in time scale); D = CLK = 1 (at 300 ps in time scale); D=1, CLK = 0 (at ~300-to-500 ps in time scale); D=0, CLK = 1 (at 500 ps in time scale); D = CLK = 0 (at ~500-to-560 ps in time scale) and D=1, CLK = 0 (at ~560-to-600 ps in time scale).

Case-I: (τ= 5 ps)

This case is illustrated in Figure 58 (a). At first, when D = CLK =1, the data emits from port#I and reaches to port#C after 5 ps, so the gain of SOA_1 do not recover. Then D =0 so, from equations (14) and (15), the data will pass through port#J , which means that $Q \to 0$ and the data is not 'HOLD'.

At 300 ps, D = CLK =1, and again we obtain Q = 1. At 305 ps, the previous phenomena happens again, but since D signal is present, port#I gets the data from D and port#C, which violate the flip-flop condition, so data is not 'HOLD'.

Case-II: (τ= 20 ps)

This situation is shown in Figure 58 (b). When data arrives to port#C after 20 ps, the gain of the SOA_1 recovers. Hence, from equation (15), we find out that the output power is not such low as the previous case, so it will increase slowly and saturates up to ~300 ps. At 300 ps, the gain of SOA_1 decreases further (as CLK = ON), and since data at port#C is absent, we obtain low power at the

output (but still Q =1). This two dips are shown in Figure 58 (b) as (i) and (ii). After that it goes to the saturation value. In this case, the 'HOLD' condition of the flip-flop is satisfied.

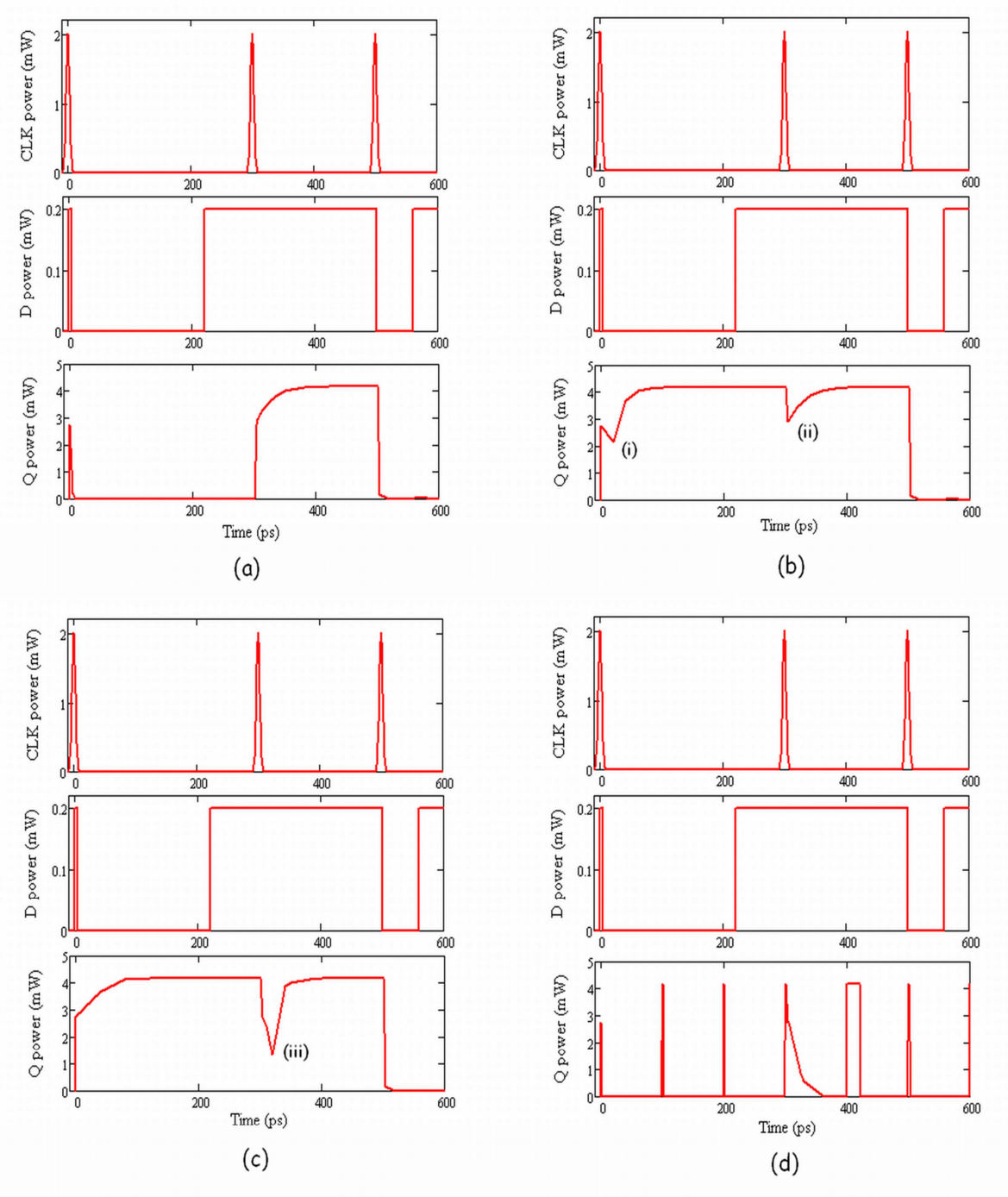


Figure 58 - Output waveforms for different loop length delay time. (a) = 5 ps, (b) = 20 ps, (c) = 40 ps and (d) = 100 ps.

Case-III: (τ= 40 ps)

The output waveform for τ= 40 ps is shown in Figure 58 (c). In this particular case, we do not found the first dip presented in case-II, because after 40 ps the data reaches to port#C, and SOA_1 recovers its gain higher than 20 ps. Therefore, we obtain more power at port#I than the previous case, which is obtained from equation (14) and (15). However, after 300 ps, the output power decreases more than case II. This large dip is indicated by (iii) in Figure 58 (c) since at 340 ps, the feedback comes before data at port#B is presented. After that the output increases slowly to saturation value.

Case-IV: (τ= 100 ps)

If we increase to τ= 100 ps or further more then, we obtain discrete pulses at every 100 ps, because data arrives to port#C after a very large time gap. The output waveform for this case is shown in the Figure 58 (d). We also find an unwanted peak at 600 ps when, according to theory, it should be present the logic value '0'. Therefore, in this case the 'HOLD' condition is not also satisfied. From Fig. 12(c), we verify that if we increase τ>20 ps there may be a problem at point (iii), since it goes below the threshold value. So, in this condition, the data cannot be 'HOLD'. For τ>>20 ps, we get unwanted discrete pulses.

From the analysis of the simulations results, we can conclude that the feedback loop length should be maintained comparable with the gain recovery time (τ_e) of the SOAs, otherwise the proposed flip-flop may not work according with its truth table.

3.3 Conclusions

In this chapter, a description of some of the most relevant implementations of all-optical flip-flops was made, presenting an overview of the up to date all-optical flip-flops design schemes. The main features of the different bistable technologies were highlighted and evaluated based on switching time, switching energy, and other performance metrics. Also, a good variety of current applications was covered and described, which may help defining the next generation of AOFF applications.

As technology scales, is important to develop AOFF techniques, with reduced electrical power consumption. Up to date, the microdisk laser AOFF proposed in [52] emerged with the lowest

electrical power consumption, obtaining 6 mW bit^{-1}.

In this chapter, we also proposed four new all-optical flip-flop configurations, focusing mainly in bistables whose state switching are triggered by a pulsed clock signal. In clocked devices, the synchronization signal is responsible for controlling the enabling of the bistable, making it sensitive or not to the binary information present at its inputs. To our best knowledge, we presented the first demonstration of all-optical clocked flip-flops, using SOA-MZI structures, taking advantage of the inherent regeneration characteristics of the active interferometers. We also proposed and demonstrated, through numerical simulations, the performance of two novel schemes: an all-optical S-R flip-flop using two gain-clamped RSOAs and an all-optical clocked D flip-flop based on a single SOA assisted symmetric MZI. The bistability of the latter optical flip-flop is caused by an external feedback loop between the output Q and the input. The loop has an optical delay line and an optical attenuator, in order to synchronize and to equalize the power of the input data signals that enter in the circuit from interferometric ports. The objective of the feedback loop is to maintain the flip-flop's previous state, in the absence of the clock input signal

In my opinion, technology advances in integration capability can bring a new age for the development of AOFF devices in terms of cost and performance integration in more complex functions, opening in this way a route for a next generation of applications and functionalities.

Chapter 4

All-optical packet routing

The electronic systems of today routers are expected to be able to follow the processing rates of the packet routing in the optical layer, however not known are the cost or energy consumed to achieve that. This fact motivates the search for transparent routing schemes that can potentially provide solutions to the continuously increasing bandwidth demand in telecommunications.

An optical packet routing/switching scheme can forward optical packets to the appropriate destination port, based on the address information that is encoded by the attached labels [24]. The information required for optical routing is carried together with the optical signal (e.g. label) and since it can be extracted and added from the optical signal without optical-electrical-optical (O/E/O) conversion, lower power consumptions can be expected.

This chapter, based on journal [J9], is focused on the technical solution of the contention problem that can arise from packets aiming the same switch port but, firstly, an overview of some of the most preeminent all-optical routing designs, with particular relevance for the ones using SOA-MZI structures, is outlined.

To perform contention resolution, collision is detected and then avoided after wavelength conversion using the push-pull technique, in which the control signals open and close the switching window in the interferometer. The reminiscent power of the blocked packets, due to the non ideal switching performed by the SOA-MZIs, is analyzed in every stage of the routing configuration and the performance transmission is evaluated through BER measurements and extinction ratio analysis.

A 1x2 multi-wavelength optical switching node is also experimentally studied.

4.1. All-optical packet switching

In the last years, some optical packet switching schemes were designed and experimentally validated and the most relevant are discussed, in more detail, below.

4.1.1 State-of-the-art

The setup of a packet switching scheme is shown in Figure 59 and uses an optical flip-flop, based on a single SOA-MZI, with a coupler inside the feedback loop that can be used as an optical packet-forwarding unit, depending on the optical set/reset information [42]. Data flow is forwarded through the flip-flop, without compromise the latching operation. The operation principle of this packet switching scheme is very simple: the packet comes out if the flip-flop is ON, and is blocked otherwise. Accordingly, if a packet is delimited with valid header and trailer, the address recognition module will deliver a Set pulse at the beginning of the packet and a Reset pulse at the end of packet. The first pulse will turn the flip-flop ON and allow the packet to propagate to its destination. The second pulse will turn it OFF so that further packets with invalid addresses are blocked.

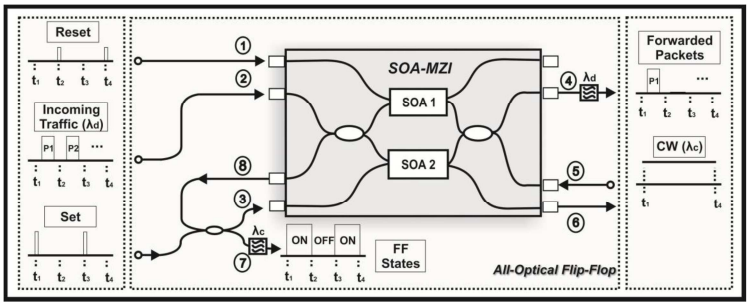


Figure 59 - Packet forwarding gate based on flip-flop [42].

Control signals, generated by label recognition module, toggle the states of the gate in less than 30 ps. These short response times allow the processing of packet-flows with short inter-packet delay and short time-guard between payload and headers/trailer.

An error free operation with two packets at 40 Gb/s, with only 1 dB penalty, was experimentally demonstrated, however, the achieved performances could be greatly enhanced by means of optical integration, that can lead to loop length reduction and thus the pulses duration.

In [69], a wavelength routing structure is proposed, suitable for optical packet switching, in which the packet is routed to a specific port, depending on the AOFF bistable state. Figure 60 illustrates the proposed wavelength routing structure and it comprises a wavelength-tunable source, an optical wavelength converter based on cross-gain modulation in a SOA and an optical demultiplexer.

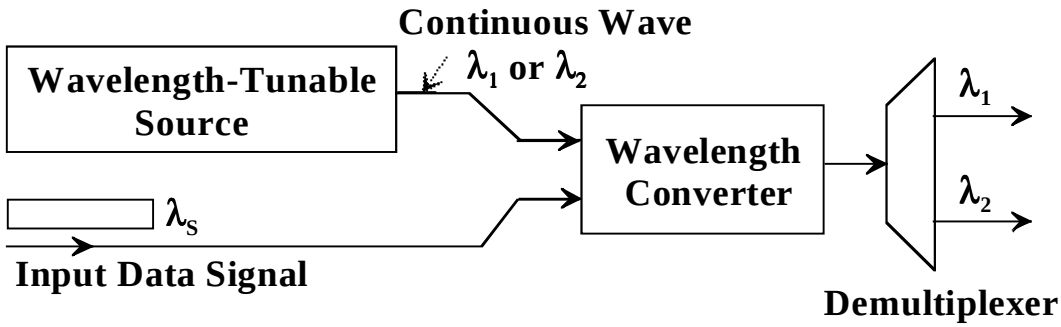


Figure 60 - Basic configuration of wavelength routing subsystem [69].

The wavelength-tunable source is realized using the S-R AOFF, presented in [70], which outputs a CW signal with a tunable and specific wavelength. The CW light controls the optical wavelength converter in order to change the wavelength of the input data signal (80 Gb/s data-packets). The optical demultiplexer consists of a 3 dB coupler and two optical filters, and spatially routes the converted data packets to a specific port. The central wavelengths of the filters are chosen such that in the upper branch, only light with wavelength λ_1 can pass, while in the lower branch, can pass only light with wavelength λ_2. In both branches, inverted wavelength conversion at 80 Gb/s is realized. The inverted signal is injected into a delayed-interferometer to change the polarity of the converted signal (i.e., inverted signal is changed into non-inverted signal). Thus, during the time-slot that the flip-flop outputs light at wavelength λ_1, the wavelength of the data packet is converted into λ_1 and the packet is routed to the upper port. Conversely, if the flip-flop outputs light at wavelength λ_2, the packet is routed to the lower port.

Routing 80 Gb/s data-packets is demonstrated by operating the AOFF dynamically, as shown in figure 61. It is clearly visible that the input packets are routed to different ports when the AOFF toggles between two bistable states. Error-free operation is achieved, and no error-floor is observed, indicating an excellent performance of the wavelength routing system.

In [71], all-optical 10 Gb/s packet switching is achieved, using a SOA-MZI switch and the MMI-BLD optical flip-flop memory, reported in [47] to store the labels. The output of the flip-flop acts as the control signal of the SOA-MZI, which switches the optical packets through cross phase modulation. An error-free operation was obtained, with no error floor.

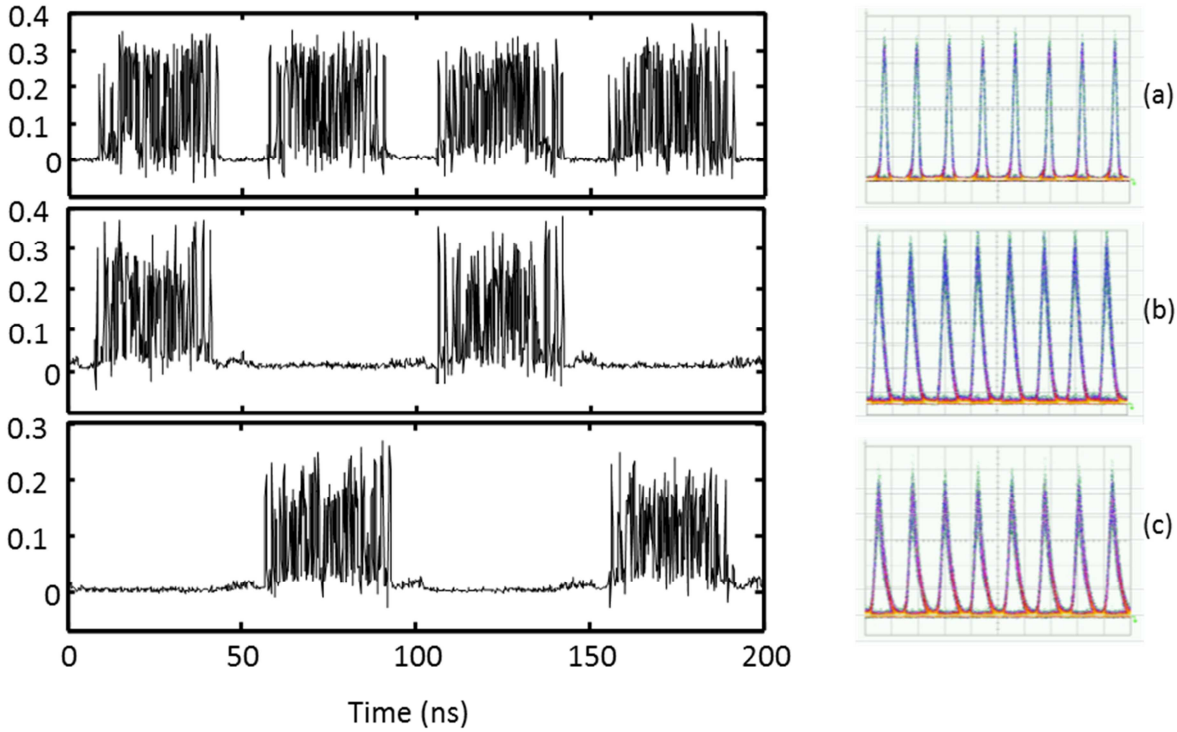


Figure 61 - 80 Gb/s data packets and the associated eye-diagrams. a) Input; b) and c) switch ports. The eye-diagrams are measured by a 700 GHz optical sampling scope [70].

4.1.2 Experimental multi-wavelength optical switching

In a wavelength division multiplexing (WDM) network, multiple optical carriers at different wavelengths can be multiplexed together onto the same fiber, demultiplexed into separated channels by means of optical techniques and sent to the correspondent receiver. Each of the channels present on the WDM fiber can carry any transmission format being the network completely transparent. This technique allows fully exploiting of the large bandwidth offered by the optical fibers. So, essentially, the optical spectrum is used more efficiently. The minimum channel spacing is determined by the inter channel crosstalk and four wave mixing effect. Thousands of Gb/s channels can be transmitted over the same fiber when spaced bellow 100 GHz.

We implemented the 1x2 multi-wavelength optical switching node, depicted in Figure 62, by multiplexing together 10 input wavelengths using DFB laser diodes, modulated to 50 Gb/s PRBS signal (2^{11}-1) by a Mach-Zehnder modulator with the Pulse Pattern Generator (PG).

A DFB laser, centered at 1546.12 nm and modulated at 622Mb/s, was used to generate the header pulse.

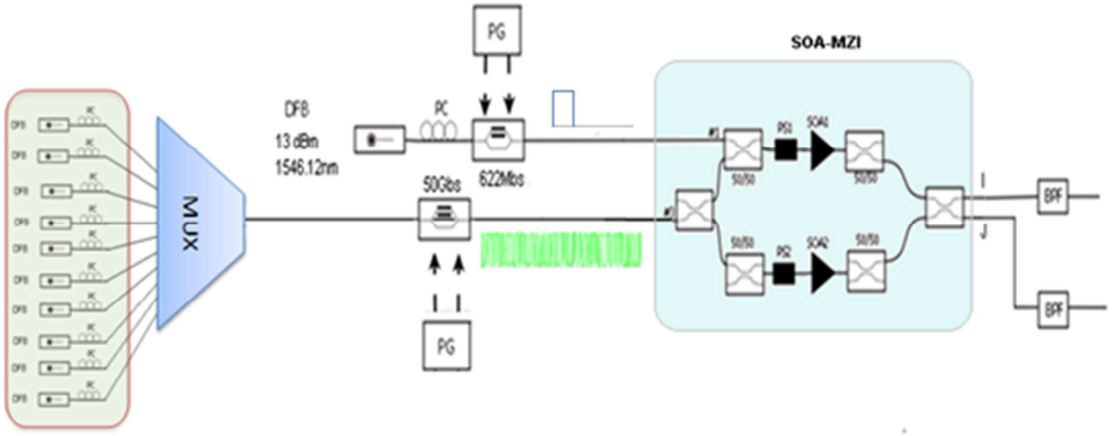


Figure 62 - Experimental setup of a multi-wavelength optical switching node.

Depending on the information of the header, the wavelength-multiplexed optical packet can be forwarded to the appropriate destination port of the wideband optical SOA-MZI switch, according to the truth table of the optical switch (Table 13).

Table 13: Truth table of the optical switch

Header	I	J
0	Packet	0
1	0	Packet

Figure 63 a) and b) show the experimental results obtained at the outputs of the switch, which are a result of an interference process that can be constructive or destructive. We can see in these figures a shift of the output signals, but this occurs only due to the use of different lengths in the fibers connected between the switch outputs and the PIN photodiodes. Although the difficulty in obtaining an exactly π phase shift between the two MZI arms and gain compression, extintion ratios beyond 9 dB were obtained.

a) **b)**

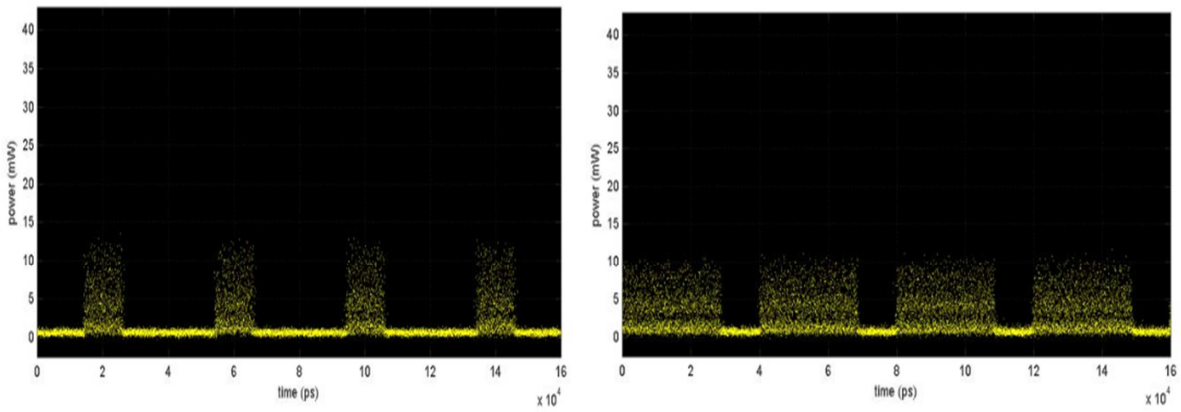


Figure 63 - Experimental results of a multi-wavelength optical switching node. a) at port #J of the switch, b) at port #I of the switch.

4.2. All-optical contention resolution

The all-optical packet switching schemes, presented in 4.1, can forward one packet at any given moment. However, when multiple packets arrive for the same output port, at the same time, contention occurs. All-optical packet contention can be solved in the wavelength, space and time domain. In the wavelength domain, wavelength conversion is needed to prevent the collision of the packets. In the space domain, space deflection provides separate routes, which avoids the contention of the packets. Finally, in the time domain, when packets arrive at the same time, they are routed to different optical delay lines (ODLs) and the collision is avoided [44].

4.2.1 State-of-the-art

In [20], an optical circuit is demonstrated, relying on the hybrid integrated optical flip-flop presented in [18], that performs on-the-fly contention resolution between 40 Gb/s packets of the same wavelength.

Besides the hybrid integrated optical flip-flop, the proposed configuration comprises a SOA-MZI gate and two wavelength converters based on the SOA-filter technique (SOA-OBF). Figure 64 illustrates the diagram of the contention resolution circuit.

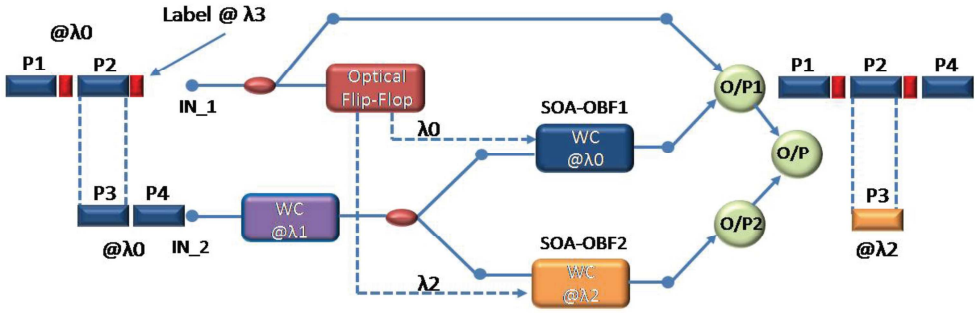


Figure 64 - Contention resolution concept [20].

The scheme makes optimal use of the single flip-flop by using both of its outputs to perform packet-by-packet wavelength conversion either to the original (no contention) or to a new wavelength (contention). Error-free performance was achieved at 40 Gb/s to solve the contention (Figure 65).

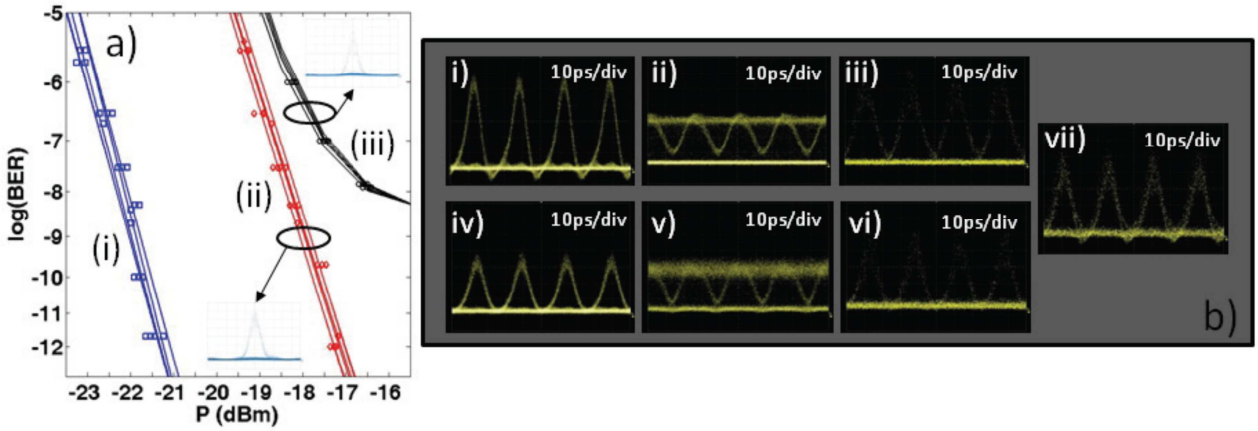


Figure 65 - 17 a) BER curves of i) input packets, ii) output of SOA-OBF_1, iii) output of SOA-OBF_2. b) 40 Gb/s eye diagrams of i) input packets, ii) inverted signal at SOA-OBF_1, iii) non-inverted signal at SOA-OBF_1, iv) output of SOA-MZI WC, v) inverted signal at 1554 WC, vi) O/P2, vii) O/P1 [20].

Another scheme for all-optical contention resolution is proposed in [72], and it takes into account priority information of the data packets. Priority information is transmitted alongside with the packets (pulse = high priority, no_pulse = low priority). Contention is solved at both space and wavelength domain so as to provide additional flexibility: combined with a packet buffer, packet collisions can be avoided for successive contentions.

Figure 66 shows the functional diagram of the proposed contention resolution scheme. The incoming packets are routed by two 1x2 switches (Switch_1 and 2), which are controlled by an AOFF based on[18] and a Packet Envelope Detection circuit (PED). The high priority packets are routed to O/P1 and the contending low priority packets exit from port 5, thus resolving contention

in the space domain. Wavelength-domain contention resolution is obtained at O/P2 via a 160 Gb/s all-optical Wavelength Converter (WC).

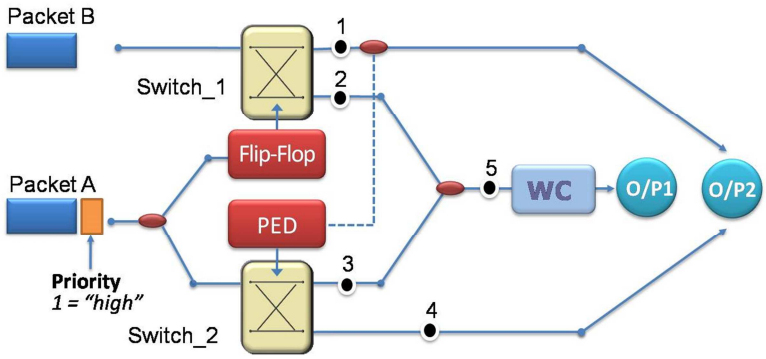


Figure 66 - Block diagram of the contention resolution circuit with priority control [72].

Figure 67 depicts the pulse traces obtained at each stage of the contention resolution scheme. The feasibility of the scheme was validated at 160 Gb/s and error free operation was obtained at all the outputs of the circuit, providing the potential for system-on-chip integration.

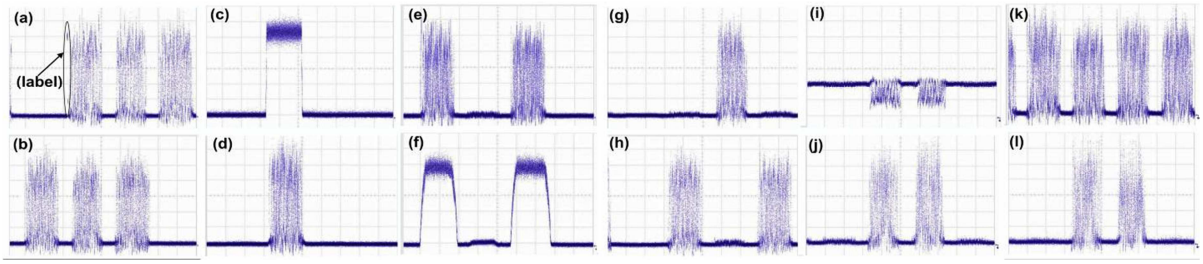


Figure 67 - Experimental results. (a) Packet stream A, (b) packet stream B, (c) flip-flop (d) SOA-MZI_1 (switch 1) switched port, (e) SOA-MZI_1 (switch 1) unswitched port, (f) PED, (g) SOA-MZI_2 (switch 2) switched port, (h) SOA-MZI_2 (switch 2) unswitched port, (j) low-priority contending packets (point 5 of the circuit shown in Fig.66), (k) O/P2, (i) SOA-filter output (inverting WC) and (l) DI output (O/P1). Time scale: 38 ns/div [72].

4.2.2 Experimental analysis of an all-optical packet routing

The effect of the reminiscent power of the blocked packets, due to the non ideal switching performed by the SOA-MZIs, can be an issue in the system performance, since it can be verified in every stage of the router system. Thus, the effect can be cumulative and, consequently, the blocked packets in the router output ports can have amplitude comparable to the unblocked packets or increase the crosstalk effect, degrading the unblocked packets.

We demonstrate experimentally a packet forwarding configuration, with contention resolution

capability based on wavelength conversion. In the proposed all-optical packet routing scheme, two data packets at the rate of 40 Gb/s are introduced in co-propagation way. The header information is stored temporary in a buffer, and depending on the information of the headers, the packets are forward to the appropriate destination port of a 2x2 router.

The reminiscent power of the blocked packets, due to the difficulty in obtaining an exact π phase shift between the MZI arms and gain compression, is analyzed in every stage of the routing configuration

Figure 68 shows the experimental setup of the proposed all-optical packet router based on cascaded hybrid integrated SOA-MZI structures. For practical purposes, only one part of the system is implement so we can easily identify how the traffic at output #1 (OUT1) are affected by the residual cross talk coming from the non ideal switching performed by the SOA-MZIs (the faded SOA-MZI 5 was not experimentally implemented).

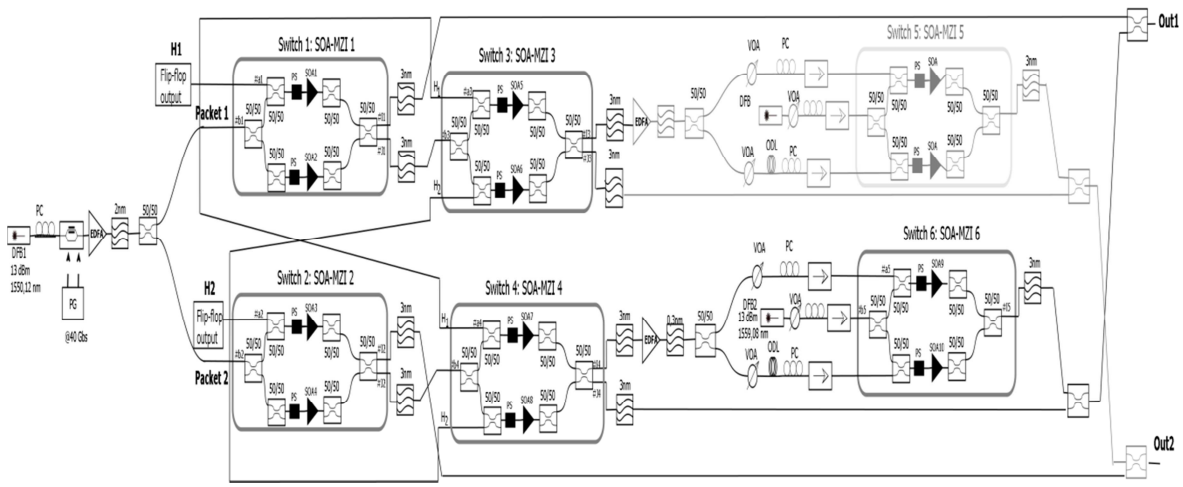


Figure 68 - Experimental setup of the all-optical packet routing.DFB: distributed-feedback laser; PC: polarization controller; MZM: Mach-Zehnder modulator; EDFA: Erbium Doped Fiber Amplifier; ODL: optical delay line; VOA: variable optical attenuator; SOA: semiconductor optical amplifier; PS: phase shifter; PG: pattern generator.

By acting on the SOAs gains, in the polarization controllers and by applying voltage to the phase shifters, the SOA-MZI structures of the system were previously balanced in order to obtain the maximum extinction ratio (ER) possible between the interferometric outputs. In the balancing, ER values of almost 30 dB were achieved.

The all-optical memory block used for holding the packet duration was an S-R flip-flop based on two coupled SOA-MZIs and powered by two continuous wave (CW) signals, at different wavelengths. The optical flip-flop device switches between two states (0 or 1) by injecting set and reset optical pulses into the SOA-MZI that is currently dominant. A DFB laser, centered at 1546.12 nm and modulated at 2.5Gb/s, was used to generate set and reset pulses. Different set and reset

patterns were obtained by dividing and then delaying the signals by 28ns. By toggling between the two bistable states, the flip-flop stores the optical header that controls the appropriate destination port to forward the packets and an extinction ratio of 14 dB was achieved.

In order to generate the optical packet traffic, an external cavity laser, peaking at 1550.12 nm, was used. This pulse train was encoded by a pattern generator, driven at 40Gb/s, with a 2^{11}-1 return-to-zero (RZ) pseudorandom bit sequence (PRBS). After amplification by an erbium-doped fiber amplifier (EDFA), the data packet was split using a 3 dB coupler and finally launched in Switch 1 (SOA-MZI1) and Switch 2 (SOA-MZI2), in co-propagation way.

The experimental waveforms of the optical flip-flop and the optical packet traffic results are presented in Figure 69.

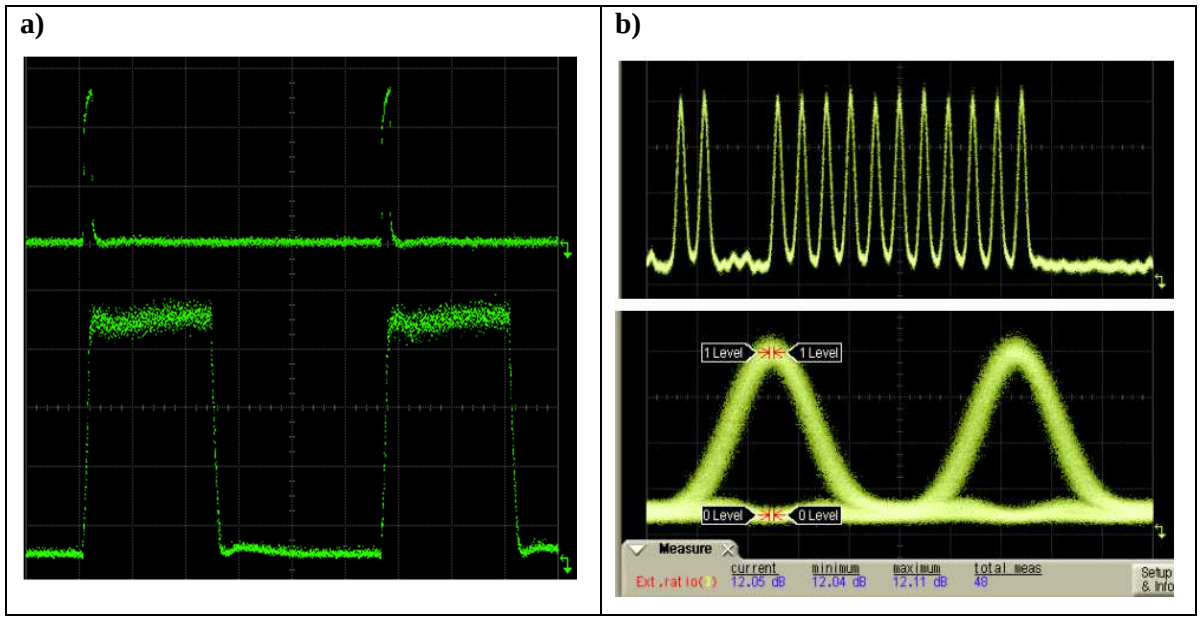


Figure 69 – a) Experimental results of the optical flip-flop based on coupled SOA-MZI. Vertical scale is arbitrary and horizontal scale is 10 ns/div. Upper: Set signal; Down: Optical S-R flip-flop output. b) Optical data packets with a 2^{11}-1 return-to-zero (RZ) pseudorandom bit sequence (PRBS). Upper: characteristic of data sequence; Down: eye diagram of data sequence.

Since the two incoming packet streams can be forwarded to the appropriate destination port of the router depending on the information of the header, different possible scenarios were studied.

Suppose that only packet 1 is injected into port #b1 of Switch 1 with a correlated header, H1=1, injected into port #a1. We refer to this situation as Case 2, being Case 1 the Back to Back measurement. Since the header is correlated, this signal modulates the gain of SOA1, which induces a modulation of its refractive index. Therefore, data packet 1 suffers different gains and phase shifts in the upper and in the lower arms of the MZI, which lead to the unbalance of the

SOA-MZI1. In this case, packet 1 is switched to its corresponding bar-port (port #I1) and, consequently, emerges directly to Out1 router output.

In case 3, we consider two packets (packet 1 and packet 2) with correlated headers (H1=1 and H2=1). Again, due to the presence of the header signals, SOA-MZI1 and SOA-MZI2 will be unbalanced, therefore packet 1 and packet 2 will be forwarded to their bar-ports and therefore routed to different output ports: Packet 1 goes out in Out1 and Packet 2 goes out in Out2. However, due to the non ideal switching performed by the cascaded SOA-MZIs, a small part of the not perfectly blocked packet 2 reaches Out1 with some reminiscent power, which can degrade the output signal.

Another situation occurs when the two packets have both headers uncorrelated (H1=0 and H2=0), which corresponds to Case 4. In this case, packet 2 will be evenly amplified by both SOAs (SOA3 and SOA4) and will recombine at the output of the interferometer destructively (port #I2) and constructively (port #J2). In this situation, SOA-MZI2 is balanced. Therefore, packet 2 is forward through another SOA-MZI stage (SOA-MZI4) and will cross the router architecture, going out in Out1. In the same way, packet 1 will cross the router, going out in Out2. However, Out1 will also suffer the influence of the residual of packet 1 due to the non ideal switching performance of SOA-MZI1 so there is still a reminiscent power of packet 1 passing and mixing with packet 2.

If only one header is correlated, both packets are addressed to the same output port, at the same time. When this happens, packet collision must be detected and avoided. In the particular case of H1=1 and H2=0 (Case 5), packet 1 goes out directly in Out1 output port. However, packet 2 will cross Switch 2 (SOA-MZI2) and then reaches to SOA-MZI4, which decides that packet 2 should be wavelength converted due to the existence of the correlated header of packet 1. The collision is solved in wavelength domain using the push-pull technique in order to further reduce the transmission switching window. The specific technique is demonstrated by splitting in two the optical modulated signal launched in the control ports of the SOA-MZI6 (differential mode). One of these control signals has an additional delay and attenuation when compared to the other control signal. The switching window is dependent upon the pulse duration and the time delay between the two control pulses. In this situation, at OUT1 go out packet 1, a residual of packet 2 at the same wavelength of packet 1(λ=1550.12 nm) and the wavelength converted packet 2, at 1559.08nm. Figure 70 illustrates how the packets flow at the routing system in Case 5. Since packet 1 and packet 2 have the same wavelength (represented in the color green in Figure 70), it can be seen that both packet will collide at Out1 port. So, it is clear the reason we need to perform a wavelength conversion at SOA-MZI 6 to prevent the collision of the packets.

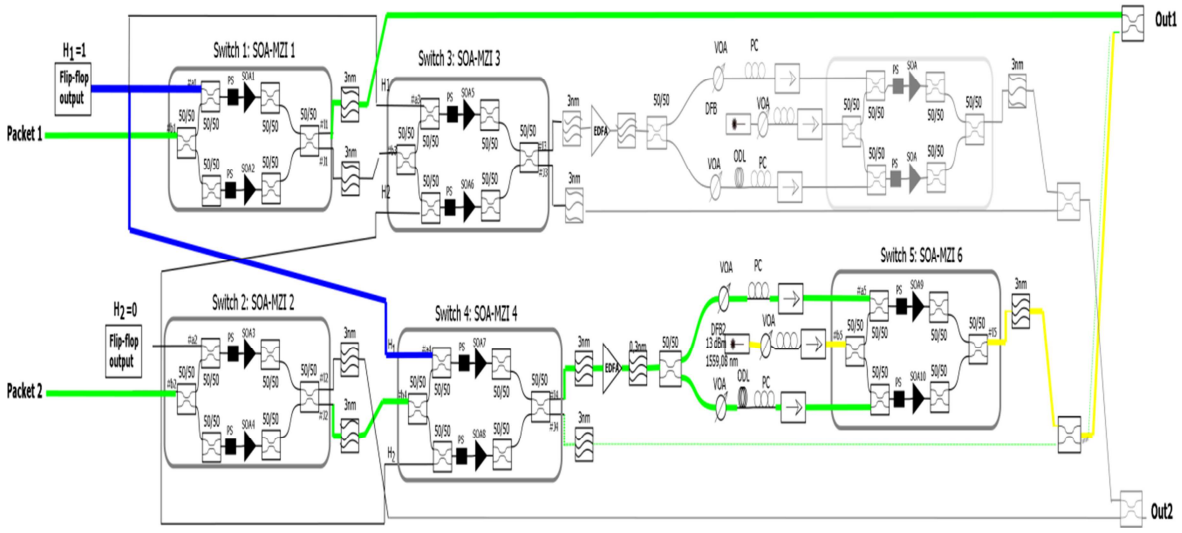


Figure 70 – Packet traffic in a routing system.

In Figure 71 is depicted the BER curves as function of the received power measured at Out1 and the respective eye diagrams, for all the presented routing cases (Case 1- Case 5). The received power was adjusted with a variable attenuator before amplification and detection of the signal. Finally, the detector output was evaluated through bit-error ratio (BER) measurements at 40 Gb/s.

Performance deterioration is observed as consequence to the non-ideal switching performed by the SOA-MZI routing cascade. Namely, the expected packet routed to OUT1 is affected by crosstalk from the not expected packet, still present as residual signal which is not totally suppressed by the SOA-MZI switching operation.

Cases 2 and 3 represent the straight forwarding operation of packet1 which is sent to output 1. With respect to the B2B case and the error free condition (BER=10^-9), these first two cases report a power penalty of about 3 dB due to the non-ideality of SOA –MZI 1 operation. A residual coming from the lower arm is responsible for a slightly higher power penalty for case 3. Regarding the following case 4, corresponding to the crossing operation, the expected packet undergoes not just a single SOA-MZI stage (as the previous ones) but a SOAs-MZI cascade. This condition results in further deterioration accounted, again, together with the residuals presence on output 1. Last case 5 is the contention resolution case, here we find the impact on power penalty mainly due to the not wavelength converted contribution from packet 2.

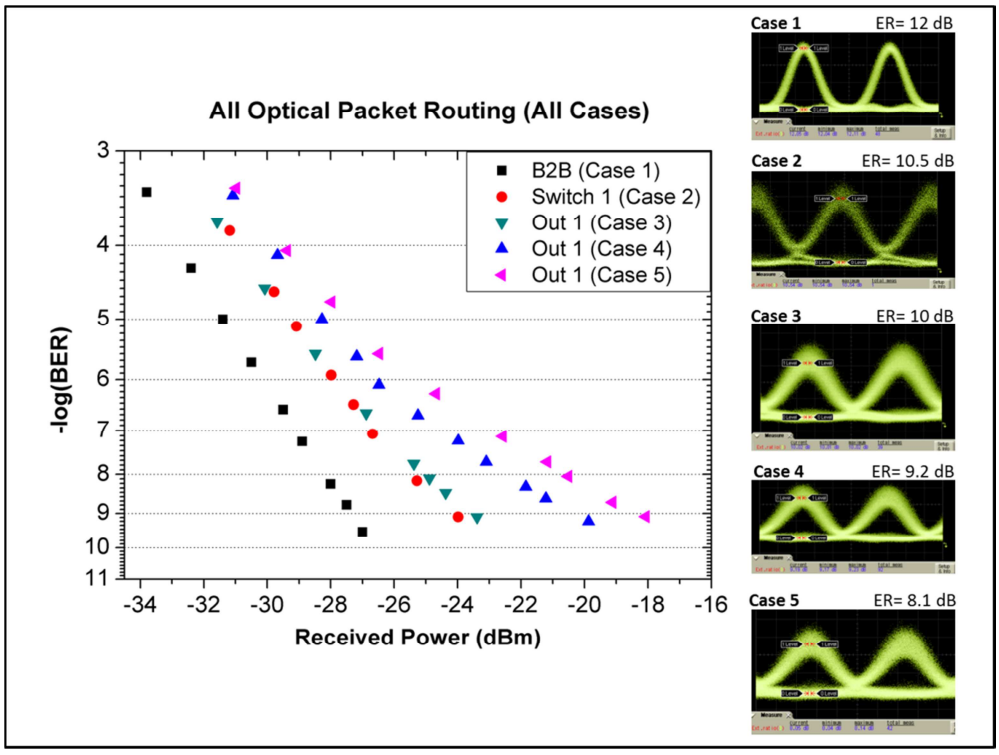


Figure 71 - BER measurements as function of received power measured at output port #1 (Out 1). Insets: Eye-diagrams measured at Out_1 for each analyzed case.

4.3. Conclusions

This chapter has presented an overview of all-optical packet routing using mostly SOA-MZI structures. These routing configurations have been divided in two groups based on their ability to forward one or more packets at any given moment.

We also addressed the experimental implementation of an all-optical packet routing scheme, with contention resolution capability, using interconnected SOA-MZIs. Since the data packets can be forwarded to the appropriate destination port of the router depending on the information of the header, different possible scenarios were studied. The reminiscent power of the blocked packets, due to the non ideal switching performed by the SOA-MZIs, was also analyzed through extinction ratio analysis and BER measurements, in every stage of the routing configuration, since this effect can be cumulative.

Chapter 5

Conclusions and future work

The increase of traffic load and the well known limitations of the electronic routers lead to a new interest of the transmission capacity of optical fibers. The advances on optical integration techniques is making possible that optical packet switching become a reality, and in the next years we believe that all photonic routers can be commercially available.

5.1 Conclusions

The objective of this thesis work plan was to investigated and developed essential functionalities for all-optical signal processing and photonic switching. The work developed was mostly based on SOA-MZI structures due to their inherent characteristics such as, high extinction ratio, high operation speed, high integration capability and compactness.

The basic building block of any processing system, electrical or optical, is the logic gate since it is a fundamental element for the development of complex processing functionalities. In particular, optical gates are capable to perform Boolean logic operations at high data bit rates not allowed for their electronic counterparts**.**

In the first part of this work, novel solutions to perform optical logic operations were proposed. The presented optical combinational circuits differ from the traditional ones, since instead of offering a single output, we take advantage of the two output ports of a SOA-MZI based interferometric switch, obtaining in this way multi-output logic functions. Logical operation using a single SOA-MZI switch is an attractive technology due to the small size and low power consumption of the device. The first proposed logical scheme was simulated and experimentally demonstrated, showing the operation of four all-optical logic gates, based on a single hybrid integrated SOA-MZI, and using NRZ-OOK modulated signals driven at 10 Gbit/s as control signals. Their operation principle was explained through the analysis of the truth table and a black box model for operational point optimization. Extinction ratio values in order of 10 dB were obtained.

Regarding this research topic, it was also proposed for the first time, to our knowledge, a configuration that provided 16 optical logic operations, based on a single MZI with controlled phase modulators in each arm, without changing the setup scheme. Using this single unit configuration, a more complex circuit, based on three cascaded MZIs was designed. This complex circuit consisted on one optical data input and four optical outputs. The control signals created a phase difference in the circuit, which allowed optical data to be directed to the selective output.

The behavior of an all-optical logic XOR gate based on a SOA-MZI was also assessed in terms of the way the incoming signal is injected (co or counter propagation). We conclude that for both co- and counter-propagation schemes, the performance of the XOR gate is almost independent of the input power, since the power variation of the two data signals involved in the comparison is the same. However, the counter-propagation scheme showed a better performance, with a slightly improvement on the extinction ratio.

The second topic discussed in this PhD work was the optical memory elements, especially the ones that work with a synchronization signal. We demonstrated novel techniques to construct all-optical flip-flops and their applications in all-optical packet switching schemes. In particular, we proposed and experimentally demonstrated two synchronous bistable schemes based on two coupled SOA-MZIs and additional combinational logic circuits. To our best knowledge, these were the first demonstration of all-optical clocked flip-flops, using SOA-MZI structures.

A performance comparison of the up-to-date all-optical flip-flops design schemes was evaluated based on experimental results in terms of commuting speed, switching energy and integration capability. We concluded that the optical one-bit memories require, in general, low energies to operate, without compromising state integrity, and have potential high operation speed, making them suitable for future optical packet switching networks.

We also proposed and demonstrated, through numerical simulations, the performance of an all-optical S-R flip-flop, using two gain-clamped RSOAs, that can be integrated with planar semiconductor technology. This optical flip-flop configuration presents a cavity with small millimeters and by using few components, it reduces the complexity.

To finalize this topic, an all-optical clocked D flip-flop based on a single SOA assisted symmetric MZI was also proposed. The bistability of this optical flip-flop was imposed by an external feedback loop between the output Q and the input. The loop presented an optical delay line and an optical attenuator, in order to synchronize and to equalize the power of the input data signals that enter in the circuit from interferometric ports. The objective of the feedback loop was to maintain the flip-flop's previous state, in the absence of the clock input signal. Depending on the internal phase condition of the interferometer, we obtained different logic values at the flip-flop output.

The last subject discussed in this work addressed the experimental implementation of an all-optical packet routing scheme, with two contention free outputs, using interconnected SOA-MZIs. The main target of this research topic was to assess the impact on the system performance of the reminiscent power of the blocked packets from the non ideal switching performed by the SOA-MZIs. This effect can be an issue in the system performance, since it can be verified in every stage of the router system. Thus, it can be cumulative and, consequently, the blocked packets in the router output ports can have amplitude comparable to the unblocked packets or increase the crosstalk effect, degrading the unblocked packets. The performance transmission was experimentally evaluated through BER measurements and extinction ratio analysis.

5.2 Directions for Future Work

This PhD work focused on the investigation and development of digital functions for the next generation photonic transmission systems. From this work, several investigations can be conducted in future studies, namely:

- All the main building blocks of the proposed synchronous flip-flops were based on hybrid integrated SOA-MZIs however, the interconnection between the blocks were, experimentally, implemented using discrete fiber pigtailed, which affects the switching behavior. Although, we achieved switching speeds in order of picoseconds and extinction ratios beyond 10 dB, a complete integration would enhance the performance and reduce the device size.

- Experimental demonstration of our all-optical clocked D flip-flop based on a single SOA assisted symmetric MZI could also be interesting. The main challenge of the experimental setup could be the difficulty to maintain comparable the feedback loop length with the gain recovery time of the SOAs.

- Logic gates are the key devices for the majority of all-optical signal processing applications and they are far from being a closed-topic. Silicon photonics, photonic crystals, quantum dot, among other technologies, can bring a new age for the development of novel devices in terms of cost and performance integration in more complex functions.

- The impact how the reminiscent power of the blocked packets (due to the non ideal switching performed by active MZIs) affect the routing performance could be assessed, quantitatively, using different advanced modulation formats.

- Although an all-optical random access memory (RAM) has already been proposed in [60], the development of an optical memory element that can replace the functionality of the electronic RAM remains one of the most important missing links in the development of photonic computation. Today, commercially available all-optical computer are still very far from short-term implementation and is still considered idealistic.

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