



**Henrique António
Magalhães Martins
Antão**

**Modelação física do compressor audio UREI
1176LN**



**Henrique António
Magalhães Martins
Antão**

**Modelação física do compressor audio UREI
1176LN**

Dissertação realizada na Technical University of Hamburg sob o regime de Mobilidade para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Electrónica e Telecomunicações, realizada sob a orientação científica do Prof. Dr. Udo Zölzer, Professor da Helmut Schmidt University e do Prof. Dr. José Vieira, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

o júri / the jury

presidente / president

Prof. Dr. Udo Zölzer

Professor at Helmut-Schmidt-University / Guest lecturer at Technical University of Hamburg

vogais / examiners committee

Prof. Dr. José Vieira

Professor Auxiliar at Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro

M.Sc Marco Fink

Research Assistant at Helmut-Schmidt-University

Resumo

As novas tecnologias digitais são constantemente aclamadas como mais um passo em direcção à perfeição. No entanto, no campo das tecnologias da área da música, este paradigma é muitas vezes questionado uma vez que é comum encontrar novas aplicações tentando replicar sistemas analógicos antigos.

Este projeto de tese propõe-se a investigar a aplicação de um método de modelação física derivado da análise de circuitos analógicos e modelação de dispositivos eletrónicos não-lineares para simular com mais precisão sistemas analógicos que ao longo da história da produção musical continuam a gerar interesse. Utilizando como objecto de estudo o compressor de gama dinâmica de nome UREI 1176LN, aplicou-se nesta dissertação o método Nodal DK em circuitos audio de controlo de gama dinâmica para implementar uma simulação digital do mesmo.

Os resultados da implementação são posteriormente comparados com gravações audio retiradas de um protótipo do circuito construído durante o período deste projeto.

Abstract

New digital technology is constantly hailed as another step towards perfection yet this paradigm is being questioned in the music technology field, where new tools attempt at replicating old technology. This thesis project proposed to investigate the application of a physical modeling method derived from analog circuit analysis and modeling of non-linear electronic devices to more accurately simulate vintage circuits that have generated increasing demand throughout the history of music production. For this matter, a popular Dynamic Range Compressor by the name UREI 1176LN was chosen as a case study for application of the Nodal DK Method to Dynamic Range Control audio circuits. The results of the implementation are compared to audio recordings taken from a circuit prototype built during the time of this thesis.

Statement

Hereby I do state that this work has been prepared by myself and with the help which is referred within this thesis.

Henrique Antão
Hamburg, February 13th 2014

Foreword

The work presented here was developed in the Department of Signal Processing and Communication in the Helmut-Schmidt University Hamburg, as a guest student from the Technical University Hamburg-Harburg and as an exchange student from Universidade de Aveiro, Portugal.

I would like to express my gratitude towards Prof. Udo Zölzer for allowing me to develop a thesis on a field that I'm very fond of. Same goes for my supervisor Dipl.-Ing. Marco Fink for his infinite patience and support. I am also grateful to Felix and Sebastian for always being present when help was needed, Dr.-Ing Martin Holters for his input and suggestions and all the lab colleagues that made this research a more pleasant experience. I would also like to thank Prof. José Vieira from my home university for showing interest in my work and assisting me along the way. Lastly, I can't forget the support of my family and friends who, during this time, provided me with constant encouragement without which it would have been difficult to complete my studies.

Hamburg, February 12th 2014

Contents

List of Figures	xi
List of Tables	xv
List of Sourcecodes	xvii
List of Symbols	xix
1 Introduction	1
1.1 Motivation	1
1.2 Structure of the Thesis Project	2
2 Dynamic Range Compression	3
2.1 Fundamentals	5
2.1.1 Signal Flow	5
2.1.2 Static Curve	6
2.1.3 Dynamic Behaviour	8
2.2 UREI 1176LN	8
2.2.1 Theory of Operation	10
3 Circuit Modeling	15
3.1 Device Models	15
3.1.1 Diode	15
3.1.2 Bipolar Junction Transistor	17
3.1.3 Junction Field-Effect Transistor	20
3.2 State-space Representation of Non-linear Systems	23
3.3 Nodal DK Method	25
3.3.1 Discretization of Energy-storing Elements	25
3.3.2 Matrix Description of the Circuit	26
3.3.3 Non-linear Iterative Solver	30
4 Implementation	33
4.1 Parameter Extraction	33
4.1.1 Measurement System	33
4.1.2 Diode	34
4.1.3 Bipolar Junction Transistor	37
4.1.4 Junction Field-effect Transistor	38
4.2 Circuit Prototype	41
4.2.1 Component Measurement	41
4.2.2 Circuit Calibration	42
4.3 State-space Implementation	42

4.3.1	Circuit Simplifications	42
4.3.2	Adaptations for Nodal DK Method	43
4.3.3	State-space Model	44
4.3.4	User Controls	46
4.3.5	Calibration	48
5	Results and Evaluation	49
5.1	Parameter Extraction Results	49
5.1.1	Diode Parameters	49
5.1.2	BJT Parameters	51
5.1.3	JFET Parameters	56
5.2	Simulation Results	58
5.2.1	DC Analysis	58
5.2.2	Static Curve	60
5.2.3	Audio Tests	61
6	Conclusion and Future work	69
A	Measured Components	71
B	Matrix Model	73
C	Sourcecodes	75
	List of Abbreviations	87
	List of Software	89
	Bibliography	91

List of Figures

2.1	Dynamic range of typical audio signal.	3
2.2	Block diagram of the two compressor topologies.	5
	(a) Feedback topology	5
	(b) Feed-forward topology	5
2.3	Static curve of the UREI 1176LN compressor [10].	6
2.4	Typical compression applied to music.	7
	(a) Before compression	7
	(b) After compression	7
	(c) After make-up gain	7
2.5	Universal Audio 1176LN.	9
2.6	Block Diagram of the UREI 1176LN.	10
2.7	Voltage-variable Resistor Attenuator.	10
2.8	Signal Preamplifier.	11
2.9	Gain Reduction Control Amplifier.	12
2.10	Line Amplifier.	13
3.1	Ideal diode current-voltage relation.	16
3.2	Diode Representation.	17
	(a) Circuit representation for ideal diode	17
	(b) Equivalent representation	17
3.3	An npn BJT.	17
	(a) Basic semiconductor structure [14]	17
	(b) Circuit representation	17
3.4	Ideal characteristic curve of a BJT in the forward active region with different base currents.	18
3.5	Equivalent circuit diagram of a BJT [13].	19
3.6	Ideal relation between V_{GS} and I_D of a JFET.	20
3.7	An n-channel JFET.	21
	(a) Basic semiconductor structure [14]	21
	(b) Circuit symbol representation	21

3.8	Equivalent circuit diagram of the JFET.	21
3.9	Forward current-voltage characteristic of the JFET.	22
3.10	Block diagram of the K method.	24
3.11	Equivalent circuit diagram of a capacitor.	26
3.12	Example of the Newton's Method application.	30
4.1	Diagram of the measurement system.	33
4.2	Semi-logarithmic plot of I-V characteristic of an ideal diode.	34
4.3	Test circuit for I-V measurements of the diode.	35
4.4	Test circuits for extracting the Shockley equation parameters of the BJT.	37
	(a) Base-emitter junction test circuit	37
	(b) Base-collector junction test circuit	37
4.5	Test circuit for extracting the current gain of the BJT.	38
4.6	Test circuit for extracting the threshold voltage of the JFET.	39
4.7	UREI 1176LN circuit prototype.	41
4.8	Compression Ratio push-buttons implementation.	43
	(a) Original implementation	43
	(b) Simplified implementation as a resistor switch	43
4.9	Substitution of potentiometer to avoid floating nodes [26].	44
4.10	Circuit schematic to be implemented as a state-space model.	45
4.11	Front view of the Universal Audio 1176LN.	46
5.1	Semi-logarithmic plots of I-V characteristics of diodes D1 and D2.	50
	(a) Diode D1	50
	(b) Diode D2	50
5.2	I-V characteristics of diodes D1 and D2.	50
	(a) Diode D1	50
	(b) Diode D2	50
5.3	Residual error of the diode device model.	51
	(a) Diode D1	51
	(b) Diode D2	51
5.4	Semi-logarithmic plots of I-V characteristics of each junction in the BJT.	52
	(a) Base-emitter junction of 2N3391 BJT	52
	(b) Base-collector junction of 2N3391 BJT	52
	(c) Base-emitter junction of 2N3707 BJT	52
	(d) Base-collector junction of 2N3707 BJT	52
5.5	I-V characteristics of each junction in the BJT.	53
	(a) Base-emitter junction of 2N3391 BJT	53

(b)	Base-collector junction of 2N3391 BJT	53
(c)	Base-emitter junction of 2N3707 BJT	53
(d)	Base-collector junction of 2N3707 BJT	53
5.6	Forward current gain of the BJT.	53
(a)	2N3391	53
(b)	2N3707	53
5.7	I-V characteristics of the BJT.	55
(a)	2N3391	55
(b)	2N3707	55
5.8	Residual error of the BJT device model.	55
(a)	2N3391	55
(b)	2N3707	55
5.9	Gate characteristic of the 2N5457 JFET.	56
5.10	I-V characteristics of the 2N5457 JFET for $V_{GS} = 0$ V.	56
5.11	I-V characteristics of the 2N5457 JFET.	57
(a)	Against V_{GS}	57
(b)	Against V_{DS}	57
5.12	Residual error of the JFET device model.	58
(a)	Against V_{GS}	58
(b)	Against V_{DS}	58
5.13	Comparison of measured (dashes) and simulated (line) static curve	60
5.14	Waveforms of original uncompressed bass guitar and prototype and simulation results.	62
(a)	Original.	62
(b)	Prototype.	62
(c)	Simulation.	62
5.15	Residual of prototype and simulation bass guitar test results.	63
5.16	Waveforms of original uncompressed vocal track and prototype and simulation results.	64
(a)	Original.	64
(b)	Prototype.	64
(c)	Simulation.	64
5.17	Residual of prototype and simulation vocal test results.	64
5.18	Waveforms of original uncompressed drum track and prototype and simulation results.	66
(a)	Original.	66
(b)	Prototype (Example 1).	66
(c)	Simulation (Example 1).	66

(d) Prototype (Example 2).	66
(e) Simulation (Example 2).	66
5.19 Residual of prototype and simulation drum test results.	67
(a) Example 1.	67
(b) Example 2.	67

List of Tables

4.1	Parameters of the user controls.	47
4.2	Parameters of the Compression Ratio push-buttons	47
5.1	Extracted parameters of diodes D1 and D2.	50
5.2	Extracted parameters of the BJTs.	54
5.3	Extracted parameters of the 2N5457 JFET.	57
5.4	JFET DC voltages and absolute difference between measured and simulated results in V.	58
5.5	BJT DC voltages and absolute difference between measured and simulated results in V.	58
5.6	Diode DC voltages and absolute difference between measured and simulated results in V.	59
5.7	Results of compression ratios.	60
5.8	User control settings for bass guitar track test.	61
5.9	User control settings for vocal track test.	63
5.10	User control settings for drum track test.	65
A.1	Measured values of the resistors used in the circuit prototype and state-space implementation	72
A.2	Measured values of the capacitors used in the circuit prototype and state-space implementation	72
A.3	Measured values of the potentiometers used in the circuit prototype and state-space implementation	72
A.4	Measured resistance values of the overall resistor ladder switch formed by the Compression Ratio push-buttons	72
C.2	List of Software.	89

List of Sourcecodes

4.1	Parameter extraction script for the Shockley diode equation parameters (Step 1).	35
4.2	Parameter extraction script for the Shockley diode equation parameters (Step 2).	36
4.3	Parameter extraction script for the Shockley diode equation parameters (Step 3).	36
4.4	Non-linear equations of the diode for the non-linear solver.	37
4.5	Non-linear equations of the BJT for the non-linear solver.	38
4.6	Parameter extraction script for the threshold voltage of the JFET.	39
4.7	Non-linear equations of the JFET for the non-linear solver.	40
C.1	Circuit model of the UREI 1176LN.	75
C.2	Simulation script of the UREI 1176LN.	83

List of Symbols

dB	Decibel
I_D	Diode current
I_S	Saturation current
V_D	Diode voltage
k	Boltzmann constant
T	Temperature
q	Electron charge
n	Emission coefficient
V_T	Thermal voltage
B	Base
C	Collector
E	Emitter
I_F	Forward current
I_R	Reverse current
I_{ES}	Emitter saturation current
I_{CS}	Collector saturation current
V_B	Base voltage
V_C	Collector voltage
V_E	Emitter voltage
V_{BE}	Base-emitter voltage
V_{CE}	Collector-emitter voltage
V_{BC}	Base-emitter voltage
I_B	Base current
I_C	Collector current
I_E	Emitter current

α_F	Forward current gain of common-base BJT
α_R	Reverse current gain of common-base BJT
β_F	Forward current gain of common-emitter BJT
β_R	Reverse current gain of common-emitter BJT
V_A	Early voltage
D	Drain
S	Source
G	Gate
V_{GS}	Gate-source voltage
V_{DS}	Drain-source voltage
V_{GD}	Gate-drain voltage
V_{Th}	Threshold voltage
V_P	Pinch-off voltage
I_G	Gate current
I_D	Drain current
I_{GD}	Gate-drain current
I_{GS}	Gate-source current
I_{DSS}	Saturated drain current
V_{rms}	RMS voltage

Chapter 1

Introduction

In the last thirty years, consumer electronics have seen a shift of paradigm from analog to digital, and while there has been time enough for newer technology to prove it's worth, certain fields seem to raise demand for outdated standards. When it comes to music technology, a lot of focus remains on the topic of analog versus digital and while certain factors such as lower production cost or product portability play a big role in driving the industry, other arguments like the superior noise performance of digital systems fall to personal preference.

Today's society consensually accepts the widespread idea that the introduction of new digital technology represents always an improvement towards perfection yet more and more we see digital technology aiming at replicating older equipment. Often terms like "warm" or "fat" are used to describe the sound of analog equipment and this could only make sense when one's referring to the natural distortion these systems carry. For this reason, often software implementations try to include the same noise that made analog special, a curious contradiction if one takes in consideration that the advent of digital technology was greatly motivated by its ability to overcome such issues [1].

The resurgence of vintage equipment is many times justified on the basis of feelings of nostalgia or cultural trends but such reducing arguments don't take into account that the mere sonic characteristic of the vintage technology plays the major role in such phenomena [2]. The non-linearities of the analog are the reason each piece of equipment has its characteristic sound and why some are still in high demand in today's digital world. It is also where the biggest challenge of digital audio solutions arises: to accurately simulate the behavior of these non-linear systems.

1.1 Motivation

The demand that vintage audio equipment is still able to generate in the current days, where certain out-of-production items go for outstanding amounts in the second-hand market, is certainly responsible for the increasing interest in the development of new digital tools that aim at producing the same high quality sonic characteristic.

In an age where professional studios had long accepted the new paradigm and are today fully equipped with professional standard audio interfaces, and where it was never so easy for musicians to own a home studio, it is obvious that a vintage sounding digital implementation of

these circuits would gather a wide market acceptance. Not only such implementations provide musicians and recording engineers a more portable version of their needs, but also more flexibility when it comes to edit recorded material. Another advantage is the predictive behaviour of such systems, where no electronic faults are to be expected as such to require service assistance and tedious debugging. On the contrary, they provide the user with a product which lifetime is only defined by the progress of digital processors. Such progress enables more realistic simulations, leading the focus into the achievement of a vintage sound that will please everyone.

Many commercial products have been loudly advertised as having achieved this but these are purely subjective claims that lack scientific basis and results are often unsatisfactory to experienced musicians who have made significant use of the analog equipment.

This thesis focus on the application of a physical modeling method that is derived from the analog circuit analysis and the appropriate modeling of the non-linear electronic components that provide the distinct behavior of the unit. These can be usually diodes, bipolar or field-effect transistors, valve tubes or transformers, and by obtaining the non-linear currents these elements generate we can apply a white-box approach [3] to the overall circuit, where Kirchoff's Current Law (KCL) and Kirchoff's Voltage Law (KVL) provide the basis for its analysis. This approach takes as reference the previous works based on this implementation that have been published in [4] [5].

As a case study, this work aims at investigating the simulation of a Dynamic Range Compressor, an effect discussed more thoroughly in the further chapter, and takes as reference the circuit of the UREI 1176LN unit, a classic compressor prasiad throughout the history of modern professional music studios.

1.2 Structure of the Thesis Project

This thesis project is structured as follows:

- Chapter 2 attempts at describing a dynamic range control effect known as Dynamic Range Compression, introducing fundamental concepts as well as the analog unit subject to physical modeling throughout this work and its operation;
- Chapter 3 presents theory aspects behind device modeling, focusing on the non-linear devices used in the circuit in study, and introduces the topic of state-space representation of non-linear systems, with a description of the Nodal DK method;
- Chapter 4 deals with the implementation of parameter extraction methods used to accurate simulate the devices in hand, as well as the presentation of a built circuit prototype and further considerations in the application of a state-space model.
- Chapter 5 presents the results of parameter extraction methods for the non-linear devices used in the circuit, as well as results of the state-space implementation of the circuit, focusing on DC analysis, the static curve of the compressor and comparing audio tests performed both on the circuit prototype and simulation.
- Chapter 6 presents an overview of the work performed and concludes this thesis project with suggestions for further improvements in studies on this subject.

Chapter 2

Dynamic Range Compression

The dynamic range of a signal is defined as the difference between its maximum and minimum Sound Pressure Levels (SPL) (Fig. 2.1), expressed in dB. Its typical values span over the range of 40 to 120 dB [6].

Dynamic Range Compression (DRC) consists in reducing the dynamic range of an audio signal. The basic principle is to automatically attenuate the louder parts of the signal, making them closer to the quieter parts.

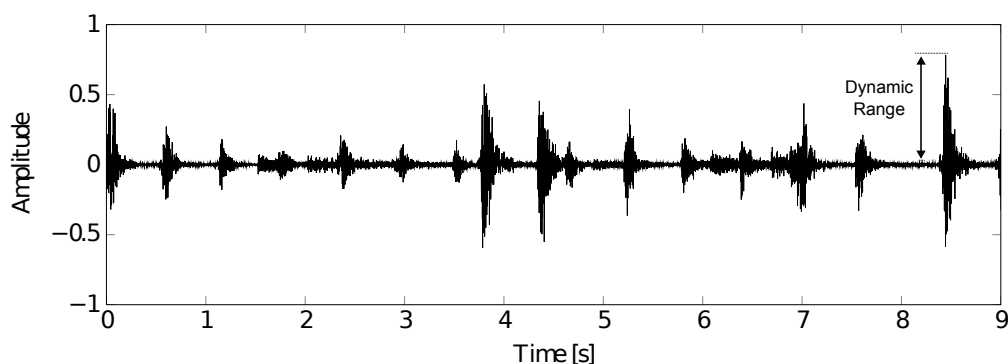


Figure 2.1: *Dynamic range of typical audio signal.*

Such effect came to find most of its relevance in modern music production, but it fits a wider and more general range of application. In broad terms, DRC is required in order to fit the dynamic range of a source material to the different requirements of listening equipment, recording mediums or reproduction environments.

This technique was proposed in 1934 as a way to improve telephone line transmission against static noise by reducing the range of the speech intensity at the transmitter end [7]. In broadcasting stations, it allows for a louder transmission while keeping the same signal peak amplitude. The same application can benefit sound reproduction in noisy environments such as restaurants, cars or shopping centers, where softer parts of the sound can be overshadowed by background noise. In recording and mastering applications, it can be used to prevent overload of AD converters or to fit the source material to the dynamic range of storage mediums as vinyl or CD.

However, most of its popularity arises from its use in modern music production studios, where it is critical to apply compression to different instrument and vocal tracks, in order to achieve a consistently balanced mix. This becomes more apparent if one takes as example the recording of a singer with a wide vocal range and a varying distance to the microphone, where the level variation becomes critical and softer passages of his voice may be drowned out by other instruments making the lyrics harder to understand. DRC comes in hand in avoiding such problems by making the vocals level more consistent throughout the song (i.e., reducing the singers dynamic range).

2.1 Fundamentals

2.1.1 Signal Flow

The basic operation behind Dynamic Range Compression is derived from two main steps:

1. Level sensing,
2. Varying-gain control

These two steps are accomplished in separate circuit blocks and form the fundamental architecture of any dynamic range compressor, linking a varying-gain amplifier and a level detector. In the main signal path, audio is amplified by a low noise and low distortion gain stage while in parallel a level detector circuit senses its envelope and converts it into a control voltage. In return, this control voltage is used to vary the amount of gain of the amplifier.

This can be achieved in two different topologies, where the main difference relies on when to sense the signal from the audio path.

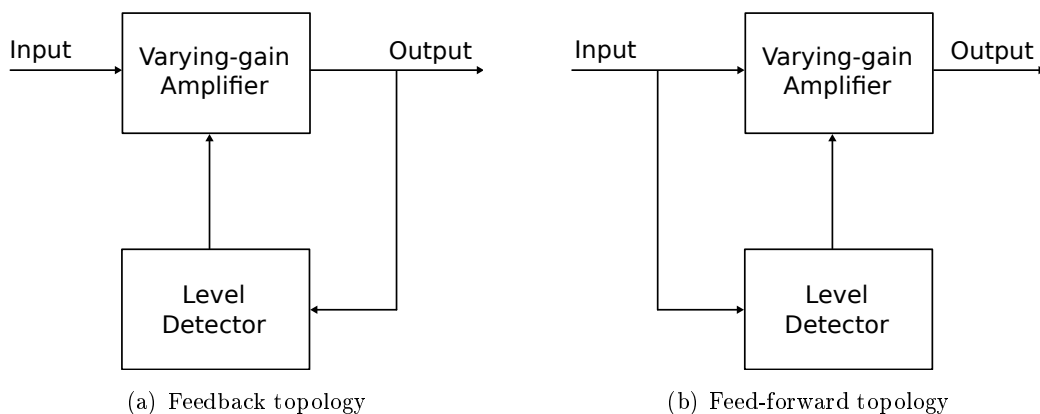


Figure 2.2: Block diagram of the two compressor topologies.

As it can be seen in Figure 2.2, feedback compressors sense the signal at the output of the audio path while feed-forward compressors use the input signal to derive the control voltage.

Furthermore, both topologies can be implemented with different designs and four main types of hardware compressors can be identified [8] [9]:

- Tube compressors, which use a valve as the gain-controlling element. They are also known as Vari-Mu compressors and their operation is based on feeding the resultant signal from the level detector to the grid of the valve, hence varying its gain;
- Optical compressors, where the level detector circuit consists of a light source and a photoresistor sensor which resistance decreases for higher incident light intensity, i.e. higher signals;

- VCA compressors, where a control voltage derived from the input signal controls the amount of gain reduction supplied by a voltage-controlled amplifier;
- FET compressors, which similarly to tube and VCA compressors, make use of a control voltage to vary the bias of a gain-controlling element, here a Field Effect Transistor.

Each design provides different output characteristics based on the different gain-controlling elements used and the additional non-linear distortion they may introduce, thus making each one preferred for different applications in the studio environment [8]. The circuit in study here is a feedback compressor of the FET type and will be explained in detail further in this chapter.

2.1.2 Static Curve

The amount of gain reduction can be mapped into an input-output function from where the compression ratio of the compressor can be derived. Such mapping defines the static curve of a compressor and an example taken from the UREI 1176LN is shown in Figure 2.3.

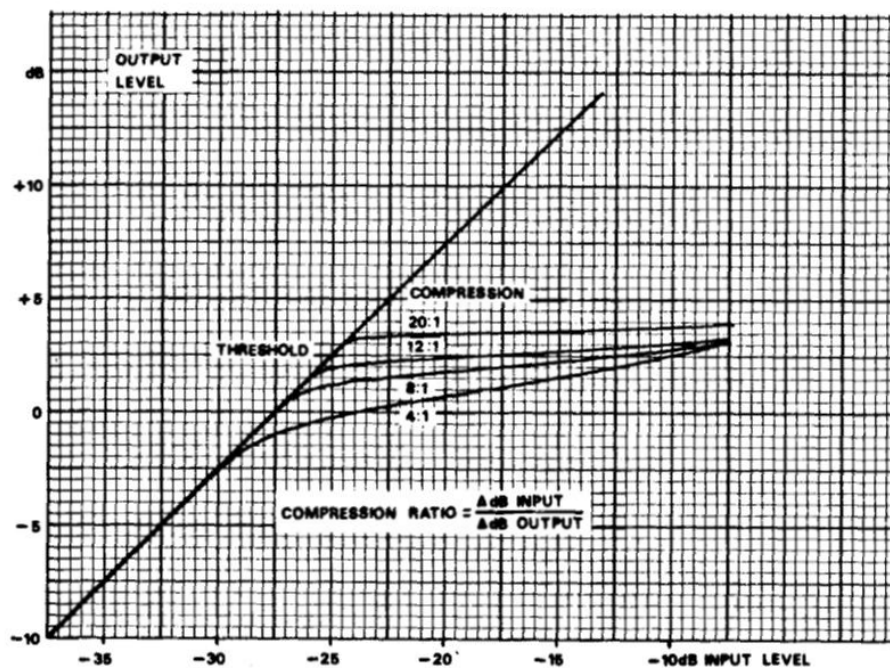


Figure 2.3: Static curve of the UREI 1176LN compressor [10].

In the horizontal axis the dB level of the input signal is mapped while the vertical axis corresponds to the output. Apart from a linear curve where no compression occurs, it also shows four different curves representing each a different compression ratio. Shown is also how the compression ratio is defined by the ratio of change in the input and output signal amplitudes $\frac{\Delta Input}{\Delta Output}$ in dB, and for a compressor this value is always greater than 1.

As an illustrative example, when a compression ratio of 4:1 is selected, for every increase of the input signal by 4 dB above a certain threshold, only an increase of 1 dB results at the output.

Below the threshold level no change occurs. When operating under compression ratios of 12:1 or higher, where the static curve becomes almost flat, the compressor is usually thought of as a limiter but, in reality, both terms describe the same effect. Imposing an upper limit for the signal is particularly useful to avoid headroom overloads from high-amplitude peaks [10].

The drop in the level of the louder signals is then compensated by the varying-gain amplifier and controlled by an output potentiometer. This is called the make-up gain and allows for processed signals to increase back to the original peak level. The result will often be a louder perceived sound. Figure 2.4 illustrates how this is achieved.

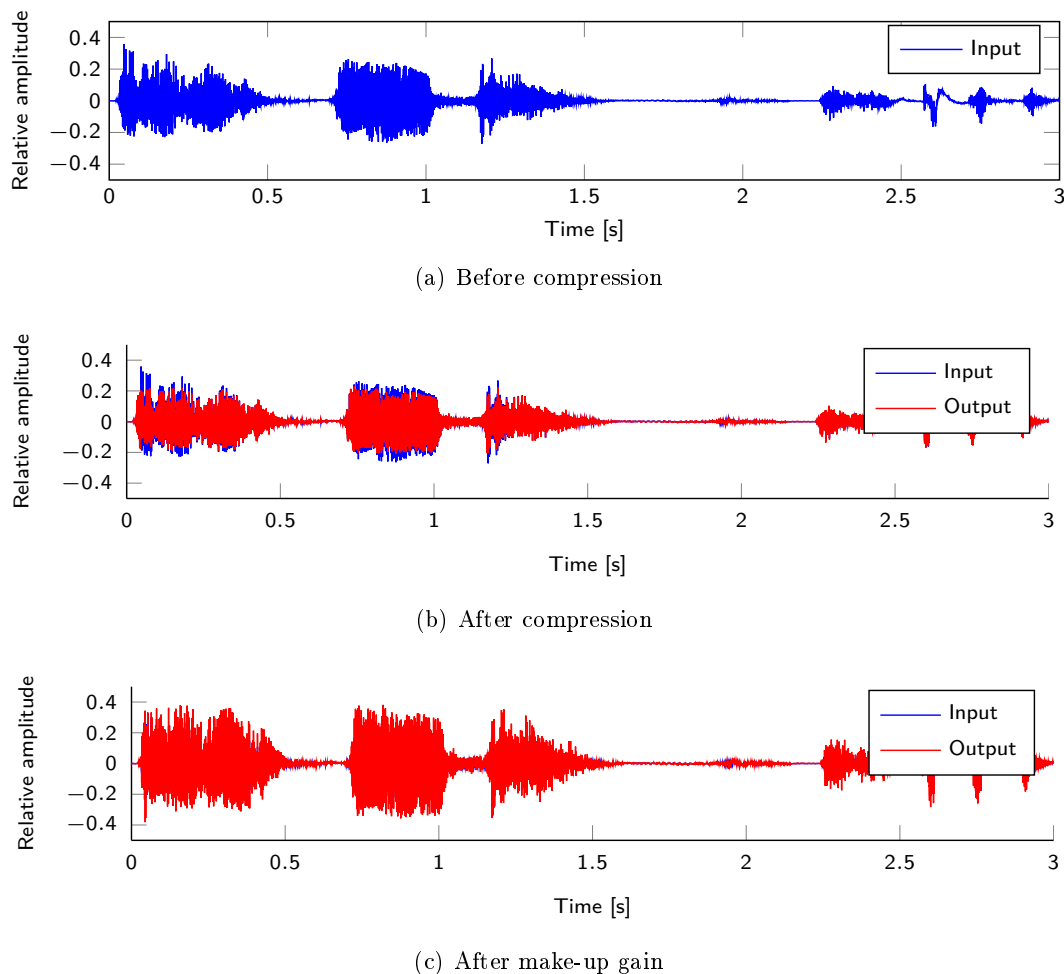


Figure 2.4: Typical compression applied to music.

An input signal with a relative peak amplitude of 0.4 is shown in Figure 2.4(a). After the signal is processed, it is visible that the louder parts of the sound have triggered gain reduction and are now attenuated in comparison with the input. The result is a smaller signal but also a gain in headroom as the new relative peak amplitude is about 0.2 (Fig. 2.4(b)). This means an increase in loudness is possible by applying make-up gain to the signal and restoring its peak back to the original value. As it can be seen in Figure 2.4(c), the output signal is now consistently greater than the input resulting from the peak compression applied.

2.1.3 Dynamic Behaviour

Another important aspect that might influence the sound quality considerably has to do with the time constants that shape the control signal derived from the level detector. These are the Attack and Release times and are specially crucial when processing music material, where specific settings work better with specific sources (i.e., different instrument or vocal tracks) [10] [8].

The Attack time can be defined as the time occurring between the instant the input signal reaches the threshold and the instant the gain reduction actually starts. Release time, on the other hand, is the time it takes for the compressor to return to its normal state after the same signal drops below the threshold. Both parameters are variably adjustable and one can think as adjusting the delays before and after compression when dealing with these controls.

For better illustration of their effect, serves the example of processing a snare drum or other percussive instrument, where fast transients compose the actual characteristic of the sound. A fast attack setting will make the compressor act on the fast transient and the effect of the snare drum will be severely reduced. For such material, a slow attack setting allows the fast transient to remain unaltered, maintaining the original sonic characteristic and is more appropriate. The release time is also important to avoid severe gain variations (if it's set too short) and unwanted gain reduction in the softer passages (if too long).

2.2 UREI 1176LN

The first version of the 1176 Peak Limiter came in 1966 when Universal Audio founder Bill Putnam introduced a FET design to his line of already successful vacuum tube based audio compressors. It was, at the time, the first compressor completely based on transistor circuitry, so-called solid-state technology. It soon became one of the most popular and present compressors in professional music production studios.

This solid-state design and the use of the JFET as the gain-controlling element allowed for very fast time constants, one of the reasons it is still widely used today. Its user manual states attack time to be adjustable between 20 and 800 μs . Other reason for its popularity comes from its versatility, not only in recording studios where it can be applied to a wide range of instruments as well as vocals, but also in its range of application that can include disc mastering, broadcasting, live performance or sound reinforcement installations [10]. Another interesting feature is the tonal shaping capability that it provides to its input source, derived from the use of the JFET as well as the output transformer. As an example, an application of the 1176 as a source for a low noise distortion effect was provided by Universal Audio's own webzine in 2003 [11].

Since the introduction of the first version, several revisions of the original circuit consisting of design changes have surfaced the market. The circuit in study here comprises the so-called Revision D and its main feature is the inclusion of low-noise circuitry in the audio path that improves stability and noise performance of the varying-gain amplifier. It is also one of the most popular revisions of the UREI 1176 [12].

Figure 2.5 shows the front view of the Universal Audio 1176LN, a current reissue and an exact



Figure 2.5: *Universal Audio 1176LN.*

replica of the original unit produced by the same company. One can see that the front panel features all the controls mentioned before:

- An input potentiometer attenuates the signal before being applied to the circuit in order to guarantee that enough headroom is available for the varying-gain amplifier stage and no clipping distortion occurs. It is adjustable from $-\infty$ up to 0 dB;
- the output potentiometer provides the gain compensation also known as make-up gain by controlling the amount of signal used to drive an output stage. It is adjustable in the same range as the input potentiometer;
- Attack and Release potentiometers adjustable from 1 to 7 shape the dynamic behaviour of the gain reduction as described before. A fastest setting is obtained with the potentiometer set to position 7;
- four Compression Ratios (4:1/8:1/12:1/20:1) are selectable with four push-buttons;
- an analog VU meter display can indicate the amount of gain reduction applied or the amplitude of the input signal given, depending on the setting of the corresponding four push-button farther right.

An additional feature originally not intended is achieved by pressing the four compression ratio push-buttons at the same time, resulting in a high ratio (between 12 and 20) with a low threshold that shows a very unpredictable behaviour but that soon became another favourite trademark of this compressor.

In the following pages of this chapter, the operation of the UREI 1176LN will be subject to a more insightful explanation, starting from a high-level block description and going through each block circuit in further detail.

2.2.1 Theory of Operation

The operation of the UREI 1176LN can be summarized in the block diagram depicted in Figure 2.6 and it can be observed that it follows the feedback type configuration described before. Each block is then explained more explicitly further in this chapter.

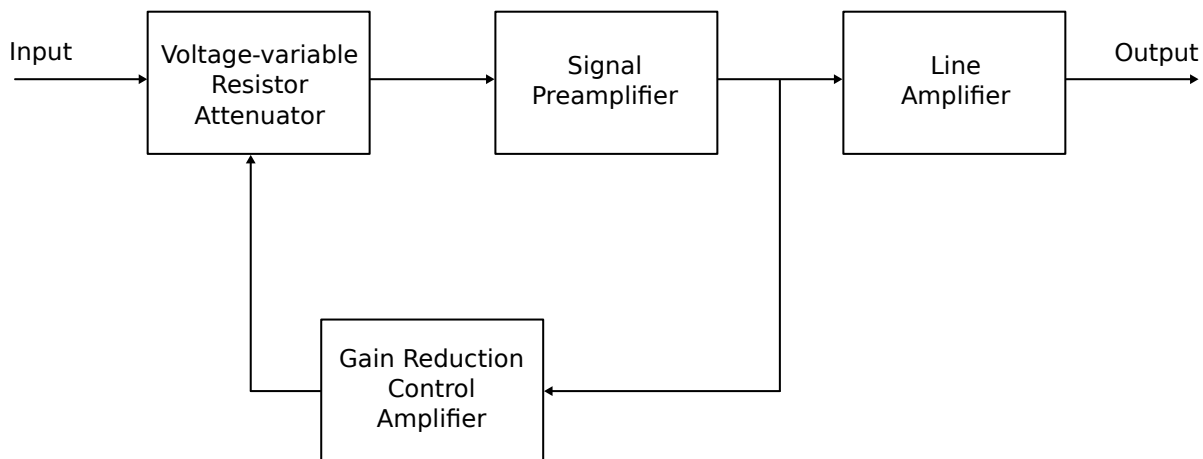


Figure 2.6: Block Diagram of the UREI 1176LN.

After a first attenuation by the input control potentiometer, the signal is applied to a Voltage-variable Resistor Attenuator (VVRA) that will further attenuate it if gain reduction is to be applied. This is defined by a control voltage supplied by the Gain Reduction Control Amplifier (GRCA) in the feedback path. The additional attenuation is the actual gain reduction that is only triggered once the signal sensed after the Signal Preamplifier (SP) block is sufficiently high to trigger compression. In other words, a large signal at the input results in a higher control voltage at the GRCA and some attenuation by the VVRA, thus lowering the signal level. The Attack and Release times as well as the Compression Ratio setting are controlled by the GRCA stage. The Signal Preamplifier increases the signal level back to line levels and an output control potentiometer is used to control the amount of signal applied to the Line Amplifier stage.

2.2.1.1 Voltage-variable Resistor Attenuator

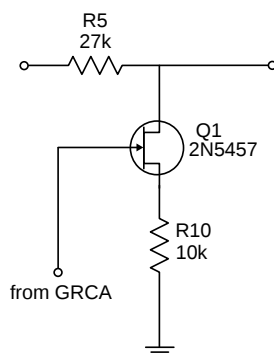


Figure 2.7: Voltage-variable Resistor Attenuator.

The first stage of the circuit is shown in Figure 2.7 and consists of a voltage-variable resistor attenuator that controls the overall gain of the compressor. Simply put, it is formed by a voltage divider where R5 is the series element and the field-effect transistor acts as a voltage controlled resistor to ground, together with R10. This resistance is dependent on the voltage between gate and source of the JFET. At its quiescent state, a negligible current flows through the transistor and thus its resistance is very high. This means that the input signal is not attenuated and thus no compression occurs. For greater gate-source voltages, when threshold of compression is reached, current starts flowing and resistance is decreased, resulting in a lower signal flowing to the preamplifier stage and consequently more gain reduction. As previously stated, this is the basic process for achieving compression in a FET style compressor.

The input signal at this stage is previously attenuated by an input level potentiometer, resulting in a low drain voltage of the JFET (range of mV) and assuring that it remains in its linear region of operation, hence keeping distortion to minimum levels.

2.2.1.2 Signal Preamplifier

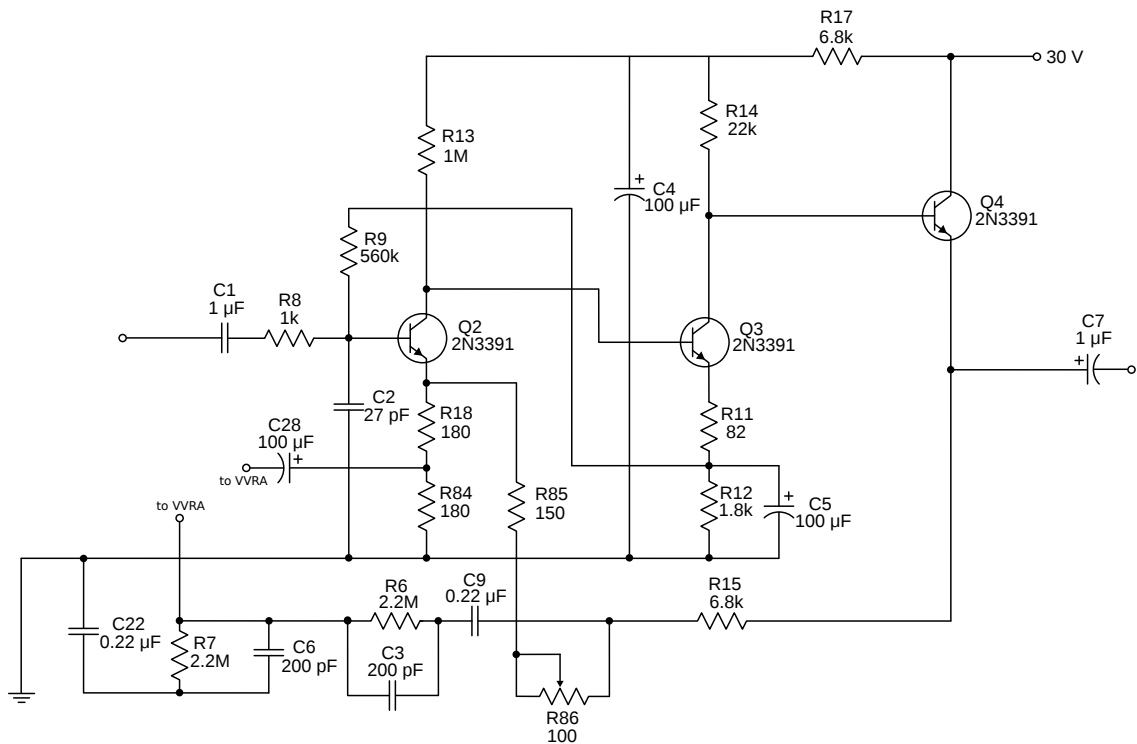


Figure 2.8: Signal Preamplifier.

Figure 2.8 shows the Signal Preamplifier, which is formed by a three-stage circuit given by the transistors Q2, Q3 and Q4. The first two stages follow a common-emitter configuration, each inverting the phase of the signal by 180° and providing a voltage gain of approximately 26 dB. Transistor Q4 follows a common-collector configuration, hence providing the necessary amount of current to drive the subsequent Line Amplifier.

Furthermore, a large amount of negative feedback is fed from this stage back to the gate of the JFET in the Voltage-variable Resistor Attenuator block of the circuit. This is part of the so-

called Low Noise circuitry that was introduced in this revision of the circuit, further reducing distortion and increasing linearity of this stage.

2.2.1.3 Gain Reduction Control Amplifier

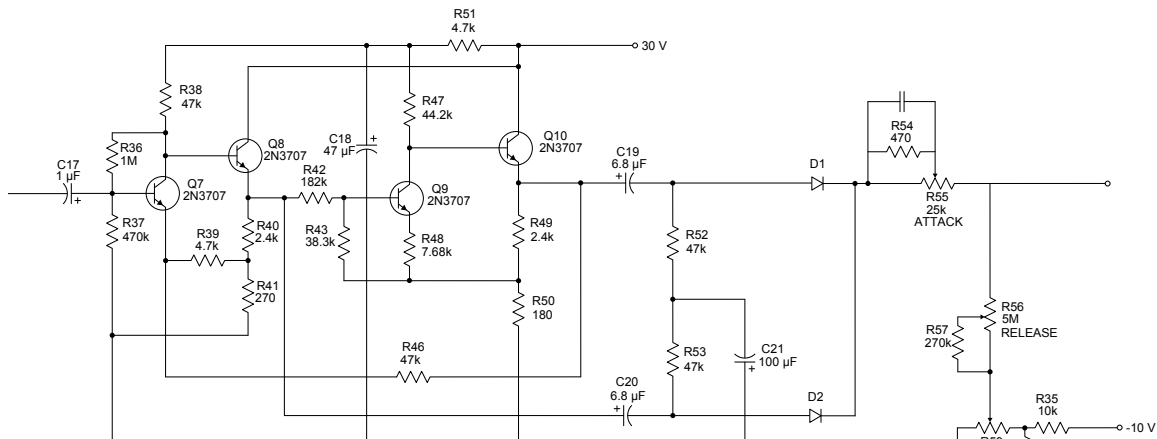


Figure 2.9: Gain Reduction Control Amplifier.

The feedback block of the compressor is comprised of the Gain Reduction Control Amplifier (Fig. 2.9). This block is fed from the output end of the Signal Pre-amplifier and it acts as a level-sensing circuit. Its function is to supply a control voltage to the gate of the JFET, that is proportional to the magnitude of the signal received at its input, taken after the pre-amplifier and a voltage divider formed by the Compression Ratio switch-buttons. This is achieved first by using two phase-inverter amplifiers, formed by a combination of common-emitter and emitter-follower stages (Q7-Q8 and Q9-Q10). The signal resulting from the first combination is sent to the bottom current rectifier diode (CR3) and simultaneously to the second combination of transistors, after attenuation with R42. The output of this second amplifier is 180° inverted in phase with respect to the first one and sent to the upper rectifier diode (CR2). This pair of diodes form a full-wave rectifier providing a signal with constant polarity. Signal amplitudes that reach the compression threshold modulate this rectified voltage while the Attack and Release potentiometers filter and control the DC level of the signal, respectively. The result is a DC voltage proportional to the input signal that increases the gate voltage bias in the JFET, triggering its conduction, for the louder parts to be compressed.

Not shown in Figure 2.9 is a resistive ladder forming a voltage divider between the output of the SP and the input of the GRCA, that is used to select different compression ratios by varying the amount of signal present at the input of the amplifier stage.

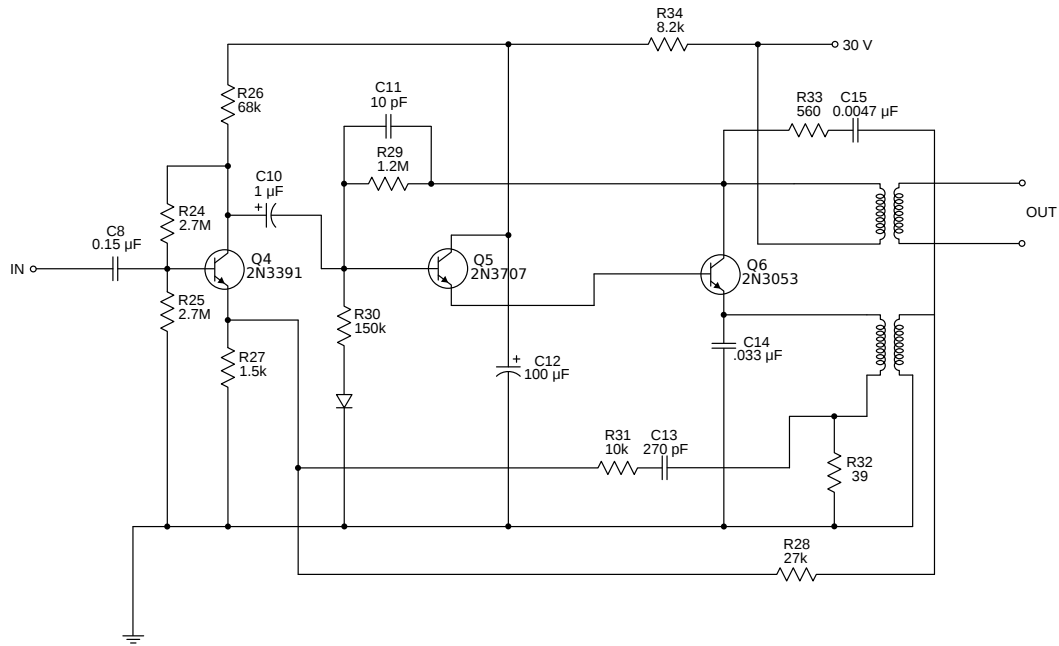


Figure 2.10: Line Amplifier.

2.2.1.4 Line Amplifier

The output of the feedback configuration is comprised of the three blocks already described is fed into an output control potentiometer and subsequently to the Line Amplifier stage. The three transistors Q4, Q5 and Q6 shown in Figure 2.10 form a Class A output that is connected to an output transformer. Part of the transformer winding is used to provide feedback to the first stage as well as DC biasing of transistor Q5. This compensates for stability of the amplifier while also converts the unbalanced signal into a high output balanced output.

Chapter 3

Circuit Modeling

3.1 Device Models

As with typical analog circuitry, analog audio effects are comprised of several different circuit components. Looking into these circuits, one will certainly find resistors and capacitors but also inductors, diodes, field-effect or bipolar junction transistors, operational amplifiers, vacuum tubes or transformers are other favourite components used when dealing with audio signals. In order to successfully model the circuit under analysis, accurate models have to be described for the non-linear devices. However, although accuracy of the model is desired, this is compromised by the need of relative simple models that can guarantee the capability of fast processing. The models described in this chapter accomplish such necessity by taking parasitic resistances and capacitances out of consideration. In this section, models describing the relation between current and voltage for the devices comprising the UREI 1176LN circuit are proposed. Whenever possible, these models are based on the same models implemented in SPICE2 (Simulation Program with Integrated Circuit Emphasis) [13].

3.1.1 Diode

The diodes found on the 1176LN circuit are of p-n junction type. This type of diode is formed by a silicon semiconductor structure of neighbouring p- and n-type regions. Associated to each region there is a contact terminal which for the case of the p-type region is called Anode and for the n-type region is called Cathode. If a positive voltage is applied between anode and cathode the diode is said to be forward-biased and a large current will flow across the p-n junction. In the inverse case, the diode is reverse-biased and only a residual current will flow in the opposite direction.

The ideal diode current is given by

$$I_D = I_S(e^{\frac{qV_D}{kT}} - 1). \quad (3.1)$$

This is also known as the Shockley diode equation, where I_S is defined as the diode reverse saturation current, $\frac{kT}{q}$ is the thermal voltage and will be expressed by V_T from now on, q is

the electric charge and k is the Boltzmann constant. Figure 3.1 shows this I_D vs V_D relation where the diode reverse saturation current can be observed for the reverse-biased region ($V_D < 0$) and the exponential behaviour of the current is shown in the forward region ($V_D > 0$).

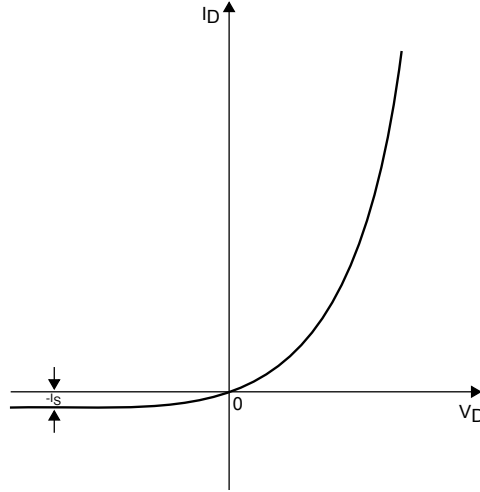


Figure 3.1: *Ideal diode current-voltage relation.*

There are however some limitations to this ideal diode model that should be noted [13]:

- Carrier generation-recombination in the depletion region. Real diodes exhibit impurities in the depletion region and this gives rise to the so-called recombination and generation current, depending on which effect is dominant. To account for this contribution to the diode current the Shockley diode equation is rewritten including a coefficient n called emission coefficient or ideality factor.
- Voltage drop due to series resistance. For large values of the diode current there is a small voltage drop across it due to the existence of a series resistance generated by an electric field in the neutral regions of the junction. This effect is however neglected here for reasons of model simplicity.
- Junction breakdown. If large reverse voltages are applied to the junction, a so-called avalanche breakdown occurs and the diode starts conducting an increasingly large reverse current, departing from the characteristic curve. This is also neglected in the model as such situation is not possible in the circuit simulation.

Considering this, the diode current equation is rewritten in the form

$$I_D = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right), \quad (3.2)$$

where n assumes a value between 1 (ideal behaviour) and 2 (dominant recombination current) and thermal voltage V_T is well approximated by 25.85 mV for the typical range of temperatures observed.

In practical terms, a diode will be modelled by a voltage-dependent current source and the equivalent circuit representation is shown in 3.2(b)

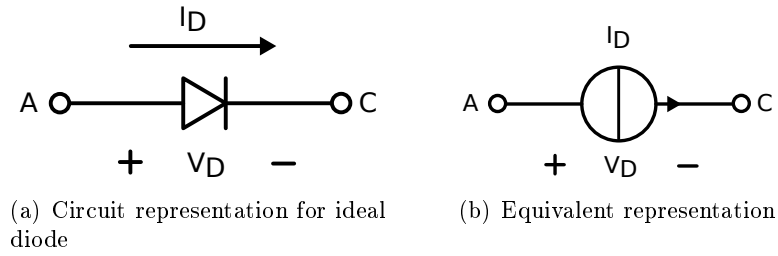


Figure 3.2: Diode Representation.

3.1.2 Bipolar Junction Transistor

Bipolar Junction Transistors (BJT) are three-terminal devices essential to audio circuits. They can be used for a wide range of applications but when it comes to audio circuits they are mostly responsible for signal buffering and amplification in discrete-circuit designs. Much like the diode, p-n junctions are at the basis of a BJT operation. Each of its three terminals forms a contact with three semiconductor regions: emitter (n-type), base (p-type) and collector (n-type). Furthermore, two junctions between these regions are formed: emitter-base junction and collector-base junction.

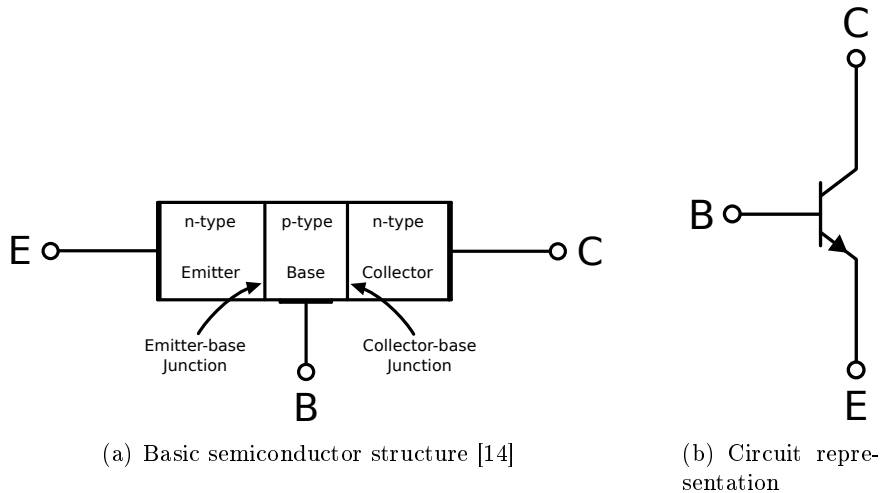


Figure 3.3: An npn BJT.

Taking this structure into consideration, the two p-n junctions allow one to represent the BJT as a diode based device and the derivation of its model follows the same principles. Likewise, the limitations of the ideal diode model described above also apply to the bipolar transistor. Currents across the two junctions can be expressed again with the Shockley diode equation (3.2)

$$I_F = I_{ES} \left(e^{\frac{V_{BE}}{V_T}} - 1 \right), \quad (3.3)$$

$$I_R = I_{CS} \left(e^{\frac{V_{BC}}{V_T}} - 1 \right) \quad (3.4)$$

where I_F and I_R define the currents of the forward- and reverse-biased diodes, I_{ES} and I_{CS} represent their reverse saturation currents, respectively, and n_E and n_C the corresponding emission coefficients.

Four different regions of operation are possible for a transistor, depending on the voltage bias applied to the three terminals [13, 14]. The BJTs found on the 1176LN circuit function as amplifiers and so are biased to operate in the active region. This behaviour is achieved when the collector voltage is greater than the base voltage and this one greater than the emitter voltage ($V_C > V_B > V_E$). This results in the emitter-base junction being forward-biased while the collector-base junction is reverse-biased.

This region is further described by the output characteristic curve and a typical example for a BJT is shown below.

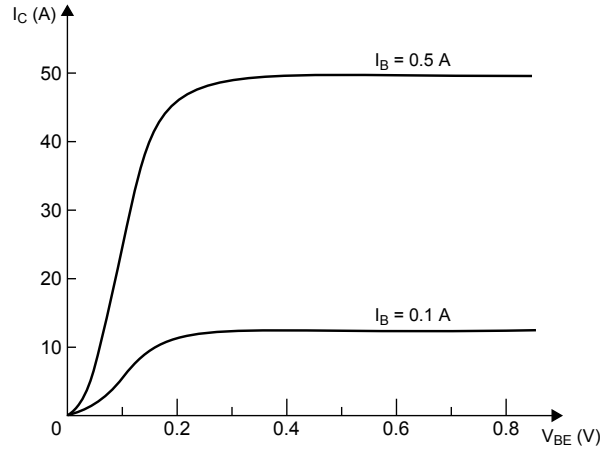


Figure 3.4: Ideal characteristic curve of a BJT in the forward active region with different base currents.

As seen in Figure 3.4, different values of base current result in different curves of the collector current I_C and collector-emitter voltage V_{CE} . For V_{CE} values of up to 0.2 V, the transistor is said to be in saturation. This is the region where collector current starts to flow. Beyond the saturation voltage ($V_{CE} = 0.2$ V) the transistor is in the active region and acts as a linear amplifier, where the collector current is stabilized at its maximum for a given base current I_B .

Further analysis of the terminal currents comes from the widely used Ebers-Moll Model.

The diodes seen in Figure 3.5 represent the two p-n junctions already described, while the two current sources account for the coupling between both junctions [13].

From Kirchoff's current law, one can now derive the collector, emitter, and base currents

$$I_C = \alpha_F I_F - I_R, \quad (3.5)$$

$$I_E = -I_F + \alpha_R I_R, \quad (3.6)$$

$$I_B = (1 - \alpha_F) I_F + (1 - \alpha_R) I_R, \quad (3.7)$$

where α_F and α_R are the forward and reverse large-signal current gains of a common-base BJT. Substituting Equations (3.3) and (3.4) through Equations (3.5), (3.6), (3.7), the general

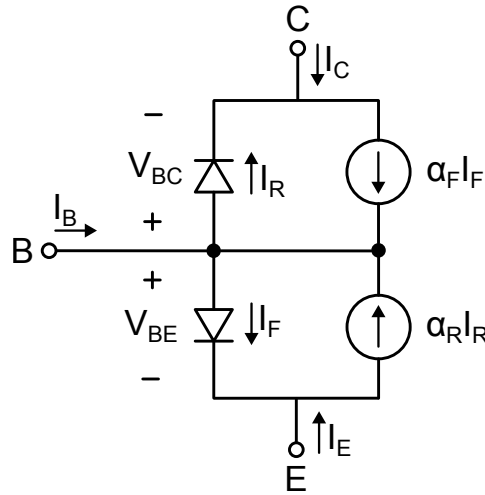


Figure 3.5: Equivalent circuit diagram of a BJT [13].

equations for the Ebers-Moll model

$$I_C = \alpha_F I_{ES} (e^{\frac{V_{BE}}{n_E V_T}} - 1) - I_{CS} (e^{\frac{V_{BC}}{n_C V_T}} - 1), \quad (3.8)$$

$$I_E = -I_{ES} (e^{\frac{V_{BE}}{n_E V_T}} - 1) + \alpha_R I_{CS} (e^{\frac{V_{BC}}{n_C V_T}} - 1), \quad (3.9)$$

$$I_B = (1 - \alpha_F) I_{ES} (e^{\frac{V_{BE}}{n_E V_T}} - 1) + (1 - \alpha_R) I_{CS} (e^{\frac{V_{BC}}{n_C V_T}} - 1) \quad (3.10)$$

are obtained.

The Ebers-Moll equations show six unknown parameters: I_{ES} , I_{CS} , n_E , n_C , α_F and α_R . In the ideal transistor, the relation $\alpha_R I_{CS} = \alpha_F I_{ES}$ holds. The same assumption can be made for a real device based on the reciprocity characteristic of a two-port device [15]. Another assumption made is that there are no generation-recombination currents in the depletion region of the transistor [15], therefore the emission coefficients can be assumed to be 1. This results in only three parameters to determine: I_{ES} , I_{CS} and α_F .

The current gain α_F can be more easily obtained from a common-emitter configuration, following the relation

$$\alpha = \frac{\beta}{\beta + 1}, \quad (3.11)$$

and β being the large-signal current gain of a common-emitter BJT.

In addition to the limitations of the ideal diode model, further aspects arising from the simplicity of Ebers-Moll Model should be mentioned:

- Parasitic base, collector, and emitter resistances are not considered.

- It assumes constant current gains whereas in reality these show some dependency on base current and collector-emitter voltage.
- Real devices exhibit a slight increase of the collector current with increasing collector-emitter voltage in the saturation region. This is known as Early Effect and is here introduced with the inclusion of the term $(1 - \frac{V_{BC}}{V_A})$ in the Ebers-Moll equation of the collector current (eq. 3.8), where V_{BC} is the base-collector voltage and V_A is known as Early voltage. The collector current equation then takes the form

$$I_C = \alpha_F I_{ES} (e^{\frac{V_{BE}}{n_E V_T}} - 1) (1 - \frac{V_{BC}}{V_A}) - I_{CS} (e^{\frac{V_{BC}}{n_C V_T}} - 1). \quad (3.12)$$

3.1.3 Junction Field-Effect Transistor

Although it is also a three-terminal device, a Junction Field-Effect Transistor (JFET) is very different from the BJT. The main difference consists in its input impedance which is significantly higher than the one of a BJT. While the latter is strongly dependent on the current that its base can draw, JFETs are solely voltage-controlled. Most of its application falls into the design of amplifiers and switches, but here it is used in a different class of application, as a voltage-controlled attenuator. [14]

An n-channel JFET like the one used in this work consists of an n-region channel with two p-regions on the sides as can be seen in Figure 3.7(a). Across the n-channel are the two electrical contacts Drain (D) and Source (S) and the p-type regions form the Gate (G). Unlike the BJT, the JFET find its application when the p-n junction between gate and channel is reverse-biased, meaning that a negative gate-to-channel voltage is used to control the channel width and thus its current flow. This dependency is depicted below in Figure 3.6, where it can be observed that the drain current I_D is controlled by a range of negative gate-source voltage V_{GS} . Below a voltage known as threshold voltage V_{Th} no significant current flows across the JFET and for a $V_{GS} = 0$ the saturated drain current I_{DSS} is obtained, over which the JFET is prone to permanent damage.

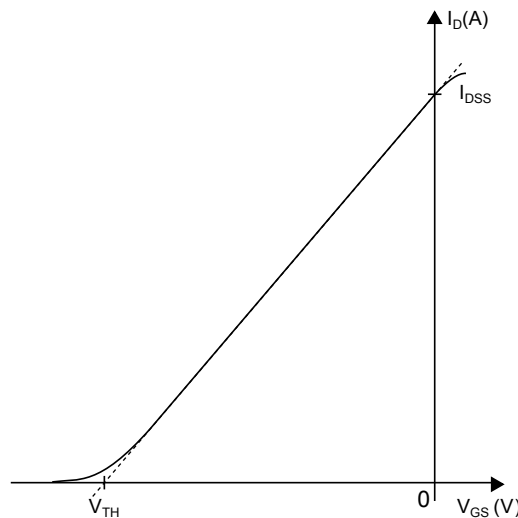


Figure 3.6: Ideal relation between V_{GS} and I_D of a JFET.

Figure 3.7(a) shows the maximum channel width which is obtained with the application of a

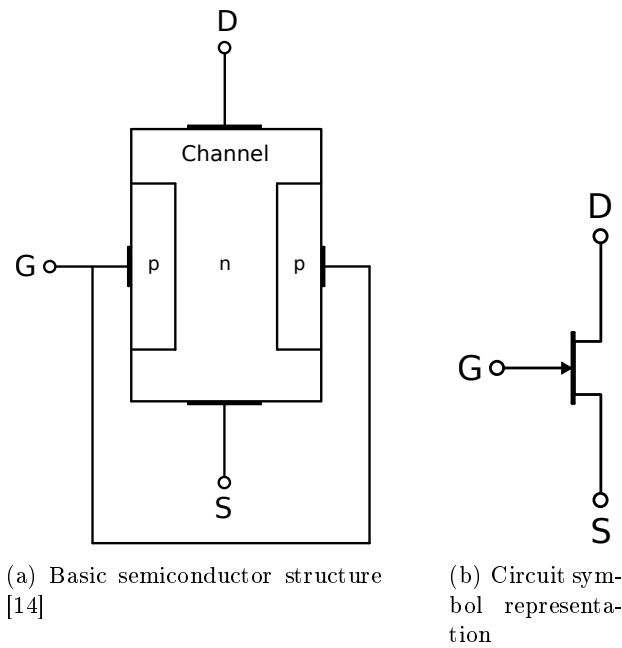


Figure 3.7: An *n*-channel JFET.

gate-source voltage $V_{GS} = 0$. Applying a positive voltage across drain and source ($V_{DS} > 0$) will then give origin to a current flow from drain to source, while a negative V_{DS} will cause a flow in the reverse direction. By applying further negative V_{GS} values, a depletion region between the gate and channel increases, and in turn the channel width gets shortened. This results in less current flow, up to a point where the depletion region occupies the whole channel width, thus cutting off any current flow. This is achieved when V_{GS} reaches the so-called threshold voltage V_{th} or pinch-off voltage V_P [13, 14].

The most common model used to describe the JFET operation is the Shichman-Hodges Model [16]. SPICE2 makes use of it for describing both gate current I_G and drain current I_D of the JFET [13], and an equivalent circuit diagram of the device can be seen in Figure 3.8.

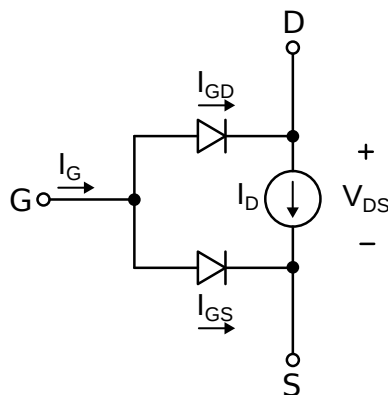


Figure 3.8: Equivalent circuit diagram of the JFET.

The currents across the two diodes compose the gate current of the JFET and can be again calculated from the Shockley diode equation (3.2)

$$I_{GD} = I_S(e^{\frac{V_{GD}}{V_T}} - 1), \quad (3.13)$$

$$I_{GS} = I_S(e^{\frac{V_{GS}}{V_T}} - 1), \quad (3.14)$$

resulting in the sum

$$I_G = I_S(e^{\frac{V_{GD}}{V_T}} + e^{\frac{V_{GS}}{V_T}} - 2), \quad (3.15)$$

where I_S is the gate junction saturation current, V_{GD} the gate-drain voltage and V_{GS} the gate-source voltage.

For the drain current calculation, however, the model based on Shockley equations and Shichman-Hodges work proposes different expressions for the different regions of operation, which can be a cause of errors derived from points of discontinuity. Instead, an approximation consisting of the square-law relation governing the V_{GS} dependency and a hyperbolic function to account for V_{DS} is preferred, as proposed in [17]. The drain current can be calculated from

$$I_D = \begin{cases} I_{DSS}(1 - \frac{V_{GS}}{V_{Th}})^2 \tanh(\lambda |\frac{V_{DS}}{V_{Th} - V_{GS}}|) & \text{for } V_{DS} \geq 0 \\ -I_{DSS}(1 - \frac{V_{GD}}{V_{Th}})^2 \tanh(\lambda |\frac{V_{DS}}{V_{Th} - V_{GD}}|) & \text{for } V_{DS} < 0, \end{cases} \quad (3.16)$$

where I_{DSS} is the saturated drain current, V_{Th} is the threshold voltage and λ an empirical constant adjusting the curve-fitting process. The expected forward output characteristic ($V_{DS} \geq 0$) is plotted in Figure 3.9 for different values of gate voltage V_{GS} . Up to a V_{DS} value known as pinch-off, which here is the absolute value of the threshold voltage V_{Th} , the JFET operates in the linear region. This is where it becomes useful as a resistor attenuator, if its V_{DS} is varied along this region. After pinch-off, the JFET is in the saturation region where it can work as an amplifier.

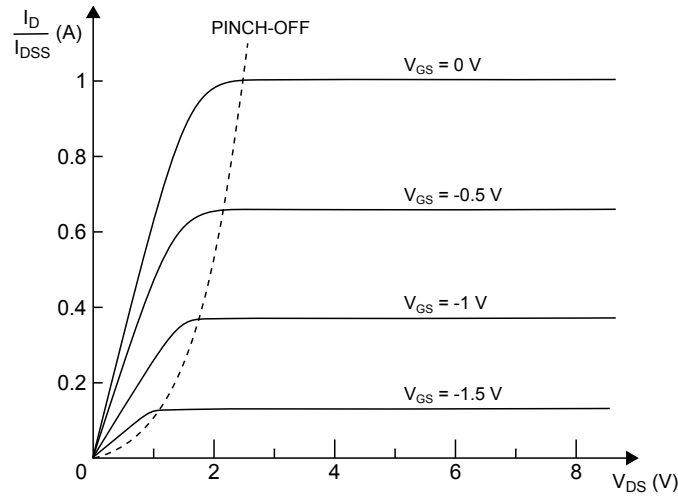


Figure 3.9: Forward current-voltage characteristic of the JFET.

3.2 State-space Representation of Non-linear Systems

Derived from control engineering and systems theory [18], state-space representation makes use of a set of first-order differential equations to describe the dynamic behaviour of a system in a matrix form, where its output is computed from a set of inputs and state variables. When such tool is applied to circuit modeling, the number of state variables is defined by the amount of energy-storing elements in the circuit, hence accounting for the terminal voltage across a capacitor or current of an inductor.

In the case of a non-linear system, as is the case of the circuit in study here, the circuit elements described in the previous section require an extension of the set of equations to account for the memoryless non-linearities. The state-space representation then takes the form

$$\dot{x} = Ax + Bu + Ci, \quad (3.17)$$

$$y = Dx + Eu + Fi, \quad (3.18)$$

$$v = Gx + Hu + Ki, \quad (3.19)$$

where x is a vector representing the state variables of the system, \dot{x} being its time derivative, u represents the inputs, y is the output vector, i consists of the non-linear currents mapped from their elements terminal voltages v and $A, B, C, D, E, F, G, H, K$ are the corresponding state-space matrices representing linear combinations of these vectors. The assumption made is that the voltages and currents of the non-linear elements are given by the current-voltage law

$$i = f(v), \quad (3.20)$$

which was presented for each non-linear device in section 3.1.

The system can then be thought of as consisting of a dynamical part given by equation (3.17) and a non-linear part given by the multiple-input multiple-output mapping of equation (3.20) that requires a non-linear iterative solver. This approach to solve this system was proposed in [19] and is known as the K method. It can be briefly summarized as presented in the block decomposition of Figure 3.10.

In order to obtain a discrete-time representation of the system, application of trapezoidal rule [20]

$$\frac{T}{2}(\dot{x}(n) + \dot{x}(n-1)) = x(n) - x(n-1) \quad (3.21)$$

as described in [5] is used. Such approach yields the discrete-time formulation of the system

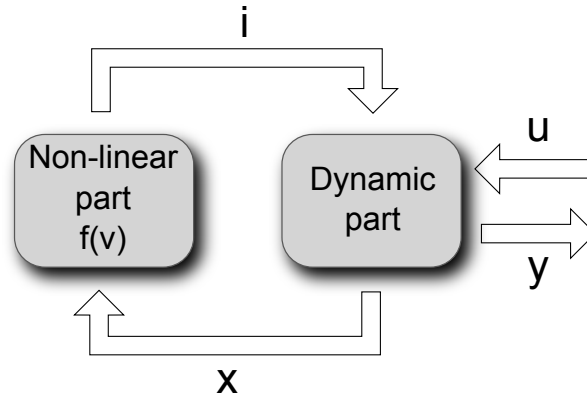


Figure 3.10: Block diagram of the K method.

$$x(n) = \bar{A}x(n-1) + \bar{B}u(n) + \bar{C}i(n), \quad (3.22)$$

$$y(n) = \bar{D}x(n-1) + \bar{E}u(n) + \bar{F}i(n), \quad (3.23)$$

$$v(n) = \bar{G}x(n-1) + \bar{H}u(n) + \bar{K}i(n), \quad (3.24)$$

with the corresponding state-matrices

$$\bar{A} = \left(\frac{2}{T}I + A\right)\left(\frac{2}{T}I - A\right)^{-1}, \quad (3.25)$$

$$\bar{B} = 2\left(\frac{2}{T}I - A\right)^{-1}B, \quad (3.26)$$

$$\bar{C} = 2\left(\frac{2}{T}I - A\right)^{-1}C, \quad (3.27)$$

$$\bar{D} = \frac{2}{T}D\left(\frac{2}{T}I - A\right)^{-1}, \quad (3.28)$$

$$\bar{E} = E + D\left(\frac{2}{T}I - A\right)^{-1}, \quad (3.29)$$

$$\bar{F} = F + D\left(\frac{2}{T}I - A\right)^{-1}C, \quad (3.30)$$

$$\bar{G} = \frac{2}{T}G\left(\frac{2}{T}I - A\right)^{-1}, \quad (3.31)$$

$$\bar{H} = H + G\left(\frac{2}{T}I - A\right)^{-1}B, \quad (3.32)$$

$$\bar{K} = K + G\left(\frac{2}{T}I - A\right)^{-1}C, \quad (3.33)$$

where I is the identity matrix. For reasons of simplicity, and because this work is implemented in the discrete-time domain, the discretized state-space matrices will be from now on represented without the corresponding bar.

The rest of this chapter focuses on the methods for obtaining these state-space matrices and the solution of the non-linear mapping part.

3.3 Nodal DK Method

The Discrete K method is, as the name implies, derived from the already mentioned K method, but instead of making use of the continuous-time state-space representation (3.17, 3.18, 3.19), it is applied with its discrete-time version [21]. Therefore, energy-storing elements governed by a differential equation need to be first discretized. The solution for the non-linear system is then derived from the computation of a set of matrices representing the physical model of the circuit in analysis, based on Modified Nodal Analysis (MNA) [22].

3.3.1 Discretization of Energy-storing Elements

Energy-storing elements like capacitors and inductors are described by differential equations relating the voltages and currents across them. These equations can be replaced by companion circuits comprising only resistors and current sources if trapezoidal discretization [20] is applied. A successful implementation of such approach can be found in [4]. Since no inductors are to be found on the UREI 1176LN, only the capacitor model will be described.

The current equation of a capacitor is given by the differential equation

$$i_C = C \frac{d}{dt} v_C \quad (3.34)$$

and the trapezoidal rule introduces a discrete-time approximation

$$i_C(n) = \frac{2C}{T}(v_C(n) - v_C(n-1)) - i_C(n-1), \quad (3.35)$$

which denotes a system with memory held by the voltages and currents of the previous input, and where T is the sampling interval. Representing memory with the canonical state

$$x_C(n) = i_C(n) + \frac{2C}{T}v_C(n) \quad (3.36)$$

leads to the state update equation

$$x_C(n) = 2\frac{2C}{T}v_C(n) - x_C(n-1). \quad (3.37)$$

Equations (3.36) and (3.23) allow the current across the capacitor to be obtained from

$$i_C(n) = \frac{2C}{T}v_C(n) - x_C(n-1), \quad (3.38)$$

which can be represented in the form of a companion circuit like the one shown in Figure 3.11.

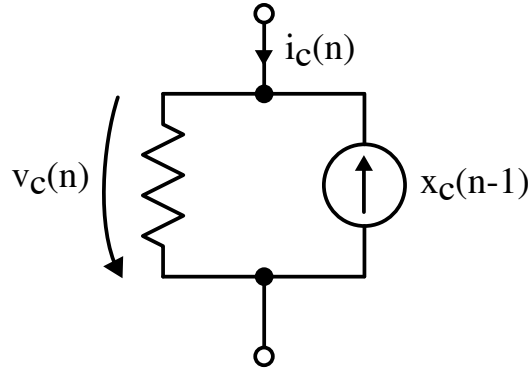


Figure 3.11: Equivalent circuit diagram of a capacitor.

This equivalent circuit allows one to replace all capacitors in the circuit with resistors and current sources where the resistor value is given by $\frac{2C}{T}$ and the current source holds the state information.

3.3.2 Matrix Description of the Circuit

In order to obtain the state-space matrices required for the solution of the non-linear system, an adapted form of Modified Nodal Analysis is performed. MNA sets the ground for such matrix description by approaching the circuit in study using the form

$$G\nu = c, \quad (3.39)$$

where G is the conductance matrix, ν represents the voltages in each node of the circuit, and c is a vector containing any current source related to the nodes.

The application of the DK method requires that the MNA system is in the form of the discrete state-space system and an adapted form of MNA is derived. The current source vector c is extended to include contributions from the state variables, inputs and non-linear currents, while the unknowns vector ν is augmented with the state derivatives. Conductance matrix G is adapted to include contributions from each component, resulting in a system where the number of rows correspond to the number of nodes in the circuit. The solution of the system comes from inversion of system matrix G to obtain vector ν containing all the node voltages, voltage source currents and state derivatives \dot{x} [21].

This approach implies a KCL analysis at all nodes of the circuit, hence adopting a physical model. A reference node is chosen while the voltages at the other nodes and currents through the voltage sources are introduced as unknowns. The complete system is then defined by

$$(N_R^T G_R N_R + N_v^T R_v^{-1} N_v + N_x^T G_x N_x) \varphi + N_u^T i_s = N_x^T x + N_n^T i_n, \quad (3.40)$$

where N_R , N_v , N_x , N_u , N_n are called incidence matrices, specifying to which nodes are the resistors, potentiometers, energy-storing elements, voltage sources and non-linear devices, connected.

$$G_R = \begin{pmatrix} \frac{1}{R_1} & 0 & \cdots \\ 0 & \ddots & \cdots \\ \vdots & \vdots & \frac{1}{R_N} \end{pmatrix} \quad (3.41)$$

is a diagonal matrix with the corresponding resistance values,

$$R_v = \begin{pmatrix} \alpha VR_1 & 0 & \cdots & \cdots & \cdots \\ 0 & (1-\alpha)VR_1 & 0 & \cdots & \cdots \\ \vdots & 0 & \ddots & \cdots & \cdots \\ \vdots & \vdots & \vdots & \alpha VR_N & 0 \\ \vdots & \vdots & \vdots & 0 & (1-\alpha)VR_N \end{pmatrix} \quad (3.42)$$

is a diagonal matrix with the variable resistances of the potentiometers parametrized with position α , and

$$G_x = \begin{pmatrix} \frac{2C_1}{T} & 0 & \cdots & \cdots & \cdots & \cdots \\ 0 & \ddots & \cdots & \cdots & \cdots & \cdots \\ \vdots & \vdots & \frac{2C_N}{T} & 0 & \cdots & \cdots \\ \vdots & \vdots & 0 & \frac{T}{2L_1} & 0 & \cdots \\ \vdots & \vdots & \vdots & 0 & \ddots & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \frac{T}{2L_N} \end{pmatrix} \quad (3.43)$$

is a diagonal matrix corresponding to the resistances of the companion circuits of the energy-storing elements, φ is the unknown node voltages vector, i_s the vector of unknown voltage source currents, x the current states of the energy-storing elements, and i_n the currents of the non-linear devices.

The incidence matrices describe how the respective component is connected in the circuit, where each row is associated with one component and each column corresponds to a node in the circuit, excluding the reference node. This results in a sparse matrix where most elements are zero and where, at most, there are two entries (1 and -1) in a row, corresponding to the terminal nodes of the respective component. The inclusion of the voltage sources as the inputs vector u and combination with equation 3.40 allows the formulation of the system

$$S \begin{pmatrix} \varphi \\ i_s \end{pmatrix} = \begin{pmatrix} N_x^T \\ 0 \end{pmatrix} x + \begin{pmatrix} 0 \\ I \end{pmatrix} u + \begin{pmatrix} N_n^T \\ 0 \end{pmatrix} i_n, \quad (3.44)$$

where

$$S = \begin{pmatrix} N_R^T G_R N_R + N_v^T R_v^{-1} N_v + N_x^T G_x N_x & N_u^T \\ N_u & 0 \end{pmatrix} \quad (3.45)$$

is the system matrix.

The solution of the unknown voltages comes from left-multiplication with S^{-1} and the incidence matrices

$$v_x = (N_x \ 0) S^{-1} \left(\begin{pmatrix} N_x^T \\ 0 \end{pmatrix} x + \begin{pmatrix} 0 \\ I \end{pmatrix} u + \begin{pmatrix} N_n^T \\ 0 \end{pmatrix} i_n \right), \quad (3.46)$$

$$v_n = (N_n \ 0) S^{-1} \left(\begin{pmatrix} N_x^T \\ 0 \end{pmatrix} x + \begin{pmatrix} 0 \\ I \end{pmatrix} u + \begin{pmatrix} N_n^T \\ 0 \end{pmatrix} i_n \right), \quad (3.47)$$

$$v_o = (N_o \ 0) S^{-1} \left(\begin{pmatrix} N_x^T \\ 0 \end{pmatrix} x + \begin{pmatrix} 0 \\ I \end{pmatrix} u + \begin{pmatrix} N_n^T \\ 0 \end{pmatrix} i_n \right), \quad (3.48)$$

where v_x , v_n and v_o are the voltages across energy-storing elements, the non-linear elements and the chosen output nodes, respectively.

In case of a circuit containing potentiometers, the system matrix needs to be recomputed as this variable elements change. This is done efficiently by decomposing the system matrix as

$$S = S_0 + (N_v \ 0)^T R_v^{-1} (N_v \ 0) \quad (3.49)$$

where S_0 becomes the static part of the system matrix and is defined as

$$S_0 = \begin{pmatrix} N_R^T G_R N_R + N_x^T G_x N_x & N_u^T \\ N_u & 0 \end{pmatrix}. \quad (3.50)$$

The inverse of the system matrix of Equation (3.49) makes use of the Woodbury identity [23] and is written as

$$S^{-1} = S_0^{-1} - S_0^{-1} (N_v \ 0)^T (R_v + Q)^{-1} (N_v \ 0) S_0^{-1}, \quad (3.51)$$

where

$$Q = (N_v \ 0) - S_0^{-1} (N_v \ 0)^T. \quad (3.52)$$

The state-space matrices can now be obtained from

$$A = A_0 - 2ZG_x U_x (R_v + Q)^{-1} U_x^T, \quad (3.53)$$

$$B = B_0 - 2ZG_x U_x (R_v + Q)^{-1} U_u^T, \quad (3.54)$$

$$C = C_0 - 2ZG_x U_x (R_v + Q)^{-1} U_n^T, \quad (3.55)$$

$$D = D_0 - U_0 (R_v + Q)^{-1} U_x^T, \quad (3.56)$$

$$E = E_0 - U_0 (R_v + Q)^{-1} U_u^T, \quad (3.57)$$

$$F = F_0 - U_0 (R_v + Q)^{-1} U_n^T, \quad (3.58)$$

$$G = G_0 - U_n (R_v + Q)^{-1} U_x^T, \quad (3.59)$$

$$H = H_0 - U_n (R_v + Q)^{-1} U_u^T, \quad (3.60)$$

$$K = K_0 - U_n (R_v + Q)^{-1} U_n^T, \quad (3.61)$$

where

$$U_x = (N_x \ 0) S_0^{-1} (N_v \ 0), \quad (3.62)$$

$$U_o = (N_o \ 0) S_0^{-1} (N_v \ 0), \quad (3.63)$$

$$U_n = (N_n \ 0) S_0^{-1} (N_v \ 0), \quad (3.64)$$

$$U_u = (0 \ I) S_0^{-1} (N_v \ 0), \quad (3.65)$$

$$A_0 = 2ZG_x (N_x \ 0) S_0^{-1} (N_x \ 0)^T, \quad (3.66)$$

$$B_0 = 2ZG_x (N_x \ 0) S_0^{-1} (0 \ I)^T, \quad (3.67)$$

$$C_0 = 2ZG_x (N_x \ 0) S_0^{-1} (N_n \ 0)^T, \quad (3.68)$$

$$D_0 = (N_o \ 0) S_0^{-1} (N_x \ 0)^T, \quad (3.69)$$

$$E_0 = (N_o \ 0) S_0^{-1} (0 \ I)^T, \quad (3.70)$$

$$F_0 = (N_o \ 0) S_0^{-1} (N_n \ 0)^T, \quad (3.71)$$

$$G_0 = (N_n \ 0) S_0^{-1} (N_x \ 0)^T, \quad (3.72)$$

$$H_0 = (N_n \ 0) S_0^{-1} (0 \ I)^T, \quad (3.73)$$

$$K_0 = (N_n \ 0) S_0^{-1} (N_n \ 0)^T, \quad (3.74)$$

and the discrete-time non-linear state-space system presented first in section 3.2 is now complete. The computation of an output sample follows the steps:

1. Calculation of $p(n) = Gx(n-1) + Hu(n)$;
2. Numerical solving of $p(n) + Ki_n(n) - v_n(n) = 0$ to obtain i_n , recurring to a non-linear iterative solver;
3. Computation of the output with Equation (3.24);
4. Calculation of state update with Equation (3.23).

3.3.3 Non-linear Iterative Solver

As mentioned before, the non-linear part of the system described in 3.2 is computed recurring to a non-linear iterative solver. In the context of physical modeling, it can be seen as the responsible for the operation of the non-linear devices by returning the currents across these in respect to the voltages observed during simulation. For that reason, it is also within this process that lies the core of the computational effort in circuit simulation. In the following, the basic method known as Newton's Method and a further improvement of it are presented.

3.3.3.1 Newton's Method

The Newton's Method is an iterative method for solving the roots (or zeros) of a continuous real-valued function, i.e. $x : f(x) = 0$. The algorithm consists in approximating the curve of function $f(x)$ by a tangent at point $x = x_0$. The intercept of this tangent with the x-axis is then given by $x_1 = x_0 - \frac{f(x_0)}{f'(x_0)}$ and the assumption is that x_1 lies closer to the root of the function than x_0 . The second iteration performs the tangent of $f(x)$ at $x = x_1$ to obtain a x_2 which now lies closer to the root than x_1 . This process can be formulated for n iterations as

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)}. \quad (3.75)$$

The final iteration will be reached for a value of $f(x_n)$ that is within a small tolerance range previously defined, and x_n assumed as the function's root. Such process is depicted below in Figure 3.12, where the solution of root r is achieved after three iterations.

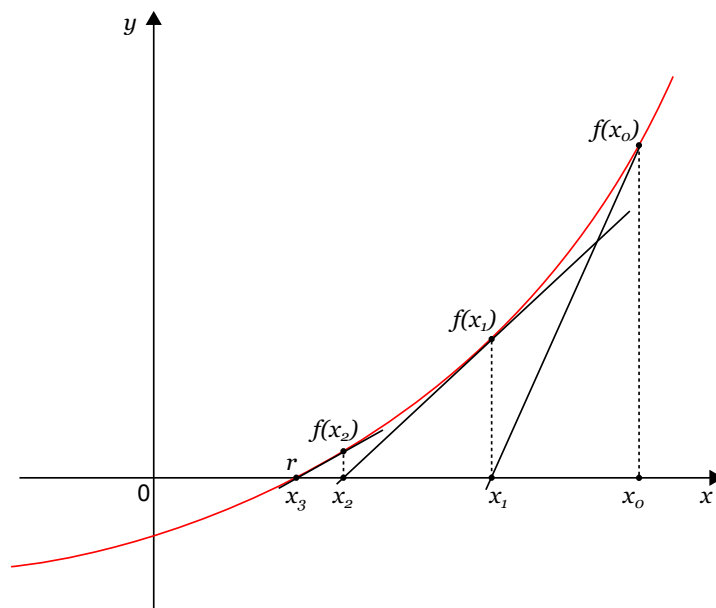


Figure 3.12: Example of the Newton's Method application.

3.3.3.2 Damped Newton's Method

In certain scenarios, the Newton's Method might not converge even if $f(x) = 0$ has a solution. One example is a function f for which the derivative is not continuous in the whole range (e.g. horizontal tangents), or a very steep function that can lead to cyclic iteration, i.e., consecutive values of $f(x_{n+1})$ that jump back and forth the root and won't converge within the tolerance range. One can identify erratic behaviour by setting a number of maximum iterations and check whether the solver breaks this number. In such scenario, these problems can be fixed by the damped Newton's method

$$x_{n+1} = x_n - \frac{f(x_n)}{\alpha f'(x_n)}, \quad (3.76)$$

in which the derivative of $f(x)$ is multiplied by a damping factor α , with $0 < \alpha < 1$, if two consecutive iterations result in a greater residual error. Therefore, in order to perform the non-linear mapping of the non-linear currents and voltages of the devices described in 3.1 it is required that derivative or Jacobian expressions for the current equations are given.

Chapter 4

Implementation

4.1 Parameter Extraction

To accurately simulate the vintage audio circuits in study, not only should the device models presented in the previous chapter closely approximate the device behaviour but also the parameters one can find in the expressions governing the current-voltage relations of these devices should be obtained in respect to the real circuits. This is necessary because often these parameters are defined by analytic expressions who require exact knowledge of the device structure, or are not defined by analytic expressions and instead result from fitting curve techniques. This chapter describes different parameter extraction methods for the different devices used in the prototype of a UREI 1176LN unit.

4.1.1 Measurement System

Common to all parameter extraction methods presented in this chapter, a measurement system composed of the setup shown in Figure 4.1 allowed for processing experimental measurements from real devices.

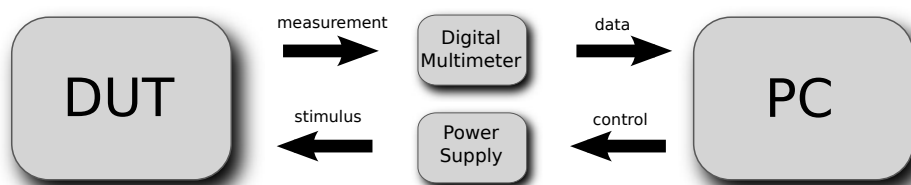


Figure 4.1: *Diagram of the measurement system.*

A Device Under Test (DUT) consisting of a diode or a transistor is connected in a test circuit optimized for providing significant measurements. This test circuit is in turn powered by a Agilent E3631A power supply that is controlled by a PC running a MATLAB script. Two digital Fluke 8846A multimeters collect experimental data that is consequently recorded and available for processing in MATLAB.

4.1.2 Diode

As presented in Chapter 3, the current-voltage characteristic of a diode is approximated by the Shockley diode equation (3.2)

$$I_D = I_S(e^{\frac{V_D}{nV_T}} - 1).$$

The equation shows two parameters that are linked to each specific diode and thus need to be extracted: the diode reverse saturation current I_S and the emission coefficient n .

The procedure for extracting such parameters follows a conventional method of extracting data from the linear range of operation of the diode and extrapolating a linear curve from the semi-logarithmic current-voltage (I-V) plot.

For values of $V_D > 3V_T$, the exponential term in (3.2) becomes significantly higher than 1 and the equation is rewritten as

$$I_D = I_S(e^{\frac{V_D}{nV_T}}) \quad (4.1)$$

and can now be linearised by plotting the current in a logarithmic scale

$$\ln(I_D) = \frac{V_D}{nV_T} + \ln(I_S). \quad (4.2)$$

By fitting a straight line of the form $y = mx + b$ to the semi-logarithmic plot of equation (4.2), shown in Figure 4.2, both parameters can be extracted from the curve. The current axis intercept (at $V = 0$) gives the saturation current $I_S = e^b$ and the slope of the straight line gives the ideality factor $n = \frac{1}{mV_T}$.

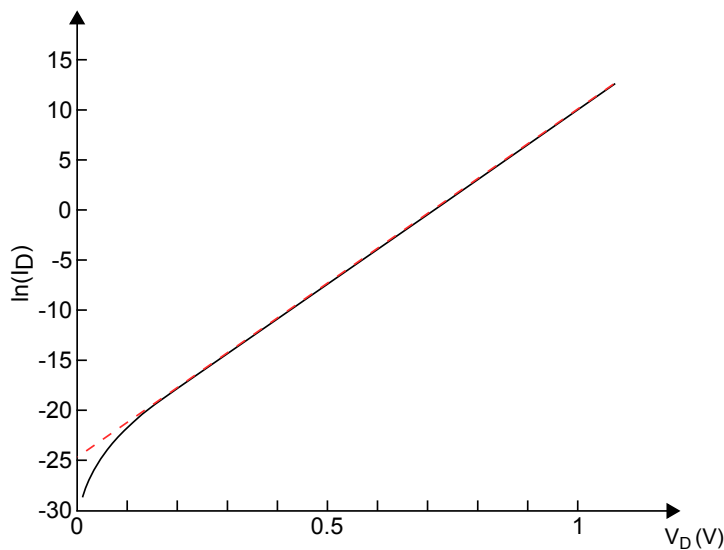


Figure 4.2: Semi-logarithmic plot of I-V characteristic of an ideal diode.

Data measurements are obtained by connecting the diode under test in a test circuit as shown

in Figure 4.3.

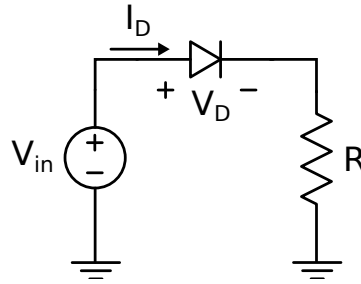


Figure 4.3: Test circuit for I-V measurements of the diode.

An input voltage V_{in} sweep from 0 V to 10 V in steps of 10 mV was applied to the circuit and a resistor value of $R = 10 \text{ k}\Omega$ was chosen to compute the current across the diode using Ohm's Law. An extra multimeter records the voltage across the diode V_D . The collected V_D vs I_D data is then used to obtain a similar plot as the one shown in Figure 4.2. For the correct assessment of the parameters, only extracted data in the voltage range of $0.4 \text{ V} < V_D < 0.8 \text{ V}$, where the diode starts showing significant conduction, is usually considered. Parameter extraction is accomplished in three steps as shown in the Sourcecodes 4.1,4.2,4.3.

```

1 for i=1:length(vm(:,1))-1
2     v1 = vm((i:length(vm(:,1))),1);
3     i1 = im((i:length(vm(:,1))),1);
4
5     lin = fit(v1,log(i1),'poly1');
6     is(i) = exp(lin.p2);
7     n(i) = 1/(lin.p1*vt);
8
9     id = is(i)*(exp(vm/(n(i)*vt)) - 1);
10    res(i) = max(abs(id-im));
11    i=i+1;
12 end
13 minrange = find(res==min(res));

```

Sourcecode 4.1: Parameter extraction script for the Shockley diode equation parameters (Step 1).

The first approach consists in finding the appropriate range of values from the measured dataset that result in the minimum residual error between the measurement and approximation provided by equation 3.1. This is performed in two steps. First, in the Sourcecode 4.1, the minimum limit for the appropriate range is defined, and in turn, Sourcecode 4.2 defines the maximum limit. Datasets vm and im contain the measured data of voltage across diode V_D and current I_D , correspondingly. Variable vt represents the thermal voltage and is previously defined as 26 mV . In Sourcecode 4.1, for each measured value i , the considered data range is made to vary by increasing the minimum limit in each iteration while maintaining a fixed maximum. The extracted data is stored in the variables $v1$ and $i1$ (code lines 2 and 3). Afterwards this datasets are used to perform data fitting by recurring to MATLAB's own function `fit`, with $v1$ and $\log(i1)$ as data inputs and parameter `poly1` used to achieve a linear polynomial curve as described in Figure 4.2. This function returns this curve coefficients m and b as `lin.p1` and

`lin.p2` respectively and these are used to obtain the diode parameters I_S and n as described before (code lines 5 to 7). These parameters are then used to calculate the diode current I_D as proposed in Chapter 3 (line 10) and the result is compared to the measured data in the residual error form (line 11). This process is performed for every iteration and the corresponding result is stored in the variable `res`. After completion, the minimum limit `minrange` for the data range is found from the iteration for which the residual error was smaller (line 15). The same procedure is used in Sourcecode 4.2, in which the used data range is now varied between the `minrange` and every possible onwards measurement `i`.

```

1 for i=minrange+1:length(vm(:,1))-1
2     vl = vm(minrange:i,1);
3     il = im(minrange:i,1);
4
5     lin = fit(vl,log(il),'poly1');
6     is(i) = exp(lin.p2);
7     n(i) = 1/(lin.p1*vt);
8
9     id = is(i)*(exp(vm/(n(i)*vt)) - 1);
10    res(i) = max(abs(id-im));
11    i=i+1;
12 end
13 maxrange = find(res==min(res))

```

Sourcecode 4.2: *Parameter extraction script for the Shockley diode equation parameters (Step 2).*

Finally, the parameters that result in the least residual error are found in the same way by considering only the obtained data range limits.

```

1 vl = vm(minrange:maxrange,1);
2 il = im(minrange:maxrange,1);
3
4 lin = fit(vl,log(il),'poly1');
5 is = exp(lin.p2)
6 n = 1/(lin.p1*vt)

```

Sourcecode 4.3: *Parameter extraction script for the Shockley diode equation parameters (Step 3).*

4.1.2.1 Implementation for the Non-linear Solver

As explained in 3.3.3, the non-linear iterative solver returns the device currents from the non-linear equations and the voltages across the device terminals. Also described was the Newton's Method, that requires the derivative of the current expressions.

The diode is then implemented as seen in the Sourcecode 4.4.

The first expression is the diode current equation (3.2), where $V_x(1)$ represents the voltage across the diode V_D and the second expression constitutes the derivative of the diode current equation in respect to V_D . These are the two inputs taken by the non-linear solver for the case of the diode.

```

1 Ix1 = -Is*(exp(Vx(1)/(N*Vt)) - 1);
2 dIx1dVx1 = -(Is*exp(Vx(1)/(N*Vt)))/(N*Vt);

```

Sourcecode 4.4: *Non-linear equations of the diode for the non-linear solver.*

4.1.3 Bipolar Junction Transistor

The theory of BJTs was presented in section 3.1.2 and it was shown that the BJT can be thought of as a diode based device. Four parameters were identified as needed to model the device. The first two consist of the two junctions respective reverse saturation currents (I_{ES} , I_{CS}) of the Shockley diode equation (3.3) (3.4), while the latter two consist of the forward and reverse current gains (α_F , α_R), of which only one is needed to derive the other. The parameter extraction process has been described already and can be found in section 4.1.2. However, in order to collect the two necessary datasets (I_E vs V_{BE} , I_C vs V_{BC}) different test circuits are used and presented in Figure 4.4.

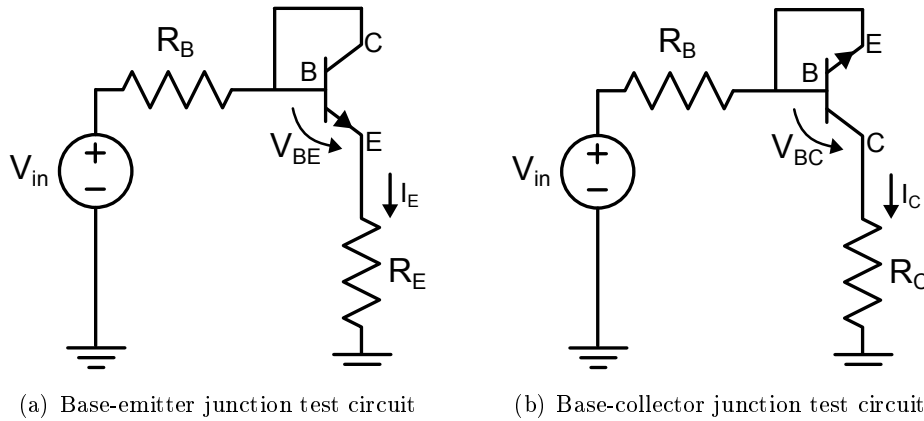


Figure 4.4: *Test circuits for extracting the Shockley equation parameters of the BJT.*

For this case, the same input voltage sweep as for the diode case was applied. Resistors values were chosen $R_B = 99.51 \text{ k}\Omega$, $R_E = 1 \text{ k}\Omega$ and $R_C = 1 \text{ k}\Omega$ as to provide significant measured data. The datasets I_E vs V_{BE} and I_C vs V_{BC} , taken while the other junction is kept constant, are then used to extract the parameters recurring again to the script shown in Sourcecodes 4.1,4.2,4.3.

The parameter left to extract is the forward current gain β_F , used to describe the Ebers-Moll model presented in section 3.1.2. This can be obtained from the measurement of collector current I_C and base current I_B in the forward active region and given by the current relation $\frac{I_C}{I_B}$ of the transistor in a common-emitter configuration. If β_F is plotted against the collector-emitter voltage V_{CE} , the result should show a flat curve for the greater range of voltages. To obtain this, the test circuit of Figure 4.5 was used.

Two voltage sources were used in order to apply voltages V_{BB} and V_{CC} . The BJT was first biased so that base-emitter voltage V_{BE} was approximately 0.67 V , a typically observed value in the circuit in study, by applying $V_{BB} = 1.45 \text{ V}$, while the other voltage source V_{CC} was stepped from 0 V to 3.5 V . To compute perform measurements of the currents, external current sensing resistors are used. The base resistor was measured as $R_B = 99.51 \text{ k}\Omega$ and collector resistor $R_C = 1 \text{ k}\Omega$. For typical current gains of over 100, these resistor values guarantee a good resolution

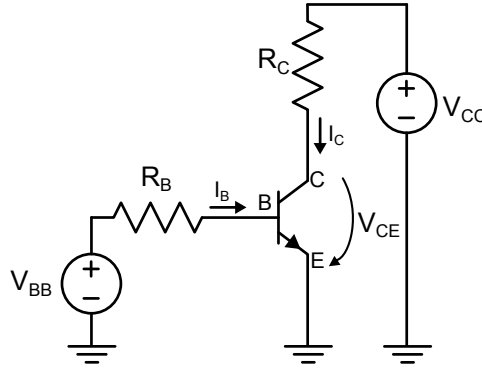


Figure 4.5: Test circuit for extracting the current gain of the BJT.

of the data extracted. Measurements were taken for the voltage across base resistor V_{R_B} and collector-emitter voltage V_{CE} . The currents I_B and I_C were computed from Ohm's Law using $I_B = \frac{V_{R_B}}{R_B}$ and $I_C = \frac{V_{CC} - V_{CE}}{R_C}$ and consequently the current gain was obtained from $\frac{I_C}{I_B}$.

4.1.3.1 Implementation for the Non-linear Solver

The non-linear equations describing the BJT are implemented as seen in the Sourcecode 4.5.

```

1 Ix1 = Ies*(exp(Vx(1)/Vt) - 1)*(alphaF - 1) + Ics*(exp((Vx(1) - Vx(2))/Vt)
  - 1)*(alphaR - 1);
2 Ix2 = Ics*(exp((Vx(1) - Vx(2))/Vt) - 1) - Ies*alphaF*(exp(Vx(1)/Vt) - 1)
  .* (1 - ((Vx(1) - Vx(2))/Va));
3
4 dIx1dVx1 = Ies*exp(Vx(1)/Vt)*(alphaF - 1)/Vt + (Ics*exp((Vx(1) - Vx(2))/
  Vt)*(alphaR - 1))/Vt;
5 dIx1dVx2 = -(Ics*exp((Vx(1) - Vx(2))/Vt)*(alphaR - 1))/Vt;
6 dIx2dVx1 = (Ics*exp((Vx(1) - Vx(2))/Vt))/Vt + (Ies*alphaF*(exp(Vx(1)/Vt) -
  1))/paramQ2.Va + (Ies*alphaF*exp(Vx(1)/Vt)*((Vx(1) - Vx(2))/paramQ2.Va
  - 1))/Vt;
7 dIx2dVx2 = -(Ics*exp((Vx(1) - Vx(2))/Vt))/Vt - (Ies*alphaF*(exp(Vx(1)/Vt)
  - 1))/paramQ2.Va;

```

Sourcecode 4.5: Non-linear equations of the BJT for the non-linear solver.

Here, I_{x1} and I_{x2} represent the base current I_B (eq. 3.10) and the collector current I_C (eq. 3.12) respectively, while $V_x(1)$ and $V_x(2)$ account for the non-linear voltages V_{BE} and V_{CE} . The existence of 2 current equations and 2 non-linear voltages requires the derivative to be represented by a Jacobian matrix, for which the first-order partial derivatives are calculated through lines 4 and 7.

4.1.4 Junction Field-effect Transistor

The JFET model described in 3.1.3 can be defined by Equations 3.15 3.16, therefore four parameters can be identified for extraction: the gate saturation current I_S , saturated drain current I_{DSS} , threshold voltage V_{Th} and the empirical constant λ . One of the main characteristics of

a JFET is that it is a voltage-controlled device and it draws little to none gate current. For this reason, and because the interest relies on its output characteristics, a standard value of $10e^{-14}$ A, used in the simulation software SPICE2, is defined for this parameter. The maximum value of drain current I_D occurs in the saturation region for $V_{GS} = 0$ and it is the designated I_{DSS} . The threshold voltage is the most important parameter in modeling the JFET as it represents the value at which conduction starts to occur. The procedure for its extraction is based on the Extrapolation in the Linear Region (ELR) method [24]. A small drain voltage V_D of 10 mV is applied to the JFET to keep it in the linear region and I_D is plotted against an increasingly negative gate-source voltage V_{GS} . A linear curve is traced tangentially to the point of maximum slope in the plotted data to find its intercept with the x-axis, where $I_D = 0$. To this value, a voltage $\frac{V_D}{2}$ is subtracted to find the threshold voltage V_{Th} . The procedure is shown in the Sourcecode 4.6. Data collection was performed with the JFET connected as shown in Figure 4.6.

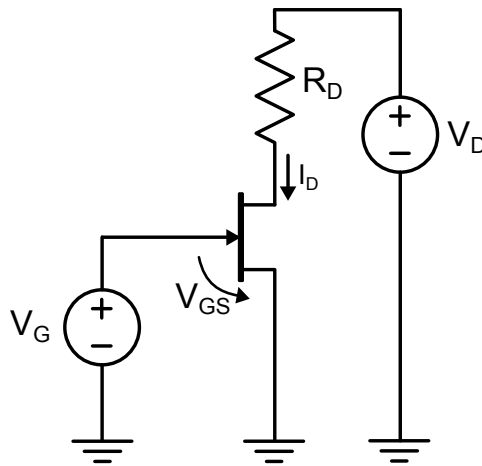


Figure 4.6: Test circuit for extracting the threshold voltage of the JFET.

Gate voltage V_G is stepped from -2 V to 0 V while V_D is kept constant at 10 mV. A current sensing resistor measured with $R_D = 10.2 \Omega$ is placed. The gate-source voltage V_{GS} is directly measured with one multimeter while the drain current is computed from the voltage across the drain resistor with $\frac{V_{R_D}}{R_D}$.

```

1 gm = diff(i_ds) ./ diff(v_gs);
2 i = find(gm == max(gm));
3 m = (i_ds(i+1) - i_ds(i)) / (v_gs(i+1) - v_gs(i));
4 b = i_ds(i) - m * v_gs(i);
5 vth = -b/m - v_ds/2;

```

Sourcecode 4.6: Parameter extraction script for the threshold voltage of the JFET.

The recorded datasets v_gs and i_ds are used to compute the slope across the curve I_D vs V_{GS} in line 1. The result represents as well the transconductance of the JFET g_m . In line 2, the point of maximum transconductance is found and afterwards a linear curve (i.e., of the form $y = mx + b$) tangent to this point is derived (line 3 and 4). At the end, the threshold voltage vth is calculated from the intercept of this curve with $i_ds = 0$ and the subtraction of $v_d/2$.

The parameter left to extract is the empirical constant λ used for data fitting of the measured

data and can be obtained with the same test circuit as Figure 4.6 by setting $|V_{DS}| = |V_{Th}|$ and $V_{GS} = 0V$ and computing the relation

$$\lambda = \tanh^{-1}\left(\frac{I_{DP}}{I_{DSS}}\right) \quad (4.3)$$

where I_{DP} is the drain current when $|V_{DS}| = |V_{Th}|$ and $V_{GS} = 0V$ [17].

4.1.4.1 Implementation for the Non-linear Solver

The non-linear equations describing the JFET are implemented as seen in the Sourcecode 4.7.

```

1 if Vx(2) >= 0
2   Ix2 = -Idss*tanh((lambda*abs(Vx(2)))/abs(Vp - Vx(1)))*(Vx(1)/Vp - 1)^2*exp(12*Vx(1)+12)
   / (1+exp(12*Vx(1)+12));
3   dIx2dVx1 = (12*Idss*tanh((lambda*abs(Vx(2)))/abs(Vp - Vx(1)))*exp(24*Vx(1) + 24)*(Vx(1)/
   Vp - 1)^2)/(exp(12*Vx(1) + 12) + 1)^2 - (12*Idss*tanh((lambda*abs(Vx(2)))/abs(Vp -
   Vx(1)))*exp(12*Vx(1) + 12)*(Vx(1)/Vp - 1)^2)/(exp(12*Vx(1) + 12) + 1) - (2*Idss*tanh
   ((lambda*abs(Vx(2)))/abs(Vp - Vx(1)))*exp(12*Vx(1) + 12)*(Vx(1)/Vp - 1))/(Vp*(exp
   (12*Vx(1) + 12) + 1)) + (Idss*lambda*exp(12*Vx(1) + 12)*abs(Vx(2))*sign(Vp - Vx(1))
   *(tanh((lambda*abs(Vx(2)))/abs(Vp - Vx(1)))^2 - 1)*(Vx(1)/Vp - 1)^2)/(abs(Vp - Vx(1)
   )^2*(exp(12*Vx(1) + 12) + 1));
4   dIx2dVx2 = (Idss*lambda*exp(12*Vx(1) + 12)*sign(Vx(2))*tanh((lambda*abs(Vx(2)))/abs(Vp -
   Vx(1)))^2 - 1)*(Vx(1)/Vp - 1)^2)/(abs(Vp - Vx(1))*(exp(12*Vx(1) + 12) + 1));
5 else
6   Ix2 = Idss*tanh((lambda*abs(Vx(2)))/abs(Vp - Vx(1)+Vx(2)))*((Vx(1)-Vx(2))/Vp - 1)^2*exp
   (12*Vx(1)+12)/(1+exp(12*Vx(1)+12));
7   dIx2dVx1 = (12*Idss*exp(12*Vx(1) + 12)*tanh((lambda*abs(Vx(2)))/abs(Vp - Vx(1) + Vx(2)))
   *((Vx(1) - Vx(2))/Vp - 1)^2)/(exp(12*Vx(1) + 12) + 1) - (12*Idss*exp(24*Vx(1) + 24)*
   tanh((lambda*abs(Vx(2)))/abs(Vp - Vx(1) + Vx(2)))*((Vx(1) - Vx(2))/Vp - 1)^2)/(exp
   (12*Vx(1) + 12) + 1)^2 + (2*Idss*exp(12*Vx(1) + 12)*tanh((lambda*abs(Vx(2)))/abs(Vp
   - Vx(1) + Vx(2)))*((Vx(1) - Vx(2))/Vp - 1))/(Vp*(exp(12*Vx(1) + 12) + 1)) - (Idss*
   lambda*exp(12*Vx(1) + 12)*sign(Vp - Vx(1) + Vx(2))*abs(Vx(2))*((Vx(1) - Vx(2))/Vp -
   1)^2*(tanh((lambda*abs(Vx(2)))/abs(Vp - Vx(1) + Vx(2)))^2 - 1))/(abs(Vp - Vx(1) + Vx
   (2))^2*(exp(12*Vx(1) + 12) + 1));
8   dIx2dVx2 = - (2*Idss*exp(12*Vx(1) + 12)*tanh((lambda*abs(Vx(2)))/abs(Vp - Vx(1) + Vx(2)))
   *((Vx(1) - Vx(2))/Vp - 1))/(Vp*(exp(12*Vx(1) + 12) + 1)) - (Idss*exp(12*Vx(1) + 12)
   *((Vx(1) - Vx(2))/Vp - 1)^2*(tanh((lambda*abs(Vx(2)))/abs(Vp - Vx(1) + Vx(2)))^2 -
   1)*((lambda*sign(Vx(2)))/abs(Vp - Vx(1) + Vx(2)) - (lambda*sign(Vp - Vx(1) + Vx(2))*
   abs(Vx(2)))/abs(Vp - Vx(1) + Vx(2))^2))/(exp(12*Vx(1) + 12) + 1);
9 end
10
11 Ix1 = -Igs*(exp((Vx(1) - Vx(2))/Vt) + exp(Vx(1)/Vt) - 2);
12 dIx1dVx1 = -Igs*(exp(Vx(1)/Vt)/Vt + exp((Vx(1) - Vx(2))/Vt)/Vt);
13 dIx1dVx2 = (Igs*exp((Vx(1) - Vx(2))/Vt))/Vt;

```

Sourcecode 4.7: Non-linear equations of the JFET for the non-linear solver.

The if-block of lines 1 to 9 implement the drain current equation (eq. 3.16) and corresponding partial derivatives, where $Vx(1)$ and $Vx(2)$ stand for V_{GS} and V_{DS} , correspondingly. Here, a weighting factor $\frac{e^{12V_{GS}+12}}{1+e^{12V_{GS}+12}}$ of logistic form is required in order to guarantee the correct V_{GS} vs. I_D behaviour for values below the threshold voltage ($V_{GS} < V_{Th}$) as shown in Figure 3.6. This is explained by the modulus nature of the hyperbolic tangent approximation used to describe the drain current (3.1.3), that results in an increase in current for $V_{GS} < V_{Th}$ when in reality is tending towards zero (JFET off). From lines 11 to 13, the gate current is given by I_{x1} with corresponding partial derivatives.

4.2 Circuit Prototype

Throughout the implementation of the digital simulation, not only the circuit schematic provided by UREI [10] and shown in section 2.2.1 served as a reference but, most important, a prototype of the circuit was built (Fig. 4.7), based on the M.NATS 1176LN REV D V2.2 [25] printed circuit board of the same revision. The state-space implementation is based on both linear and non-linear components used throughout the assembly of this prototype. While it fully implements the block diagram shown in Figure 2.6, the built prototype strips the circuit out of some of the original features, namely the transformer-balanced input connection, the internal power supply unit and the VU meter. The assumption made is that these features don't have influence on the operation of the circuit and realization of the DRC. On the other hand, the prototype features an unbalanced input connector; it is supplied with +30 V and -10 V voltage rails by a TOE 8433 power supply; and signal visualization is made possible with the use of a HAMEG HMO03524 oscilloscope.

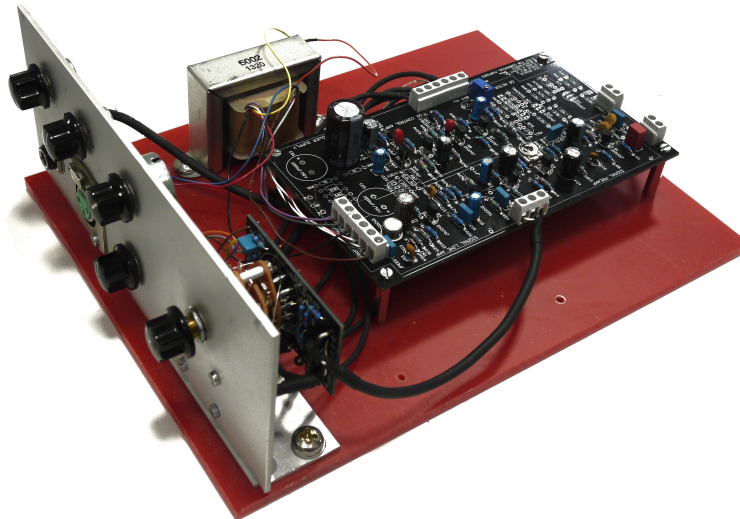


Figure 4.7: UREI 1176LN circuit prototype.

4.2.1 Component Measurement

Each used component was previously tested and a measurement of its correct value was taken. The state-space implementation is then implemented with the measured values, assuring that it is as close as possible to the circuit in test. The measurements for resistors, capacitor and potentiometer values can be found in Appendix A.

4.2.2 Circuit Calibration

In order to guarantee the proper operation of the circuit, further adjustments need to be performed. The most important one is the Q Bias Adjustment, critical for the realization of DRC.

4.2.2.1 Q-Bias Adjustment

The Q Bias Adjustment is the only adjustment that directly affects the compression response of the circuit. It is performed by adjusting the variable resistor R59 in the GRCA block of the circuit (Fig. 2.9). The function of this variable resistor is to set a correct quiescent bias of the signal going out from the GRCA to the VVRA. What one does while performing this adjustment is to directly set a quiescent voltage in the gate of the JFET that is close to its threshold voltage V_{Th} . This means that the JFET is put into a slight conduction mode and that the further transients generated by the GRCA will affect conduction across the JFET.

The first step in order to perform this adjustment is to apply a signal to the input (1 kHz, 0 dBu) with R59 completely turned counter-clockwise. At this stage, the gate of the JFET is set much more negative than its threshold voltage and thus no drain current flows. This means that the maximum signal passes the VVRA and no attenuation is performed by the JFET. By being biased at a value far from the threshold voltage, no transient from the GRCA can cause the JFET to conduct. In other words, no threshold of compression can be reached. The input control potentiometer is then raised from $-\infty$ up to a point where the oscilloscope reads 5 dBu at the output of the compressor, and R59 is adjusted until a drop of 1 dB is observed and the oscilloscope read 4 dBu. This process sets the gate bias of the JFET close to the threshold voltage hence setting it into slight conduction. This guarantees that further transients from the GRCA will result in gain reduction.

4.3 State-space Implementation

In this section, the implementation of the state-space model first approached in Chapter 3 is applied to the UREI 1176LN circuit described in section 2.2.1. First, several adaptations to the circuit are discussed and finally the resulting circuit and state-space model is presented. For the purpose of this work, the Line Amplifier is assumed to be linear and therefore focus will be given to the modeling of the fundamental blocks in the DRC effect: the Voltage-variable Resistor Attenuator, the Signal Preamplifier and the Gain Reduction Control Amplifier.

Several adaptations of distinct nature have been applied to the original circuit in order to optimize its digital implementation. Two different classes of adaptations can be identified: circuit simplifications that don't affect its behaviour for the purpose of this work, and adaptations necessary for the application of the nodal DK method.

4.3.1 Circuit Simplifications

The first simplification and a minor one is the non-inclusion of capacitor C2 present in the Signal Preamplifier block (Fig. 2.8). This 27 pF capacitor is placed at the input of the first BJT stage in order to assure filtering of radio-frequency interference (RFI). This might be an

issue when dealing with analog circuitry but definitely not in a software implementation. The removal of this capacitor from the circuit in study allows for less state variables (see section 3.2) hence improving the performance of the simulation, even if only slightly.

More significant is the implementation of the Compression Ratio push-buttons. As presented in Chapter 2, the UREI 1176LN features four compression ratios selectable with four push-buttons. This is done by controlling the series element of a voltage divider via a switched resistor ladder. In fact, it controls two voltage dividers acting on different parts of the circuit. The first one is fitted in the path between the output of the Signal Pre-amplifier and the GRCA. Its function is to determine the level of the signal that is sent to the GRCA. Another voltage divider is connected to the GRCA and affects it by applying a bias level to the rectifying diodes D1 and D2 (Fig. 2.9), hence controlling the threshold of compression. From these two voltage dividers one can acknowledge how each selected compression ratio results in different amounts of compression and different threshold of compression. Shown in Figure 4.8 is the original implementation of the first described voltage divider and the resulting simplification.

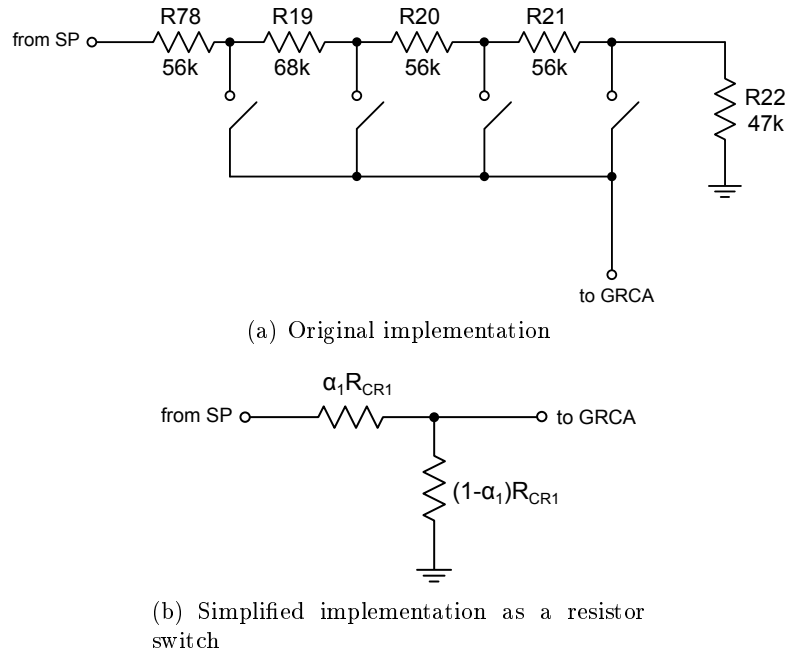


Figure 4.8: *Compression Ratio push-buttons implementation.*

By taking the overall resistance value as the sum of all resistors in the voltage divider of Figure 4.8(a) one can represent the push-button selection as a variable resistor switch with fixed discrete resistor values, so that α_1 takes a set of values defined for each selected button. The same procedure is assumed for the second voltage divider already described.

4.3.2 Adaptations for Nodal DK Method

The solution of the state-space system presented in section 3.2 requires that the system matrix of Equation 3.50 is invertible so that the state-space matrices can be obtained. This equation relates the resistors, capacitors and inputs to each node of the circuit. In case of a node to which none of this elements is connected (floating node), the resulting S_0 matrix will be singular and

no solution of the system can be obtained. Such situations are not so uncommon in analog circuits and require special attention. Another problems may arise with convergence aspects of the non-linear iterative solver. In the case of the UREI 1176LN circuit this happens too and adaptations are suggested here.

The first encountered problem was found to happen when consecutive BJT stages link the collector of the first BJT to the base of the second BJT on the same node, as can be seen in both SP and GRCA blocks. This introduce convergence problems within the non-linear iterative solver where the solution of one BJT is directly dependent on the other. This is solved by introducing $1\ \Omega$ resistors in between the stages, hence making them independent in the view of the non-linear solver.

Another problem related to floating nodes was observed from the use of potentiometers. Both output and attack potentiometers introduced floating nodes. To avoid these, resistors are connected in parallel to the potentiometer so that resistance values are maintained, as shown in Figure 4.9.

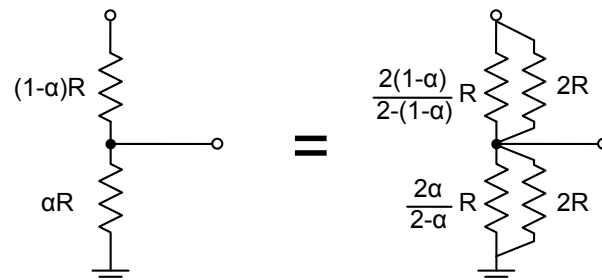


Figure 4.9: Substitution of potentiometer to avoid floating nodes [26].

4.3.3 State-space Model

The circuit to be implemented as a state-space model is shown in Figure 4.10 with the resulting adaptations and measured component values. Potentiometers are highlighted in the dashed areas and a total of 50 nodes were identified and numbered.

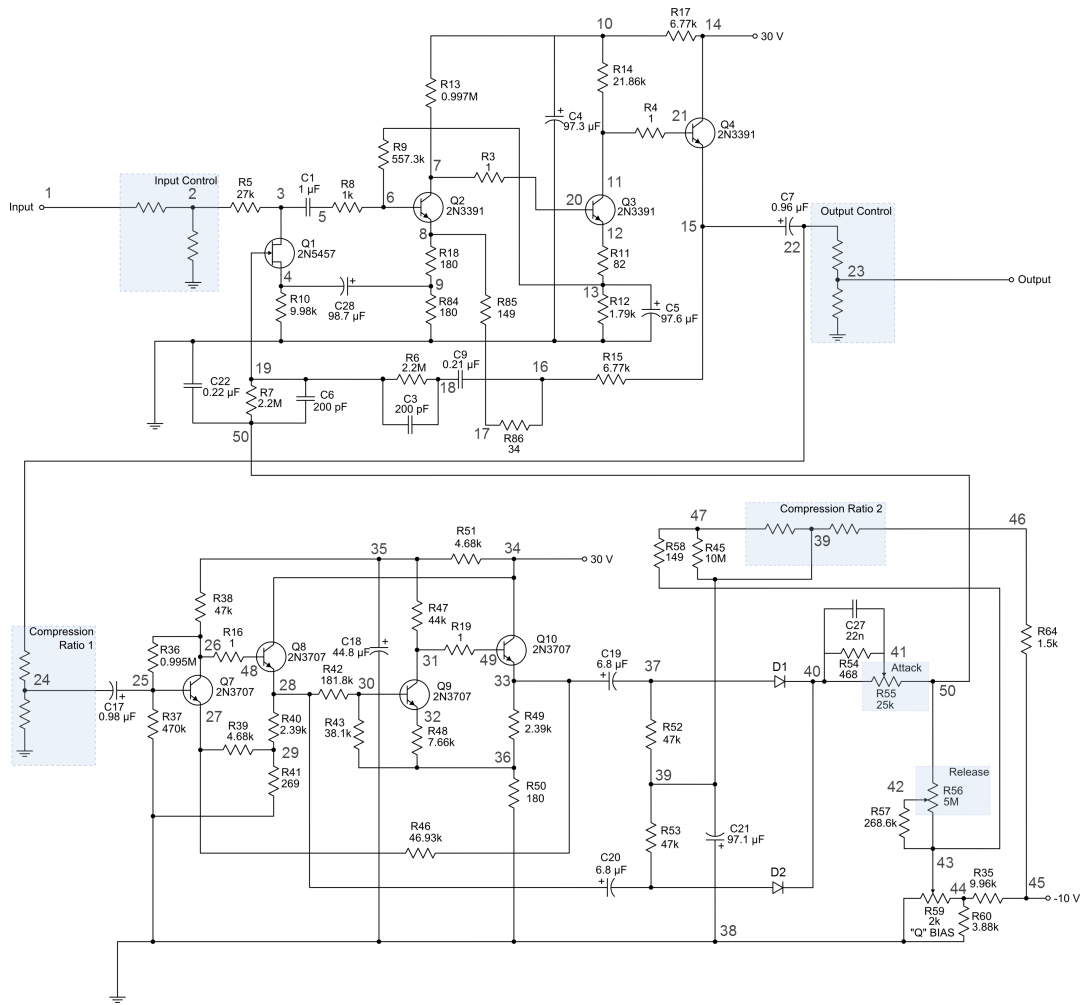


Figure 4.10: Circuit schematic to be implemented as a state-space model.

The incidence matrices (defined in section 3.3) resulting from the nodal analysis are shown in Appendix B. The 45 resistors seen in the circuit plus the augmented 4 from the potentiometer substitution described in 4.3.2 give a matrix N_R of size 49×50 with each of the 50 nodes described by each column. Fifteen capacitors are present and so N_x is of size 15×50 . Each potentiometer is modelled by two resistors so the six potentiometers shown in the circuit give N_v of size 12×50 . Furthermore, 10 non-linear devices are used: seven BJTs, one JFET and two diodes. BJTs are described by their base-emitter and collector-emitter voltages (V_{BE} and V_{BC}), JFETs are similarly described by the gate-source and drain-source voltages (V_{GS} and V_{DS}) and the two diodes are solely described by the voltage across them V_D . This results in a matrix N_n of size 18×50 . Finally, N_u is comprised of 4 rows, one for the input signal (node 1), two for the 30 V supply rail (nodes 14 and 34), and one for the 10 V rail (node 45), while N_o states the only output to be taken from node 23, resulting in a 1×50 matrix.

4.3.4 User Controls

Aside from the matrix description of the circuit elements positioning and their values, a set of dynamic controls that complement the state-space system have to be defined. More specifically, the user controls that make part of the unit front panel as mentioned in Chapter 2 and visible in Figure 4.11.



Figure 4.11: Front view of the Universal Audio 1176LN.

For each of the continuously variable potentiometers (Input, Output, Attack, Release), static positions were chosen to represent typical usage of the unit. These were defined as marked in the original unit front panel, and measurements of the voltage divider resistances were taken while different positions were tested in the prototype. This allows one to calculate the multiple values of the constant α that multiply with the potentiometers resistor values forming the voltage divider. The positions defined taking as reference the unit front panel and the corresponding measurements yielded the α values observed in Table 4.1. Similarly, the compression ratio push-buttons form two voltage dividers, as explained in 4.3.1 and visible in Figure 4.10, where they are labelled Compression Ratio 1 (CR1) and Compression Ratio 2 (CR2). The measurement of their resistance values provided Table 4.2.

The α values are then multiplied with the measured potentiometer and switch overall resistance values as shown in Tables A.3,A.4.

Potentiometer	Position	α
Input	24	0.87
	18	0.67
	12	0.36
	6	0.02
Output	36	0.97
	30	0.94
	24	0.91
	18	0.79
	12	0.41
Attack	1	0.00
	3	0.36
	5	0.73
	7	1.00
Release	1	1.00
	3	0.68
	5	0.27
	7	0.00

Table 4.1: *Parameters of the user controls.*

Potentiometer	Position	α
4:1	CR1	0.835
	CR2	0.000
8:1	CR1	0.636
	CR2	0.186
12:1	CR1	0.438
	CR2	0.407
20:1	CR1	0.199
	CR2	0.999

Table 4.2: *Parameters of the Compression Ratio push-buttons*

4.3.5 Calibration

With a matrix model of the circuit implemented and the equations of the non-linear devices described with their corresponding parameters, the simulation was ready to compute a solution of the state-space system. The first simulations followed somewhat similar procedures as those expected of troubleshooting an hardware unit. These include an initial performance check as well as circuit calibration, particularly the Q-Bias adjustment 4.2.2.1. Both hardware calibration procedures require that compression is disabled in the circuit and this is typically accomplished by shorting node 24 (Fig. 4.10) to ground, thus avoiding the audio signal from feeding the GRCA block. The same thing is required for calibrating the state-space simulation and, for that matter, the following procedures were implemented with the same node shorted to ground in the matrix description of the circuit.

First, a performance check consisting of feeding a sine wave signal of approximately 0 dBu (0.775 Vrms), turning the Input control to approximately half-rotation (position 24) and adjusting the Output control until +4 dBu were measured at the output was performed. In the case of the hardware unit, this certifies that the audio signal path in the unit is performing as expected. In the context of the simulation, a simultaneous measurement of the voltage across the signal path in the unit, allowed one to compare it with the signal evolution in the simulation, and because the output of the hardware unit is taken after the Line Amplifier (not implemented in the state-space system), one could find the gain of this stage and implement it as a scaling factor applied to the signal in node 23. This measurement resulted in a gain of 18.33 V/V (25.26 dB) for the Line Amplifier stage and the first simulation was performed successfully.

Secondly, the Q-Bias adjustment was performed. The procedure consisted in applying a sine wave of 1 kHz and 0 dBu, turning the Input control until the output read 5 dBu, with the Output control set in the maximum rotation, and turning the Q-Bias Adjust (R59) until a drop of 1 dB occurred in the output. This resulted in consecutive simulations and finally R59 was decomposed as two resistors with the values $R59a = 0.4885 \text{ k}\Omega$ and $R59b = 1.5125 \text{ k}\Omega$. This setting assured the circuit was now calibrated accordingly to the prototype.

Chapter 5

Results and Evaluation

In this chapter, two categories of results are presented. First, results of the device parameter extraction methods described in the previous chapter are shown and afterwards the final results are presented and discussed taking into account a comparison between audio tests performed in both the simulation and the circuit prototype.

5.1 Parameter Extraction Results

Several parameter extraction methods have been described in Chapter 4 attempting at approximating the real devices used in the circuit to the models described in Chapter 3. In more detail, a total of ten non-linear devices are present in the circuit (two diodes, seven BJTs and one JFET) and the parameters used to model these are found below.

5.1.1 Diode Parameters

Two diodes of type FDH333 are used to perform signal rectification in the GRCA (Chapter 2) and labeled D1 and D2. The process for extracting the parameters used in the diode model was introduced in 4.1.2 and the results are here presented for both diodes.

Figure 5.1 shows the semi-logarithmic plot of the collected current-voltage data. Comparing with the idealized plot of Figure 4.2, it is clear that real diodes show a deviation from the ideal model: while the semi-logarithmic I-V characteristic of an ideal model tends to a linear curve early at about 0.2 V, measurements of the real diodes only provide coherent data at a later point. This is, however, in agreement with the known operation of silicon and germanium devices, for which significant conduction is only achieved for voltage values greater than their threshold voltage [15]. The script detailed in Sourcecodes 4.1,4.2 came in use at this point and provided the data range for which parameter extraction is less erratic. Without surprise, these came to be approximately the same for both diodes, between 0.60 V and 0.67 V, a range at which the semi-logarithmic current data (in blue) seems to better approximate a linear curve, and coherent with the idea of the diode threshold voltage being achieved. This range is delimited in Figure 5.1 by the two dashed vertical lines seen in both plots.

With the significant data range defined, the diode saturation current and emission coefficient

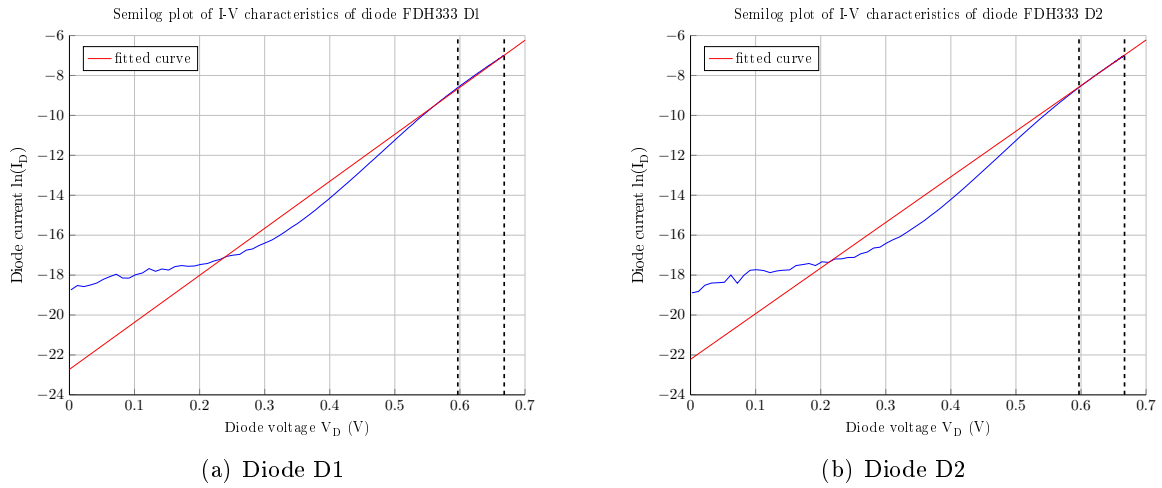


Figure 5.1: Semi-logarithmic plots of I - V characteristics of diodes $D1$ and $D2$.

can be retrieved in the last step of the parameter extraction script (Sourcecode 4.3), and the results are presented in Table 5.1.

	I_S	n
D1	2.7791×10^{-10} A	1.7102
D2	2.2455×10^{-10} A	1.6831

Table 5.1: Extracted parameters of diodes $D1$ and $D2$.

With these values, the Shockley diode equation (3.2) can be computed for any value of voltage applied to the diode. In order to validate the model described by this equation, the exact same voltage values used throughout the measuring process (Fig. 4.1) were used to compute the current, providing a direct comparison between the simulated and the measured I - V curves. The result is shown in Figure 5.2, in which the blue curve represents the simulated model while the red dashed curve respects the measured data.

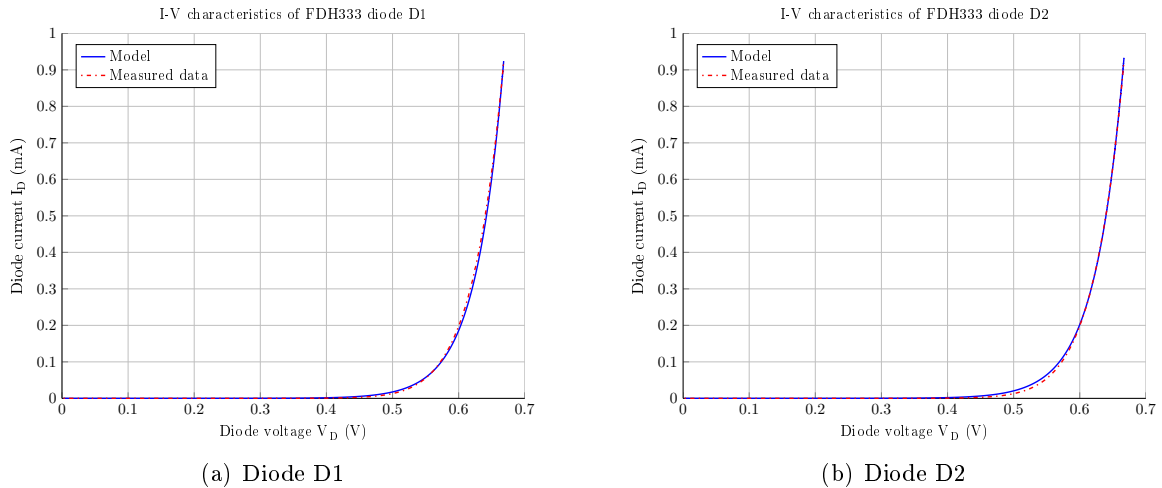


Figure 5.2: I - V characteristics of diodes $D1$ and $D2$.

From a first inspection of both curves, it is clear that the model closely follows the measured data and that both behave accordingly to what is expected from a diode. Further analysis is performed by plotting the residual error of the model in respect to the measured data (Fig. 5.3). This value is computed as the absolute value of the difference between the two.

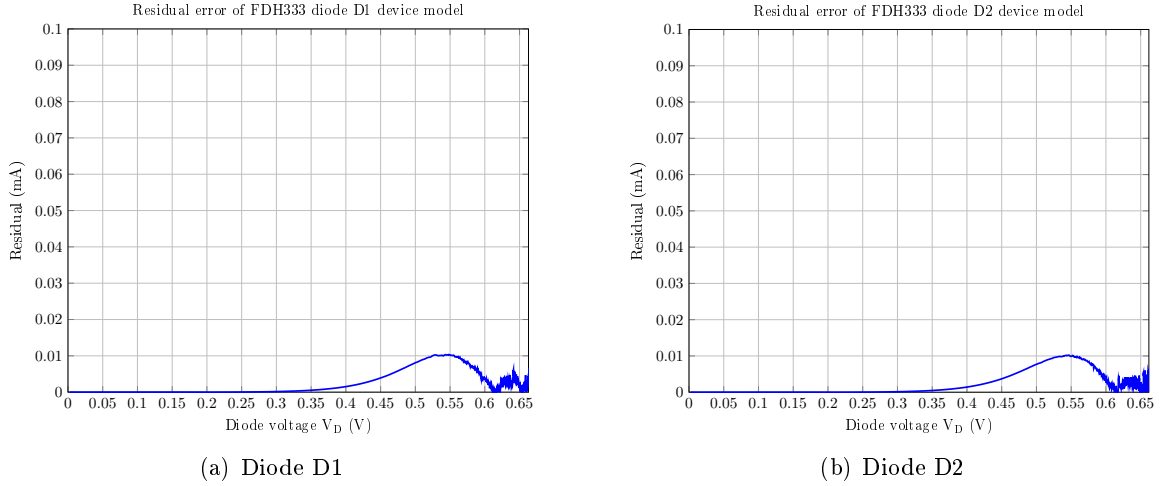


Figure 5.3: *Residual error of the diode device model.*

Figure 5.3 shows a similar behaviour for both diodes. The maximum residual error is observed approximately at 0.55 V, at the brink of significant conduction, after which it decreases and is maintained below this value. The maximum residual error calculated was $10.34 \mu\text{A}$ for D1 and $10.22 \mu\text{A}$ for D2, both values that represent a negligible difference in current. This leads to the satisfactory conclusion that the implemented model accurately simulates the device, for the context of this thesis.

5.1.2 BJT Parameters

In total, an amount of 7 BJTs are present in the implemented circuit. The Signal Preamplifier block makes use of 3 of the type 2N3391 (labeled Q2, Q3 and Q4), while the remaining 4, consisting of type 2N3707 (labeled Q7, Q8, Q9 and Q10), are present in the GRCA block. Here, each type of BJT is represented by a single device, an assumption made possible after verification of similar behaviour between same species during the measurement process. The first stage of parameter extraction follows the same method used for the diode, as discussed in Chapter 4, and is depicted in Figures 5.4,5.5, yielding the results for the saturation current of each BJT junction.

Figure 5.4 shows the semi-logarithmic plots of voltage-current for each junction in the two species of BJTs. The results showed coherent behaviour in each of the four different cases (two junctions for each BJT). Data ranges selected for consideration were approximately defined in between 0.53 V and 0.57 V in all cases and shown in the vertical dashed lines. The parameters extracted at this stage, presented in Table 5.2, resulted again in close approximations between the Shockley diode equation and the junction characteristics of each BJT, as can be observed in Figure 5.5. These results constitute no surprise as the diode device model, on which they

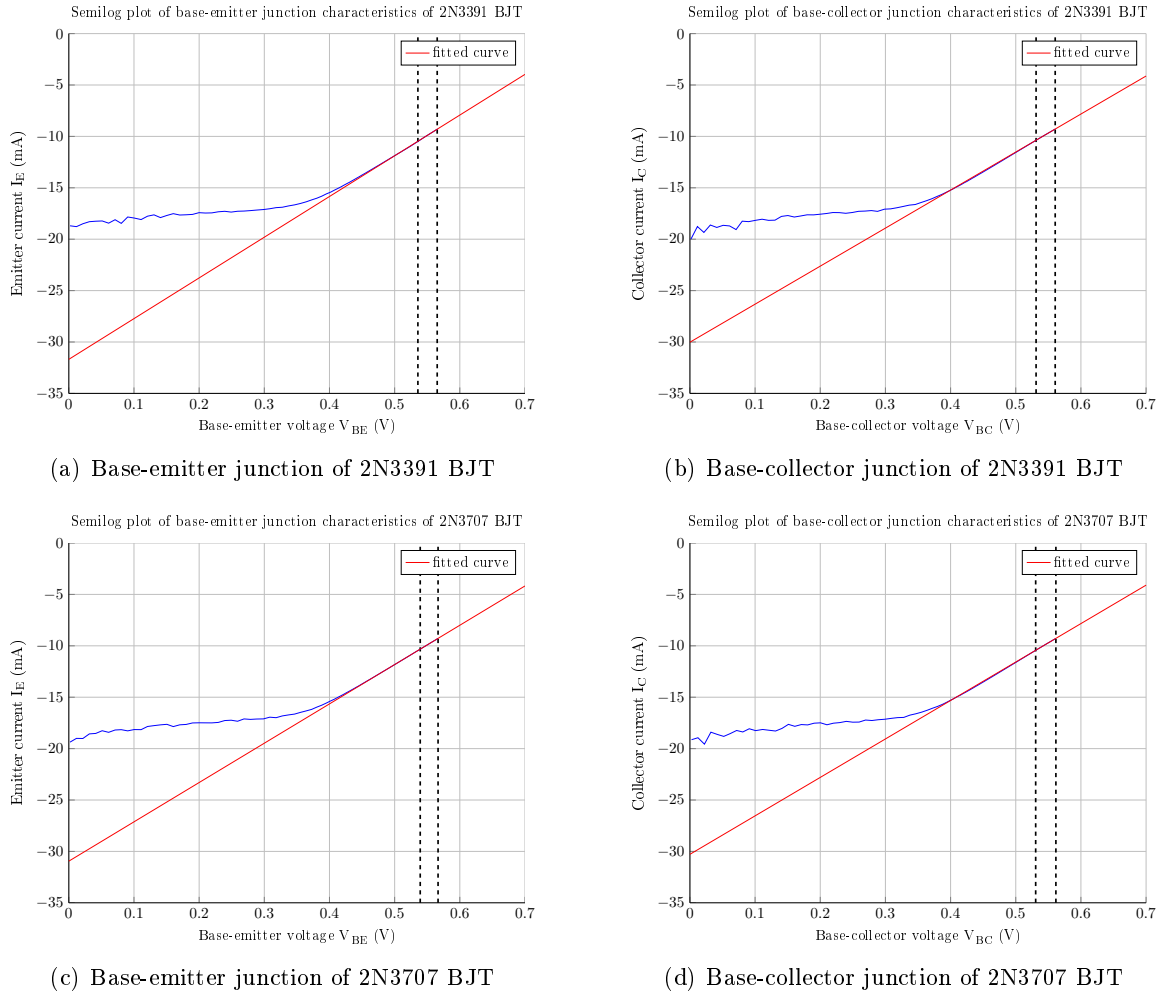
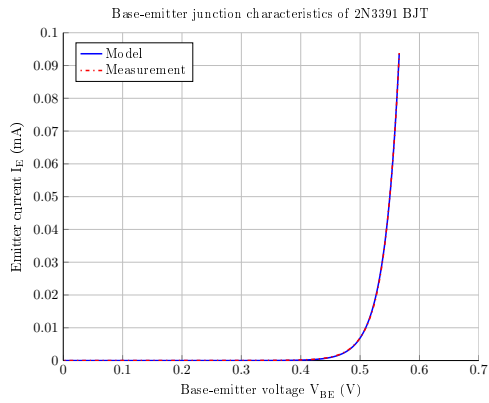


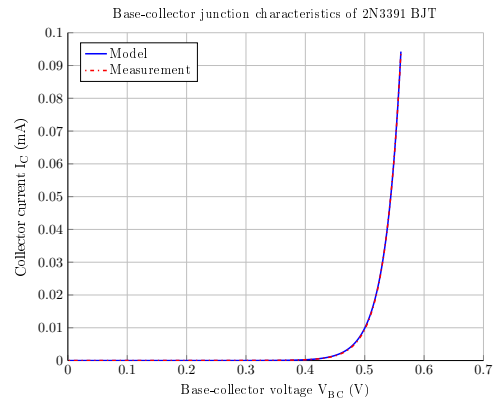
Figure 5.4: Semi-logarithmic plots of I - V characteristics of each junction in the BJT.

are based, was already validated in this section.

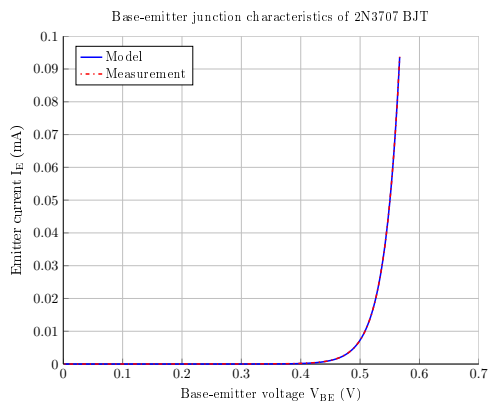
The extraction of the forward and reverse current gains is achieved by plotting the ratio $\frac{I_C}{I_B}$ against V_{CE} and taking the value at which it saturates for increasing voltage. Figure 5.6 shows such plots for both BJT species, where the blue curve represents the mentioned current ratio, known as β_F , and the horizontal red dashed line signals its value in the saturation region. The forward current gain β_F was found to be 293.5 for the 2N3391 and 315.9 for the 2N3707 BJTs. This value was then computed to provide α_F , which in conjunction with the saturation current of each junction, extracted before, allows the computation of reverse current gain α_R (Chapter 4). The four parameters are summed in Table 5.2.



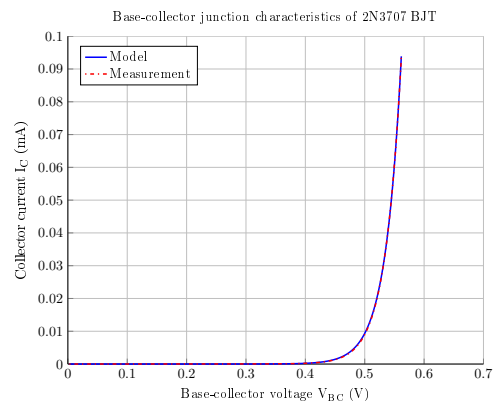
(a) Base-emitter junction of 2N3391 BJT



(b) Base-collector junction of 2N3391 BJT

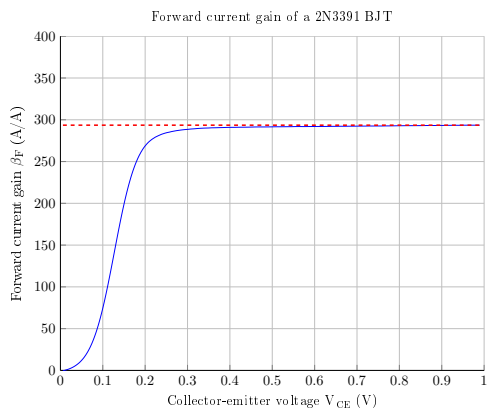


(c) Base-emitter junction of 2N3707 BJT

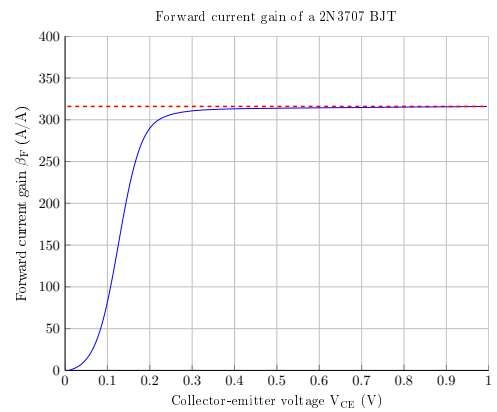


(d) Base-collector junction of 2N3707 BJT

Figure 5.5: *I-V characteristics of each junction in the BJT.*



(a) 2N3391



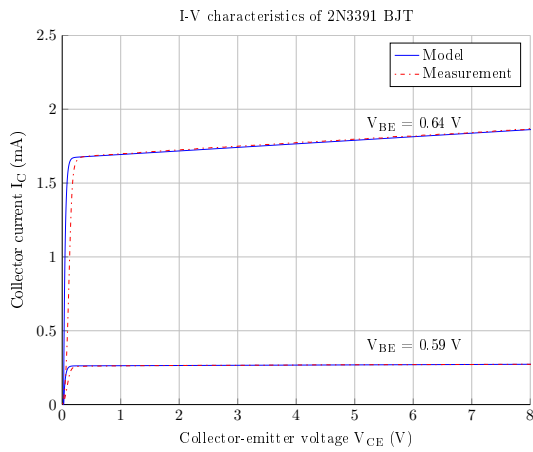
(b) 2N3707

Figure 5.6: *Forward current gain of the BJT.*

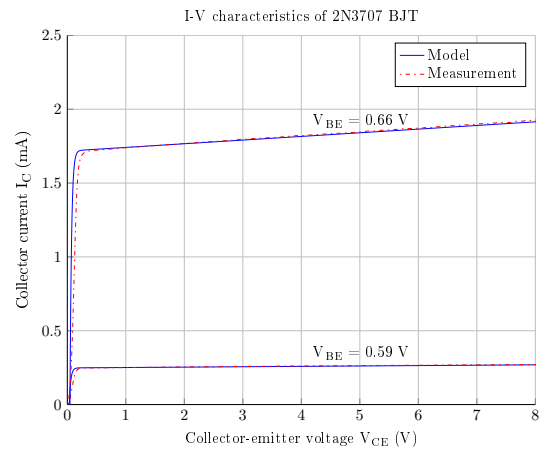
	I_{ES}	I_{CS}	α_F	α_R
2N3391	3.55×10^{-14} A	9.17×10^{-14} A	0.9966	0.38
2N3707	3.35×10^{-14} A	10.2×10^{-14} A	0.9968	0.28

Table 5.2: *Extracted parameters of the BJTs.*

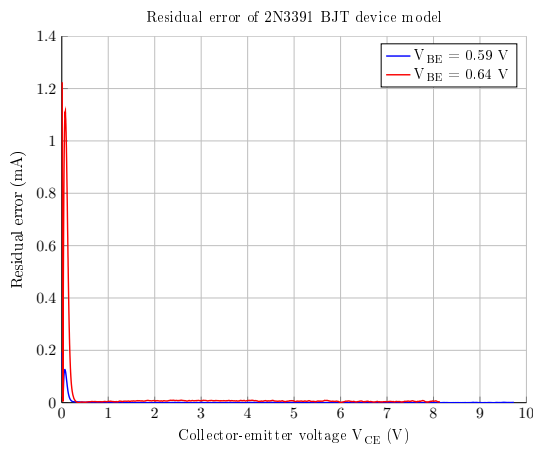
With the 4 parameters extracted, a comparison between the chosen device model and measured data is again possible as depicted in Figure 5.7, in which the blue curve represents the device model and the red dashed curve represents the measured data. Two sets of data were chosen from the measurements with base-emitter voltage V_{BE} as criteria. The two values observed in each plot of this figure attempt to represent similar voltages as observed in the circuit, shown further in this chapter (Table 5.5), so that one can more accurately simulate the Early effect, which is dependent on the value of V_{BE} . For each case, a linearization of data in the saturation region provided the Early voltage V_A as the intercept of this curve at the voltage axis. For the 2N3391, approximate V_A values of -190 V for $V_{BE} = 0.59$ V and -70 V for $V_{BE} = 0.64$ V were found, while in the case of the 2N3707, these were -96 V for $V_{BE} = 0.59$ V and -70 V for $V_{BE} = 0.66$ V. In both species, the results showed a good approximation in the saturation region while a shift in current is observed in the linear region. This is confirmed in Figure 5.8, where it can be observed that up to approximately 0.3 V there is a significant error. This error is, however, negligible when taking into consideration that all BJTs in the circuit are biased as to operate in the saturation region, where, on the contrary, the residual shows more optimistic results. For the 2N3391, residual is kept below $1 \mu\text{A}$ for $V_{BE} = 0.59$ V and $9 \mu\text{A}$ for $V_{BE} = 0.64$ V. In the case of the 2N3707, residual is kept below $2 \mu\text{A}$ for $V_{BE} = 0.59$ V and $12 \mu\text{A}$ for $V_{BE} = 0.66$ V. Similar values of the residual error were already observed for the diode model, in a magnitude for which its influence in the simulation can be neglected, making the BJT model equally validated.



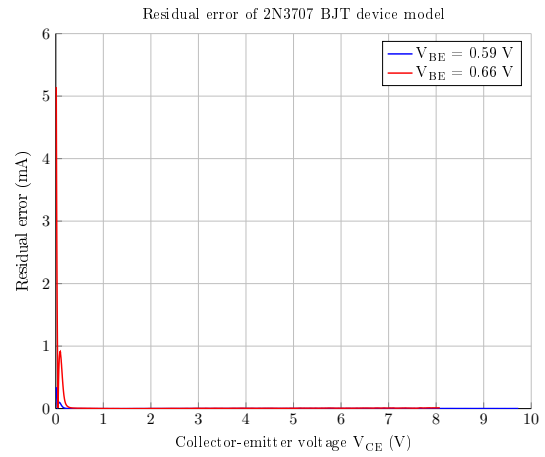
(a) 2N3391



(b) 2N3707

Figure 5.7: *I-V characteristics of the BJT.*

(a) 2N3391



(b) 2N3707

Figure 5.8: *Residual error of the BJT device model.*

5.1.3 JFET Parameters

The only JFET used in the circuit is of type 2N5457 and, as explained in Chapter 4, can be simulated by a model consisting of 3 extracted parameters. The first and most important is the threshold voltage V_{Th} which is obtained from the measurements of drain current I_D for a varying gate-source voltage V_{GS} . Figure 5.9 shows this curve in blue, and a red dashed line tangent to the curve in its point of greater slope, while a drain-source voltage of 10 mV was applied to those JFET terminals, as predicted in the ELR method (4.1.4). The computed value for V_{Th} was -1.1 V.

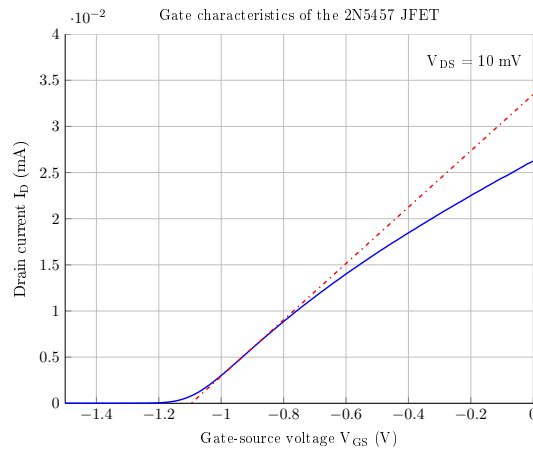


Figure 5.9: Gate characteristic of the 2N5457 JFET.

The two following parameters can be extracted from the plot of the drain current I_D against the drain-source voltage V_{DS} with $V_{GS} = 0$ V, shown in Figure 5.10. The red dashed line provides I_{DSS} , the value at which the drain current saturates for increasing voltage. The calculated result was 2.2 mA. Finally, the empirical constant λ is found from the current value at which V_{DS} is equal to the threshold voltage found before, as depicted in the green dashed lines. Application of equation 4.3, provides then the value 1.2 for this last parameter.

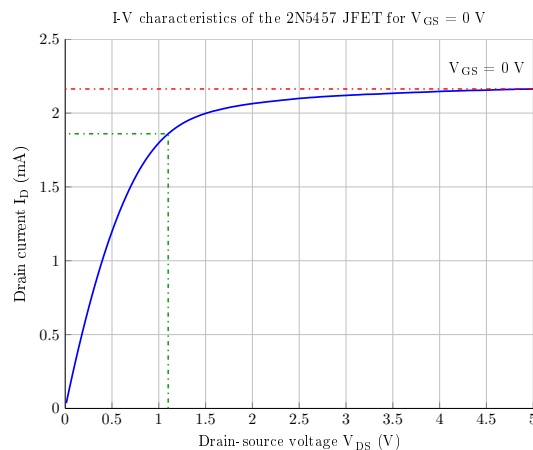


Figure 5.10: I-V characteristics of the 2N5457 JFET for $V_{GS} = 0$ V.

V_{Th}	I_{DSS}	λ
-1.1 V	2.2×10^{-3} A	1.2

Table 5.3: Extracted parameters of the 2N5457 JFET.

The three parameters are summed in Table 5.3 and result in the simulations performed in Figure 5.11.

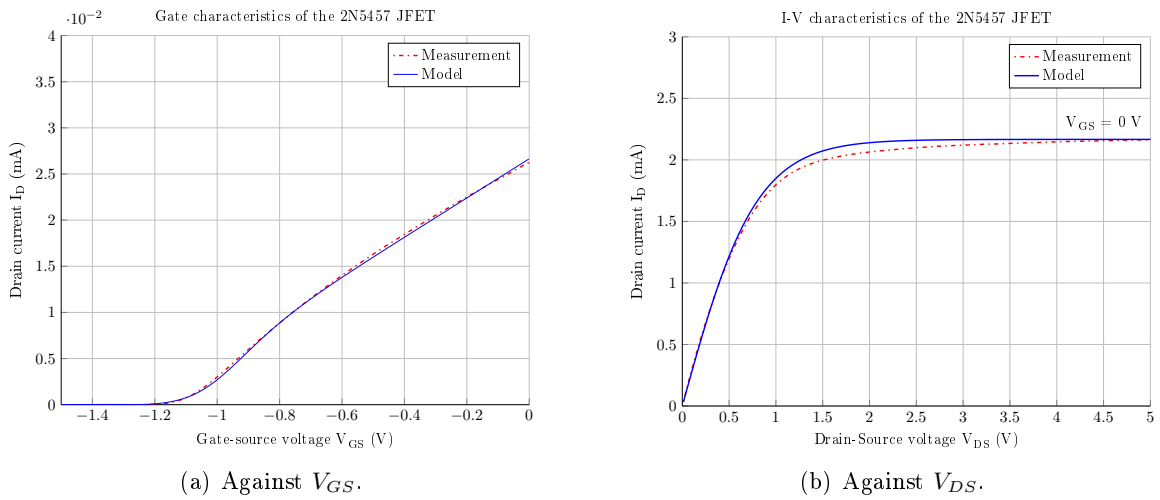


Figure 5.11: I-V characteristics of the 2N5457 JFET.

In Figure 5.11(a), drain current is plotted against the gate-source voltage. Good approximation is critical for this relation, as this represents the controlling voltage responsible for amount of compression. As observed, this requirement was successfully accomplished. The measured data is plotted in dashed red while the simulation provides the blue curve. The curved behaviour towards the threshold voltage results from the weighting function detailed in 4.1.4.1 and assures that the drain current rests at 0 for increasing negative voltage, something that wouldn't occur otherwise due to the modulus nature of the JFET drain current equation (eq. 3.16). Figure 5.11(b) depicts the relation between drain current and drain-source voltage for a fixed gate-source voltage (here of 0 V). The result shows a good approximation up to 1.1 V, which is the pinch-off voltage (absolute value of V_{Th}) and defines the linear region of the drain current. For increasing voltage, the model shows a slightly greater current until it saturates at 2.2 mA. For both figures, residual plots that validate the approximations are shown below (Fig. 5.12).

In Figure 5.12(a), maximum residual calculated was $0.39 \mu\text{A}$ and in the second case it was $78 \mu\text{A}$, values which for the given context represent negligible differences. Furthermore, the range of greater residual in Figure 5.12(b), occurs in the saturation region of the JFET, while the magnitude of the audio in this point of the signal path is in the order of a few millivolts, thus placing the JFET in the linear range of operation, where residual is even smaller.

Once more, very satisfactory results were achieved and one can say that the JFET device model is validated, allowing for the consequent circuit state-space implementation to be evaluated.

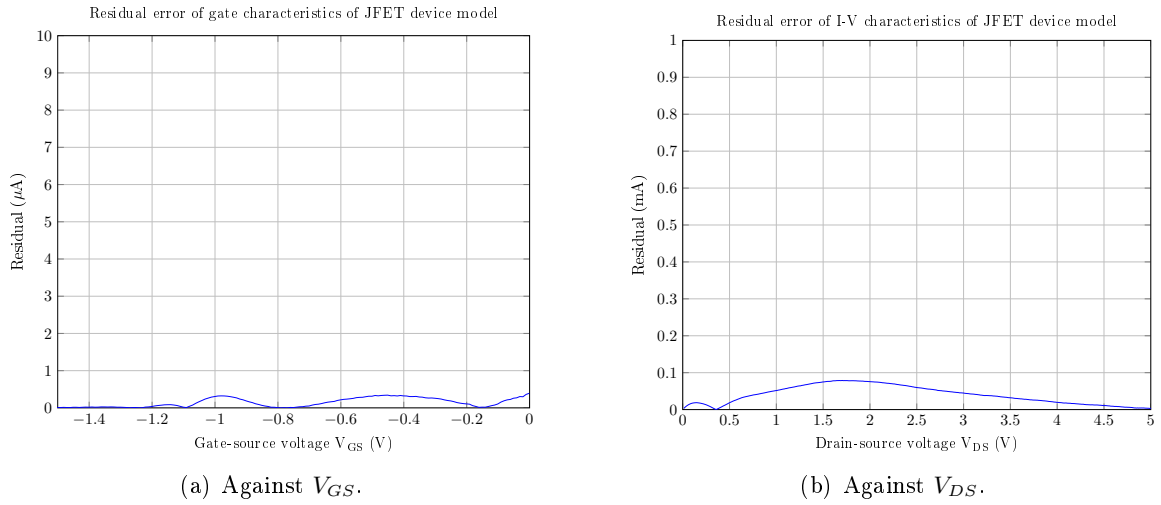


Figure 5.12: Residual error of the JFET device model.

5.2 Simulation Results

5.2.1 DC Analysis

The first simulations performed consisted of a DC analysis procedure (no input signal). These were essential, first because they allowed for node voltage comparison between the circuit prototype and the simulation, assuring the matrix model was error-free, and second because solution of the state-space system provided stable values for the terminal voltages of the non-linear devices as well as state variables of the energy-storing elements (charging of capacitors). These two vectors represent the initial state of circuit and assure the simulation is in a stable state before attempting to process any input signal.

	Prototype		Simulation		ΔV_{GS}	ΔV_{DS}
	V_{GS}	V_{DS}	V_{GS}	V_{DS}		
Q1	-1.22	0	-1.21	0	0.01	0

Table 5.4: JFET DC voltages and absolute difference between measured and simulated results in V.

	Prototype		Simulation		ΔV_{BE}	ΔV_{CE}
	V_{BE}	V_{CE}	V_{BE}	V_{CE}		
Q2	0.53	1.24	0.53	1.23	0	0.01
Q3	0.62	10.55	0.61	10.61	0.01	0.06
Q4	0.63	18.89	0.63	18.85	0	0.04
Q7	0.59	10.97	0.59	11.01	0	0.04
Q8	0.65	15.71	0.66	15.67	0.01	0.04
Q9	0.58	14.29	0.58	14.40	0	0.11
Q10	0.65	13.49	0.66	13.39	0.01	0.10

Table 5.5: BJT DC voltages and absolute difference between measured and simulated results in V.

	4:1	8:1	12:1	20:1
Prototype				
D1	-0.31	-1.26	-2.41	-5.46
D2	-0.30	-1.26	-2.40	-5.44
Simulation				
D1	-0.31	-1.30	-2.48	-5.63
D2	-0.31	-1.30	-2.48	-5.63
$\Delta_{V_{D1}}$	0.00	0.04	0.07	0.17
$\Delta_{V_{D2}}$	0.01	0.04	0.08	0.19

Table 5.6: Diode DC voltages and absolute difference between measured and simulated results in V.

Tables 5.4,5.5,5.6 show the resulting non-linear voltages for both the circuit prototype and the simulation of the DC analysis. All in all, results indicate a good functioning of the simulation. In the case of the JFET, a difference of 0.01 V is observed for V_{GS} . This voltage is directly defined by the Q-Bias adjustment and the small error can arise from particularities of this process. While, in the case of the circuit prototype, the Q-Bias adjustment is performed recurring to a multimeter, the simulation takes as reference the computed output which involves a scaling factor as well as prior discrepancies originating in the setting of the controls and all non-linear device models, that are amplified along the signal path. The simulation of the BJTs proved successful as well, where V_{BE} values showed particularly good approximation with the circuit prototype. The maximum error for this voltage was 0.01 V, and only observed for Q3, Q4 and Q5. Comparison of V_{CE} values show a greater error, while still relatively small, and apart from the possible causes already mentioned, one can include as well small voltage discrepancies in the power supply rails of the prototype, which for the simulation were set as 30 V and -10 V while the power supply might show a tolerance interval. Interesting to note is the greater error in Q9 and Q10, that results from these being the last BJTs in the compression chain, where previous errors suffered amplification already. The same argument explains the error observed for the voltages across the rectification diodes, that come as the last non-linear devices in the GRCA, as well as all error sources mentioned already.

Nevertheless, no alarming errors were produced by the simulation, that was now ready to take audio signals as input.

5.2.2 Static Curve

For measuring the compression ratios being effectively applied in the compressor, a reading of the output for different input levels and ratio settings was performed. In order to achieve similar results between the prototype and the simulation, the same control settings were applied to both. The input control was set in half-rotation (position 24) and the output control was adjusted as to read 0 dBu with an input signal of 0 dBu, while compression was disabled. Following this, different input levels (3 dB steps from +3 dBu down to -18 dBu) were tested and measurements of the output level were taken. Interpolation of this measurements resulted in the static curves shown in Figure 5.13 and the Compression Ratios of Table 5.7.

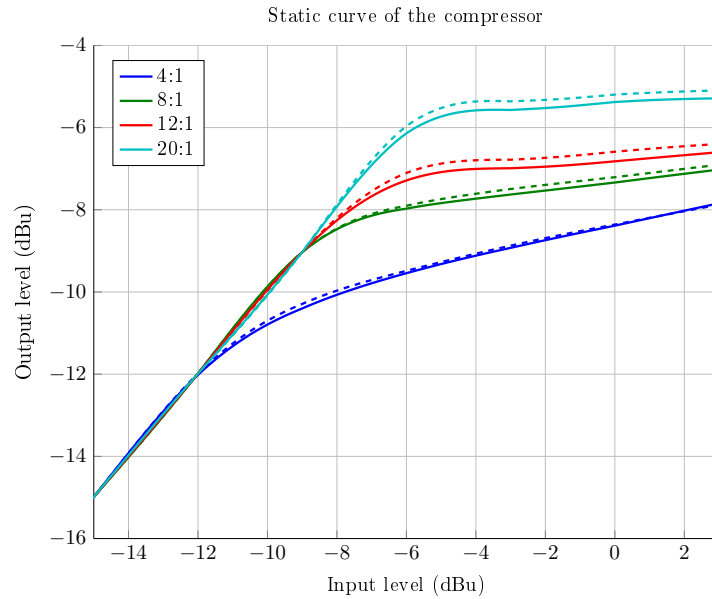


Figure 5.13: Comparison of measured (dashes) and simulated (line) static curve

	4:1	8:1	12:1	20:1
Prototype	5.5	9.4	15.6	21.2
Simulation	5.2	9.7	16.3	19.2

Table 5.7: Results of compression ratios.

While a slightly increased output is observed for the measured curves, this can be easily justified by discrepancies in the setting of the input and output controls and does not necessarily represent less total gain in the simulation. More important to note is the similar behaviour of the output in regards to the input level observed in both occasions. For this matter, a calculation of the compression ratio for each curve was performed taking into account only the measurements taken after the compression threshold is overcome and the curves exhibit a somewhat linear behaviour. The result is presented in Table 5.7. The first thing to note is that the actual compression ratios are, for the most part, higher than the reference values. This comes as no surprise as there are many variables at stake when defining this value, the most significant one being the JFET used, for there no two devices behave exactly the same.

Other influencing factors arise from the different non-linear devices used in comparison with the first original units as well as tolerance errors in resistor values. More important, is to compare the prototype and the simulation results, and these show a relative success, given the many influencing factors that can disturb the measurement (user control settings, power supply tolerances, device models).

5.2.3 Audio Tests

While the results shown above indicated good approximation between the circuit prototype and the simulation, the most significant results come from using the unit as it is intended to, that is, as a tool for the musician. For this matter, audio tests were performed on both the circuit prototype and the simulation, using drum, bass and vocal tracks taken from multitrack recordings [27], and a MOTU UltraLite-mk3 recording interface to input and record audio to and from the prototype. To assure that the input level is matched between prototype and simulation, a scaling factor was applied to the input of the simulation. This is required due to the different domains through which audio is applied. While there is no direct conversion between dBFS (digital domain) and dBu (analog domain), there is also the need for the simulation to interpret an audio source as a voltage. For this matter, a reference value was found by generating a sine wave in the audio editor software Audacity and adjusting its level until 0 dBu (0.775 Vrms) was read externally at the circuit input. This sine wave was then saved as a WAV file and loaded into the simulation environment (MATLAB), where a scaling factor is applied to the signal until it reads the same 0.775 Vrms. This process resulted in a scaling factor of 4.1246 that is further applied to every WAV input in this study. Following, a comparison between original uncompressed sources and compressed prototype and simulations results is presented for a bass, vocal and drum track, with different control settings applied.

5.2.3.1 Bass

The first test was performed with a bass guitar track, for which the user control settings shown in 5.8 were applied.

Input	Output	Attack	Release	Ratio
24	24	3	5	8:1

Table 5.8: User control settings for bass guitar track test.

Comparing to the original source, the compressed audio tests provided results where the most obvious difference is the consistence in volume. That is also suggested by visual observation of Figure 5.14, where the three waveforms are displayed. In the original track, one can observe how the waveform envelope instantly decreases after a note is struck. Audibly, this translates in fading of certain notes caused by severe volume variation. As expected, both results of compression show that bass notes are more sustained resulting in a sound that is more present without sacrificing definition.

The comparison between prototype and simulation results shows no apparent visual difference between Figures 5.14(b) and 5.14(c), which suggests the simulation of the circuit was accurate.

This is also backed by the audible tests performed, where no significant difference could be discerned. Another convincing aspect is the low average number of iterations needed by the non-linear solver to compute an output sample (2.39 iterations/sample). Further analysis is made by plotting the residual, with both compressed signals normalized to the same relative signal energy (0.0179). As expected, Figure 5.2.3.1 shows a low residual with a relative signal energy of 5.765×10^{-5} , 0.3% of the total energy, a value sufficiently low to validate the success of the simulation.

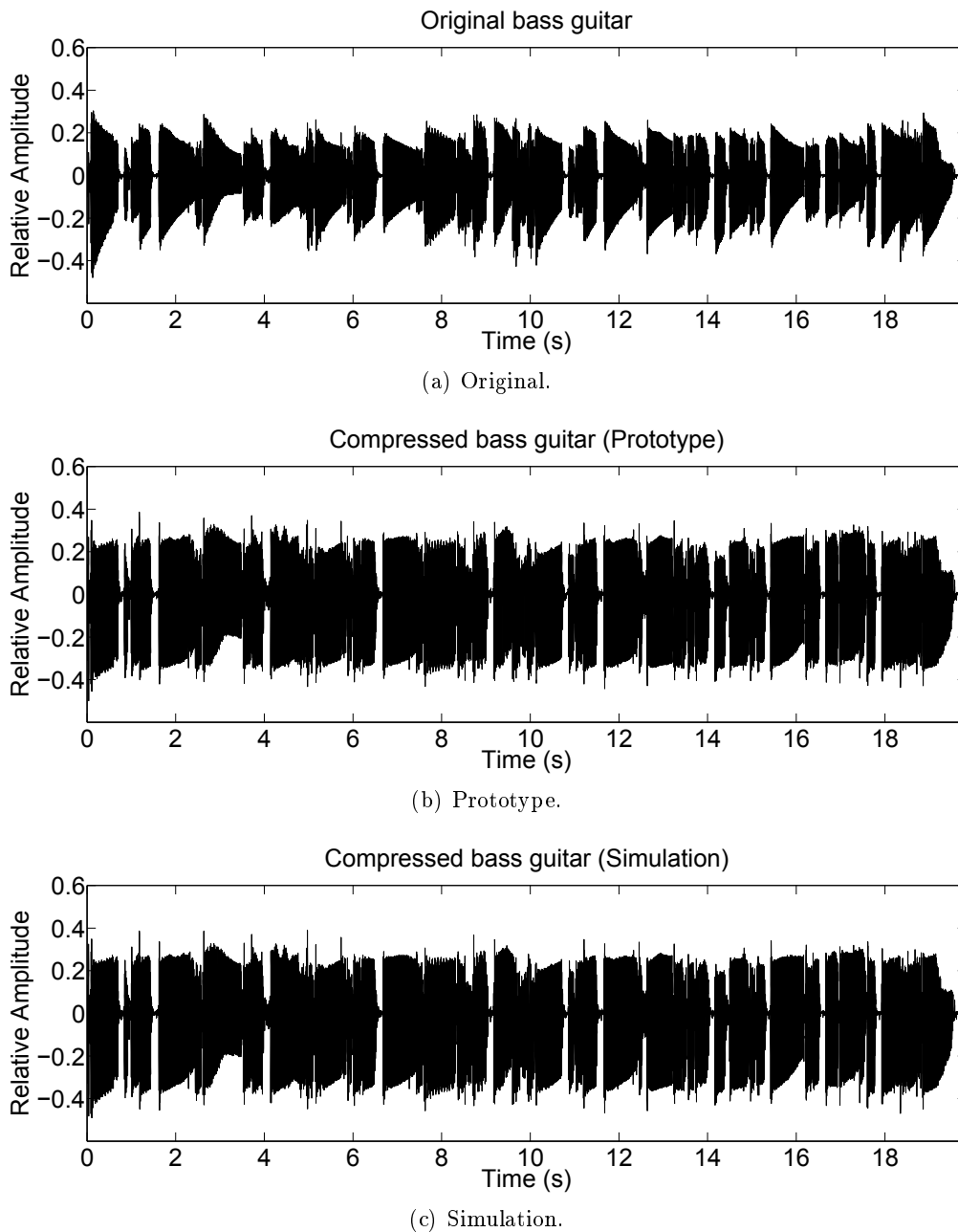


Figure 5.14: Waveforms of original uncompressed bass guitar and prototype and simulation results.

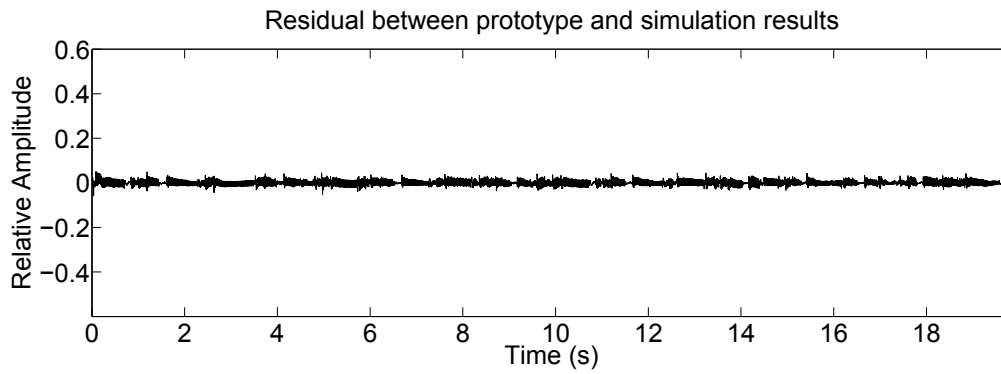


Figure 5.15: Residual of prototype and simulation bass guitar test results.

5.2.3.2 Vocal

For testing the simulation with a vocal track, user controls were set accordingly to table 5.9.

Input	Output	Attack	Release	Ratio
6	30	5	5	8:1

Table 5.9: User control settings for vocal track test.

The most notable difference between original and processed tracks, seen in Figure 5.16, lies on the increase in signal content, as experienced with the bass example. But while the latter evidenced a severe change in the signal envelope, in the case of the vocal track this is not as much pronounced. Instead, a particular difference is observed for the quieter parts of the signal, that is now much more discernible in the compressed tracks, while the louder parts maintain a similar peak level throughout the track. Sonically this can be translated in a vocal with a richer texture and less fading effects. The amplification of the quieter parts provides an added ambience to the vocal but also pronounces the breathing sounds from the singer. Comparing the results of the simulation with the prototype track, again no obvious differences arise in the visual content. Both signals have been normalized to a relative signal energy of 0.0065 and the residual (Fig. 5.2.3.2) showed a signal energy of 7.328×10^{-5} , about 1% of the total. The average number of iterations performed was 2.94, a value that indicates no severe exhaustion of the non-linear solver occurred. As expected from these results, no audible differences were experienced between listening tests.

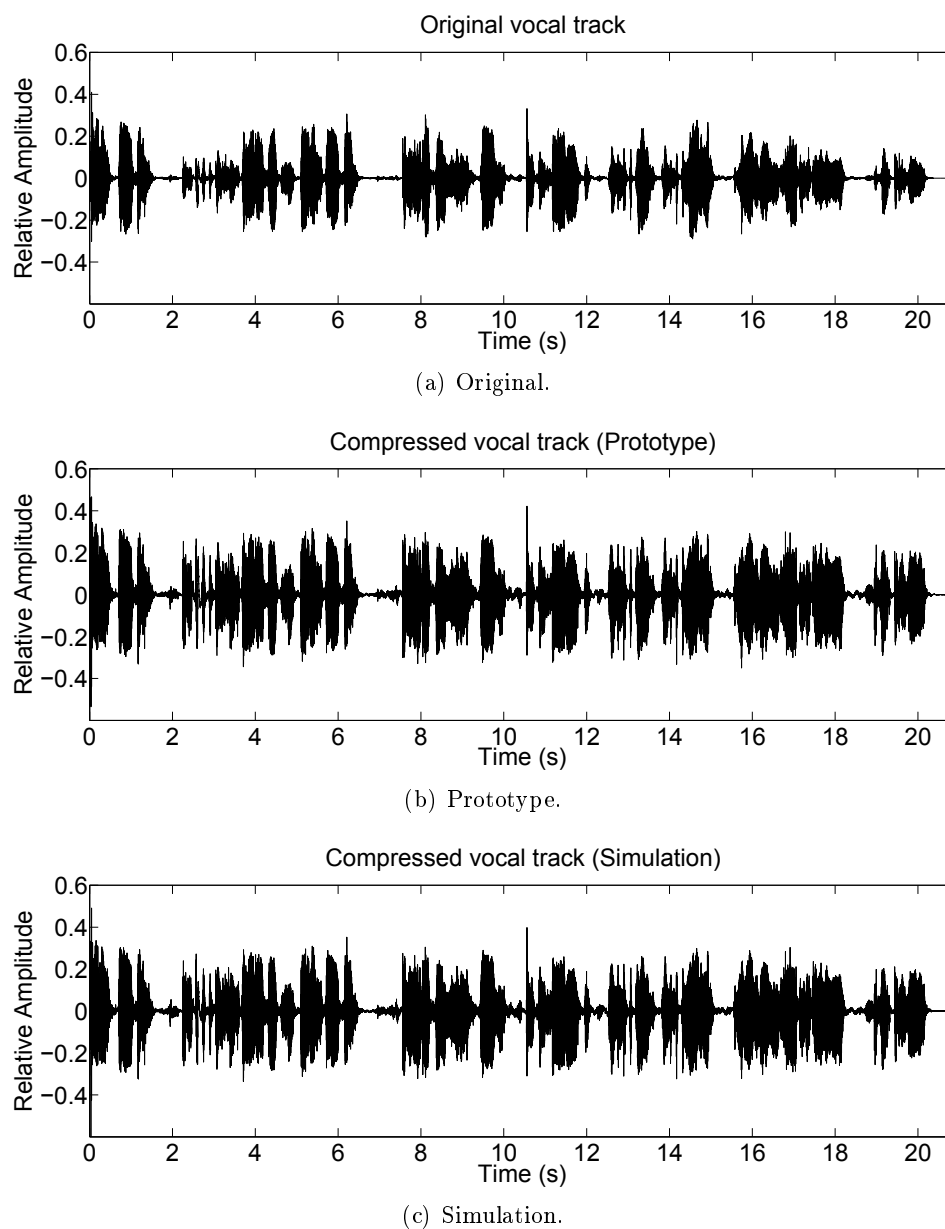


Figure 5.16: Waveforms of original uncompressed vocal track and prototype and simulation results.

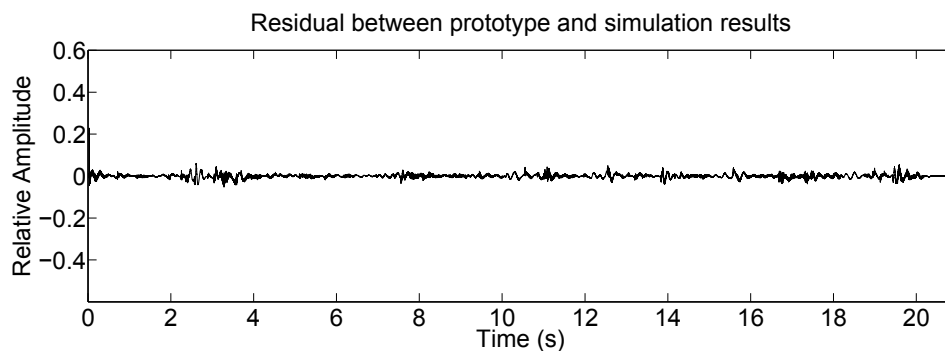


Figure 5.17: Residual of prototype and simulation vocal test results.

5.2.3.3 Drums

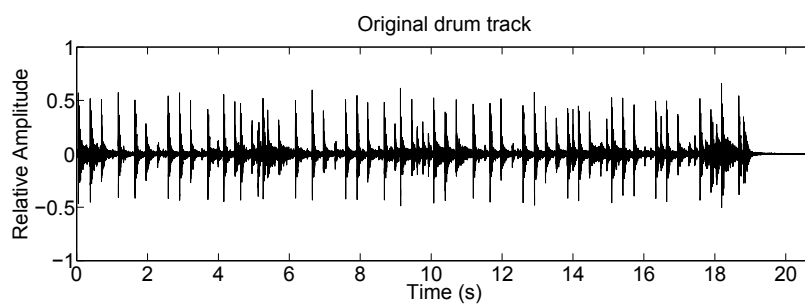
The simulation of drum tracks represents a more challenging test due to the much higher content of signal transients. For this matter, two different settings are tested in order to analyse the effect of changing user controls, as seen in Table 5.10.

	Input	Output	Attack	Release	Ratio
Example 1	18	24	3	5	12:1
Example 2	24	24	1	7	4:1

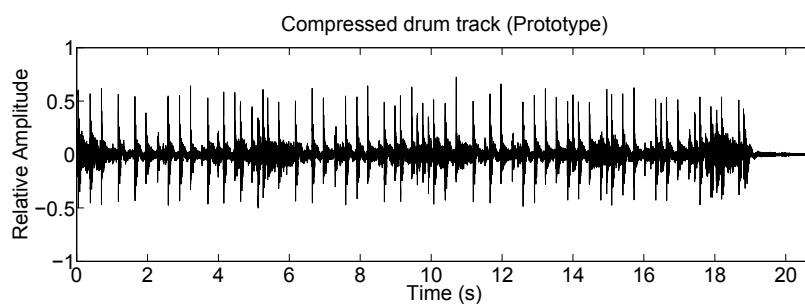
Table 5.10: User control settings for drum track test.

Concerning the differences between the original and the compressed tracks, certain effects are common to both examples. In sum, both drum tracks present a lively sound arising from the increase in room ambience and overtones. Visually this is confirmed by the increase in the lower content of the signal, particularly pronounced in Example 2 (Fig. 5.18(d),5.18(e)). The hi-hats become more present as well as can be observed by the increase in signal peaks in respect to the original (Fig. 5.18(a)). Another effect pronounced in Example 2 is the change in character of the kick drum, that due to the slow attack setting and the higher setting of the output control became more punchy and powerful. However, comparing simulation results with the prototype output, in both examples a greater difference was observed comparing with the previous tests. The main difference relies not so much in the signal peaks, hinting that the attack control was well implemented, but in the quieter parts of the signal. In Example 1, the prototype shows slightly more pronounced overtones, while not much difference is discernible between kick and snare sounds. Two probable causes can be pointed for this, the main one being possible discrepancies in the output control between simulation and prototype, the other one being the already discussed difference in the effective compression ratios (5.2.2). For the first test, both signals were normalized to a relative signal energy of 0.0058 while the residual showed a relative signal energy of 6.618×10^{-4} , about 11.4% of the total energy. Consistently with the previous tests, the average number of iterations needed was 2.88. In Example 2, similar results were obtained. The two signals, normalized to a relative signal energy of 0.0098, showed a residual with 0.0011 for the same quantity, about 11.2% of the total. The number of iterations needed was 2.91. However, this result comes as a surprise as no significant audible difference was experienced for the listening tests of Example 2.

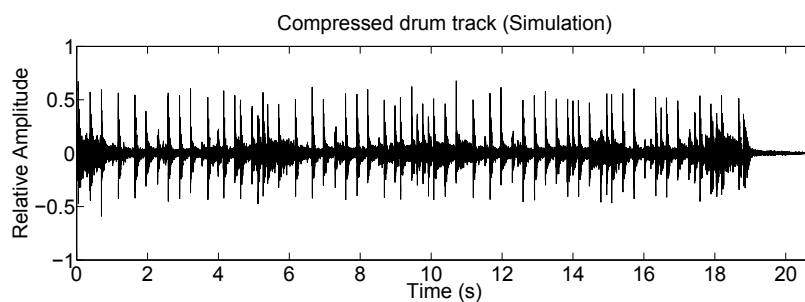
One can certainly assume that the error increase observed for the drum tests arises from the greater peak content of these signals in respect to the bass and vocal tests. Despite the low average number of iterations required, the non-linear solver reached over 50 iterations for several output samples, provoked by the high transients of drum hits. Besides increasing the simulation time this can sometimes result in erroneous output if the maximum iterations set for the non-linear solver are reached.



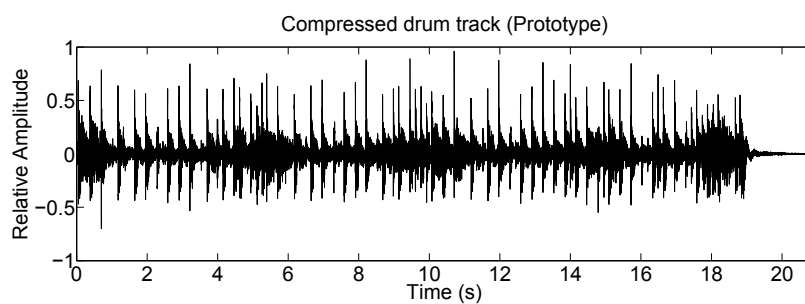
(a) Original.



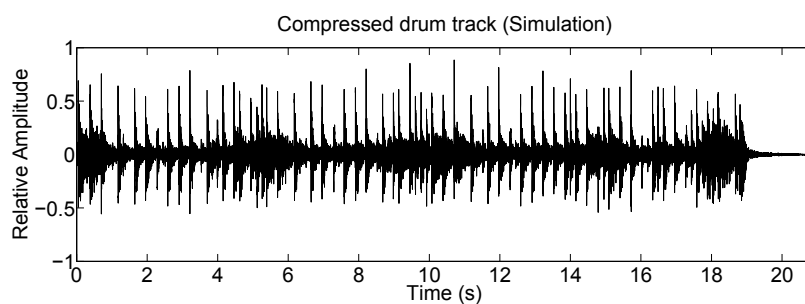
(b) Prototype (Example 1).



(c) Simulation (Example 1).



(d) Prototype (Example 2).



(e) Simulation (Example 2).

Figure 5.18: Waveforms of original uncompressed drum track and prototype and simulation results.

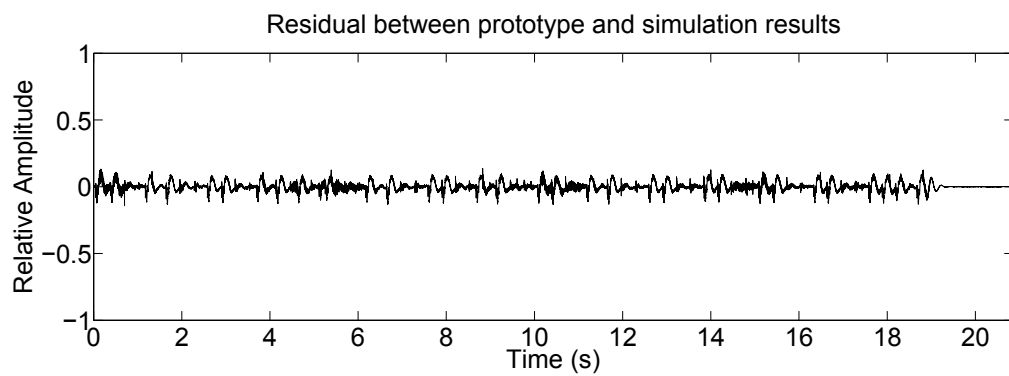
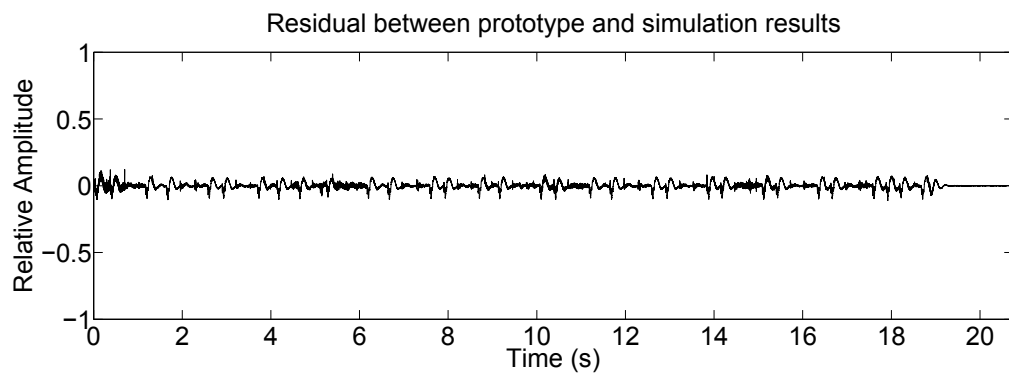


Figure 5.19: *Residual of prototype and simulation drum test results.*

Chapter 6

Conclusion and Future work

This thesis project proposed to investigate the application of a physical modeling method derived from analog circuit analysis and modeling of non-linear electronic devices to more accurately simulate vintage circuits that have generated increasing demand throughout the history of music production. For this matter, a popular Dynamic Range Compressor by the name UREI 1176LN was chosen as a case study for application of the Nodal DK Method to Dynamic Range Control audio circuits. An introduction about this type of audio effect was presented with a particular focus on the circuit operation of the unit in study.

The Nodal DK Method relies on a state-space representation of the non-linear system provided by the analog circuit in study. For this, a matrix system based on node connections describes the circuit inherent elements and, for the case of non-linear devices such as diodes and transistors, a non-linear iterative solver based on Newton's Method is introduced to compute the current given by these devices. This required a study of the devices in question to find appropriate digital models that describe their operation. In this sense, various laboratory measurements of the non-linear devices used in the circuit were taken, as part of parameter extraction methods for accurate model implementation. Improvements of the device models used in previous works were suggested based on polynomial approximations. In the case of Bipolar Junction Transistors, the influence of Early Effect was taken into account based on the measurements made. A device model based on a hyperbolic tangent approximation was proposed for the simulation of a JFET. A circuit prototype was built and provided a reference for every modeled element in the digital implementation.

Parameter extraction methods were presented and together with the applied device models yielded close approximations to the measurements obtained from the real devices, in the regions of operation of interest. DC analysis was performed on both the simulation and the circuit prototype and consistent approximations in the values of the non-linear devices terminal voltages were found. The simulation showed as well close transfer characteristics, by measuring the effective compression ratios applied to input signals, comparing to the circuit prototype. Ultimate tests were performed with multitrack recordings for the cases of interest. The results were specially satisfying with Bass and Vocal tracks where, both visually and audibly, no significant difference was found. Concerning Drum track simulations, a discrepancy was found in respect to the prototype results, due to the high transient content of these type of signal. However, audible differences were only slight and case dependent. The many simulations ran

with relatively low computational effort considering the dimension of the matrix model and the greater complexity of the device models in respect to previous works. In this sense, the Nodal DK Method was once again proved as a powerful tool for circuit simulation.

Future work should be geared into improving the implementation of this method for real-time processing capability, if this approach is to compete with already commercially available products. For this matter, an implementation of the simulation core in C/C++ should be developed and can be presented as a VST plugin or DSP solution. Although sufficiently good approximations of the non-linear device models were obtained, it is possible to improve the parameter extraction process by using dedicated equipment for measuring these. Such equipment can also lead to higher complexity models taking into account parasitic resistance and capacitance of the device, making the models more accurate yet more computational consuming. Lastly, further investigation can be done in regards to modeling output transformers, for which device models and parameter extraction methods are not yet sufficiently developed in the context of the physical modeling approach of this thesis.

Appendix A

Measured Components

Component	Value
R5	27 k Ω
R10	9.98 k Ω
R8	1 k Ω
R9	557.3 k Ω
R13	0.997 M Ω
R18	180 Ω
R84	180 Ω
R14	21.86 k Ω
R17	6.77 k Ω
R11	82 Ω
R12	1.79 k Ω
R15	6.77 k Ω
R86	34 Ω
R85	149 Ω
R6	2.2 M Ω
R7	2.2 M Ω
R37	470 k Ω
R36	0.995 k Ω
R38	47 k Ω
R39	4.68 k Ω
R46	46.93 k Ω
R40	2.39 k Ω
R42	181.8 k Ω
R41	269 Ω
R43	38.1 k Ω
R47	44 k Ω
R48	7.66 k Ω
R49	2.39 k Ω
R51	4.68 k Ω
R50	180 Ω
R52	47 k Ω
R53	47 k Ω
R45	10 M Ω

R54	468 Ω
R57	268.6 k Ω
R60	3.88 k Ω
R35	9.96 k Ω
R64	1.5 k Ω
R58	149 Ω

Table A.1: Measured values of the resistors used in the circuit prototype and state-space implementation

Component	Value
C1	1 μ F
C28	98.7 μ F
C4	97.3 μ F
C5	97.6 μ F
C7	0.96 μ F
C9	0.21 μ F
C3	200 pF
C6	200 pF
C17	0.98 μ F
C20	6.8 μ F
C19	6.8 μ F
C18	44.8 μ F
C21	97.1 μ F
C27	22 nF
C22	220 nF

Table A.2: Measured values of the capacitors used in the circuit prototype and state-space implementation

Potentiometer	Minimum value	Maximum value
Input Control	1.47 Ω	10.4 k Ω
Output Control	1.9 Ω	245 k Ω
Attack	1.5 Ω	25 k Ω
Release	1.7 Ω	4.84 M Ω

Table A.3: Measured values of the potentiometers used in the circuit prototype and state-space implementation

Compression Ratio Switch	Value
CR1	283.146 M Ω
CR2	2.525 k Ω

Table A.4: Measured resistance values of the overall resistor ladder switch formed by the Compression Ratio push-buttons

Appendix C

Sourcecodes

```
1 %% Resistors
2 R5 = 27e3;
3 R10 = 9.98e3;
4 R8 = 1e3;
5 R9 = 557.3e3;
6 R13 = 0.997e6;
7 R3 = 1;
8 R18 = 180;
9 R84 = 180;
10 R14 = 21.86e3;
11 R17 = 6.77e3;
12 R4 = 1;
13 R11 = 82;
14 R12 = 1.79e3;
15 R15 = 6.77e3;
16 R86 = 34;
17 R85 = 149;
18 R6 = 2.2e6;
19 R7 = 2.2e6;
20 R37 = 470e3;
21 R36 = 0.995e6;
22 R16 = 1;
23 R38 = 47e3;
24 R39 = 4.68e3;
25 R46 = 46.93e3;
26 R40 = 2.39e3;
27 R42 = 181.8e3;
28 R41 = 269;
29 R43 = 38.1e3;
30 R47 = 44e3;
31 R19 = 1;
32 R48 = 7.66e3;
33 R49 = 2.39e3;
34 R51 = 4.68e3;
35 R50 = 180;
36 R52 = 47e3;
37 R53 = 47e3;
38 R45 = 10e6;
39 R54 = 468;
40 Ratt1 = 50e3;
41 Ratt2 = 50e3;
42 R57 = 268.6e3;
43 R59a = 0.4885e3;
44 R59b = 1.5125e3;
45 R60 = 3.88e3;
46 R35 = 9.96e3;
47 R64 = 1.5e3;
48 R58 = 149;
49 Rout1 = 490e3;
50 Rout2 = 490e3;
```

```
51
52 %% Capacitors
53 C1 = 1e-6;
54 C28 = 98.7e-6;
55 C4 = 97.3e-6;
56 C5 = 97.6e-6;
57 C7 = 1e-6;
58 C9 = 220e-9;
59 C3 = 200e-12;
60 C6 = 200e-12;
61 C17 = 0.98e-6;
62 C20 = 6.8e-6;
63 C19 = 6.8e-6;
64 C18 = 44.8e-6;
65 C21 = 100e-6;
66 C27 = 22e-9;
67 C22 = 220e-9;
68
69 %% Potentiometers
70 Input1 = 10.4e3;
71 Input2 = 10.4e3;
72 Output1 = 245e3;
73 Output2 = 245e3;
74 RatioA1 = 283e3;
75 RatioA2 = 283e3;
76 RatioB1 = 2.53e3;
77 RatioB2 = 2.53e3;
78 Attack1 = 25e3;
79 Attack2 = 25e3;
80 Release1 = 4.84e6;
81 Release2 = 4.84e6;
82
83 %% Non-linear devices
84 paramQ1.Vp = -1.255;%-1.1019;
85 paramQ1.Idss = 2.2e-3;
86 paramQ1.alpha = 1.2;
87 paramQ1.Igs = 1e-14;
88 paramQ1.Vt = 26e-3;
89
90 paramQ2.Ies = 3.55e-14;
91 paramQ2.Ics = 9.173e-14;
92 paramQ2.alphaF = 0.9966;
93 paramQ2.alphaR = 0.28;
94 paramQ2.Vt = 26e-3;
95 paramQ2.Va = 190;
96
97 paramQ3.Ies = 3.7e-14;
98 paramQ3.Ics = 9.173e-14;
99 paramQ3.alphaF = 0.9966;
100 paramQ3.alphaR = 0.28;
101 paramQ3.Vt = 26e-3;
102 paramQ3.Va = 70;
103
104 paramQ4.Ies = 3.7e-14;
105 paramQ4.Ics = 9.173e-14;
106 paramQ4.alphaF = 0.9966;
107 paramQ4.alphaR = 0.28;
108 paramQ4.Vt = 26e-3;
109 paramQ4.Va = 70;
110
111 paramQ7.Ies = 3.35e-14;
112 paramQ7.Ics = 1.173e-13;
113 paramQ7.alphaF = 0.9966;
114 paramQ7.alphaR = 0.28;
115 paramQ7.Vt = 26e-3;
116 paramQ7.Va = 96;
117
118 paramQ8.Ies = 4.08e-14;
119 paramQ8.Ics = 2.173e-13;
120 paramQ8.alphaF = 0.9966;
121 paramQ8.alphaR = 0.28;
```



```

187     0, 0, 0, 0, 0, 0, 0, 0;...% R54
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, -1, 0, 0,
188     0;...% Ratt1
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, -1;...% Ratt2
189     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, -1,
    0, 0, 0, 0, 0, 0, 0, 0;...% R57
190     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1,
    0, 0, 0, 0, 0, 0, 0, 0;...% R59a
191     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1,
    -1, 0, 0, 0, 0, 0, 0, 0;...% R59b
192     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    1, 0, 0, 0, 0, 0, 0, 0;...% R60
193     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    1, -1, 0, 0, 0, 0, 0, 0;...% R35
194     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 1, -1, 0, 0, 0, 0;...% R64
195     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, -1,
    0, 0, 0, 1, 0, 0, 0;...% R58
196     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    -1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1,
    0, 0, 0, 0, 0, 0, 0;...% Rout1
197     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0 ...% Rout2
198   ]);
199
200 Nx = sparse([...
201 % 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
    23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44
    45 46 47 48 49 50
202     0, 0, 1, 0, -1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0;...% C1
203     0, 0, 0, 1, 0, 0, 0, 0, 0, -1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0;...% C28
204     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0;...% C4
205     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0;...% C5
206     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, -1,
    0, 0, 0, 0, 0, 0, 0;...% C7
207     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, -1, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0;...% C9
208     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, -1, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0;...% C3
209     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0;...% C6
210     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 1, -1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0;...% C17
211     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, -1, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0;...% C20

```



```

240     0, 0, 0, 0, 0, 0, 0, 0;...% Q2
0, 0, 0, 0, 0, 0, 1, -1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0;...% Q2
241     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, -1, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0;...% Q2
0, 0, 0, 0, 0, 0, 0, 0;...% Q3
242     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, -1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0;...% Q3
243     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, -1, 0, 0, 0, 0, 0, 1, 0,
0, 0, 0, 0, 0, 0, 0, 0;...% Q4
244     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, -1, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0;...% Q4
245     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 1, 0, -1, 0, 0, 0;...% Q7
246     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 1, -1, 0, 0;...% Q7
247     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, -1, 0, 0;...% Q8
248     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, -1, 0, 0;...% Q8
249     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 1, 0;...% Q9
250     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 1, -1, 0;...% Q9
251     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0, -1, 0;...% Q10
252     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0, -1, 1, 0;...% Q10
253     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, -1, 0;...% CR2
254     0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, -1, 0;...% CR3
255 ];
256
257 Nu = sparse(...
258 % 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44
45 46 47 48 49 50
259 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0;...% Vin
260 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0;...% Vcc
261 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0;...% Vcc
262 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 1, 0, 0, 0, 0, 0 ...% Vee
263 ];
264
265 NuT = sparse(...
266 % 1 2 3 4
267 1, 0, 0, 0;...
268 0, 0, 0, 0;...
269 0, 0, 0, 0;...

```

```

270     0, 0, 0, 0;...
271     0, 0, 0, 0;...
272     0, 0, 0, 0;...
273     0, 0, 0, 0;...
274     0, 0, 0, 0;...
275     0, 0, 0, 0;...
276     0, 0, 0, 0;...
277     0, 0, 0, 0;...
278     0, 0, 0, 0;...
279     0, 0, 0, 0;...
280     0, 1, 0, 0;...
281     0, 0, 0, 0;...
282     0, 0, 0, 0;...
283     0, 0, 0, 0;...
284     0, 0, 0, 0;...
285     0, 0, 0, 0;...
286     0, 0, 0, 0;...
287     0, 0, 0, 0;...
288     0, 0, 0, 0;...
289     0, 0, 0, 0;...
290     0, 0, 0, 0;...
291     0, 0, 0, 0;...
292     0, 0, 0, 0;...
293     0, 0, 0, 0;...
294     0, 0, 0, 0;...
295     0, 0, 0, 0;...
296     0, 0, 0, 0;...
297     0, 0, 0, 0;...
298     0, 0, 0, 0;...
299     0, 0, 0, 0;...
300     0, 0, 1, 0;...
301     0, 0, 0, 0;...
302     0, 0, 0, 0;...
303     0, 0, 0, 0;...
304     0, 0, 0, 0;...
305     0, 0, 0, 0;...
306     0, 0, 0, 0;...
307     0, 0, 0, 0;...
308     0, 0, 0, 0;...
309     0, 0, 0, 0;...
310     0, 0, 0, 0;...
311     0, 0, 0, 1;...
312     0, 0, 0, 0;...
313     0, 0, 0, 0;...
314     0, 0, 0, 0;...
315     0, 0, 0, 0;...
316     0, 0, 0, 0 ...
317 ];
318
319 No = eye(50);
320
321 Gr = sparse(diag([1/R5,1/R10,1/R8,1/R9,1/R13,1/R3,1/R18,1/R84,1/R14,1/R17,1/R4,1/R11,1/R12,1/
R15,1/R86,1/R85,1/R6,1/R7,1/R37,1/R36,1/R16,1/R38,1/R39,1/R46,1/R40,1/R42,1/R41,1/R43,1/
R47,1/R19,1/R48,1/R49,1/R51,1/R50,1/R52,1/R53,1/R45,1/R54,1/Ratt1,1/Ratt2,1/R57,1/R59a
,1/R59b,1/R60,1/R35,1/R64,1/R58,1/Rout1,1/Rout2]));
322
323 Gx = sparse(diag([2*C1/T,2*C28/T,2*C4/T,2*C5/T,2*C7/T,2*C9/T,2*C3/T,2*C6/T,2*C17/T,2*C20/T,2*
C19/T,2*C18/T,2*C21/T,2*C27/T,2*C22/T]));
324
325 Z = sparse(diag([ 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1]));
326
327 Vr = [Input1,Input2,Output1,Output2,RatioA1,RatioA2,RatioB1,RatioB2,Attack1,Attack2,Release1,
Release2];
328
329 vnin = [];
330
331 [rowsNn colsNn] = size(Nn);
332
333 [rowsNx colsNx] = size(Nx);

```

Sourcecode C.1: *Circuit model of the UREI 1176LN.*

```
1 %% Simulation setup
2 Fs = 48000;
3 Ts = 1/Fs;
4
5 options.MaxIter = 50;
6
7 options.TolFun = 10e-6;
8
9 %% Inputs
10 u(1,:) = wavread('sound.wav');
11 t=1:length(u(1,:));
12 u=4.1246*u(1:length(t));
13
14 vcc = 30;
15 u(2,:) = vcc*ones(1,length(t));
16 u(3,:) = u(2,:);
17
18 vee = -10;
19 u(4,:) = vee*ones(1,length(t));
20
21
22 %% User controls
23
24 switch input
25     case 24
26         input1 = 0.87;
27         input2 = 1-input1;
28         a(1,:) = input1*ones(1,length(t));
29         a(2,:) = input2*ones(1,length(t));
30     case 18
31         input1 = 0.67;
32         input2 = 1-input1;
33         a(1,:) = input1*ones(1,length(t));
34         a(2,:) = input2*ones(1,length(t));
35     case 12
36         input1 = 0.36;
37         input2 = 1-input1;
38         a(1,:) = input1*ones(1,length(t));
39         a(2,:) = input2*ones(1,length(t));
40     case 6
41         input1 = 0.02;
42         input2 = 1-input1;
43         a(1,:) = input1*ones(1,length(t));
44         a(2,:) = input2*ones(1,length(t));
45     otherwise
46         error('Input not valid. Use 24/18/12/6 instead.');
```

```
47 end
48
49 switch output
50     case 48
51         output1 = 0.9834;
52         output2 = 1-output1;
53         a(3,:) = output1*ones(1,length(t));
54         a(4,:) = output2*ones(1,length(t));
55     case 36
56         output1 = 0.973;
57         output2 = 1-output1;
58         a(3,:) = output1*ones(1,length(t));
59         a(4,:) = output2*ones(1,length(t));
60     case 30
61         output1 = 0.94;
62         output2 = 1-output1;
63         a(3,:) = output1*ones(1,length(t));
64         a(4,:) = output2*ones(1,length(t));
65     case 24
66         output1 = 0.91;
67         output2 = 1-output1;
68         a(3,:) = output1*ones(1,length(t));
69         a(4,:) = output2*ones(1,length(t));
70     case 18
71         output1 = 0.785;
```

```

72     output2 = 1-output1;
73     a(3,:) = output1*ones(1,length(t));
74     a(4,:) = output2*ones(1,length(t));
75     case 12
76         output1 = 0.412;
77         output2 = 1-output1;
78         a(3,:) = output1*ones(1,length(t));
79         a(4,:) = output2*ones(1,length(t));
80     otherwise
81         error('Output not valid. Use 48/36/30/24/18/12 instead.');
```

```

82 end
83
84 switch attack
85     case 1
86         attack1 = 0.00005;
87         attack2 = 1-attack1;
88         a(9,:) = attack1*ones(1,length(t));
89         a(10,:) = attack2*ones(1,length(t));
90     case 3
91         attack1 = 0.36;
92         attack2 = 1-attack1;
93         a(9,:) = attack1*ones(1,length(t));
94         a(10,:) = attack2*ones(1,length(t));
95     case 5
96         attack1 = 0.73;
97         attack2 = 1-attack1;
98         a(9,:) = attack1*ones(1,length(t));
99         a(10,:) = attack2*ones(1,length(t));
100    case 7
101        attack1 = 0.99995;
102        attack2 = 1-attack1;
103        a(9,:) = attack1*ones(1,length(t));
104        a(10,:) = attack2*ones(1,length(t));
105    otherwise
106        error('Attack not valid. Use 1/3/5/7 instead.');
```

```

107 end
108
109 switch release
110     case 1
111         release1 = 0.999997;
112         release2 = 1-release1;
113         a(11,:) = release1*ones(1,length(t));
114         a(12,:) = release2*ones(1,length(t));
115     case 3
116         release1 = 0.68;
117         release2 = 1-release1;
118         a(11,:) = release1*ones(1,length(t));
119         a(12,:) = release2*ones(1,length(t));
120     case 5
121         release1 = 0.27;
122         release2 = 1-release1;
123         a(11,:) = release1*ones(1,length(t));
124         a(12,:) = release2*ones(1,length(t));
125     case 7
126         release1 = 0.00000015;
127         release2 = 1-release1;
128         a(11,:) = release1*ones(1,length(t));
129         a(12,:) = release2*ones(1,length(t));
130    otherwise
131        error('Release not valid. Use 1/3/5/7 instead.');
```

```

132 end
133
134 switch ratio
135     case 4
136         ratioA1 = 0.8345;
137         ratioA2 = 1-ratioA1;
138         a(5,:) = ratioA1*ones(1,length(t));
139         a(6,:) = ratioA2*ones(1,length(t));
140
141         ratioB1 = 8e-5;
142         ratioB2 = 1-ratioB1;
```

```

143     a(7,:) = ratioB1*ones(1,length(t));
144     a(8,:) = ratioB2*ones(1,length(t));
145
146     init =
        [-0.103967947398527;-2.63723174846145;238.837191345469;10.5374838946873;1.07083604481991;0.04317
        e-15;8.43141660953955e
        -13;-0.429895636083494;10.3502968231417;11.8381570179705;118.868303142985;-14.6161399253059;-1.3
        e-12;-0.0255291233210991;-1.20876970811405;-2.08609164492749e
        -08;0.526339591883410;1.22849626979234;0.608981947304990;10.6078597735950;0.629485836388100;18.8

147     xo = init(1:15)
148     vno = init(16:33)
149
150     case 8
151         ratioA1 = 0.6364;
152         ratioA2 = 1-ratioA1;
153         a(5,:) = ratioA1*ones(1,length(t));
154         a(6,:) = ratioA2*ones(1,length(t));
155
156         ratioB1 = 0.1856;
157         ratioB2 = 1-ratioB1;
158         a(7,:) = ratioB1*ones(1,length(t));
159         a(8,:) = ratioB2*ones(1,length(t));
160
161     init =
        [-0.103967943510883;-2.63723198667503;238.837186060396;10.5374853153881;1.07083587660148;0.04317
        e-17;8.44734692758515e
        -13;-0.429895663213382;10.9948514973216;12.4827106542448;118.868303140642;-24.0948774519357;-1.3
        e-12;-0.0255292190822230;-1.20877586672012;-1.19163921859017e
        -06;0.526339591374674;1.22849663001336;0.608981951432358;10.6078578569032;0.629485831811107;18.8

162     xo = init(1:15)
163     vno = init(16:33)
164
165     case 12
166         ratioA1 = 0.4382;
167         ratioA2 = 1-ratioA1;
168         a(5,:) = ratioA1*ones(1,length(t));
169         a(6,:) = ratioA2*ones(1,length(t));
170
171         ratioB1 = 0.407;
172         ratioB2 = 1-ratioB1;
173         a(7,:) = ratioB1*ones(1,length(t));
174         a(8,:) = ratioB2*ones(1,length(t));
175
176     init =
        [-0.103967947444236;-2.63723174797070;238.837191333786;10.5374838977319;1.07083604481738;0.04317
        e-15;8.46691340560739e
        -13;-0.429895635837688;11.7640200387845;13.2518802404434;118.868303142936;-35.4061873583489;-1.3
        e-12;-0.0255295741123921;-1.20878252930295;-1.99139108521159e
        -08;0.526339591887290;1.22849627037741;0.608981947312500;10.6078597735363;0.629485836387859;18.8

177     xo = init(1:15)
178     vno = init(16:33)
179
180     case 20
181         ratioA1 = 0.1985;
182         ratioA2 = 1-ratioA1;
183         a(5,:) = ratioA1*ones(1,length(t));
184         a(6,:) = ratioA2*ones(1,length(t));
185
186         ratioB1 = 2524.55/2524.77;
187         ratioB2 = 1-ratioB1;
188         a(7,:) = ratioB1*ones(1,length(t));
189         a(8,:) = ratioB2*ones(1,length(t));
190
191     init =
        [-0.103967947172714;-2.63723175851402;238.837191392200;10.5374838818851;1.07083604761760;0.04317
        e-15;8.47675052438428e
        -13;-0.429895635949540;13.8238676871339;15.3117278850407;118.868303142996;-65.6980645119258;-1.3
        e-12;-0.0255318292385357;-1.20888359233455;-2.67617068098164e

```

```

-08;0.526339591905210;1.22849626717733;0.608981947263209;10.6078598049944;0.629485836464311;18.84
192     xo = init(1:15)
193     vno = init(16:33)
194
195     case 'all'
196         ratioA1 = 0.1985;
197         ratioA2 = 0.1654;
198         a(5,:) = ratioA1*ones(1,length(t));
199         a(6,:) = ratioA2*ones(1,length(t));
200
201         ratioB1 = 8e-7;
202         ratioB2 = 8e-7;
203         a(7,:) = ratioB1*ones(1,length(t));
204         a(8,:) = ratioB2*ones(1,length(t));
205
206         init =
                [-0.103967947386415;-2.63723175238593;238.837191464992;10.5374838620878;1.07083605114863;0.066798
                e-14;8.83293280843646e
                -13;-0.429895637085020;11.3281143179917;12.8159744718631;118.868303143022;-28.9958087530067;-1.32
                e-12;-0.0491506528301492;-2.32720768486518;-5.45543069185512e
                -10;0.526339591935902;1.22849625952902;0.608981947199511;10.6078598507282;0.629485836562435;18.84
207     xo = init(1:15)
208     vno = init(16:33)
209
210     otherwise
211         error('Compression Ratio not valid. Use 4/8/12/20/all instead.')
212 end
213
214 matrixmodelHandler = @(input,Ts,xo,vno)urei1176(input,Ts,xo,vno);
215 [y, x, in, vn, iter] = simulator(u,a,Ts,matrixmodelHandler,options,xo,vno);

```

Sourcecode C.2: *Simulation script of the UREI 1176LN.*

List of Abbreviations

A

AD	Analog-to-digital.
ANT	Allgemeine Nachrichtentechnik (Signal Processing and Communication)

B

BJT	Bipolar Junction Transistor
-----	-----------------------------

C

CD	Compact Disc
----	--------------

D

DC	Direct Current
DRC	Dynamic Range Compression

J

JFET	Junction Field-Effect Transistor
------	----------------------------------

K

KCL	Kirchoff's Current Law
KVL	Kirchoff's Voltage Law

G

GRCA	Gain Reduction Control Amplifier
------	----------------------------------

H

HSU-HH	Helmut-Schmidt-University Hamburg
--------	-----------------------------------

F

FET	Field-effect Transistor
-----	-------------------------

S

SP	Signal Preamplifier
SPL	Sound Pressure Level

V

VCA	Voltage-controlled Amplifier
VVRA	Voltage-variable Resistor Attenuator

T

TUHH Technische Universität Hamburg-Harburg

List of Software

Name	Version	URL	Comment
Java Development Kit	1.5 U6	http://java.sun.com	Java SDK
MATLAB	R2012a	http://mathworks.com	Performed simulation
Audacity	2.0.5	http://audacity.sourceforge.net	Played and recorded audio

Table C.2: *List of Software.*

Bibliography

- [1] G. Barlindhaug, “Analog Sound In The Age Of Digital Tools: The Story Of The Failure Of Digital Technology,” in *A Document (Re)turn: Contributions from a Research Field in Transition*. Peter Lang, 2007, pp. 73–93.
- [2] S. Bennett, “Endless Analogue: Situating Vintage Technologies In The Contemporary Recording And Prouction Workplace,” *Journal on the Art of Record Production*, vol. 7, Nov. 2012.
- [3] J. Pakarinen and D. Yeh, “A Review Of Digital Techniques For Modeling Vacuum-Tube Guitar Amplifiers,” *Computer Music Journal*, vol. 33, no. 2, pp. 85–100, May 2009.
- [4] M. Holters and U. Zölzer, “Physical Modelling of a Wah-Wah Effect Pedal as a Case Study for Application of the Nodal DK Method to Circuits with Variable Parts,” in *Proc. of the 14th International Conference on Digital Audio Effects (DAFx-11)*, Paris, France, Sep. 2011.
- [5] K. Dempwolf, M. Holters, and U. Zölzer, “Discretization Of Parametric Analog Circuits For Real-Time Simulatins,” in *Proc. of the 13th International Conference on Digital Audio Effects (DAFx-10)*, Graz, Austria, Sep. 2010.
- [6] U. Zölzer, *Digital Audio Signal Processing, 2nd. ed.* John Wiley & Sons, Ltd, 2008, ISBN 0-47-099785-7.
- [7] R. C. Mathes and S. B. Wright, “The compandor - an aid against static in radio telephony,” *Bell Systems Technical Journal*, vol. 13, pp. 315–322, 1934.
- [8] A. Moore, “All Buttons In: An Investigation Into The Use Of The 1176 FET Compressor In Popular Music Production,” *Journal on the Art of Record Production*, vol. 6, Jun. 2012.
- [9] A. Case, *Sound FX: Unlocking The Creative Potential Of Recording Studio Effects*. Focal Press, 2007, ISBN 0-240-52032-7.
- [10] UREI, “Model 1176LN Peak Limiter User Manual,” 1989.
- [11] D. Crane, “UAD-1 Feature: The 1176 Comp-Distortion Trick,” Available at: <http://www.uaudio.com/webzine/2003/august/text/content3.html>, Universal Audio WebZine, Volume 1, Number 5 [Accessed: November 2013], Aug. 2003.
- [12] W. Shanks, “1176 and LA-2A Hardware Revision History,” Available at: <http://www.uaudio.com/blog/1176-la2a-hardware-revision-history>, Universal Audio [Accessed: November 2013].

- [13] G. Massobrio and P. Antognetti, *Semiconductor Device Modeling with SPICE, 2nd. ed.* McGraw-Hill, Inc., 1993, ISBN 0-07-002469-3.
- [14] K. C. S. Adel S. Sedra, *Microelectronic Circuits, 5th. ed.* Oxford University Press, 2007, ISBN 0-19-531454-0.
- [15] S. Sze, *Semiconductor Devices: Physics and Technology.* John Wiley & Sons, Ltd, 1985, ISBN 0-47-187424-8.
- [16] H. Shichman and D. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," *IEEE Journal of Solid-State Circuits*, vol. 3, no. 3, pp. 285–289, Sep. 1968.
- [17] T. Taki, "Approximation of Junction Field-Effect Transistor Characteristics by a Hyperbolic Function," *IEEE Journal of Solid-State Circuits*, vol. 13, no. 5, pp. 724–726, Jan. 1978.
- [18] K. Åström and B. Wittenmark, *Computer-controlled Systems, Theory and Design (3rd ed.)*. Prentice Hall, 1996, ISBN 0-13-314899-8.
- [19] G. Borin, G. D. Poli, and D. Rocchesso, "Elimination of Delay-Free Loops in Discrete-Time Models of Nonlinear Acoustic Systems," *IEEE Transactions On Speech And Audio Processing*, vol. 8, no. 5, pp. 597–605, 2000.
- [20] K. Atkinson, *An Introduction to Numerical Analysis (2nd ed.)*. New York: John Wiley & Sons, 1989, ISBN 0-47-150023-0.
- [21] D. T. Yeh, J. S. Abel, and J. O. Smith, "Automated physical modeling of nonlinear audio circuits for real-time audio effects - Part 1: Theoretical Development," *IEEE Transactions On Speech And Audio Processing*, vol. 18, no. 4, pp. 728–737, May 2010.
- [22] A. Vladimirescu, *The Spice Book.* John Wiley & Sons, Ltd, 1994, ISBN 0-47-160926-9.
- [23] K. Petersen and M. Pedersen, "The matrix cookbook," Available at: http://www.mit.edu/~wingated/stuff_i_use/matrix_cookbook.pdf [Accessed: December 2013], May 2008.
- [24] A. Ortiz-Conde, F. G. Sanchez, J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectronics Reliability*, vol. 42, pp. 583–596, 2002.
- [25] M. Natsume, "Revision D 1176LN," Available at: http://mnats.net/1176_revision_d.html, [Accessed: December 2013].
- [26] J. Macak, J. Schimmel, and M. Holters, "Simulation of Fender Type Guitar Preamp Using Approximation And State-space Model," in *Proc. of the 15th International Conference on Digital Audio Effects (DAFx-12)*, York, United Kingdom, Sep. 2012.
- [27] M. Senior, "The 'Mixing Secrets' Free Multitrack Download Library," Available at: <http://www.cambridge-mt.com/ms-mtk.htm>, [Accessed: December 2013].