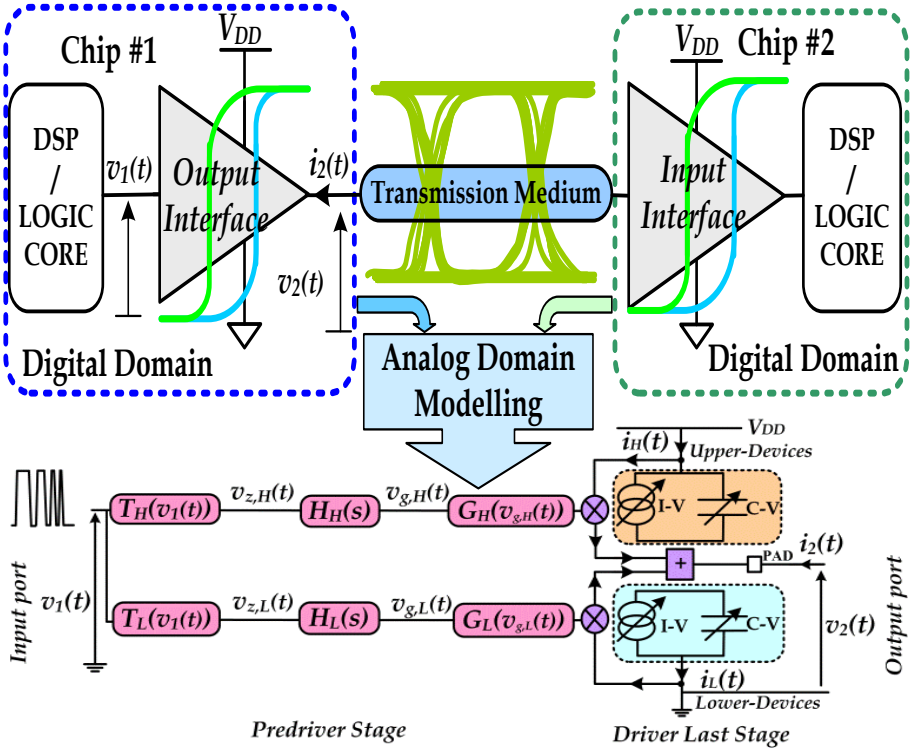
WAEL DGHAIS

Otimização e Melhoria da Modulação Comportamental para os Interfaces de E/S Analógica e de Sinal Misto de Alta Velocidade

Behavioral Modeling Optimization and Enhancement for High-Speed Analog Mixed-Signal I/O interfaces



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Wael Dghais

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Prof. Doutor. José Carlos Esteves Duarte Pedro,

Professor Catedrático do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro (Orientador).

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Palavras-chave

Interfaces analógicas e mistas de entrada/saída do circuito integrado, identificação de sistemas não-lineares, Integridade de sinal, aproximação da função, modelação comportamental baseados na tabela, análise transiente, extracção de modelo no domínio do tempo e no domínio da frequência.

Resumo

A integridade do sinal em sistemas digitais interligados de alta velocidade, e avaliada através da simulação de modelos físicos (de nível de transístor) é custosa de ponto vista computacional (por exemplo, em tempo de execução de CPU e armazenamento de memória), e exige a disponibilização de detalhes físicos da estrutura interna do dispositivo.

Esse cenário aumenta o interesse pela alternativa de modelação comportamental que descreve as características de operação do equipamento a partir da observação dos sinais eléctrico de entrada/saída (E/S).

Os interfaces de E/S em chips de memória, que mais contribuem em carga computacional, desempenham funções complexas e incluem, por isso, um elevado número de pinos. Particularmente, os *buffers* de saída são obrigados a distorcer os sinais devido à sua dinâmica e não linearidade. Portanto, constituem o ponto crítico nos de circuitos integrados (CI) para a garantia da transmissão confiável em comunicações digitais de alta velocidade.

Neste trabalho de doutoramento, os efeitos dinâmicos não-lineares anteriormente negligenciados do *buffer* de saída são estudados e modulados de forma eficiente para reduzir a complexidade da modelação do tipo caixa-negra paramétrica, melhorando assim o modelo standard IBIS. Isto é conseguido seguindo a abordagem semi-física que combina as características de formulação do modelo caixa-negra, a análise dos sinais eléctricos observados na E/S e propriedades na estrutura física do *buffer* em condições de operação práticas.

Esta abordagem leva a um processo de construção do modelo comportamental fisicamente inspirado que supera os problemas das abordagens anteriores, optimizando os recursos utilizados em diferentes etapas de geração do modelo (ou seja, caracterização, formulação, extracção e implementação) para simular o comportamento dinâmico não-linear do *buffer*. Em consequência, contributo mais significativo desta tese é o desenvolvimento de um novo modelo comportamental analógico de duas portas adequado à simulação em *overclocking* que reveste de um particular interesse nas mais recentes usos de interfaces de E/S para memória de elevadas taxas de transmissão.

A eficácia e a precisão dos modelos comportamentais desenvolvidos e implementados são qualitativa e quantitativamente avaliados comparando os resultados numéricos de extracção das suas funções e de simulação transitória com o correspondente modelo de referência do estado-da-arte, IBIS.

Keywords:

Analog mixed-signal IC I/O interfaces, nonlinear system identification, signal integrity (SI), functional approximation, table-based behavioral modeling, transient analysis, Time and frequency domain model extraction.

Abstract:

Signal integrity (SI) simulation of high-speed digital interconnected system via transistor level models is computational expensive (e.g. CPU time and memory storage), and requires the availability of physical details information of device's internal structure. This scenario raises the interest for a behavioral modeling alternative which describes the device's operation characteristics based on the observed input/output (I/O) electrical signal.

I/O buffers that interface memory's interconnects have major share in the computational load containing a very active complex functional part and high numbers of pins. Particularly, output buffers/drivers are forced to distort the I/O signals due to their nonlinear dynamics. In this concern, they constitute the integrated circuit (IC) bottleneck of ensuring reliable data transmission in the high-speed digital communication link.

In this PhD work, the previously neglected driver's nonlinear dynamic effects are efficiently captured to significantly reduce the state of the art black-box parametric modeling complexities and enhance the input/output buffers information specifications (IBIS). This is achieved by following the gray-box approach that merges the features of the black-box model's formulation, the analysis of the observed I/O electrical signals and the buffer's physical structure properties under practical operation conditions.

This approach leads to physically inspired behavioral model's construction procedure that overcomes the issues of the previous modeling approaches by optimizing the resources used at different model's generation steps (i.e. characterization, formulation, extraction, and implementation) to mimic the driver's nonlinear dynamic behavior. Moreover, the most important achievement is the development of a new two-port analog behavioral model for overclocking simulation that copes with the recent trends in I/O memory interfaces characterized by higher data rate transmission.

The effectiveness and the accuracy of the developed and implemented behavioral models are qualitatively and quantitatively assessed by comparing the numerical results of their functions extraction and transient simulation to the ones simulated and extracted with transistor level models and the state of the art IBIS in order to validate their predictive and the generalization capabilities.

TABLE OF CONTENT

LIST OF ACRONYMS

Acronyms	Definition
ANNs	Artificial Neural Networks
ANFIS	Adaptive Neuro-Fuzzy Inference Systems
AMS	Analog Mixed Signal
ADS	Advanced Design System
CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide -Semiconductor
C-V	Capacitance-Voltage
DUM	Device Under Modeling
DAC	Data Access Component
DC	Direct Current
DR	Data Rate
DSP	Digital Signal Processing
ESD	Electrostatic Discharge
ESS	Exponential Swept-Sine
ODE	Ordinary Differential Equation
Q-V	Charge-Voltage
IBIS	Input/Output Buffer Information Specification
IC	Integrated Circuit
I-Q	Current-Voltage
I/O	Input/Output
IP	Intellectual Property
I-V	Current/Voltage
ITRS	International Technology Roadmap for Semiconductors
LUT	Look Up Table
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMSE	Normalized Mean Square Error
PD	Pull-Down
PU	Pull-Up
PCB	Printed Circuit Board

PWL	Piece-Wise Linear
RE	Relative Error
RBF	Radial Basis Function
SDD	Symbolic Defined Device
SFWFTD	Spline Function With Finite Time Difference
SI	Signal Integrity
VHDL	Very high-speed integrated circuit Hardware Description
VNA	Vector Network Analyzer
VLSI:	Very Large Scale Integration
V-t	Voltage-Time

LIST OF TABLES

LIST OF FIGURES

CHAPTER I:

Preliminaries and Backgrounds

This chapter presents a general introduction to the down-scaling trend in very-large-scale integration (VLSI) circuit and concepts concerning signal integrity (SI) and working mechanisms for digital communication systems. The classifications of various mathematical modeling approaches that can be used within the computer aided design (CAD) tools to evaluate the SI performance of a high-speed digital link are then described. Moreover, the need for suitable modeling of input/output (I/O) buffers characterized by their nonlinear dynamic behaviors for an accurate and fast prediction of SI is explained. This chapter ends by discussing the organization and the flow of the PhD thesis.

1.1 Introduction

Over the last decades, the continuing downscaling of the voltage supply, the high density integration, and the switching speeds of VLSI circuits have been increasing fast in the IC CMOS process in order to achieve high performance logic operation with reduced power and cost. As shown in Figure 1.1, the number of transistors per chip grows exponentially which reduces 25% the cost-per function every year in the ITRS [1]. It is worth to note that the ITRS partially uses historical trends to project the future of the semiconductor industry.

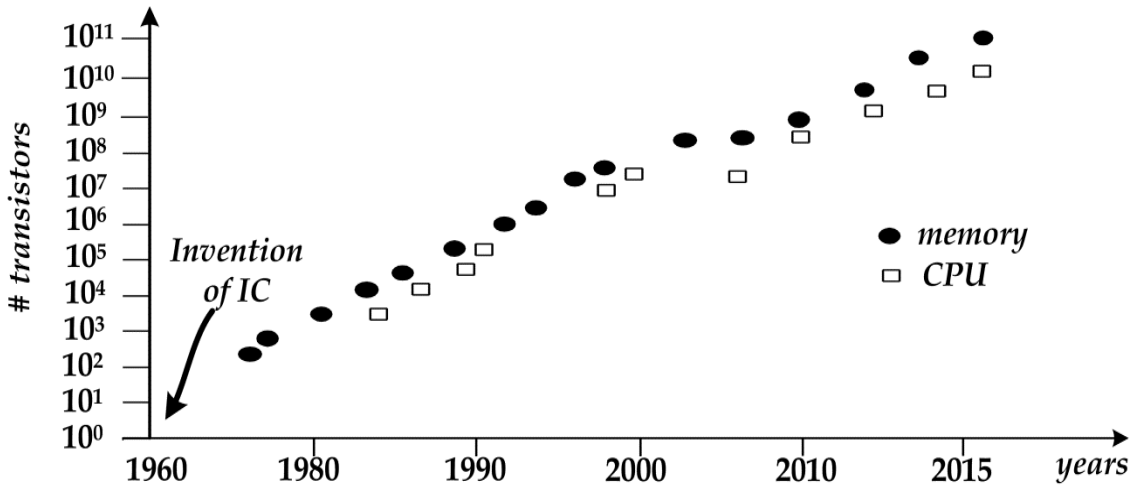

Figure 1. 1 Integration's number of transistors per chip [1].

In addition, Figure 1.2 shows the trend of the clock frequency of microprocessors which had kept increasing until it reached 3 GHz. Although it has been decreased slightly down to 1–2 GHz when introducing the multi-core scheme, the local on chip and the core clock frequency is expected to keep increasing [1]. Consequently, the high frequency effects observed in the digital interconnected subsystems that were previously ignored in the model's generation cannot be overlooked anymore and have to address these issues efficiently for accurate system level analysis [2], [3].

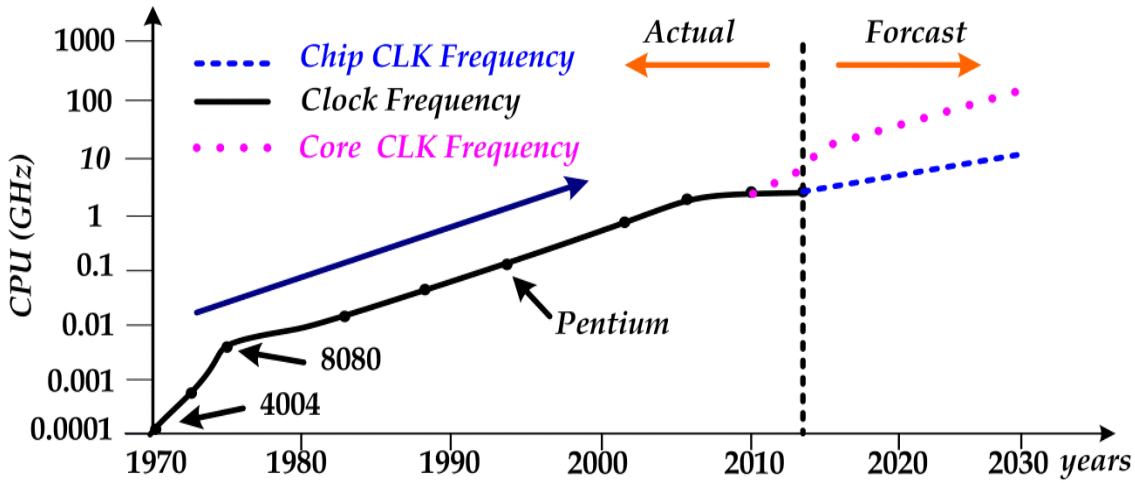

Figure 1. 2. Clock frequency trend for local on-chip (Core) and entire chip [1].

These circumstances have brought tremendous challenges to reliably transmit the data at high-speed. In fact, additional non-ideal effects may be generated and lead to severely distorted voltage and current waveforms and signal jitter, and result in faulty switching and logic errors [3], [4]. Consequently, the high-speed system's design requires some additional efforts to overcome these issues by accurately predicting these effects in early design stages in order to ensure good signal integrity. This can be achieved by developing more efficient and accurate behavioral models for the main subsystems (i.e. I/O buffers) to capture their nonlinear dynamic behavior in order to evaluate the performance of the I/O signal quality in the whole high-speed digital link [5].

1.2 SI Simulation of Digital Transmission Link

The chip's functionality is performed within the logic core. However, the I/O buffers are much larger than the core cells and they are required to bond the die to the package and the external interconnects. This transmission link within the IC introduces distortion into the propagating electrical signals. In fact, it can be decomposed as an

active part representing the I/O buffers that interface the logic core and the passive package and the printed circuit board (PCB) interconnects as depicted in Figure.1.3.

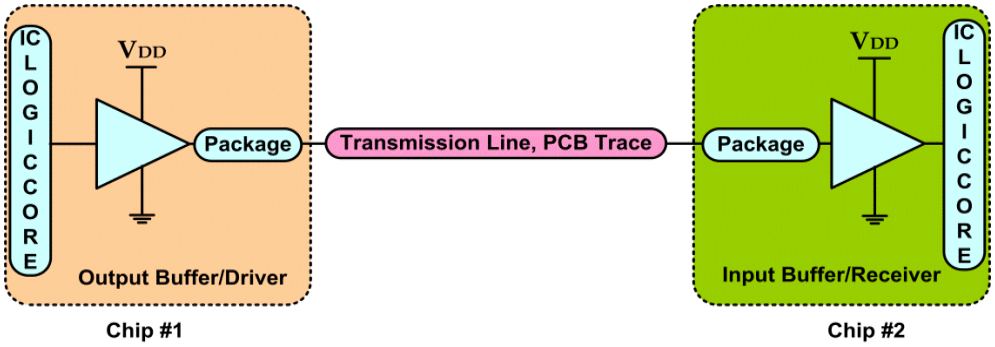

Figure 1. 3 Main parts of a generic of a high-speed digital interconnected system.

The I/O signals leave the chip #1 by means of an output buffer/driver characterized by a highly nonlinear dynamic behavior. After propagating through the IC's package, and then the PCB, which are usually modeled as passive distributed transmission line elements, the signal reaches the chip #2 where the input buffer/receiver detects the transmitted input signal with the above mentioned imperfections according to the switching point voltage. A more detailed description of the I/O buffer enclosed in its package is shown in Figure 1.4.

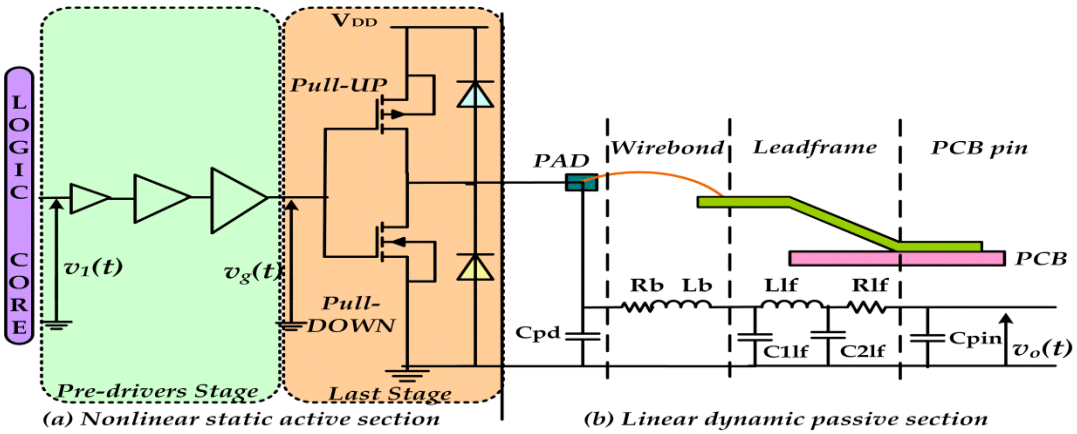

Figure 1.4 The two I/O buffer model sections: (a) Nonlinear active section and its main electrical variables. (b) Three-stages linear dynamic section of the package network.

In the active section, the last stage's large transistors are arranged as a pull-up (PU) and a pull-down (PD) network. They impose the dominant electrical behavior of the device, while the pre-drivers stage act mostly as highly nonlinear voltage transfer characteristics followed by a resistive path feeding the gate capacitances of the last stage. On the other hand, the passive section structure is extracted from the associated small-outline IC package category [6] from Spectre simulator. The first element, C_{pd},

stands for the capacitance associated to the pad where the bond wire attaches the die to the package. After that, the quantities L_b and R_b are respectively the lumped bond wire inductance and resistance. In addition, the inductance L_{lf}, the coupling capacitances C_{1lf} and C_{2lf} and the resistance R_{lf} represent the lead frame equivalent lumped model. Finally, C_{pin} models the capacitive coupling between the lead frame solder pad and the PCB backplane ground.

Therefore, in circuit-level simulation, the digital I/O buffer circuits have a major share in the computational load containing a very complex functional part and a high number of pins in the IC. Furthermore, due to the high switching frequency that is always being pushed to higher limits, and to the current intensity that is needed to source a generalized set of external ICs, output buffers are forced, in most cases, to distort the I/O signals due to their nonlinearity and dynamics. Thus, they constitute the IC bottleneck in terms of switching speed. In this concern, signal integrity (SI) is a very important task of ensuring sufficient fidelity of a signal transmitted between a driver and a receiver for proper functioning of the circuit (e.g., the signals over the high-speed bus between a processor and its chipset). A signal with good integrity characteristics is defined as one observed at the receiver within the desired time window and with adequate amplitude levels. The ideal voltage waveform in the perfect logic world and the distorted signal - in terms of amplitude and time deviations- by the active driver and the package dynamics of Figure 1.4 are illustrated in Figure 1.5 where the different manifestations of SI degradation are:

- A high logic voltage level lower than the minimum high acceptable level, V_{IH},
- A low logic voltage level higher than the maximum acceptable low level, V_{IL},
- Excessive signal delay - a rising/falling (t_r/t_f) edge shows skews longer than the acceptable timing windows,
- Overshoot, undershoot and glitch - ringing and oscillation, long settling time.

These effects are aggravated with the increase of the driver's clock frequency and the mismatch load with external interconnects.

At the receiver's input, voltage above the reference value V_{IH} is considered as logic high, while voltage below the reference value V_{IL} is considered as logic low. Any delay or amplitude's distortion of the waveform will result in a failure of the data transmission. For instance, if the signal in Figure 1.5 exhibits excessive ringing into the gray zone while the detection occurs, then the logic level cannot be correctly received.

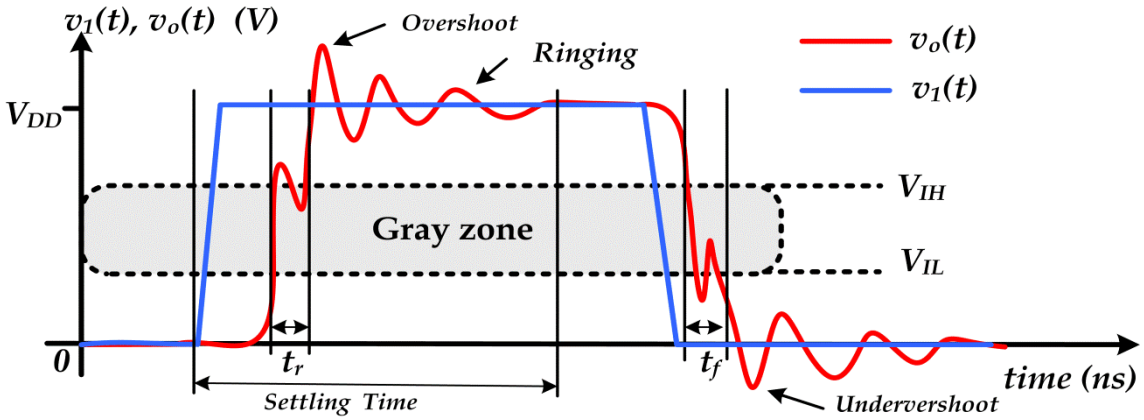

Figure 1. 5. Ideal waveform at the logic core and Real waveform at receiving gate.

According to this analysis, we conclude that the aim of SI analysis is to ensure reliable high-speed data transmission by evaluating three main issues. Firstly, the reflections that occur because of interconnect discontinuities such as impedance mismatch, vias, and other line discontinuities. Secondly, the noise induced by neighboring connections (crosstalk), produced in a signal line by other lines as inductive and capacitive coupling. Thirdly, the disturbance on power distribution by switching of the digital devices introduces a noise in a signal line that manifests itself by the voltage drop along the inductive path of the power supply network for the IC and its packaging. This noise is also called power and ground bounce, ΔI-noise or Simultaneous Switching Noise (SSN) [2], [3]. Hence, the performance evaluation of high-speed digital systems requires the accurate prediction of the waveforms propagating through the digital interconnects. Such prediction is usually carried out in a time domain simulation that allows the detailed analysis of the interactions between the digital IC peripheral devices (i.e. the input/output buffers' impedances, and the loading interconnect traces).

In order to perform such simulations, a feasible strategy must subdivide the overall system in well-defined sub-systems typically found along the signal propagation paths, i.e., active devices, package, and transmission-line interconnects as illustrated in Figure 1.3. Each sub-system is separately characterized by a macromodel, i.e., a set of equations that are able to reproduce with sufficient accuracy the electrical behavior of the sub-system which is implemented in CAD library (e.g., SPICE-like, advanced design system (ADS), etc). Hence, modeling digital I/O buffer circuits to accurately capture their nonlinear dynamic behavior becomes a big challenge for SI performance evaluation of modern digital interconnected systems. This will result in an efficient use of CAD tools by providing the valid and appropriate large-signal behavioral models of the main connected sub-circuits [7].

The next section of this chapter outlines basic modeling approaches for the development of a driver's a mathematical model suitable for system-level simulation by highlighting their strengths and limitations. Finally, the last section outlines how we can describe the driver's behavioral parametric model using system identification theory.

1.3 System Identification Framework

1.3.1 Hierarchy of Modeling Approaches

As described in the previous section, modern high-speed digital communications systems are too complex to permit the complete simulation of the nonlinear behavior at the transistor level (TL) description. This model is the most accurate solution, and usually it is considered as the reference for the device. Unfortunately, the model completely discloses the internal details of the device. In addition detailed physical descriptions are generally large in size and their effect is to drastically slow down the simulation.

Finally, they cannot be easily plugged in any simulator, since they are usually written for a specific simulator in particular when encryption holds. This problem presents a significant productivity bottleneck for design engineers. A typical design and modeling hierarchy is depicted in Figure 1.6.

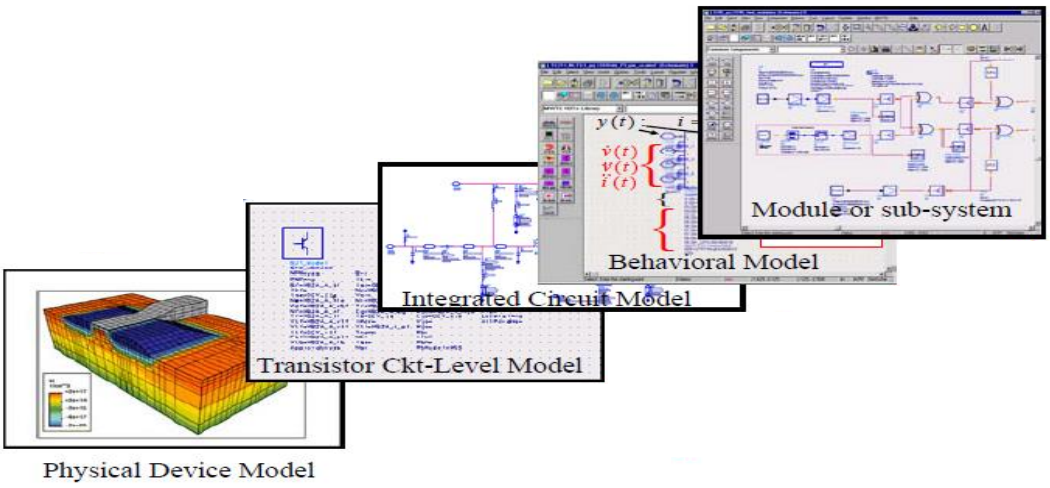

Figure 1. 6 Model hierarchy according to the physical details included in the model description and the design level copied from [8].

The modeling hierarchy begins at the bottom with the device model described by the detailed semiconductor physics. It ends at the top by a high-level abstraction that describes the terminal behavior through black-box or equivalent circuit behavioral functions. Since there are too many nonlinear interactions taking place at the system-level, the CAD simulation using TL models which is based on Newton Raphson

algorithm takes a long time to converge and uses too much memory to run [8]. A solution to this simulation bottleneck is to generate reduced-order behavioral models that describe the essential behavior of the complex active circuit blocks [9], [10].

Furthermore, behavioral modeling approaches can be classified according to the level of physical information used in the description of the model mathematical formulation (i.e. physically based (transparent) or black-box (opaque) model's structure). Firstly, we have the black-box model that accurately describes the device's experimental data by means of a high-level mathematical abstraction. The model simply solves a numerical fitting problem without reference to any underlying physics. Good examples of black box models are any form of parametric model based on artificial neural networks (ANNs) or other curve fitting techniques [11]-[13]. Secondly, the gray-box models which are parameterizations based on various degrees of physical insights. For instance, the large-signal equivalent circuit's model composed of electrical elements such as resistors, capacitors, and nonlinear current or voltage sources, which can characterize the electrical properties of the active I/O buffers. The physically meaningful structure is determined by analyzing the recorded experimental data that carries the information on the device's behavior and correlates it to the mechanism describing the device's electrical properties by the physical reasoning and approximation theory [14]-[19].

Both the black-box and gray-box approaches use system identification theory tools to generate their model functions or to extract their parameters. They aim to enable circuit designers to capture high-level descriptions of modules and subsystems that speed-up the simulation and hide intellectual property (IP) while guarantying reasonable accuracy. Therefore, circuit designers can send their models to the system design team reducing overall time-to-market and thus generating additional revenues. The behavioral modeling framework will be described in the following subsections.

1.3.2 Device Characterization

When building a mathematical model to describe the I/O buffer's circuit behavior, the model maker generally has two sources of information; *a priori* knowledge concerning the I/O buffers behavioral model properties (i.e. design circuit, application, and model structures) and a representative experimental data of the active device nonlinear dynamic effects. Furthermore, the performance of behavioral model's construction is influenced by two key aspects: the observation and the formulation. The

observation refers to the accurate acquisition of the signals at the input and output ports of the device under modeling (DUM) while exciting the appropriate behavior as shown in Figure 1.7. The formulation corresponds to the choice of a suitable mathematical relation that describes all the significant interactions between the DUM's input and output signals. Accordingly, sufficient background and *a priori* knowledge of the DUM is required to observe the right behavior and choose the adequate formulation.

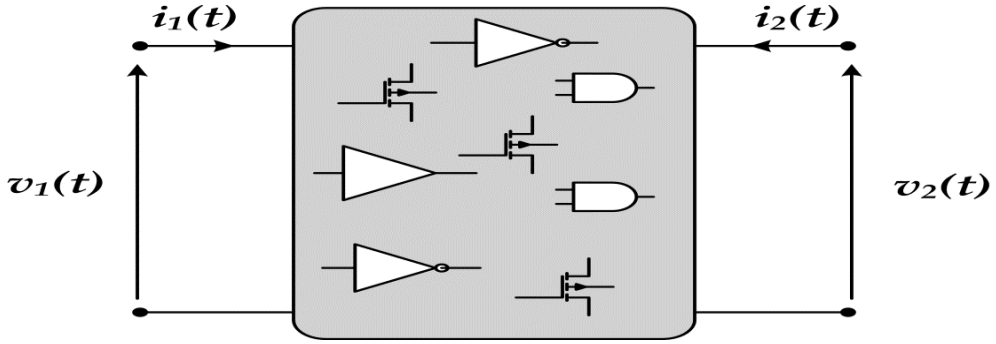

Figure 1. 7. Generic structure of the two-port I/O buffer with its relevant electrical variables.

The terminal currents $i_1(t)$ and $i_2(t)$ of the general two-port behavioral model for the general structure of Figure 1.7 can be expressed in time domain as a function of the two-port terminal voltages $v_1(t)$, $v_2(t)$, and their successive higher order derivatives

$$\begin{cases} i_1(t) = F_1\left(v_1(t), \dfrac{dv_1(t)}{dt}, \dots, v_2(t), \dfrac{dv_2(t)}{dt}, \dots i_2(t), \dfrac{di_2(t)}{dt}, \dots, \dfrac{di_1(t)}{dt}, \dots\right) \\ \qquad\qquad c \\ i_2(t) = F_2\left(v_1(t), \dfrac{dv_1(t)}{dt}, \dots, v_2(t), \dfrac{dv_2(t)}{dt}, \dots i_2(t), \dfrac{di_2(t)}{dt}, \dots, \dfrac{di_1(t)}{dt}, \dots\right) \end{cases} \tag{1.1}$$

The system identification tool does not provide foolproof that always and directly leads to the optimum results. On the basis of the *a priori* knowledge, the excitation signal is designed to reflect the observed behavior under a specific excitation, the I/O buffer simulation setup is selected, the measurement procedure is specified and the operation range is defined. For instance, the model structure defined by the nonlinear multivariate functions $F_1(.)$, $F_2(.)$ has to be optimized and identified according to the following modeling framework as depicted in Figure 1.8, which has an interactive logical flow [20].

As arrows in Figure 1.8 point out, the model construction's steps can be recursive and iterative. For instance, if the model's accuracy is not satisfying, various model structures and identification signals should be tested and the process repeated. The characterization step considers generating a large-signal data by driving the DUM with

adequate excitation signal and record the time and/or frequency domain data that carry information on its behaviour. The data obtained from stimulation or measurement is processed and analyzed to fit the proper model structure.

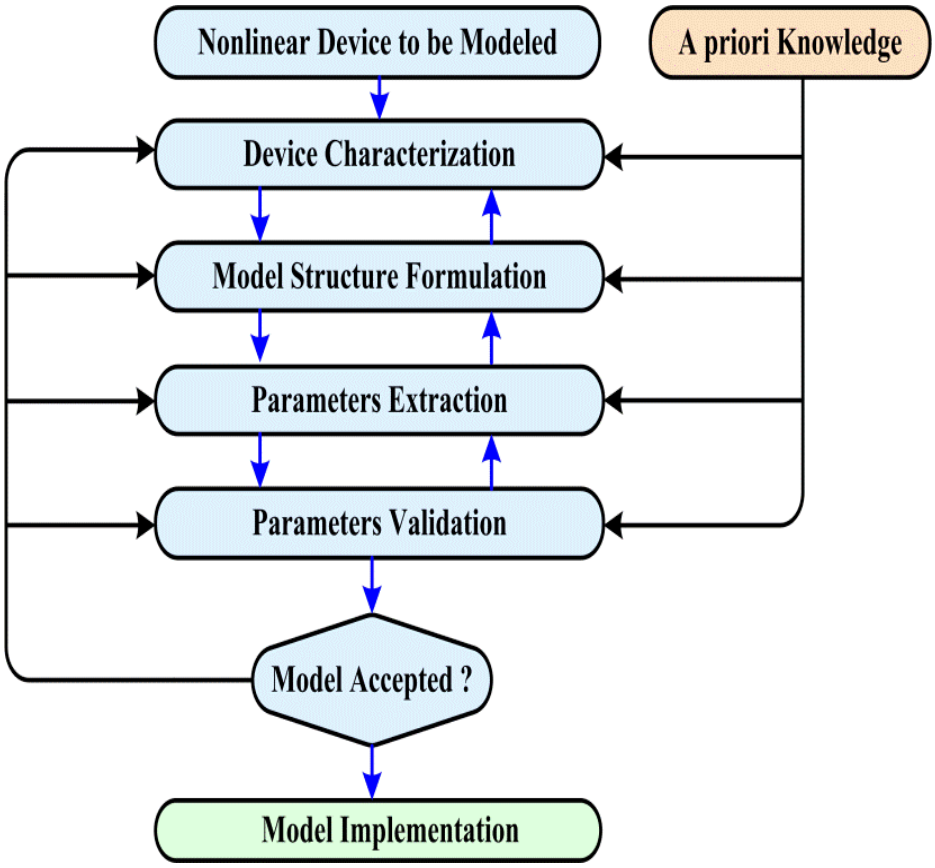

Figure 1. 8. Behavioral modeling framework based on system identification theory.

It is worth noting that the DUM's behavior can be attributed to many sources so that different simulation setups and excitation signal can be used to extract the adequate behavior and then combine them to construct the complete interaction between these effects. The gathered set of measurement results is a good representation of the device behavior only if the identification signal is properly designed to stimulate the nonlinear static characteristics and to excite all possible dynamics of the DUM. Thus, it should cover the frequency and magnitude ranges of interest which is important both for convergence of the behavioral model when used in the simulator. Besides, although the circuit terminations have no impact on the modeling process of linear circuit, the choice of terminations in nonlinear behavioral modeling directly affects the generalization property of the model. In fact, the model accuracy needs to be assessed by subjecting it to various boundary conditions (i.e. I/O signals or terminations). Finally, the resulted

model is implemented in the CAD library. More detailed descriptions of the model's construction steps are presented in the following sub-sections.

1.3.3 Model Structure Formulation and Extraction

It is worth noting that behavioral modeling activities are not only restricted to replicate the I/O data with general curve fitting methods, that will be presented in subsection 2.2, for given infinite order and complexity [45]. In fact, it involves more challenging tasks as model structure formulation and optimization by means of nonlinear multidimensional function approximation to reduce the model identification and running complexities. This is achieved by analyzing the observed I/O signals, investigating the device physical design structure, and its operation under practical operation condition in order to develop a model that is coupled with measured quantities as it is the case of Input/output Buffer Information Specification (IBIS) that will be described in more details in the subsection 2.3.

Ljung summarizes this model structure formulation problem as follows: "This is no doubt the most important and, at the same time, the most difficult choice in the system identification procedure. It is here that a priori knowledge and engineering intuition and insight have to be combined with the formal properties of the models." [9].

Furthermore, the model extraction heavily depends on the approximation methods used in the model formulation and the followed identification algorithm of its functions and parameters. In fact, model functions can be dependently extracted in order to minimize the complete model error [14]. It is worth noting that not only special care should be taken regarding the simulation setup but also the ability to perform the model extraction from laboratory measurements by collecting the required data from the available equipment and instruments. The recursive or direct model formulation depends on how deep the memory effect is exposed by the DUM behavior excited with suitable excitation signal.

1.3.4 Model Implementation and Validation

Once the adequate model structure and the corresponding identification algorithm are developed, the model must be exported to the format suitable for the use in most modern circuit simulators. It is worth noting that possible enhancements in behavioral modeling can be achieved by formulating them in language native to the simulator so it eases its implementation and interpolation by different circuit simulators.

Besides, the model validation involves various procedures to evaluate how the model relates to the measurement results and the intended usage. It amounts of verifying the correctness and the validity range of the behavioral model in the practical condition application by determining the correlation between the behavioral model's and the TL model numerical results. This requires the selection of metrics to quantify the model accuracy while using boundary conditions (i.e. I/O signals or terminations) that have never been used in its extraction.

If the model fails to meet the selected requirements, the model's identification procedure has to be restarted from an earlier step as shown in Figure 1.8. Various factors can lead to a deficient model:

- The driver's measurements do not provide sufficient information or are too noisy.
- The selected model structure (i.e. linear vs. nonlinear) is inappropriate to represent the driver's behavior.
- The chosen order (i.e. number of basis function and the memory length) of the model is too low or too high.
- The model's identification algorithm failed to correctly extract all the parameters.

The model's extrapolation assesses the predictive capabilities of the constructed model by subjecting it to excitation signal's magnitude and frequency ranges higher than the one used in the characterization and extraction steps while loaded by different terminations. In such case, the implemented model's convergence during the transient simulation should be also verified. This is because simulators solve nonlinear algebraic equations using iterative algorithms such as Newton's method and it may happen that, in the process of convergence, the iteration takes a step where the independent model variables go outside the region of validity. In fact, the simulator extrapolates the value of the dependent variable (output of the model) according to the definition given for the functions $F_1(.)$, $F_2(.)$ in (1.1) and cannot encounter the solution of the nonlinear numerical problem and thus will never converge.

1.3.5 Summary

The evaluation of the signal integrity is of a paramount importance with the recent trends in VLSI design characterized by the downscaling of the package integration and the clock frequency. As a result, the number of failures caused by SI problems is on the

rise because existing modeling methodologies for I/O buffers cannot address these issues effectively.

Since the correct operation of I/O buffers is crucial to reliably transmit data through high-speed digital links, developing an efficient model to accurately simulate their nonlinear dynamic behavior is a challenging task that is motivating several research activities [11]-[15]. In fact, the previously neglected nonlinear dynamic effects in the active I/O buffers should be captured in the supplied model to the designer in order to accurately perform time domain simulation.

In order to overcome the TL limitations, behavioral modeling appears to be effective. Such high-level abstractions are developed to characterize the device behavior by subjecting it to various types of excitation to find out the different sources of nonlinearity and dynamics and their effects on device's behavior. This enables fast and accurate prediction of magnitude and timing waveform quality degradation due to these physical imperfections. Such behavioral models can be classified in two types according to the physical knowledge reflected in the model generation's process (i.e. the black-box and gray-box techniques).

1.4 Thesis Contributions and Dissertation Outline

According to the new paradigm in the integrated electronic system and the available approaches for circuit descriptions of the output buffers/drivers switching properties in modern simulators, this doctoral thesis is focused in the construction of analog behavioral models of the nonlinear dynamic high-speed drivers enabling efficient simulation and evaluation of SI performance. In fact, modeling the input buffers/receivers is considered as a simpler case of the drivers' modeling problem and its resulting behavioral models can be extended to model the receiver case. This PhD work is centered on the system identification framework to improve the previously published behavioral modeling [11]-[15]. In fact, the model should balance the accuracy/complexity trade-off which requires profound knowledge of device nonlinearity, circuit design, and nonlinear characterization tools and model formulations.

This work will contribute to reduce the order of nonlinear parametric models [11], [12] and enhance the equivalent circuit IBIS model's structure [13]-[15] by merging the features of the black-box and gray-box driver's behavioral modeling generation. Moreover, a completely new physically inspired behavioral two-model mathematical

formulation extraction and implementation is generated for simulating the driver's behaviors in overclocking operations. These achievements have an important impact to ease the design of the future high-speed digital link by providing effective numerical models of memory I/O interfaces for better simulation performances within the CAD tools.

The remainder of the thesis is organized as follows.

Chapter 2 gives an overview of the common mathematical modeling and function approximation techniques used in nonlinear driver's behavioral modeling approaches. It also outlines other possible appealing techniques that will be used in improving the previously published approaches and eases the understanding of the achieved results in Chapter 3. Particularly, the general curve fitting and the equivalent circuit-level functions are detailed by discussing their strengths and limitations.

Chapter 3 describes the developed research work that aims improving both the state-of-the-art IBIS and the nonlinear parametric modeling approaches by presenting a physically meaningful empirical model to capture only the one-port driver's last stage output port behavior along with their different extraction procedures and implementation. In the chapter's last section, an optimum and physically inspired two-port analog behavioral model for accurately capturing the driver's operation in overclocking conditions is developed.

Finally, Chapter 4 provides the main conclusions that can be drawn from the achieved results of the PhD thesis and presents the possible future work.

CHAPTER II:

Driver's Behavioral Modeling Methodologies

2.1 Introduction

Measured or simulated nonlinear behavior can be expressed by a series of equations in time or frequency domain using voltages, currents or incident and reflected waves at all ports. If one performed an infinite number of measurements by changing the environment (i.e. power supply levels, biases, load impedances, etc.), the resulting infinite table of realizations would describe this device completely. Clearly, this is not an option. However, performing a finite set of observations that can be interpolated with confidence using mathematical modeling and function approximation is more practical.

With the aim of analyzing the origins of behavioral modeling developed for output buffer/driver to capture its nonlinear and memory effects and in a way to establish a link with their modeling approaches through large-signal equivalent circuit model and parametric curve fitting techniques, a comprehensive overview of the mathematical modeling framework based on system identification theory is presented in this chapter. For sake of simplicity, the methodology is firstly described for one-port active devices. Then, it is extended to two-ports covering the black-box and the gray-box formulations and identification for modeling the driver's nonlinear dynamic behaviors where the state-of the-art Input/output Buffer Information Specification (IBIS) and parametric modeling are analyzed and discussed.

2.2 Mathematical Modeling and Function Approximation

Device simulators such as ADS [40] or SPICE [43] require that terminal currents are expressed in some functional form. Parametric behavioral models are based on approximating the device's behavior by a simpler function over some defined region and to some specified accuracy. When a function is fitted to measured data, various candidate basis functions can be selected from a large set, such as the polynomial family, rational functions, splines, and neural networks which are discussed in [10]. Besides, the function parameters are adjusted by a proper algorithm until the data is represented with sufficient accuracy over the measured data space.

In one-port networks, the input and output signals (i.e. voltage, current or incident and reflected waves) that enter and exit the one terminal are shown in Figure 2.1.

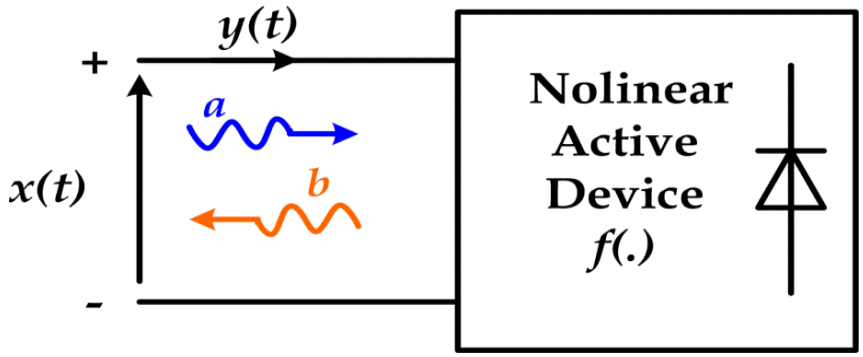

Figure 2. 1. One-port active network.

In a memoryless or static system, - in which no charge or magnetic flux storage elements (no capacitors or inductors) exist, so that the voltages and currents at any instant do not depend upon previous values of voltage or current-, the output of the one-port device, $y(t)$, can be uniquely defined as a function of the instantaneous input signal $x(t)$, and the model can be reduced to $y(t) = f(x(t))$ or $y = f(x)$ since the dependence on time is immaterial. However, the output buffers, as all active electronic circuits, present memory effects and thus they are said to be dynamic. The output now depends also on the input, or output past and system state. The input-output relation becomes an operator that maps a function of time $x(t)$ onto another function of time $y(t)$. Thus, the input–output mapping of the device can be represented by the following forced nonlinear ordinary differential equation (ODE) [21]:

$$f\left[y(t), \frac{dy(t)}{dt}, \dots, \frac{d^p y(t)}{dt^p}, x(t), \frac{dx(t)}{dt}, \dots, \frac{d^r y(t)}{dt^r}\right] = 0 \qquad (2.1)$$

This states that the output and its time derivatives can be nonlinearly related to the input and its time derivatives. By assuming the back-ward discrete-time approximation of the continuous-time derivative of a signal (t) :

$$\frac{dz(t)}{dt} \cong \frac{1}{T_s}\left(z(kT_s) - z(kT_s - T_s)\right) = \frac{1}{T_s}\left(z(k) - z(k-1)\right) \qquad (2.2)$$

the discrete time version of (2.1) can be expressed in the recursive form:

$$y(k) = f_R\left[y(k-1), \dots y(k-q_1), x(k), x(k-1), \dots, x(k-q_2)\right] \qquad (2.3)$$

The sampling period is T_s, so that the time t corresponds to the discrete variable k such as: $kT_s, t \to k \in Z$. Also, the input-output signals such as, $x(t) \to x(k), y(t) \to y(k)$. Here $y(k)$ is the present output at time instant kT_s. It depends in a nonlinear way, on the output past $y(k-q_1)$, the present input $x(k)$, and its past $x(k-q_2)$. Nevertheless, under a broad range of conditions (basically, operator causality, stability, continuity, and fading memory), such a system can also be represented with any desirable small error by a non-recursive, or direct form, where the relevant input past is restricted to $q\{0,1,2,\dots,q_D\}$:

$$y(k) = f_D\,[x(k), x(k-1), \dots, x(k-q_D)] \tag{2.4}$$

Similarly, the behaviors of active devices, (e.g. I/O buffers) encountered in the high-speed digital communication link are described by nonlinear ODE. The behavioral modeling task consists in capturing the essential observed dynamics by constructing the function, $f(.)$, which maps the $(q_2 + q_1 + 1)$ independent variables into the dependent variable. This function can have a direct or recursive formulation, $f_D(.)$ and $f_R(.)$, respectively. In the following subsections, the parametric black-box and the gray-box modeling methodologies used in fitting and representing the nonlinear functions $f_D(.)$ and$f_R(.)$, respectively, will be presented. Accordingly different identification procedures and model descriptions in time or frequency domains will be analyzed.

2.2.1 Parametric Functions

In the first case, the direct form of a memory polynomial that interpolates $f_D(.)$functions can be written as:

$$\begin{aligned} y(k) &= \sum_{q=1}^{Q} a_1(q)x(k-q) + \sum_{q_1=0}^{Q}\sum_{q_2=0}^{Q} a_2(q_1,q_2)x(k-q_1)x(k-q_2) \\ &+ \cdots \sum_{q_1=0}^{Q} \dots \sum_{q_N=0}^{Q} a_N(q_1,\dots,q_N)x(k-q_1)\dots x(k-q_N) \end{aligned} \tag{2.5}$$

where the $a_N(q_1,\dots,q_N)$ are the memory polynomial coefficients that can be estimated in a direct way by a simple least-squares method. The last equation can be written in matrix form $Y = F.A$ in which A is the vector of the model coefficients, Y is the vector

of the output data samples and F is the matrix that contains the mixture elements of the input signal$x$. The least-squares method can be used to find the polynomial coefficients:

$$A = (F^H F)^{-1} F^H Y \tag{2.6}$$

where F^H denotes the conjugate transpose of the matrix F. Although simple in concept, this finite impulse response (FIR) polynomial model architecture is known for its large number of parameters. For similar approximation capabilities and many fewer parameters, the recursive polynomial infinite impulse response (IIR) structure can be used, but its stability should be verified at the model extraction and validation steps.

In the second case, the functions $f_D(.)$ and $f_R(.)$ are built using the ANNs. The recursive structure is illustrated in Figure 2.3 in which the dynamic mapping depends on the past values of both the input and output signals.

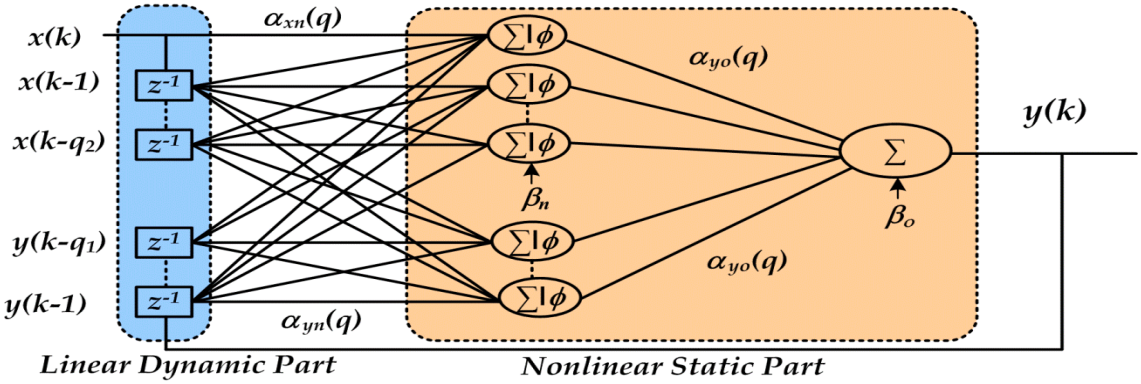

Figure 2. 2. General structure of a recursive ANN.

The ANN input-output mapping, with *N* neurons, and $\{\boldsymbol{q_1}, \boldsymbol{q_2}\}$ dynamic order for the input and the output respectively, is mathematically described by:

$$\begin{cases} u_n(k) = \sum_{q=1}^{q_1} \alpha_{yn}(q)\, y(k-q) + \sum_{q=0}^{q_2} \alpha_{xn}(q)\, x(k-q) + \beta_n \\ y(k) = \beta_o + \sum_{n=1}^{N} \alpha_{yo}(n)\, \phi(u_n(k)) \end{cases} \tag{2.7}$$

where $\alpha_{yn}(q)$, $\alpha_{xn}(q)$, $\alpha_{yo}(n)$, are weighting coefficient, β_n and β_o are bias parameters and $\phi(.)$ is the activation function. Figure 2.2 shows that the model output $y(k)$ is built from the addition of the activation functions $\phi(u_n(k))$ and the weighted outputs. The inputs $u_n(k)$ are biased sums of the various delayed version of the input $x(k)$ and output $y(k)$ weighted by the coefficient $\alpha_{xn}(q)$, and $\alpha_{yn}(q)$, respectively. The ANN model is nonlinear in the parameters $\alpha_{xn}(q)$ and $\alpha_{yn}(q)$ and linear with

respect to the parameters $\alpha_{yo}(n)$, and β_o. Various nonlinearities, $\phi(.)$, can be used as activation functions. For instance, the hyperbolic tangent function is defined as:

$$\phi(x) = \frac{e^x - e^{-x}}{e^x + e^{-x}} \tag{2.8}$$

The ANN's activation functions are bounded in output amplitude. Thus they do not share the catastrophic degradation of polynomials outside the training zone, during circuit simulation that could escalate to divergence problems.

Since, the ANNs model is usually considered as nonlinear with respect to all its parameters [22], a nonlinear least-squares algorithm is used for training by minimizing the Mean Square Error (MSE) cost function between the model and the TL outputs as shown in Figure 2.3. This means to find:

$$\Theta | \, min \left\{ \frac{1}{N} \sum_{k=1}^{N} (\hat{y}(k) - y(k))^2 \right\} \tag{2.9}$$

where $\hat{y}(k)$ is the sampled output signal, N is the total number of samples and $y(k)$ is the response of the model to the sampled input signal $x(k)$. The sampled identification signals must contain all the information of the original signals. Therefore, the sampling period T_S must be smaller than the sampling time T_N defined by the Nyquist frequency of the identification signals. On the other hand, T_N should not be too small, in order to avoid oversampling and consequent numerical problems in the minimization of (2.9). As a rule of thumb, the ratio T_N/T_S should be on the order of 2÷6.

It is worth to note that the problem (2.9) is nonconvex and the solution obtained by means of the optimization algorithm can fall into local minima of the cost function. Thereby, a good initial estimate of the model's parameters is crucial, since the initial starting point determines in which local minima the algorithm will end up which will affect the model generalization capabilities [22], [23].

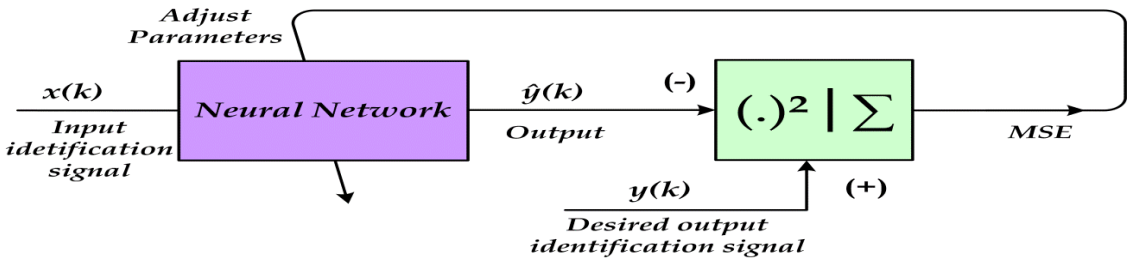

Figure 2. 3. Training scheme of an artificial neural network.

The ANNs and the polynomial expansion have been proven to universally approximate any continuous multivariate function with any degree of accuracy provided that enough neurons and dynamic orders are considered which defines the number of the ANN's weights and bias coefficients, and so its complexity. However, there is no way to know a priori the numbers of neurons or dynamic orders required for representing a specific system or the modeling improvement gained when these parameters are increased. In addition, the black-box recursive ANNs models suffer also from instability issues while the training or circuit simulation and from over-fitting during model's identification.

2.2.2 Scattering Functions

For linear dynamic devices (e.g. filters, package, linear amplifier, etc.), S-parameters provide a black-box behavioral model in frequency domain. They are small signal representation of the transmission and reflection coefficients of a DUM at the input and output ports, and are defined in terms of a given reference source and load impedances, usually 50 Ω, as shown in Figure 2.4.

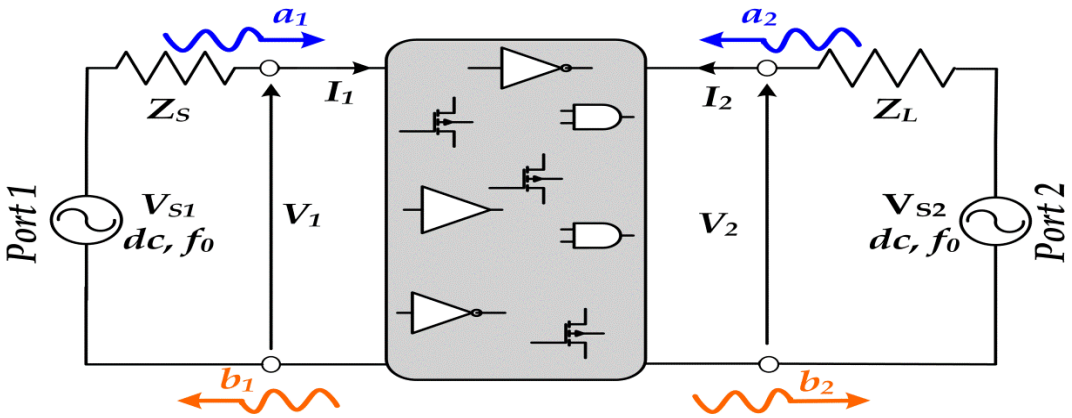

Figure 2. 4. Two port S-parameters characterization for the active device.

The two-port DUM's reflected waves b_1 and b_2 can be related to the incident waves a_1 and a_2 at the input and output ports, respectively, by the S-parameter matrix:

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \equiv \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (2.10)$$

In the large-signal case some of the energy is reflected and transmitted at harmonics of the fundamental frequency. The S-parameters can be extended as a function of the DC bias point and the measurement frequency. We can also introduce

the port indices *i* and *j* and write the two port equations in summation. The S-parameter dependence on bias point and frequency f_0 of the source frequency is expressed as:

$$b_i = \sum_{i=1}^{2} S_{ij}(V_{DC}, f_0) a_j \qquad (2.11)$$

The recorded large-signal and frequency-domain data from the TL simulation, or tailored measurement setup performed with a Vector Network Analyzer (VNA), of the active DUM (e.g. a diode or MOSFET transistors) can be fitted to an equivalent circuit model in terms of resistors, capacitors, inductors, and voltage controlled current sources or voltage controlled voltage sources, etc. In fact, the measured S-parameter data are converted into Y-parameters. Then, the circuit is extracted by fitting the data into the adequate equivalent network structure for the input and output ports. Finally, the overall equivalent circuit can be run in a SPICE based tool, and the S-parameters can be calculated and compared with the measured values. The implementation of this extraction technique is outlined in Figure 2. 5.

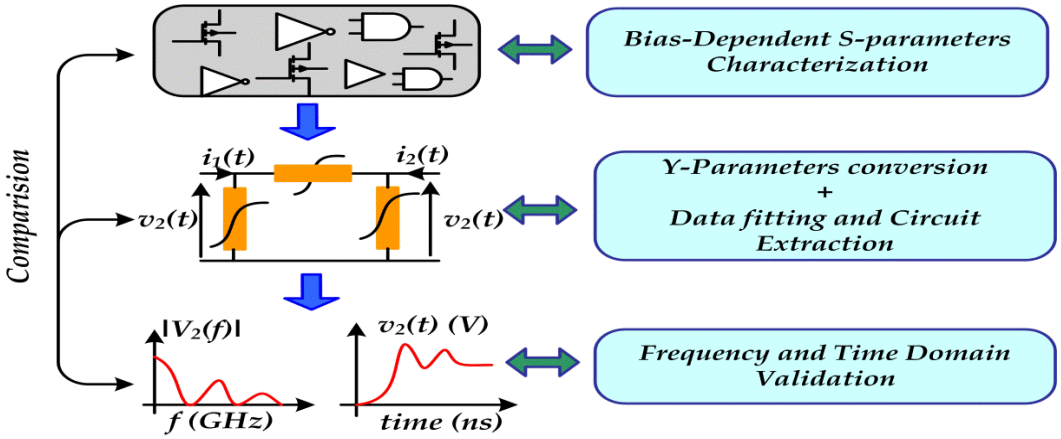

Figure 2. 5. Implementation diagram of the equivalent circuit extraction technique based on frequency domain measurements.

Qualitative and quantitative considerations on the validity of the circuit models extracted can be drawn by simulating the large-signal frequency domain (e.g. Harmonic Balance) to compare the output spectrum and transient response (e.g. SPICE) to compare the time domain signal or the eye-diagrams.

The large-signal equivalent circuit structure that fits the frequency domain data can be proposed based on the physically knowledge considerations. This approach will be described in more details in the next subsection 2.2.3. The equivalent-circuit constructed model will help the semiconductor designer to evaluate the impact of the

device characteristics affecting transmitted signal properties such as amplitude and timing distortion. These measurement-based models are usually implemented as simple look up tables (LUT) which are interpolated for any input condition to perform SI simulation. The constructed model balances the trade-off between accuracy and complexity and avoids the difficulties in model structure selection and/or its parameter estimation.

2.2.3 Equivalent Circuit Based Functions

An alternative approach to describe the model structure is based on the I/O buffers equivalent circuit or the device physical properties. Its topology is usually derived from direct inspection of the driver's physics while the value of its parameters or functions can derived from gathered measurement and system identification theory in order to generate a physically meaningful model. This is particularly evident by investigating the way how active devices are modeled by nonlinear lumped or distributed circuit elements. As a result, these equivalent circuit based driver's behavioral models are the consequence of a conscious combination of black-box behavioral and physical (e.g. white-box) modeling approaches. It can be seen as gray box modeling approach which naturally produces more efficient behavioral model by enhancing the accuracy level and reducing the complexity of the black-box model.

Since, the driver's behavioral models are expected to predict port mismatches and timing and amplitude distortions in SI simulation, they must be able to represent in the time domain the port's voltage and current or incident and reflected wave relationship in frequency domain. Therefore, their topology is of double-input double-output nature. This is a generalization of single-input single-output recursive or direct models of equations (2.3) and (2.4) of the one-port representation of the first example in the previous section 2.2. If the input and the output are components of the incident and reflected wave respectively, then equations (2.3) and (2.4) represent a nonlinear generalization of the linear scattering matrix. If they are stated as voltages and currents, we end up with a nonlinear generalization of the nonlinear admittance or impedance matrix formulation.

To illustrate the principle, the two-port large-signal model of a MOSFET is considered as represented in Figure 2.6. The intrinsic terminal behavior can be specified by the voltages v_1 and v_2 and current i_1 and i_2 at ports 1 and 2, respectively. To be complete, the extrinsic elements, as well as the non quasi-static effects should normally

be added. The simplified scheme consists of the parallel connection of a charge and current source at both port 1 and port 2. They are the device's state-functions that reproduce the two ports electrical behavior and can be extracted based on equivalent circuit or black-box model identification providing large-signal data from time domain or frequency domain measurements [17].

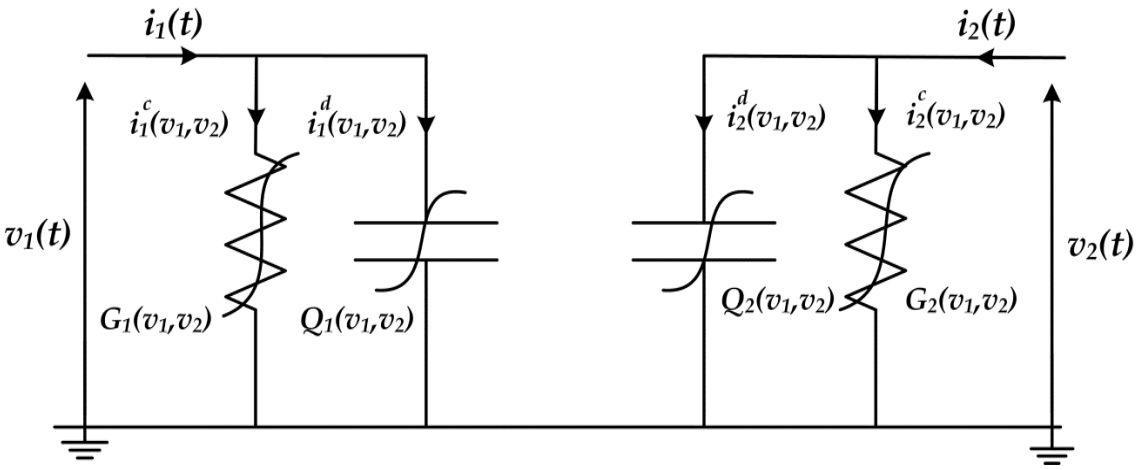

Figure 2. 6. Equivalent circuit nonlinear model with four state functions [16].

The terminal currents can be expressed in the time domain by:

$$\begin{cases} i_1(t) = i_1^c\big(v_1(t), v_2(t)\big) + i_1^d\big(v_1(t), v_2(t)\big) \\ i_2(t) = i_2^c\big(v_1(t), v_2(t)\big) + i_2^d\big(v_1(t), v_2(t)\big) \end{cases} \tag{2.12}$$

and the displacement current at the input and output ports are defined as follows:

$$\begin{cases} i_1^d\big(v_1(t), v_2(t)\big) = \dfrac{dQ_1\big(v_1(t), v_2(t)\big)}{dt} \\ i_2^d\big(v_1(t), v_2(t)\big) = \dfrac{dQ_2\big(v_1(t), v_2(t)\big)}{dt} \end{cases} \tag{2.13}$$

Defining:

$$\begin{cases} C_{11}\big(v_1(t), v_2(t)\big) = \dfrac{\partial Q_1\big(v_1(t), v_2(t)\big)}{\partial v_1} \\ C_{12}\big(v_1(t), v_2(t)\big) = \dfrac{\partial Q_1\big(v_1(t), v_2(t)\big)}{\partial v_2} \\ C_{21}\big(v_1(t), v_2(t)\big) = \dfrac{\partial Q_2\big(v_1(t), v_2(t)\big)}{\partial v_1} \\ C_{22}\big(v_1(t), v_2(t)\big) = \dfrac{\partial Q_2\big(v_1(t), v_2(t)\big)}{\partial v_2} \end{cases} \tag{2.14}$$

(2.12) can be rewritten as:

$$\begin{cases} i_1(t) = i_1^c(v_1, v_2) + C_{11}(v_1, v_2)\dfrac{dv_1(t)}{dt} + C_{12}(v_1, v_2)\dfrac{dv_2(t)}{dt} \\ i_2(t) = i_2^c(v_1, v_2) + C_{21}(v_1, v_2)\dfrac{dv_1(t)}{dt} + C_{22}(v_1, v_2)\dfrac{dv_2(t)}{dt} \end{cases} \quad (2.15)$$

The bi-dimensional nonlinear functions $i_1^c(.)$, $i_2^c(.)$, $C_{11}(.)$, $C_{12}(.)$, $C_{21}(.)$ and $C_{22}(.)$that describe the two port's large-signal model are single-valued. This results into a set of two equations with six unknowns, which can be solved if we have three distinct (independent) measurements by which the instantaneous terminal voltages remain unchanged. This imposes special experimental conditions on the large-signal measurements, such as the presence of a load pull system [18]. The extraction of C_{11} and i_2 have shown a good agreement with reference results, obtained by standard dc and S parameter measurements on the same device [19]. In this equivalent circuit model there is no feedback element that represents the dependency of the input port variables on the output port variables and vice versa. In general, this feedback element is reflected by the recursive model formulation.

2.3 Digital I/O Buffer Behavioral Modeling Approaches

Several approaches for generating driver behavioral models have been proposed over the last decade. The most popular is the IBIS model which is partially based on the large-signal equivalent circuit technique. Nevertheless, with the continued transistor scaling and the increase of the maximum operating frequency, other approaches, which are based on parametric modeling, appeared to complement the IBIS model and proved to be more accurate in SI simulation. In the next subsections, the mathematical derivation of the IBIS two-piece model formulation based on the linear interpolation concept for bi-dimensional function is introduced. Then, the description and generation of IBIS and parametric modeling [11]-[13] are presented as an illustration of the gray-box and black-box approaches for driver's behavioral modeling, respectively. Besides, the advantages and shortcomings of the parametric and IBIS methods are discussed.

2.3.1 Mathematical Formulation

The driver's basic circuit structure consists of a cascade of inverters with increasing current driving capability where the last stage comprises the largest PU and

PD transistors, with power and ground clamping diodes for electrostatic discharge (ESD) protection, as shown in Figure.2.7. Assuming a constant power supply voltage, V_{DD}, the driver consists of a two-port device. However, the two ports have quite distinct characteristics: while the input of the predriver is controlled by the IC core circuitry, whose output is just a data signal of quantized values "1" or "0", the output port drives high output currents i_2 (when compared to the almost negligible, and non-accessible, current i_1 of the input port) due to the large size of the last stage transistors.

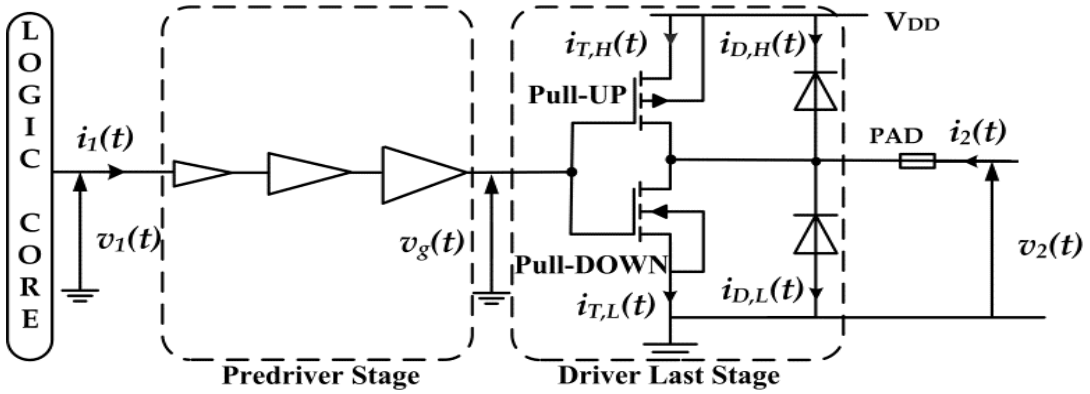

Figure 2.7. Basic structure of the two port I/O buffer and its main electrical variables.

For this reason, the model concentrates only on the output port's nonlinear and dynamic voltage-current relationship, adopting the following event-driven and time domain form:

$$i_2(t,n) = F\left(v_1(n), v_2(t), \frac{dv_2(t)}{dt}, \dots, \frac{di_2(t)}{dt}, \dots\right) \qquad (2.16)$$

where $F(.)$ is a suitable multidimensional nonlinear function. The event *n* defines the up and down transitions that mark the change between the driver's High ,"*H*", and Low, "*L*", logic states. It is controlled by the IC core output variables, $v_1(t)$ and $i_1(t)$. Because of the quantized nature of these controlling variables, and the fact that they are not accessible to the user, and in order to ease the process of modeling and simulation, we will use an interpolation technique [24] for approximating the nonlinear multi-dimensional function $F(.)$, which leads to the following model structure:

$$i_2(t) = w_L(t).\, i_L\left(v_2(t), \frac{d}{dt}\right) + w_H(t).\; i_H\left(v_2(t), \frac{d}{dt}\right) \qquad (2.17)$$

In the above expression, d/dt represents the dependency on the successive derivatives of the output currents, $i_L(t)$ or $i_H(t)$, and of the output voltage $v_2(t)$. The local models

$i_L(.)$ and $i_H(.)$ are appropriate multi-input single-output nonlinear functions. They model the nonlinear dynamic admittance of the PU and PD devices of the driver's last stage, which comprise the transistors' current, i_T, along with the clamping diodes' current i_D when the input signal, $v_1(t)$, is kept at its low and high logic levels, respectively, i.e. $i_H(t) = i_{T,H}(t) + i_{D,H}(t)$. The output current of the local models are scaled using the stepwise weighting functions $w_L(t)$ and $w_H(t)$ that capture the timing behavior of the variable $v_g(t)$, as the IC core sends the bit patterns '01' and '10' (i.e. the driver is changing from the *L* to *H* states for the up transition and from the *H* to *L* states for the down transition). Assuming that the interpolation is linear, so that the switching between the PU and PD devices is ideal and symmetric, the timing functions are complementary:

$$\begin{cases} w_L(t) = \dfrac{v_g(t) - v_{g,L}}{v_{g,H} - v_{g,L}} = \dfrac{v_g(t)}{V_{DD}} \\ c \\ w_H(t) = 1 - w_L(t) \end{cases} \tag{2.18}$$

The driver last's stage can be considered as a unilateral device such that the effect of v_2 variation, due to the loading PCB traces impedance mismatch, on v_g is negligible. The last stage buffer's current-voltage relationship can be approximated by model (2.19) relating $i_2(t)$ and $v_g(t)$ and their successive derivative based on the observed I/O signals from transient simulation, represented through:

$$i_2(t) = H\left(v_g(t), \frac{dv_g(t)}{dt}, \frac{d^2v_g(t)}{dt^2}, \dots, \frac{di_2(t)}{dt}, \frac{d^2i_2(t)}{dt^2}, \dots\right) \tag{2.19}$$

where $H(.)$ is the large-signal current source function that describes the voltage transfer characteristics (VTC) of the driver last stage while it drives a load. The interpolation (2.17) and the assumption (2.19) allow us to minimize the dependency of model structure from the immeasurable variable v_g. In fact, we can retrieve the timing behaviour of the gate voltage $v_g(t)$, by recording the output voltage $v_2(t)$ for a 50Ω environment at the driver's output port and determine the unknown timing coefficient in (2.17). Besides, in the normal IC activity the steady state of the digital input signals v_1 *H* or *L* should be reached by the other voltage variable in the predriver stage, according to the polarity of the buffer (inverting/not inverting). Thus, the functions $w_L(.)$, $w_H(.)$ and $i_L(.)$, $i_H(.)$ can be extracted based on the observation of accessible output signals.

Conceptually, the two previous driver's behavioral modeling approaches [11]-[15] share the same model structure (2.17) but only differ in the mathematical formulation and the identification process for modeling the local models, $i_L(.)$ and $i_H(.)$. Firstly, IBIS separately extracts the nonlinear static function which is implemented as LUT and then the dynamic is assumed to be linear and modeled as lumped capacitor. However, the last stage large-signal behaviors were simultaneously extracted in the parametric approach using dynamic I/O data that was fitted by ANNs or spline functions [11], [12].

2.3.2 IBIS Behavioral Modeling

The IBIS model is a set of specifications describing the I/O buffers model extraction and formatting data based on voltage timing (V-t) table for the pre-driver's stage and a simplified equivalent circuits for the driver's last stage [25]. The IBIS output buffer's description is generally divided into four elements as shown in Figure 2.8 [18]. These are the PU and PD transistors, power clamp diode, ground clamp diode with current-voltage (I-V) DC static table information. Then, to better capture the interpolation between local models ($i_L(.)$ and $i_H(.)$), IBIS version 2.1 provides the transient behavior at up and down transition by the means V-t data. Also IBIS provides the lumped RLC model for package interconnects and the pad capacitor. These elements are represented through files.

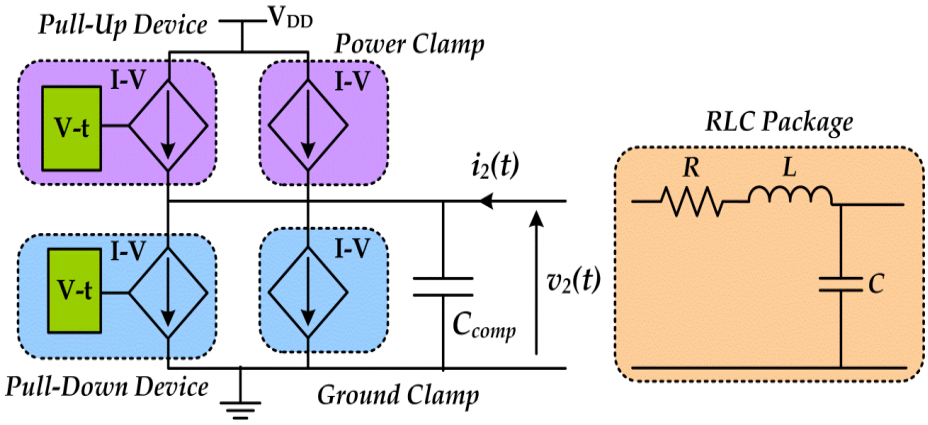

Figure 2. 8. Key portions of the active intrinsic parts of IBIS model's elements [25].

In order to generate the four I-V curves that describe the IBIS driver's last stage, we slowly increase the voltage and measure the current and voltage with an ammeter and voltmeter connected at the driver's output port as shown in Figure 2.9. This results in the PU, PD, ground clamp and power clamp curves. The PD curve is a result of subtracting the ground clamp I-V curve from the logic-low I-V curve, since this is where the PD transistor is active as shown in Figure 2.10 (a). Similarly, the PU curve is

generated by subtracting the power clamp I-V curve from the logic-high I/V curve, since this is where the PU transistor is active as shown in Figure 2.10 (b). The full range of the measurement is from $-V_{DD}$ to $2V_{DD}$ which is the possible range of voltages that the output could see in a transmission line environment.

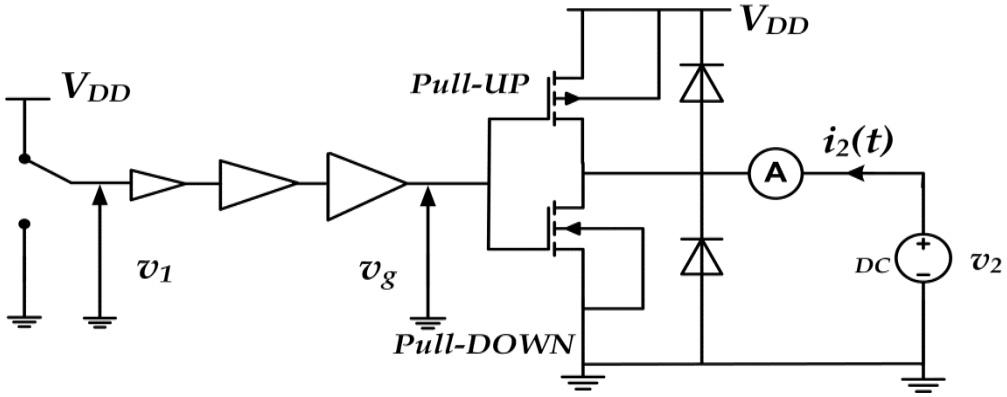

Figure 2. 9. Simulation setup for the generation the four I-V curves for IBIS model. The diodes start to conduct as $\boldsymbol{v_2}$ exceeds the supply voltage bounds by an overvoltage ($\Delta = \mathbf{0.5V}$).

The ground clamp curve is derived from the ground relative data gathered while the driver is in the high impedance state and evidences the region where the ground clamp diode is active. The range is from -V_{DD} to V_{DD}. The power clamp curve is derived from the V_{DD} relative data gathered while the buffer is in a high impedance state and shows the region where the power clamp diode is active. This measurement ranges from V_{DD} to $2V_{DD}$. The PU and power clamp curves are V_{DD} relative, meaning that the voltage values are referenced to the V_{DD} pin since the currents depends on the voltage between the output and V_{DD} pin and not the voltage between the output and ground pins.

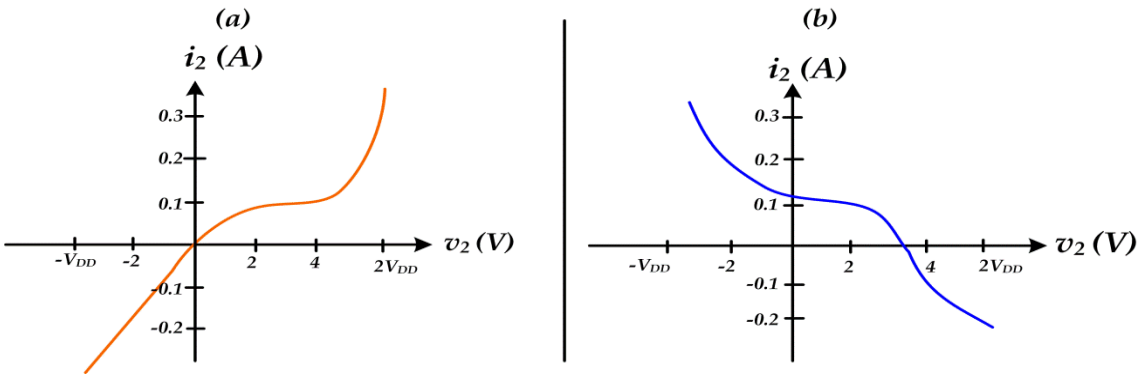

Figure 2. 10. IBIS output buffer static I-V characteristics: (a) PD I-V curve, (b) PU I-V curve.

An IBIS model also provides rising and falling timing voltage (V-t) waveforms that capture the transitions from *L* to *H* and from *H* to *L*. These curves can be recorded from SPICE simulations when the buffer output is terminated with 50Ω and dc voltage source, V_{DC}, for the up and down step excitation at buffer input as shown in Figure 2.11.

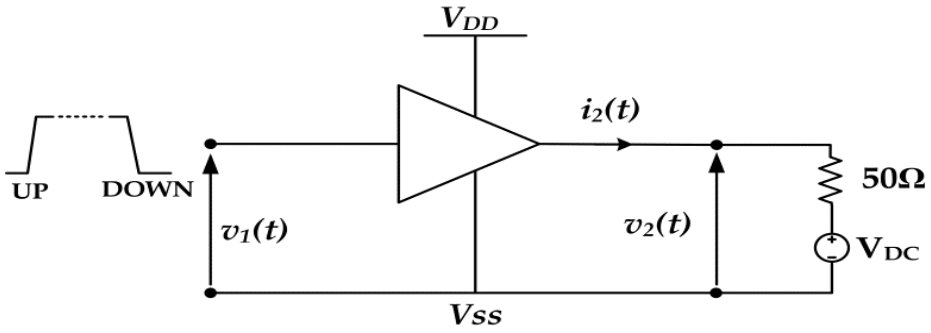

Figure 2. 11. Simulation setup for the transient identification signals $\{i_2(t), v_2(t)\}$ when V_{DC} is kept at the high or the low logic state for each up and down transitions at the input $v_1(t)$.

The dc IV curves and the timing data are used to calculate the step input describing functions (StIDFs), where the effect of package parasitic are ignored. The StIDFs are computed using linear inversion.

$$\begin{bmatrix} w_H(t) \\ w_L(t) \end{bmatrix} = \begin{bmatrix} i_{L,V_{ss}}(v_2) & i_{H,V_{ss}}(v_2) \\ i_{L,V_{DD}}(v_2) & i_{H,V_{DD}}(v_2) \end{bmatrix}^{-1} \begin{bmatrix} i_{2,V_{ss}}(t) \\ i_{2,V_{DD}}(t) \end{bmatrix} \qquad (2.20)$$

The model (2.17) can be adapted to a one waveform condition by considering assumption (2.18). In order to maximize the correlation of the complete behavioral model, IBIS adds the linear capacitive effect to model the additional output dynamic of the driver's last stage [26]. In addition, the predriver's nonlinear dynamics are encapsulated in the timing behavior of the four extracted four tables V-t.

The two-piece IBIS model structure is mathematically derived from linear interpolation of bi-dimensional functions. Data provided by IBIS, in accordance to the assumed equivalent circuit, must be translated into an executable model in order to be used in circuit simulation environments. The IBIS driver's model is popular and widely used as it is commercially available, has large sets of libraries, and run faster than actual driver's TL models.

However, IBIS models have inherent limitations. Most importantly, the IBIS model structure is derived under some assumptions, thus, it can work only for limited data rate input range. In fact, the hard algorithm implementation of the StIDFs should provide the synchronization and concatenation of the elementary timing functions to reproduce the desired bit sequence. The model's formulation, extraction, and implementations issues in IBIS generation algorithm limit its use under high data rate excitations. This is called overclocking [27] and it will be discussed in more details in the next chapter and the respective enhancement of IBIS will be presented. Besides, the physical effects to be considered are decided *a priori* when the simplified equivalent

circuit is defined. For instance, IBIS model fail to accurately capture the driver's nonlinear memory effects as it relies on static characteristics and lumped linear capacitance C_{omp}[14].

2.3.3 Black-Box Parametric Modeling

A second possible alternative to driver's behavioral modeling is via parametric curve fitting techniques as illustrated in Figure 2.12.

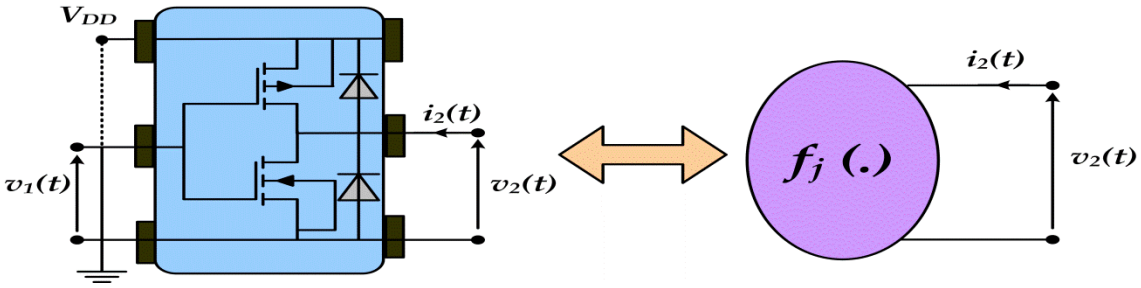

Figure 2. 12. A functional form reproducing an observed electrical behavior of the device.

The parametric approaches [11]-[13] confirm the importance of using nonlinear dynamic local models to develop more effective behavioral model [6], [28]. They use ANNs to mimic the nonlinear dynamic I/O data collected by exciting the output port with a piecewise linear (PWL) voltage with various amplitudes and rise/fall times, along with superimposed white noise [29]-[32]. Thus, the model adopts a discrete-time recursive structure of the form while the input is kept at *H* and *L* logic states:

$$\begin{cases} i_j(t) = f_j\left(\Theta_j, x_j(k)\right) \;\; ; \; j = L, H \\ x_j(k) = \left[i_j(k-1) \ldots, i_j(k-r), v_2(k) \ldots, v_2(k-r)\right]^T \end{cases} \quad (2.21)$$

The regressor vector x_j not only collects the instantaneous input-output signals, but also their delayed versions. Θ_j is the vector of unknown parameters, and $f_j(.)$ is a generic nonlinear scalar function modeled by recurrent ANNs with various activation functions such as radial basis function (RBF) [29], sigmoid basis function (SBF) [30], polynomial functions as the spline function with finite time difference (SFWFTD) [31], or rational basis functions [15]. The advantage of this approach relies in the flexibility of ANNs against the rigid representation adopted by IBIS [25].

In principle, the knowledge of the internal structure is not required and the modeling information is completely contained in the device external responses. Thus the modeled device is considered as a black-box and does not disclose the IP. The

nonlinear dynamic function $f_j(.)$ interpolates the actual performance of the circuit from the observed circuit's behavior which can be obtained from measurements or simulation. Moreover, the basis functions used in the parametric models should be first general, so it has the capability to approximate complex nonlinear behavior. Besides, it is preferable that the set of functions composing $f_j(.)$ are orthogonal so the model's parameters are extracted independently.

In order to obtain the optimum model which uses less neuron and time delays to accurately approximate the function $f_j(.)$, many training data sets have to be tried. The design of the excitation signals is a matter of repeated estimation experiments. Figure 2.13 shows the flow chart of the general procedure involved in driver's modeling.

The described parametric approaches [11]-[13] follow back-box identification by treating the number of state variables as an unknown. However, the physical knowledge via the equivalent circuit topology can be used to simplify, prune and reduce the order of the parametric model structure. As an example, in the case of a one-port nonlinear resistor, (2.4) becomes $i_1(t) = f_{D1}\,[v_1(t)]$ and in the case of a nonlinear capacitor $i_1(t) = f_{D1}\left[v_1(t), \frac{dv_1(t)}{dt}\right]$. As the derivative is related to the concept of a time delay and by considering (2.21), the terminal currents can be expressed as a function of the terminal voltages and their first derivatives.

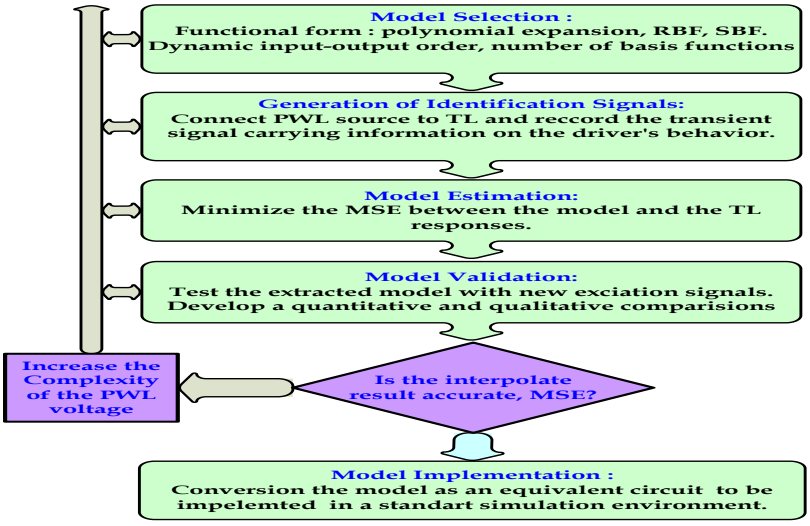

Figure 2. 13. Procedure for modeling the driver's nonlinear dynamic function $f_j(.)$.

This can be generalized for an electrical two-port by equations of the discrete form:

$$\begin{cases} i_1(k) = f_{D1}\,[v_1(k), v_1(k-1), v_2(k\,), v_2(k-1)] \\ i_2(k) = f_{D2}\,[v_1(k), v_1(k-1), v_2(k\,), v_2(k-1)] \end{cases} \tag{2.22}$$

Then, the modeling problem is simplified by the equivalent circuit knowledge (2.22) and it is transformed to find the functional relationships $f_{D1}(.)$ and $f_{D2}(.)$ by fitting the measured time domain terminal currents to the already determined independent and state variables.

In the general case, the model complexity can be reduced by determining the optimum sets of independent variables and states to predict accurately the device dynamics from the collected time series data which are representative of the device behavior. The initial set of independent variables from which the model is built consists of the measured terminal voltages and currents and their time derivative. In principle, one could use all the possible independent variables in an arbitrary fixed order, but this would result in models that are needlessly complex. There are more rigorous methods for selecting a subset of independent variables from which to construct the model. In practical terms the multivariable function that maps the input subset of independent variables to the output response is a single-valued function [8]. The technique for finding this subset is the so-called 'false nearest neighbors' method of information theory [33].

Once the dynamic order is selected of $f_{D1}(.)$ and $f_{D2}(.)$, the modeling task is essentially a function approximation problem. After the parameters extraction, the model has to be synthesized as an equivalent circuit to be included in the simulators by converting the estimated discrete-time domain model into a continuous-time domain state-space realization [29]. Such an approximation is described below for the simple case

$$i_j(t) = f_j\left(\Theta_j, \left[i_j(k-1), v_2(k), v_2(k-1)\right]^T\right) \tag{2.23}$$

This relation can be written as a first order finite differences in the following state space realization, with the auxiliary variables $z_1(k) = i_j(k-1)$ and $z_2(k) = v_2(k-1)$.

$$\begin{cases} z_1(k) - z_1(k-1) = f_j\left(\Theta_j, x_j(k-1)\right) - z_1(k-1) \\ z_2(k) - z_2(k-1) = v_2(k-1) - z_2(k-1) \\ i_j(t) = f_j\left(\Theta_j, x_j(k)\right) \end{cases} \tag{2.24}$$

where $x(k) = [z_1(k), v_2(k), z_2(k)]^T$. Using (2.2), the model's discrete-time representation is restored to its continuous-time form:

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} z_1(t) \\ z_2(t) \end{bmatrix} = \dfrac{1}{T}\begin{bmatrix} f_j\left(\Theta_j, x_j(t)\right) - z_1(t) \\ v_2(t) - z_2(t) \end{bmatrix} \\ i_j(t) = f_j\left(\Theta_j, x_j(t)\right) \end{cases} \tag{2.25}$$

This state-space equation can be implemented as a voltage-controlled current, and charge sources or current controlled flux source in any CAD tools enabling the time derivatives in each time step of terminal voltages and currents in fitting functions to be evaluated.

2.4 Summary

Various methodologies can be followed to select the behavioral model's structure and different techniques can be used to extract its functions and parameters. Furthermore, the knowledge of the interaction between the design of experimental setups, I/O data analysis, and adequate model formulation and extraction algorithm should be acquired and considered in order to generate an efficient behavioral model.

The driver's behavioral models developed based on parametric curve fitting technique are purely black-box. They use various basis functions to capture the nonlinear dynamic driver's behavior. Their parameters can be extracted by means of linear or nonlinear least square approaches. Generally, the resulted model is complex because there are a large number of extracted parameters to capture the device behavior in a wide range of specifications. In order to obtain an efficient model, the followed approach is focused on the optimization of model extraction in an environment close to the actual DUM working conditions. This optimization follows the functional approximations based on usual input signal features, physical device characteristics, identification procedure, and macromodel implementation. For instance, the functional model of the time domain digital I/O buffer models should be approximated and optimized to achieve the practical trade-off between accuracy and the simulation computational cost.

The further enhancements to the large-signal equivalent circuit IBIS model by nonlinear parametric modeling of the one-port output stage introduce a more complexity and stability issues. Hence, a new methodology should be investigated to merge both model features in order to optimize the extension of the parametric modeling approaches and included it into the IBIS model.

CHAPTER III:

Behavioral Modeling Optimization and Enhancement

3.1 Introduction

Based on the theoretical framework and the state of the art of driver's behavioral modeling, the developed work in this PhD thesis is dedicated to optimize both the IBIS and the nonlinear parametric modeling approaches in the extraction and implementation steps. Concerning the IBIS approach, a current-charge (I-Q) tabular extension is developed to improve model accuracy and computational efficiency with time and frequency domain extraction techniques. Moreover, a reduced-order parametric model is presented in order to ease the model's extraction procedure and to reduce the simulation's complexities and to avoid the convergence problems of the previous recursive parametric approaches based on purely black-box ANNs. Finally, a novel two port analog behavioral model is conceived and extracted in order to enhance the IBIS modeling approach to cope with new trend in digital I/O buffers design characterized by higher transmission data rate (leading to the use of I/O buffers under overclocking conditions).

This chapter is organized as follows. In the first section, a reduced-order parameter I-Q behavioral model is conceived by merging the driver's equivalent circuit knowledge and constitution allied to nonlinear curve fitting techniques. This is achieved by incorporating the devices' voltage-dependent (i.e. nonlinear) output capacitance – which is missing in the IBIS model – allowing the model to be extracted from a simple a single-step large signal characterization that is very close to the digital drivers' actual working conditions. The resulted stable model generates a much better tradeoff between model complexity, easiness of parameters' extraction, accuracy of prediction and model implementation and it is capable of significantly improving simulation speed and accuracy of prediction.

In the second section, an efficient and accurate table-based behavioral model extraction is presented for the I-Q model formulation. The nonlinear current-voltage (I-V) and charge-voltage (Q-V) functions describing the grey-box model structure are extracted via least-squares methods using identification signals recorded from large signal transient simulation. The resulting continuous time domain model is easily

implemented as lookup table and leads to an increase in modeling accuracy, and a decrease in computation time.

In the third section, a frequency domain extraction of the I-Q model is described. The model extraction procedure is based on the device's measured bias-dependent frequency domain small-signal characteristics. Then, the best fit (in least-squares sense) of the driver's output large signal admittance model over a frequency range is constructed.

In the fourth section is presented the first behavioral model solution to the computationally efficient simulation of digital I/O buffers under overclocking operation. The physically meaningful two-port approach relies on predicting the timing signals that control the activation of the driver's output stage. The identified nonlinear dynamic model operators of the input port substitute the concatenated fixed StIDFs of the previous table-based IBIS, and of other parametric approaches. The implemented gray-box model produces more accurate results than the previous methodologies when assessing the SI performance of high-speed digital links in normal and overclocking conditions under various input excitations. However, it still preserves the computational efficiency recognized for its behavioral model predecessors.

It is worth noting that the developed behavioral models, during this PhD, are validated and their performance and numerical results are qualitatively and quantitatively evaluated in a typical SI simulation scenario involving commercial driver.

3.2 Reduced-Order Parametric Extraction

As described in the previous chapters, with the continued transistor scaling and the increase of the maximum operating frequency, the parametric approaches [11]-[13] appeared to complement the IBIS model and proved to be more accurate in SI simulation. However, these models do not have a physical circuit-basis and use mathematical curve fitting techniques, such as recurrent neural networks [28]-[31], to construct a behavioral model only for the driver's last stage, as seen in Figure 2.7.

Unfortunately, as they are pure black-box models, using general behavioral model structures, they require involved parameter extraction procedures [11]-[13], or many small-signal and DC measurements that are far from the driver's real operating conditions [15]. This results in inconsistency between measured and modeled driver's nonlinear dynamics behavior.

The approaches [11]-[15] differ in the model formulation and identification process for capturing the behavior of the PU and PD devices. For example, the IBIS model assumes static local models for $i_L(.)$ and $i_H(.)$, which are thus extracted by a dc voltage sweep. Unfortunately, by doing that, the IBIS neglects any charge accumulation effects in the output transistors' channels. Therefore, it has to rely on a capacitance lumped with the pad capacitance and the package parasitic, which are modeled as a RLC π-network [6], [25]. The drawback of this approach is that it can only represent linear charge accumulation, while it can be nonlinear. Although the enhancement provided by the black-box parametric modeling based on the general nonlinear modeling capability of ANNs and the polynomial expansion, there remain several issues to be addressed. Firstly, the recursive structure suffers from potential instability (i.e. lack of convergence to the desired solution) not only during extraction, using nonlinear optimization algorithms [32], but also in simulation as happens in the case of the SFWFTD or the rational basis functions, because it results in unreliable model outside the operating range of the training data [21]. Secondly, the obtained model has to be synthesized as an equivalent circuit to be included in standard circuit simulators by converting the estimated discrete-time domain model into a continuous-time domain state-space realization [29]. Thirdly, the resulted model is a network with a large set of parameter impossible to physically interpret because the information is opaquely stored.

In order to address the previous limitations, but still avoiding highly complex model structures, a parametric current-charge, I-Q, model, which is supported by the *a priori* knowledge of the general output buffer physical operation is herein proposed. In addition, an appropriate identification signal is designed to excite the nonlinear dynamic behavior of interest and thus ease the extraction of the I-Q model's parameters.

3.2.1 The Current-Charge (I-Q) Description

This subsection describes the analysis followed in the derivation of the current-charge model and then explains the parametric procedure proposed for its extraction. Such a model representation reveals the improvement introduced by the previous black-box parametric approaches, [28]-[32], which mostly served to capture the voltage-dependent output capacitance added to the memoryless conductance, but using a much more complex and recursive structure.

At a constant input voltage (v_1), the output one-port circuit comprises a parallel connection of a MOSFET transistor and a diode (see Figure.2.7). This physical

observation encourages the construction of a model structure that comprises a parallel combination of a nonlinear voltage-dependent conductance and capacitance for each PU and PD devices [34]. In fact, the local models $i_L(.)$ and $i_H(.)$ capture the nonlinear dynamic output admittance of the PU and PD devices of the driver's last stage, respectively. Therefore, the adopted model is shown in Figure 3.1.

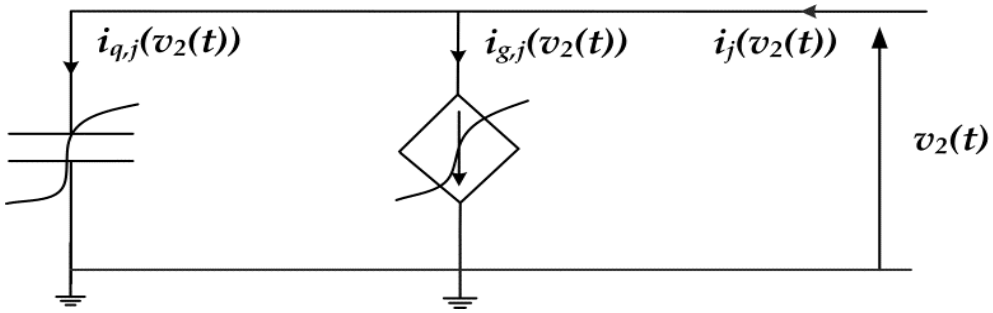

Figure 3. 1. One-port representation of the PU or PD devices of the driver's last stage.

The description of the I-Q elements can be defined in the continuous-time domain by:

$$i_j(t) = i_{gj}(t) + i_{qj}(t) = i_{gj}\big(v_2(t)\big) + \frac{dQ_j\big(v_2(t)\big)}{dt} \; ; \; j = L, H \qquad (3.1)$$

The voltage-controlled functions $i_g(v_2)$ and $Q(v_2)$ represent the current and the accumulated charge, respectively, of the MOSFET's channel plus the diode's junction. These constitutive functions share the same form as the general expression (3.1), but are much simpler since they only depend on the state variable $v_2(t)$ and its first order derivative (therefore making the model non-recursive and of first order dynamics). The model suggested for the I/O buffer PU and PD last stages can also be expressed as a voltage-dependent conductance plus a voltage-dependent capacitance [34]:

$$i_j(t) = i_{gj}\big(v_2(t)\big) + C_j\big(v_2(t)\big)\frac{dv_2(t)}{dt}; \quad j = L, H \qquad (3.2)$$

where the functions $i_{gj}(.)$ and $C_j(.)$ are nonlinear static functions. This model structure describes the nonlinear dynamic effect of the $i_T - v_2$ characteristic of the large last NMOS and PMOS transistors as well as the $i_D - v_2$ characteristic of the ESD diodes. Indeed, the form of (3.2) shows that, with the proposed I-Q model, the complex I/O buffer nonlinear dynamics can be accurately modelled by simply identifying two static nonlinearities.

In the I-Q model, the output current relationship with the output voltage is expressed as a summation of a static nonlinearity plus linear dynamics. This separation

in the model format is supported by both measurements and the physical reasoning of the driver electrical structure of a general driver circuit. This proposed structure merges the strengths of both the IBIS and parametric approaches. Indeed, it not only extends the IBIS by accurately capturing the device's constitution (mainly the voltage-dependent output capacitor, (C-V)), as it also takes profit from the flexibility offered by customised behavioural models – e.g. implemented as neural networks – that represent the device's intrinsic nonlinear dynamics.

3.2.2 Parametric Extraction of the I-Q Model

The first step in the driver's model identification is to extract the $i_L(.)$ and $i_H(.)$ functions. For this, the excitation voltage waveform $v_2(t)$should be carefully designed in order to reflect the nonlinear dynamic behavior of the one-port upper and lower devices and to ease the identification process. In fact, the excitation has to cover all the amplitude levels and frequency range found in the driver's operation. In particular, the exponential swept-sine (ESS) excitation plus a dc component was proven sufficient to expose the essential PU and PD non-linearity and dynamics. The ESS signal reaches higher frequency within a shorter time avoiding large data storage as it the case of linear frequency sweep. This signal is a sine wave with an instantaneous frequency that is exponentially increases from f_1 to f_2 over *T* seconds [35]:

$$\begin{cases} v_2(t) = a_0 + a_1.sin\left(2\pi f_1 L.\left(e^{-\frac{t}{L}} - 1\right)\right) \\ L = T/Ln(f_1/f_2) \end{cases} \tag{3.3}$$

where f_1 is the initial frequency at *t=0*, f_2 is the ending frequency at *t = T*, and *L* is the rate of exponential increase in frequency. For satisfactory measurements and efficient model extraction, the sweep parameters f_1, f_2, and *T* must be thoughtfully selected considering the following aspects. The frequencies f_1 and f_2 must be chosen such that the interesting behavior of the DUM is in the frequency band $[f_1, f_2]$. The time duration *T* should be as large as possible to separate the contributions of the conduction and the displacement currents and to avoid long estimation times. The frequency f_1 is chosen as low as possible to excite only the conduction current, however, the frequency f_2 of the excitation is chosen close to the I/O buffer's maximum frequency of operation (e.g $f_2 = 0.35/t_{r,f}$, where $t_{r,f}$ is the rise/fall time of the bit transmitted through the driver) so that it excites both the conduction and displacement currents. The excitation voltage

amplitude is determined by $a_0 = V_{DD}/2$ and a_1, and must be within the range of $[-\Delta, V_{DD} + \Delta]$. This covers the voltage excursion necessary to fully excite the driver up to the conduction of the clamping diodes, i.e., by reaching the overvoltage margin Δ.

The simulation setup required to collect the signals for the identification of local models is presented in Figure 3.2. The voltage $v_2(t)$ and the corresponding current response $i_j(t)$ are sampled avoiding any aliasing effect during the transient analysis at the driver's pad.

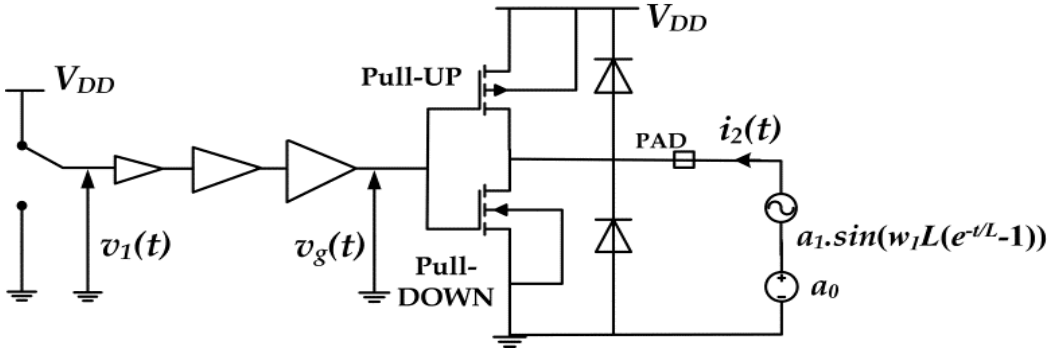

Figure 3. 2.Simulation setup for generating the driver's identification signals for $i_L(.)$ and $i_H(.)$.

Both local models share the same model structure. However, the parameters that describe the nonlinearity of conduction and displacement currents differ because the physical constitutions of the PU and PD devices also differs. This model structure is implemented as a customized neural network using Adaptive Neuro-Fuzzy Inference Systems (ANFIS) using MATLAB [36]. The ANFIS is known as a universal function approximate that enables the model designer to select mixed activation functions (sigmoid, Gaussian, linear, etc.) suited for the device's nonlinearity and dynamics for the construction of a simple model with the smallest possible number of parameters [36], [37]. The model's architecture is shown in Figure 3.3.

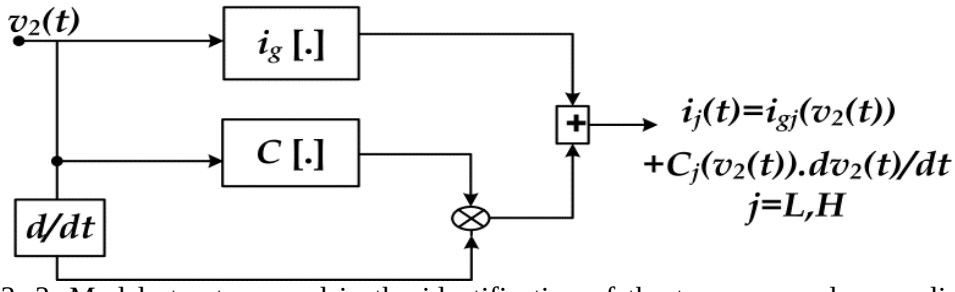

Figure 3. 3. Model structure used in the identification of the two memoryless nonlinearities $i_{gj}(.)$ and $C_j(.)$ for each local model.

The extraction of the basis function parameters is facilitated by computing the gradient vector through the learning process. Several nonlinear optimization routines can be applied to the gradient vector in order to adjust the parameters by minimizing the

MSE cost function (2.9) between the reference and model outputs. The parameters Θ are now identified using a hybrid algorithm. It applies a combination of the least-squares method and the backpropagation gradient descent (i.e. Levenberg-Marquardt) algorithm [38], [39].

This developed extraction approach requires only one simulation setup to properly excite the nonlinear dynamic behavior of the PU and PD last stage devices by means of a biased large ESS. Then, the acquired input-output transient data is used to extract simultaneously the memoryless nonlinearities, I-V and C-V, that complementarily describe the local models $i_L(.)$ and $i_H(.)$ by minimizing the MSE.

3.2.3 Step Input Describing Function Identification

Once the I-Q model parameters are identified for $i_L(.)$ and $i_H(.)$ functions, the device input-output timing behaviors are captured by identifying the StIDFs $w_L(t)$ and $w_H(t)$, corresponding to the positive and negative transitions (i.e. rising and falling edges) of the input voltage, for different load impedances, as shown in Figure 2. 11. The resistive load is fixed at 50Ω, while the dc voltage source is connected, for each step input, to the power supply V_{DD} or to the ground V_{SS}. The transient sequences $\{i_{2,V_{ss}}(t), v_{2,V_{ss}}(t)\}$ and $\{i_{2,V_{DD}}(t), v_{2,V_{DD}}(t)\}$ are recorded at the driver output pad for both transitions, when the voltage V_{DC} is connected to V_{SS} or V_{DD}, respectively. Then, the identified complete I-Q models of (3.2), and not only of its dc I-V characteristics [15], were subjected to the measured voltage $v_{2,V_{ss}}(t)$ and $v_{2,V_{DD}}(t)$ for both transitions. Therefore, the simulated currents for such excitation are $i_{L,V_{ss}}(t)$ and $i_{L,V_{DD}}(t)$ for the PD last stage, and $i_{H,V_{ss}}(t)$ and $i_{H,V_{DD}}(t)$ for the PU last stage. These measurements and simulations allow the construction of the following linear equation system:

$$\begin{bmatrix} w_L(t) \\ w_H(t) \end{bmatrix} = \begin{bmatrix} i_{L,V_{ss}}\left(v_{2,V_{ss}}(t), d/dt\right) & i_{H,V_{ss}}\left(v_{2,V_{ss}}(t), d/dt\right) \\ i_{L,V_{DD}}\left(v_{2,V_{DD}}(t), d/dt\right) & i_{H,V_{DD}}\left(v_{2,V_{DD}}(t), d/dt\right) \end{bmatrix}^{-1} \cdot \begin{bmatrix} i_{2,V_{ss}}(t) \\ i_{2,V_{DD}}(t) \end{bmatrix} \quad (3.4)$$

The StIDFs give a valuable transient information about the driver's nonlinear dynamics (e.g. asymmetric gain, overshoot, rise/fall time, settling time and ringing) by capturing the potentially different dynamic distortion at the rising and falling edges. In fact, they scale the output current produced by PU and PD devices during the state transition to transmit the bit pattern '010'. Their combination with the nonlinear local models results in a correct model that accurately describes the I/O buffer behavior in the

transient analysis for trapezoidal input signal spaced enough in time to allow the previous transition to reach the steady state.

3.2.4 Model Validation Results

The performance of the proposed modeling approach is demonstrated on a commercial high-speed BT8P 3B CMOS driver from Austria Microsystems. This device operates at 270 Mbps (maximum switching frequency specified by the vendor). . It is a 0.35µm technology from c35 IOLIB cells (power supply: $V_{ss} = 0\ V; V_{DD} = 3.3\ V$). Firstly, the extraction procedure with the ESS excitation is presented and the performance of the I-Q structure applied to the PD devices, $i_L(.)$, to capture the nonlinear dynamic current-voltage relation-ship is assessed. Then, the global I-Q model performance is compared to the IBIS and TL models.

For the considered illustrative device, the input-output data needed for the development of the I-Q model are recorded from the transient response of the device's TL description by means of Spectre-SPICE simulations, while the input is kept at the low logic level. The adequate values for the parameters in (3.3) are $a_0 = 1.65\ V$ and $a_1 = 2.15\ V$ for $\Delta = 0.5\ V$, f_1=10 MHz and f_2 = 800 MHz and T = 20 ns.

The extraction performance of the PD driver parametric model (2.3) is compared considering the piece-wise linear (PWL) signal normally used to extract parametric models (e.g. in [29]) and the now proposed ESS excitation signal. An illustrative view of the time domain waveform of these excitations with the above parameters is shown in Figure 3.4's left side. Since the frequency content of the excitation is also very important, the spectrum magnitudes of these time domain signals are generated via Fourier transform. In order to determine which frequencies are present or missing in these excitation signals, Figure 3. 4's right side compares these amplitude spectra with the one of the pad voltage, $v_2(t)$, recorded in usual driver's working conditions.

From Figure 3.4.c, it is worth noting that the ESS signal is richer in frequency than the PWL signal and can thus better mimic the signals encountered in mismatch loading conditions, something crucial for accurate model prediction. Furthermore, Figure 3.5 shows that the ESS gives more consistent results, not only in observing the adequate behavior of the last stage upper and lower device's dynamics, but also in providing a better convergence speed and approximation quality (i.e. MSE) after fewer epochs than the PWL excitation. In fact, the ESS reduces the identification signals data

file and enables the separation of the nonlinear static behavior effect due to the conduction current and the linear dynamic effect caused by the displacement current.

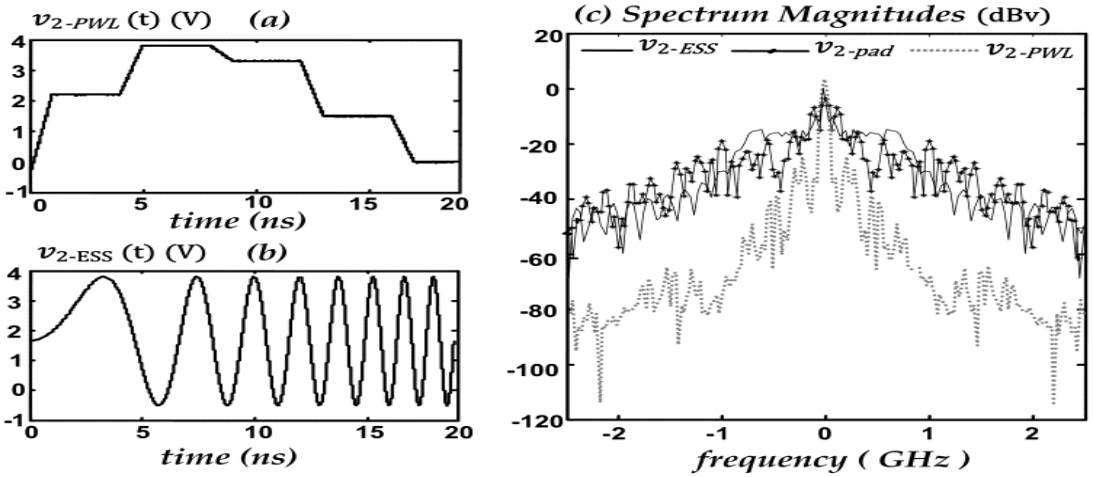

Figure 3. 4. Time domain waveforms: (a) PWL signal, (b) ESS signal.(c) Spectrum magnitudes in dBv of the ESS, the PWL, and the pad voltage in mismatch loading condition.

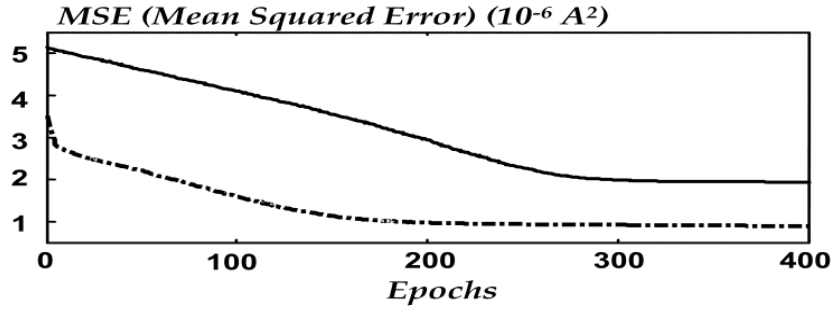

Figure 3. 5. Comparison between the MSE convergences when the model of the driver's PD last stage is trained with PWL(solide line) and ESS (dashed line).

An example of the trained surface of the PD device, which relates the output current with the excitation voltage and its first derivative, is shown in Figure 3.6

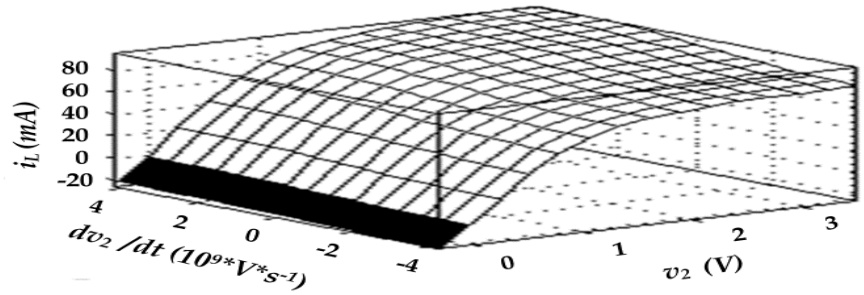

Figure 3. 6. Single-valued nonlinear surface relates the output current to the output voltage and its first derivative (state variable).

This single-valued nonlinear surface confirms that the first derivative of the output voltage was enough to fairly embed the input-output space dynamics with a good accuracy. The I-Q model uses three SBFs to model the I-V and C-V relationships as shown in Figure 3. 7.

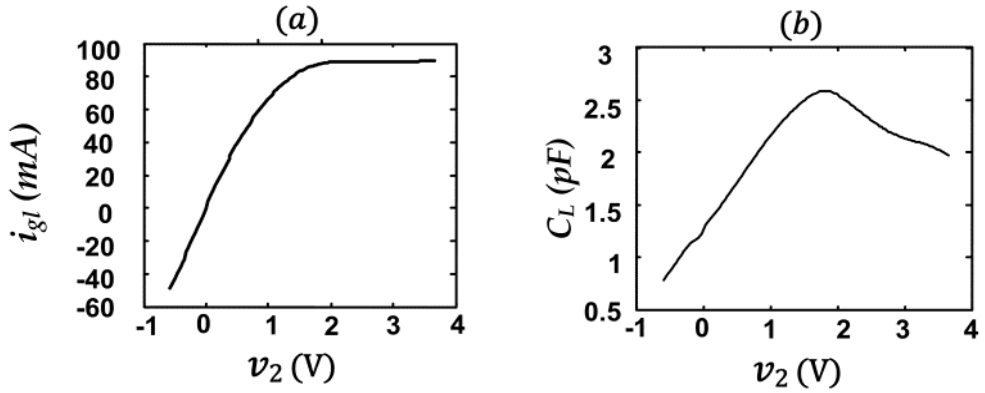

Figure 3. 7. Static model's functions of the PD last stage: (a) I-V function, (b) C-V function.

Figure 3.8 highlights the difference between the extracted C-V functions using the bias dependent small-signal analysis [15] at *f*=700 MHz and only an ESS signal. As the PD device enters into the nonlinear regime (saturation), the small-signal extraction is no longer correct and results in an inaccurate description of the local model C-V function.

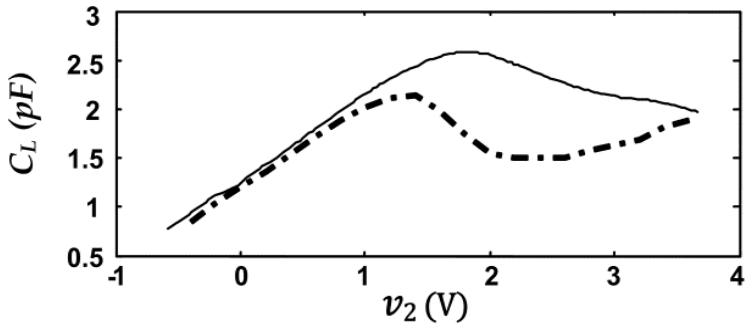

Figure 3. 8. Comparison between the C-V functions extracted with ESS large signal (solid line) and the bias-dependent ac (dashed line).

In order to assess the prediction performance of the identified model, it was simulated in the presence of pulsed voltage waveform with an amplitude range of [-0.3V 3.5V], a 1 ns rise/ fall time and 4 ns pulse width. Its good predictive capability is shown in Figure 3. 9. Beyond the visual inspection for verifying the good agreement between the TL model and the I-Q model results, we adopted the relative timing error (RE) and the normalized mean square error (NMSE) metrics for quantifying the accuracy between simulated and predicted signals to assess the prediction performance of each model. The RE and the NMSE metrics are defined as:

$$\begin{cases} RE(k) = 100 * \dfrac{y(k) - \hat{y}(k)}{y(k)} \\ NMSE_{dB} = 10log_{10}\left[\dfrac{\sum_{k=1}^{K}(y(k) - \hat{y}(k))^2}{\sum_{k=1}^{K}(y(k))^2}\right] \end{cases} \tag{3.5}$$

where the signals y and $\hat{y}$ correspond to the current wave-forms of the driver's last stage for the TL model and the I-Q model (or the model of [15]), respectively. *K* represents the total number of recorded samples.

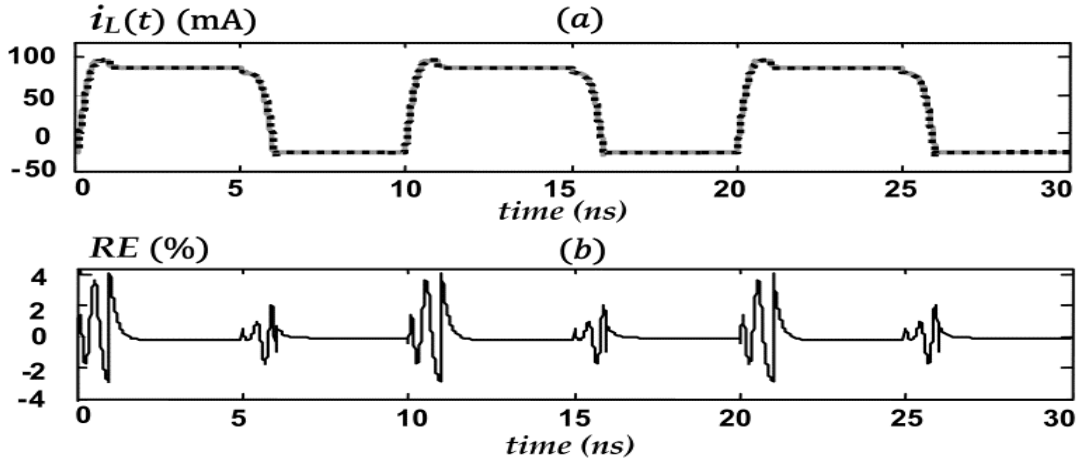

Figure 3. 9. Model extrapolation (a) Comparison between the $i_L(t)$ of the TL model (solid line) and the I-Q behavioral model (dashed line) when excited with a pulse. (b) The relative error with a much finer scale. The obtained NMSE was -30.08 dB.

The difference between the current waveforms produced by the TL and the I-Q behavioral models is very small. The good accuracy of the I-Q model's simulation result confirms its good predictive capabilities. Moreover, it shows that an ESS with a dc offset is enough to excite the dominant nonlinear dynamic effects of the driver's last stage composed by a transistor in parallel with clamping diodes.

After the parameters of the static I-V and C-V were extracted for both local models, the nonlinear dynamic functions $i_L(.)$ and $i_H(.)$ were implemented through Symbolic Defined Device (SDD) elements in the Advanced Design System (ADS) [40] in order to validate the global I-Q model for the CMOS driver. The SDD - a user defined voltage-controlled current or charge (according to the nonlinear electron device model quasi-static approximation) - enables the creation of custom nonlinear models specified by their algebraic relationships, relating the port voltage, the port current, and their derivatives [40]. The transient describing functions, StIDFs, $w_L(t)$ and $w_H(t)$ were stored in the Data Access Component (DAC) as a *.tim* file and were implemented using PWL components. It is worth to notice that the mapping between the digital input signal (bit stream) and the timing functions, which are the inputs of the behavioral model, requires the simulator to have event-driven capabilities. Detailed examples of I-Q behavioral model functions' implementation in ADS are presented in [40].

The performance of the proposed behavioral model was verified in a SI scenario, typically considered to assess the performance of digital interconnected systems.

Following the strategy described in the previous section, the I-Q structure was extracted with three SBFs for the $i_g(.)$ and $C(.)$ static nonlinearities for both PU and PD stages. Figure 3.10 shows the considered SI simulation setup, where the transmission line representing the PCB trace was loaded with series RC circuit that emulates the input impedance of the receiving device. The package interconnects of the driver are also considered and modeled by an RLC π-network as it is detailed in [6].

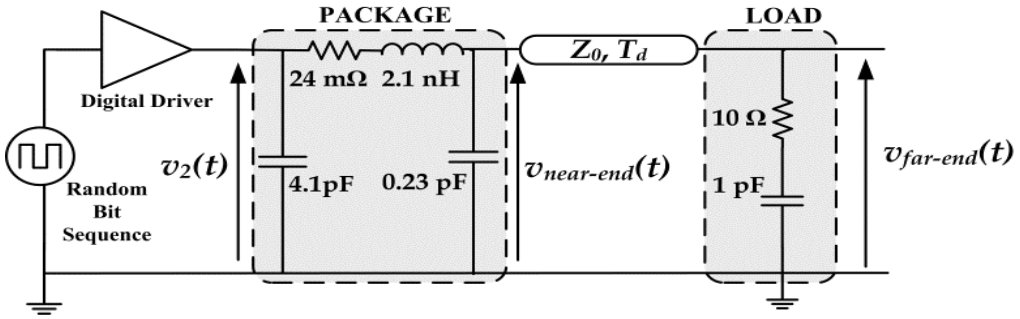

Figure 3. 10. SI simulation setup used for the model validation.

The input signal is the bit pattern "0100110110" where the rise and fall times are equal to 0.5 ns, and a pulse width of 3 ns. In this realistic validation setup, the driver is tested with a dynamic load that present a high mismatch, much different from the one used during the model extraction (Figure 2.11). These considerations are crucial for the SI analysis of on-board high-speed digital systems. The transient waveforms were computed through the Spectre-SPICE simulator from Cadence, providing the TL description and the I-Q behavioral model implemented in ADS. Figure 3.11 and Figure 3.12 illustrate the good accuracy of the developed model in predicting the output voltage (and, consequently, the output current) waveforms at the near-end and far-end of the ideal transmission line, respectively. For the cases (a) and (b) the delay was T_d=1.5ns and T_d=1ns, respectively, while the impedance was Z_o=50Ω for both cases.

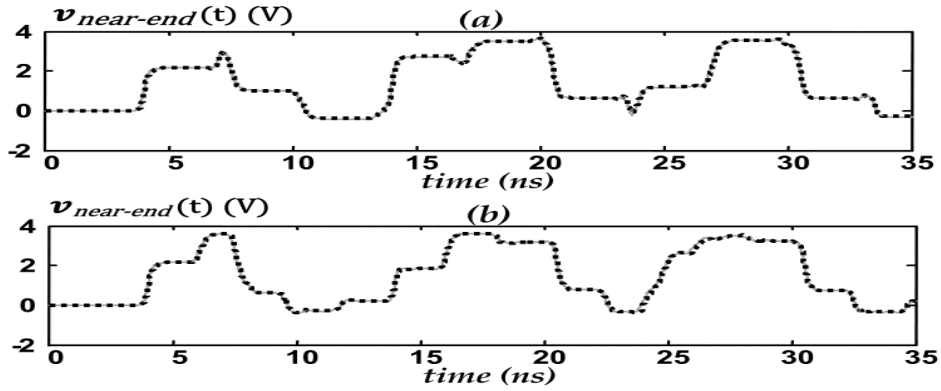

Figure 3. 11. Validation of the I-Q behavioral model. The near-end voltage waveforms: (a) T_d=1.5ns and (b) T_d=1ns. TL model response: solid line; I-Q model response: dotted line.

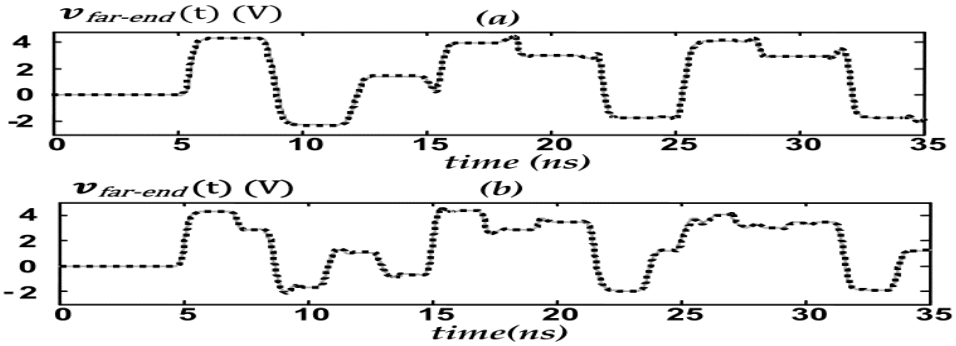

Figure 3. 12. Validation of the I-Q behavioral model. The far-end voltage waveforms: (a) T_d=1.5ns and (b) T_d=1ns. TL model response: solid line; I-Q model response: dotted line.

In order to compare the IBIS model performance against that of the I-Q behavioral model, their accuracy has been quantified by computing the relative timing error, RE, of (3.5). The IBIS model for this CMOS driver was generated and implemented according to the specifications [25], [41]-[43]. The far-end transmission line voltage generated by IBIS model for T_d=1.5ns is plotted in Figure 3.13. The improvement that the novel approach adds to the model accuracy is noticeable, mainly, at the rising and falling edge due to the reflection caused by the dynamic impedance mismatch of the driver, the package interconnects and the transmission lines. As seen in Figure 3.14, the RE was always smaller than 10% in the up and down transitions for the I-Q model, while it reached values close to 30% for the IBIS.

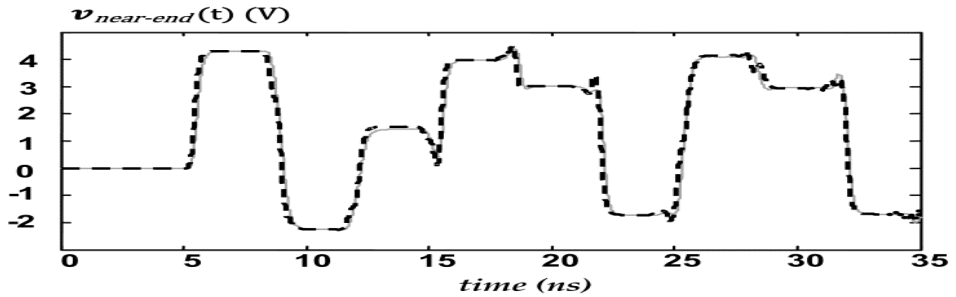

Figure 3. 13. Comparison between the IBIS (dashed line) and the TL model (solid line) of the far-end voltage.

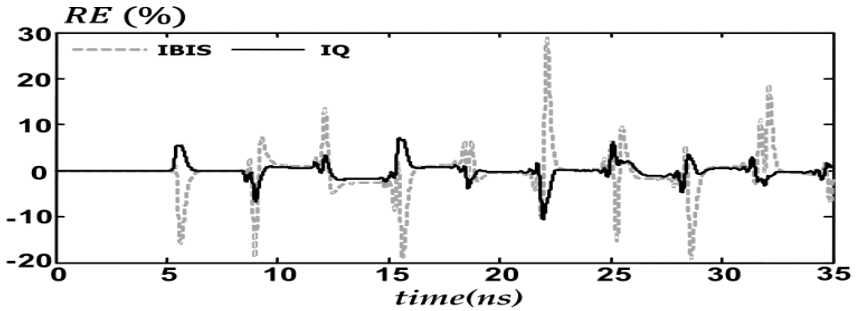

Figure 3. 14 Accuracy of I-Q and IBIS behavioral models is illustrated by the RE for each model in predicting the far-end voltage.

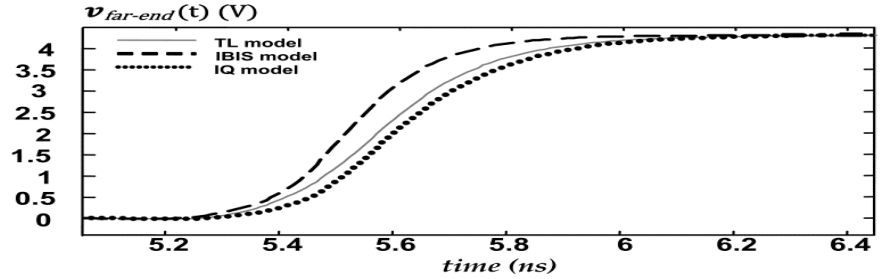

Figure 3. 15. Zoomed perspective of the first up transition of Figures 3.12.a and 3.14. IBIS model response: dashed line; I-Q model response: dotted line; TL model :solid line.

The high peak values of RE shown in Figure 3. 14 correspond to the trajectory difference that the signals generated by the different models have during the low-to-high and high-to-low transitions. This is highlighted in Figure 3. 15, which is a zoomed perspective of the first low-to-high transition of the signals presented in Figure 3.12.a and Figure 3.13. As during this transition time the signals' values are changing very fast, a slight deviation on their trajectory makes the difference between signals, at each sample, to achieve high values, leading to high peaks of the RE figure. However, it must be noticed that even during the transition times the I-Q model provides a very good estimate of the TL reference signal, achieving a very significant accuracy increase with respect to the IBIS estimate during this period. Nevertheless, the steady state error for both models is very small, as expected. Additional indexes quantifying the cost and efficiency of the model are shown in Table 3.1.

Table 3. 1. Performance of the TL, IBIS, and the I-Q Model for the SI simulation setup of at the far-end voltage, when the buffer is driven by the bit pattern "0100110110".

Model	NMSE(dB)	CPU time (s)
TL	-	107
I-Q	-32.96	4.14
IBIS	-19.82	4.01

The CPU time required by the I-Q model is in the order of seconds on a Pentium-IV PC. In fact, the obtained model can be evaluated as fast as the IBIS and it is 25 times faster than the TL model. Moreover, we noticed a -13.14 dB improvement in the NMSE of the far-end voltage between the IBIS and the I-Q models.

3.2.5 Summary

This section 3.2 demonstrates that the I-Q model provides an extended structure for the nonlinear local models ($i_L(.)$ and $i_H(.)$) of the IBIS model by capturing the nonlinear voltage-dependent capacitive effect showed by the driver output impedance.

This approach results in a global model not only as simple and stable as the IBIS model, but also presenting better accuracy. The proposed model is parametric in the sense that it relies on the parameter's estimation by training according to the provided large signal time domain input-output data using a hybrid algorithm. In fact, its structure was carefully selected based on the knowledge of the equivalent circuit constitutions of the driver last stage (a transistor in parallel with a diode). Therefore, including only the first derivative of the output voltage, our direct parametric model does not suffer from the instability issues of the recursive model formulation of the previous approaches [29]-[33]. This modeling approach can be regarded as a gray-box technique on the boundary between black-box ANNs and transparent-box equivalent circuit models, reducing the neural network static nonlinearity and dynamic orders.

Besides, this work also advances a simple and fast experiment that provides all the data needed for model extraction from a single step test, this way reducing the number of required measurements. The validation of the proposed I-Q model was performed in mismatch loading conditions and various trace delays, demonstrating that the proposed model has good predicting capabilities under loading conditions that were significantly different from those considered in the model extraction stage.

3.3 Least-Squares Extraction of a New Table-Based Model

As described in the previous chapter II**,** the IBIS model present a nice balance between accuracy, complexity and stability and it is arranged in a LUT format comprising the static I-V characteristics of the driver's last stage and the switching V-t tables. The dynamic behavior of the one-port driver's last stage is linearly modeled by a lumped capacitor [25], and it is captured by recursive ANN formulations in other proposed models [28]-[32] that require complex and time consuming identification procedures that incorporate nonlinear optimization algorithms for the computation of the model parameters with various basis functions. Besides, the model accuracy depends on the initial guess of the parameters and on local minima of the MSE [32].

In this section the extraction of the gray-box model formulation, which is supported by the I/O buffer physical constitution, leading to a complexity reduction of the modeling problem is presented. The proposed methodology reduces the amount of required identification data, the extraction cost, and the simulation time. The static model's functions are identified via linear least-squares optimization from large-signal measurements and stored as LUTs. In fact, the model captures the I-V and the Q-V

functions, for the upper and lower devices comprising the PU and PD transistors with the ESD diodes, as shown in Figure 3.1.

3.3.1 Model Extraction and Enhancement

The new extraction procedure relies on the linear least-squares method. The underlying approach is described in [44]. In this work, a more compact matrix mathematical formulation is given to this approach that allows simultaneous extraction. Theoretically, two independent measurements are required to extract the voltage-current, $G_j(.)$, and voltage-capacitance, $C_j(.)$, functions. Nevertheless, it is possible to extract the two unknowns by means of only one transient measurement as detailed here for the lower devices of the last stage. Firstly, we consider that the excitation voltage $v_2(t)$ is a pulse with short rise and fall times and that covers all the voltage amplitude range. Then, we record the transient response $\{i_L(t), v_2(t)\}$ of the lower devices. Secondly, we pick the duplicate values of the voltage amplitudes at different time instants t_1 and t_2 that verify $v_2(t_1) = v_2(t_2)$ and their corresponding currents $i_L(t_1)$ and $i_L(t_2)$. Thirdly, by taking into account that the state functions are single-valued, so that they depend only on the instantaneous excitation voltage, we realize that $G_L\big(v_2(t_1)\big) = G_L\big(v_2(t_2)\big)$ and $C_L\big(v_2(t_1)\big) = C_L\big(v_2(t_2)\big)$. The value of the output voltage derivative at the time instant t_k is defined as:

$$E(t_k) = \left.\frac{dv_2(t)}{dt}\right|_{v_2(t)=v_2(t_k)} \tag{3.6}$$

We now can write (3.2) for the time instants t_1 and t_2 as

$$\begin{cases} i_L(t_1) = G_L\big(v_2(t_1)\big) + C_L\big(v_2(t_1)\big).E(t_1) \\ i_L(t_2) = G_L\big(v_2(t_2)\big) + C_L\big(v_2(t_2)\big).E(t_2). \end{cases} \tag{3.7}$$

The above equation shows that we have two equations with two unknowns for the two selected time instants. The $G_L(.)$ and $C_L(.)$ functions are obtained by linear inversion:

$$\begin{bmatrix} G_L\big(v_2(t_1)\big) = G_L\big(v_2(t_2)\big) \\ C_L\big(v_2(t_1)\big) = C_L\big(v_2(t_2)\big) \end{bmatrix} = \begin{bmatrix} 1 & E(t_1) \\ 1 & E(t_2) \end{bmatrix}^{-1} . \begin{bmatrix} i_L(t_1) \\ i_L(t_2) \end{bmatrix} \tag{3.8}$$

In order to avoid the ill-conditioning of (3.8) when inverting the matrix, it is necessary to select two time instants t_1 and t_2 in which $E(t_1)$ and $E(t_2)$ are significantly different, e.g. during the rising and falling edges because at the high or low logic steady states both derivatives equal to zero, as depicted in Figure 3.16 The amplitude of the excitation signal is within $[-\Delta, V_{DD}+\Delta]$, where Δ is the overvoltage margin. It is defined to be slightly beyond the range of the edge transition values to take into account the effects of signal overshoot and undershoot caused by the termination mismatch between the driver output nonlinear dynamic impedance and the PCB traces.

It is worth noting that the input-output time domain data recorded under a longer large signal excitation with different rise and fall times enables the extraction of the I-Q model functions using the linear least-squares method.

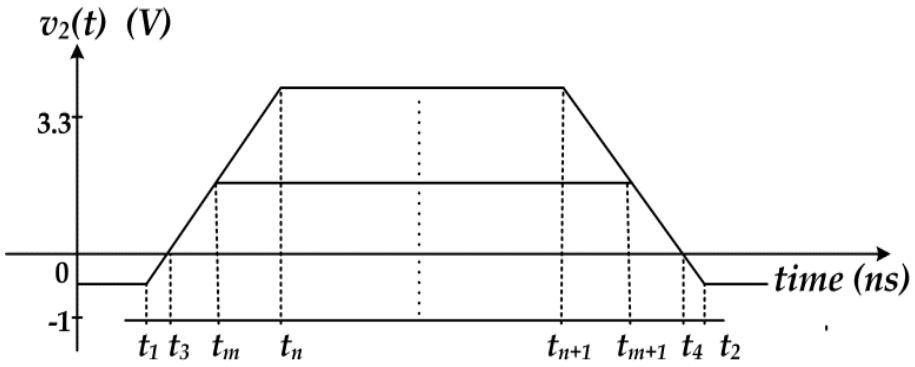

Figure 3. 16. Selected time instants of the duplicate amplitude of the $\boldsymbol{v_2(t)}$ for model extraction.

In fact, by picking more than two time instants, t_k, $k=1,..,N$, for which $v_2(t_i) = v_2(t_j), \forall_{i,j\in\{1,..,N\}}$, and the derivative $E(t_k)$ assumes distinct values for every k. N represents the total number of samples.

$$\begin{bmatrix} G_L(v_2) \\ \\ C_L(v_2) \end{bmatrix} = \left(\begin{bmatrix} 1 & E(t_1) \\ 1 & E(t_2) \\ \vdots & \vdots \\ 1 & E(t_N) \end{bmatrix}^T \begin{bmatrix} 1 & E(t_1) \\ 1 & E(t_2) \\ \vdots & \vdots \\ 1 & E(t_N) \end{bmatrix} \right)^{-1} \begin{bmatrix} 1 & E(t_1) \\ 1 & E(t_2) \\ \vdots & \vdots \\ 1 & E(t_N) \end{bmatrix}^T \cdot \begin{bmatrix} i_L(t_1) \\ \vdots \\ i_L(t_N) \end{bmatrix} \qquad (3.9)$$

The main advantages of this extraction procedure, compared to that of (3.8), are the higher immunity to measurement noise and better fitting of extracted I-V and C-V functions, minimizing the sum of squared error between the observed input-output data As an example, the current response of a driver's TL model versus the pulsed $v_2(t)$ (as seen in Figure 3.16) is shown in Figure 3.17. The looping in the trajectory in the I-V plane is a clear indication that the voltage-dependent capacitive effect is significant in the behavior of the one-port upper and lower devices of the driver's last stage.

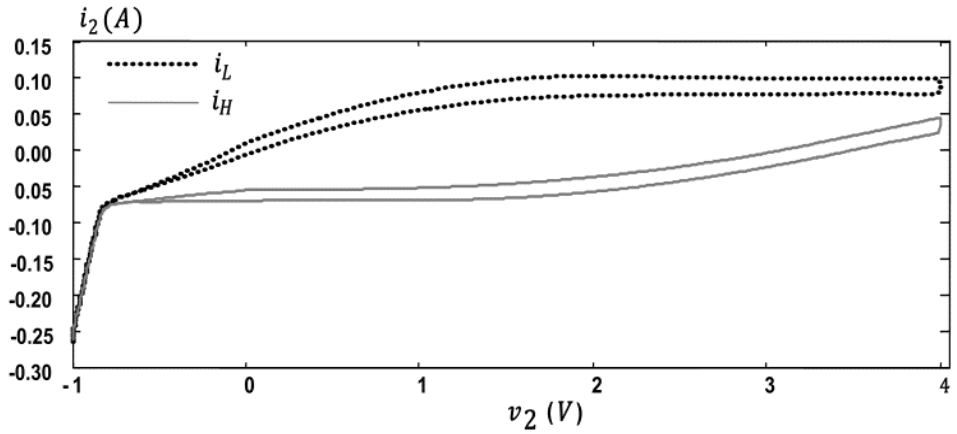

Figure 3. 17.Nonlinear dynamic characteristic of the output port of the lower and upper devices.

Consequently, with only one input-output time domain measurement, where the input signal $v_2(t)$ is a sequence of pulses of varying rise and fall times, it is possible to extract the nonlinear current and capacitance functions by solving (3.9) for different sets of $v_2(t_k)$ values. This extraction method leads directly to the C-V function from which the Q-V function can be obtained by integration [44].

$$Q_j(v_2) = \int_{-\Delta}^{V_{DD}+\Delta} C_j(v_2)dv_2\,; \quad j = L, H \tag{3.10}$$

This relation is used to further enhance the model proposed in (4) to its final formulation in the structure presented in Figure 3.18. By implementing the Q-V LUT instead of the C-V one, the model computational complexity measured in terms of the number of floating point operations is significantly reduced by 33% [45], [46].

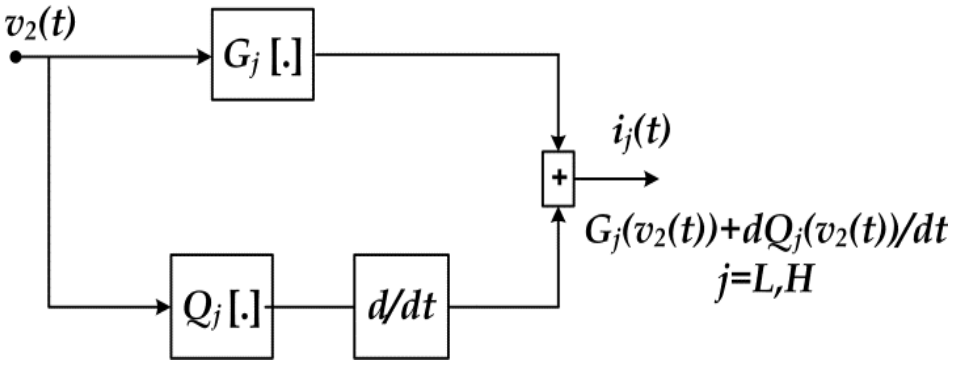

Figure 3. 18. Proposed model structure for the output behavior of an I/O buffer ($G_j(.)$ and $Q_j(.)$ are implemented as static LUTs).

The described methodology has a physical support for the model formulation. Besides that, since it uses the linear least-squares method, which does not require initial values for the parameters, the global minimum of the unique solution is guaranteed.

These are clear advantages over techniques based on ANN formulation [28]-[32]: Not only the resulting ANN models are more complex (and their topologies are arbitrarily tuned), as they require nonlinear optimization algorithms for the parameter extraction process which can easily fall into local minima solutions (and such solutions are dependent on the initial values that are assumed for the parameters) [32]. Additionally, the continuous time-domain model is easily implemented with fewer errors in circuit simulators since it does not require the conversion from a discrete-time domain model to a continuous state space representation, nor the modification of the model equations, as was done for the nonlinear parametric model [29].

It should be noted that these I-Q model formulation and extraction methodologies can also be extended to model the low voltage differential devices or drivers with pre-emphasis features. In fact, this new modeling problem can also be understood as capturing the nonlinear behavior of the two-dimensional I-V and Q-V tables controlled by the two output voltage terminals of the last stage's upper and lower devices [25].

The device I/O timing behaviors are captured by identifying the StIDF, $w_L(t)$ and $w_H(t)$, as it was carried out in the previous section. Their combination with the $i_L(.)$ and $i_H(.)$ functions results in the model (2.17) that describes the driver's behavior in the transient analysis, avoiding the measurement of the device's response for multiple input rising and falling edge transitions [47]. It is worth noting that the StIDFs should be carefully extracted by capturing the different transition edges of the voltage levels that schedules the activation of the I-Q model upper and lower devices according to the predriver's characteristics [25], [48].

3.3.2 Model Implementation

Generally, the various CAD tools (e.g. SPICE-type [40], Spectre, ADS [43], etc) provide the necessary components to implement the analog nonlinear functions of the I-Q model. For instance, the conduction, I-V, and displacement, Q-V, single-valued nonlinearities for the driver are implemented as LUTs in the ADS simulator as SDD elements [40]. However, the implementation of the logic mapping between the digital excitation and the analog StIDFs requires a mixed-domain processing of the input digital signal to select the appropriate scaling coefficient for I-Q functions of the upper and lower devices of the driver's last stage as shown in Figure 3.19. The StIDFs for up and down transitions, $w_L^i(t); i = u, d$ and $w_H^i(t); i = u, d$, are stored in a DAC in ADS as a *.tim* file in which the time is the independent variable. Then, they were

implemented using PWL voltage components [40]. Although the basic components available in simulators do not allow to easily implement the juxtaposition of the StIDFs, the ADS simulator provides a numeric communication advanced component [49] which is extensible to MATLAB logic functions that eases the implementation of the mixed-domain interface. This way the model remembers the driver's states and generate control signals to properly select the analog StIDFs.

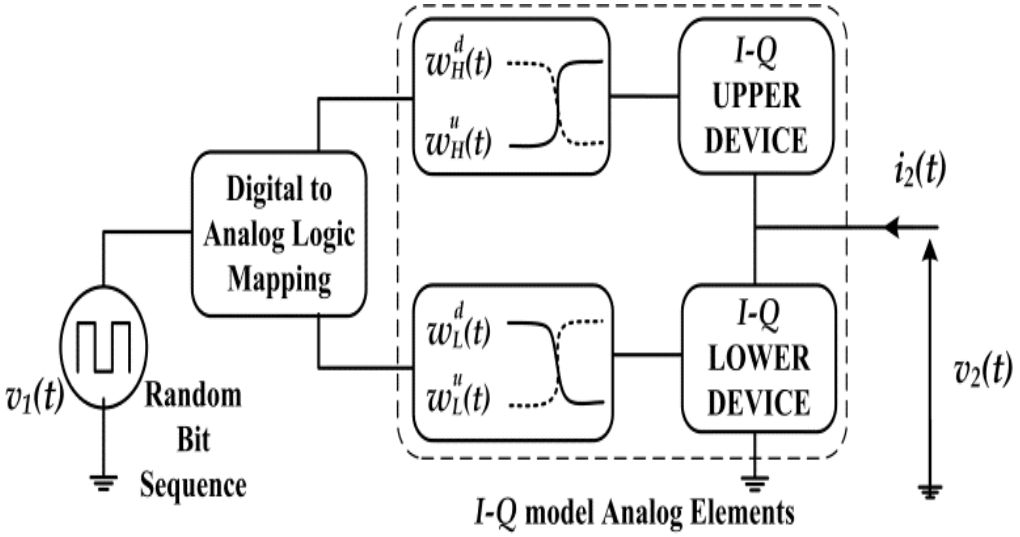

Figure 3. 19. The mixed-model driver's behavioral model circuit components within a CAD.

3.3.3 Nonlinear Output Functions' Validation

The performance of the proposed modeling approach is demonstrated on a high-speed BT4P_3B CMOS output buffer, which is used in memory interfaces from Austria Microsystems operating at 270 Mbps (maximum switching frequency specified by the vendor). It is a 0.35µm technology from c35 IOLIB cells ($V_{ss} = 0\ V; V_{DD} = 3.3\ V$). Firstly, the extraction procedure is presented and the performance of the I-Q structure, applied to the lower devices - $i_L(.)$ - to capture the nonlinear dynamic current-voltage relationship, is assessed. Then, the global table-based I-Q model performance is compared with those of IBIS and TL models, when considering channel reflections and crosstalk between PCB traces. The time domain data is obtained from transient analysis of the TL description using Spectre-SPICE from Cadence Design Systems, Inc.

The transient response of the physical model for both the lower and upper devices is recorded when they are excited with a train of trapezoidal pulses with various rising and falling edge transitions. Then, the nonlinear functions describing the conduction and displacement currents are extracted by means of the least square formulation of (3.9). The obtained functions are shown in Figure 3.20.

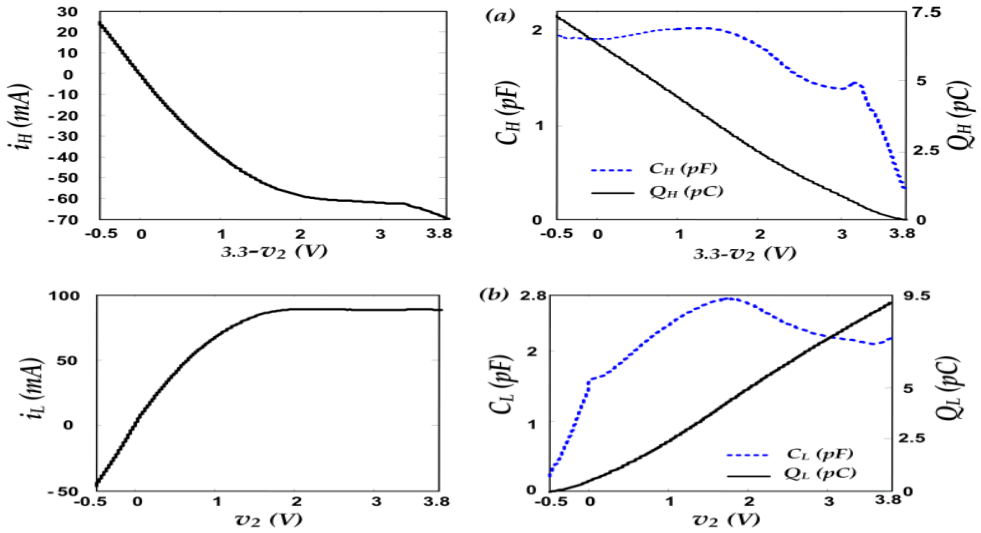

Figure 3. 20. Conduction and displacement single valued nonlinearities for (a) the upper, and (b) the lower devices of the driver's last stage.

In [15], the I-V and C-V curves are extracted separately and modeled as rational basis functions. In fact, a two-step extraction procedure was used in that case: the dc sweep is used for extracting the conduction function, and a bias-dependent small-signal ac measurement was used for recording the displacement current. This requires a more time consuming extraction procedure with a higher number of measurements. The accuracy of [15] and that of the proposed I-Q model, for modeling the I-V looping trajectory of the lower device, and the prediction capability in the presence of pulsed voltage waveforms with the amplitude range of [0V, 3.3V], a 1 ns rise/fall time and 4 ns pulse width, are compared in Figures 3.21 and 3.22, respectively. They clearly show a very good agreement between I-Q model extraction methods and the TL model. It is worth mentioning that the inaccuracy of the approach of [15] arises from the bias-dependent small-signal ac extraction method with a single frequency excitation. On the other hand, the I-Q extraction uses a large-signal pulsed time domain excitation close to the driver usual operation conditions, with a reduced number of required measurements.

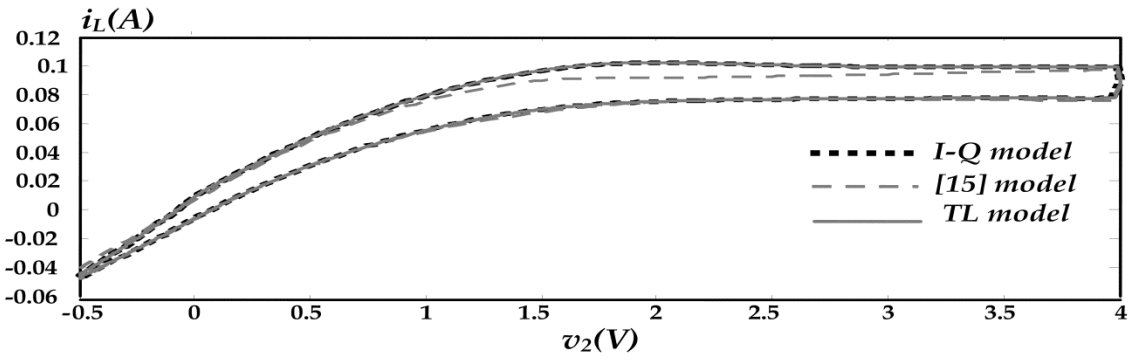

Figure 3. 21. Comparison between the measured $\boldsymbol{i_L(t)}$ versus $\boldsymbol{v_2(t)}$ trajectories for the TL model, the proposed I-Q model and the model of [15].

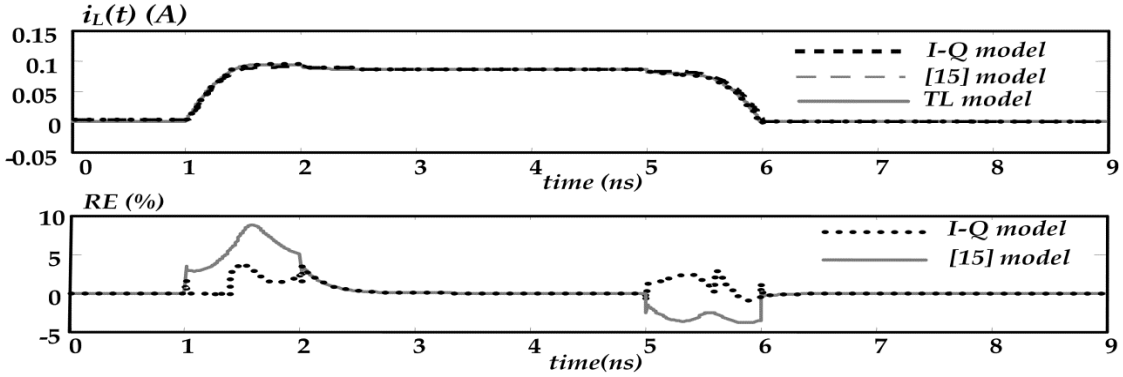

Figure 3. 22. Comparing the time-domain $i_L(t)$ waveforms estimated by the TL model, the I-Q model and the model of [15].

Using the TL results as reference, the simulation results of the I-Q behavioral model present a better accuracy than the model of [15], which confirms its good predictive capabilities. Moreover, the NMSE is improved by 8 dB with a signal different from that used in the extraction as shown in Table 3.2.

Table 3. 2. Performance of the simulation of the TL, [15], and the I-Q models.

Model	NMSE(dB)	CPU time (s)
TL	-	73
[15]	-28.94	1.29
I-Q	-36.97	1.02

3.3.4 Channel Reflection Simulation

In order to assess the performance of the I-Q model in practical SI validation setups, the model's nonlinear and timing functions extracted for CMOS driver were implemented as LUTs in the ADS simulator. The signal degradation in high-speed digital design resulting from reflections due to mismatched impedances is one of the most common SI case studies. To demonstrate how suitable the proposed model is for channel reflection analysis, the complete I-Q model is compared to the IBIS model when both models were implemented in the same channel reflection simulation setup as shown in Figure 3.23.

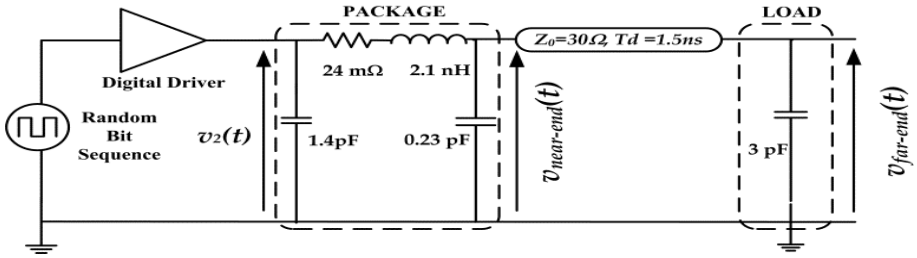

Figure 3. 23. Channel reflection setup used for the evaluation of the I-Q and IBIS models.

The considered input sequence is the bit pattern "0100110110" where the rise and fall times are equal to 0.5 ns, and the pulse width is 3 ns. In this realistic validation setup, the driver is tested with dynamic load conditions that present a high mismatch, much different from the one used during the model extraction. These considerations are crucial for the SI analysis of on-board high-speed digital systems. The transient waveforms were computed through Spectre-SPICE, providing the TL description, the IBIS model implementation [25] and the I-Q behavioral model implemented in ADS. Figure 3.24 illustrates the good accuracy with which the developed model predicts the $\boldsymbol{v_{far-end}(t)}$ on the ideal transmission line ($\boldsymbol{Z_0 = 30\Omega}$ and $\boldsymbol{T_d}$ = 1.5 ns).

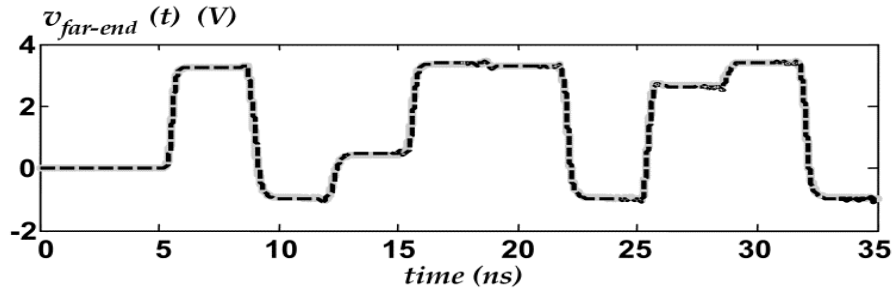

Figure 3. 24. $\boldsymbol{v_{far-end}(t)}$ waveform. Solid lines: TL model; dashed line I-Q model.

The zoomed view of the predicted far-end voltage of the I-Q and IBIS models is shown in Figure 3.25 along with the respective relative errors. The high peak values of RE correspond to the trajectory difference that the signals generated by the different models have during the low-to-high and high-to-low transitions. However, it must be noticed that even during the transition times the I-Q model provides a very good estimate of the TL reference signal, achieving a very significant accuracy increase with respect to the IBIS estimate during this period. Nevertheless, during the steady state, the error for both models is very small, as expected.

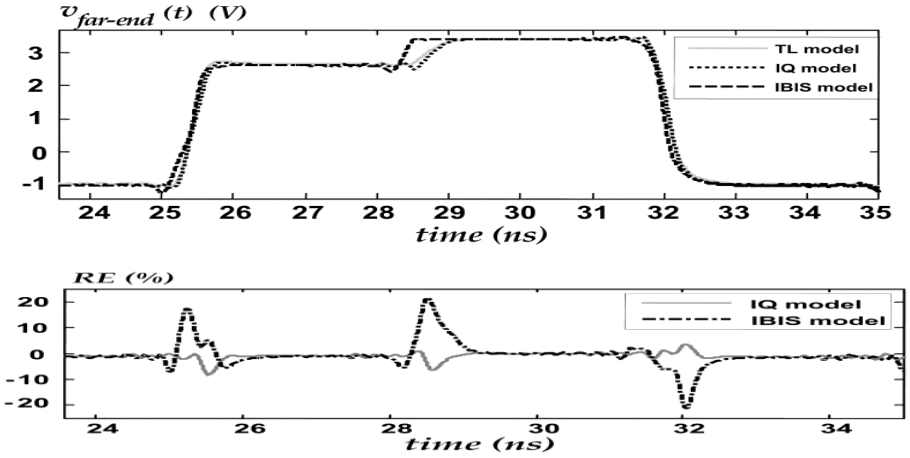

Figure 3. 25. RE of the results obtained with the I-Q and IBIS models, w.r.t to the TL model.

Additional indexes quantifying the accuracy and the computational efficiency of the models are shown in Table 3.3. The CPU time required by the I-Q model is on the order of a few seconds on a Pentium-IV PC. In fact, the obtained model can be evaluated as fast as the IBIS and it is 25 times faster than the TL model. Moreover, we noticed a 12 dB improvement in the NMSE of the far-end voltage estimation between the IBIS and the I-Q models.

Table 3. 3. Performance of the transient simulation of the TL, IBIS, the work of [15] and the I-Q models for the SI Setup of Figure 3.24 at the far-end voltage.

Model	NMSE(dB)	CPU time (s)
TL	-	101
I-Q	-37.87	4.14
[15]	-35.61	4.14
IBIS	-25.92	4.01

3.3.5 Crosstalk Simulation

Crosstalk refers to the noise produced in a signal line by the electromagnetic activity in a nearby trace or circuit. It is more noticeable when drivers switch (i.e., at the rising and the falling edges). During this time, the driven trace induces current in the adjacent quiet trace due to their capacitive and inductive coupling. The crosstalk simulation setup shown in Figure 3.26 is based on a lossy coupled microstrip transmission line driven by two similar CMOS output buffers and terminated by 1 pF capacitors. The active device transmits the bit pattern “0100110110”, while the quiet device transmits the bit pattern “0000000000”.

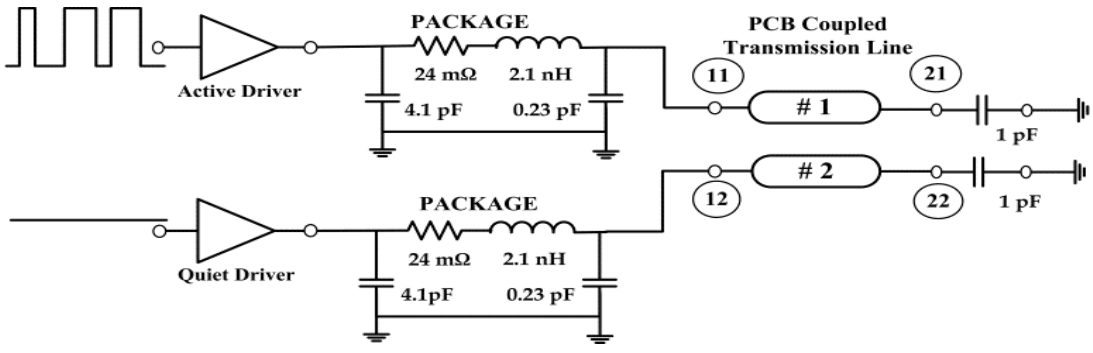

Figure 3. 26. Crosstalk validation setup with the RLCG coupled-line structure (Length=0.1m; R_{11}=R_{22}=45.97Ω/m,R_{12}=5.23Ω/m;C_{12}=-17.69pF/m,C_{11}=C_{22}=317.72pF/m;L_{11}=L_{22}= 251nH/m, L_{12}=41.38nH/m; G_{11}= G_{12}= G_{22}= 0.00 S/m).

Figure 3.27 shows the good accuracy of the of I-Q model in predicting the signal reflections on the active channel (#1) constituted by the package and the coupled

transmission line (signals measured at the near- and far-ends of the transmission line). Moreover, the voltage waveform transmitted in the adjacent channel (#2) was also calculated and compared with the reference TL model, as shown in Figure 3.28. This comparison highlights that the near-end and far-end crosstalk can be accurately predicted when using the I-Q model.

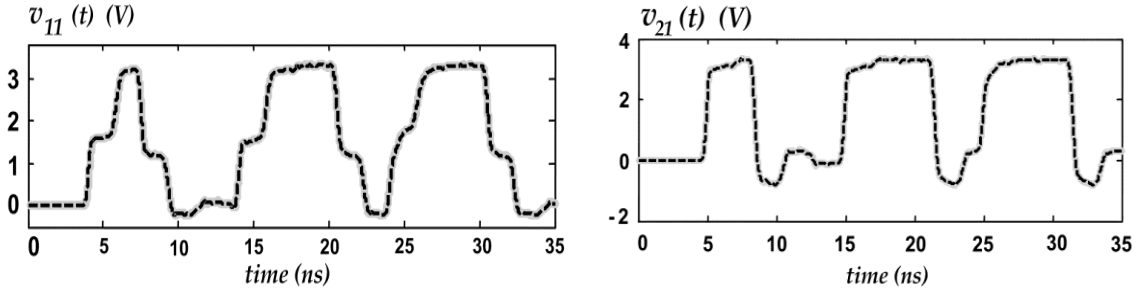

Figure 3. 27. Comparision between the near-end and far-end voltage waveform $v_{11}(t)$ and $v_{21}(t)$ on the active channel of Figure 3.27. Solid lines: TL; dashed lines: I-Q model.

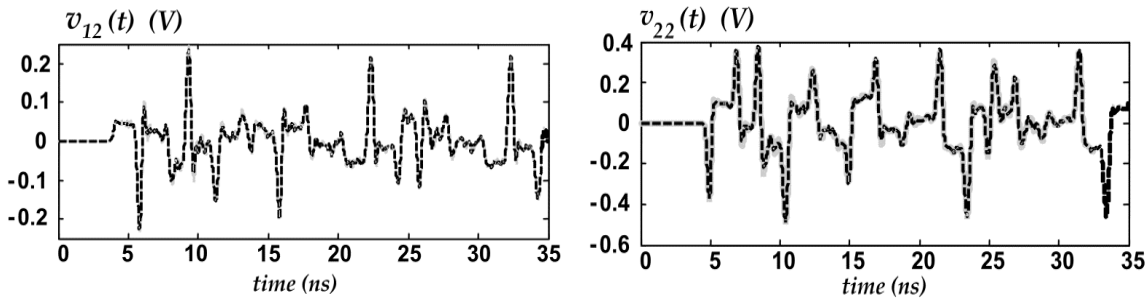

Figure 3. 28. Comparision between the near-end and far-end voltage waveforms $v_{12}(t)$ and $v_{22}(t)$ on the quiet channel of Figure 3.27. Solid lines: TL; dashed lines: I-Q model.

3.3.6 Summary

A new extraction procedure of the I-Q behavioral model for digital I/O buffers, is proposed. Such procedure is based on the linear least-squares optimization method, which avoids the drawbacks of nonlinear optimization algorithms (such as instability, local minima, training time, and dependence on parameter initialization) used for the training of ANN-based models, as suggested in previous publications. Additionally, the fast extraction and the easy implementation steps help the automation of the I-Q behavioral model generation.

The extracted single-valued I-V and Q-V functions physically describe the constitution of the electrical output impedance of the driver's last stage. Besides, it was demonstrated that the combination of the proposed model with the corresponding extraction procedure has led to a model with highly accurate prediction ability, keeping a highly reduced computational complexity. This is very important in signal integrity

analysis since a significant number of I/O buffer devices need to be accurately and simultaneously, in an efficient way, simulated in such applications. The proposed formulation outperformed that of other state-of-the-art models, being significantly more accurate than the IBIS model, for the same level of computational complexity.

3.4 Frequency Domain Extraction

The efficient construction of behavioral models requires the selection of a sufficiently accurate model structure that simultaneously reproduces the device behavior, for a wide range of operation conditions, and reduces the computational cost. But, the model's functions must also be identified reasonably with an easy way from straightforward lab measurements or circuit level simulations. There are three major model's extraction methodologies for capturing the driver's output behavior. Firstly, for models like ANNs nonlinear regression in discrete time domain is usually considered [28], [32]. This approach requires a time consuming extraction of a recursive black-box model structure from laboratory extraction [50]. Fortunately, it was recently shown that their associated complexity and stability issues can be reduced by a physically inspired parametric model structure [51]. Secondly, two simulation setups, dc and ac simulations, were used by IBIS [14] and by the work of [15] for capturing the nonlinear output I-V and C-V characteristics. While IBIS and [52] use a LUT-based implementation, the rational basis functions were used to fit the model's nonlinear functions in [15]. Finally, a linear least-square and simultaneous extraction of a table-based I-V and C-V functions from a fully time domain pulsed measurement dataset is presented in [53].

In this section, a frequency-domain model extraction procedure, based on the device's measured bias-dependent small-signal characteristics, is presented to construct the best fit (in least-squares sense) of the driver's output large signal admittance model over a frequency range. The model's formulation is based on the empirical I-Q description that can be applied to a wide range of digital I/O buffer structures. The data-based model's functions, which include the nonlinear conduction (I-V) and displacement (Q-V) characteristics, are extracted from S-parameter data and implemented as LUTs. The advantages of this approach to I/O buffers behavioral modeling include its wide applicability to several technologies, rapid parameter extraction from laboratory measurements using a vector network analyzer (VNA), accuracy in time domain simulations, and computational efficiency.

3.4.1 Frequency Domain Model Formulation

As detailed in the first section of this chapter, the one-port output behavior of the driver's last stage upper and lower devices is efficiently expressed in terms of the large-signal memory-less conduction current and stored charge as the input is either kept at "*H*" and "*L*" logic states:

$$i_K(v_2(t)) = I_K^c(v_2(t)) + \frac{dQ_K(v_2(t))}{dt}\ ; \quad K = L, H \tag{3.11}$$

The model (3.11) can be rewritten in terms of small-signal voltage and currents in frequency domain [55], [56]:

$$I_k = \frac{\partial I_k^c(V_2)}{\partial V_2} v_2 + j\omega \frac{\partial Q_k(V_2)}{\partial V_2}\ v_2\ ; k = l, h \tag{3.12}$$

where I_l, I_h, and v_2 are the output port's small signal currents and voltage, respectively. The bias voltage, V_2, is swept within the range [-Δ, Δ+V_{DD}], while the input voltage, V_1, is connected to the ground or to V_{DD}. The overvoltage margin, Δ, is established to account for the effects of signal overshoot and undershoot. The partial derivative of the model's static functions, $I_K^c(.)$ and $Q_K(.)$, can be described in terms of the bias-dependent admittance or Y-parameters.

$$Y_{22,k}(V_2, \omega) = \frac{I_k}{v_2} = G_k^c(V_2) + j\omega C_k(V_2)\ ;\ k = l, h \tag{3.13}$$

Consequently, the extraction is based on the above theory and it is illustrated in the following analysis. Firstly, the single-port S-parameters of the driver's last stage are measured – either in the lab using a VNA or via a circuit simulator – and the effects of the extrinsic circuit elements are de-embedded from the data leaving the Y-parameters of the intrinsic upper and lower devices as shown in Figure 3.29.

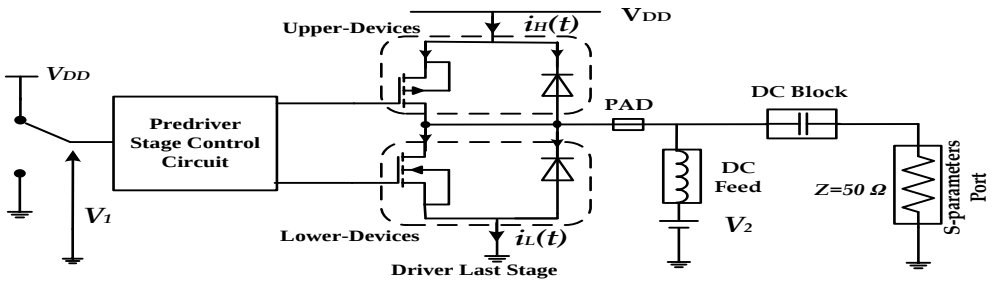

Figure 3. 29. Simulation setup for the extraction the bias-dependent Y-parameters data characterizing the upper and lower devices of driver's output admittance.

The output small signal conductance, $G_k^c(.)$, and capacitance, $C_k(.)$, can be derived from the bias-dependent Y-parameters using linear regression. This minimizes the sum of squared residuals over the frequency range of interest by solving the following minimization problem.

$$\begin{cases} C_k(V_2) = \min\limits_{C_k} \sum\limits_{\omega} \left| Im\left(Y_{22,k}(V_2,\omega)\right) - \omega C_k(V_2) \right|^2 \\ G_k^c(V_2) = \min\limits_{G_k^c} \sum\limits_{\omega} \left| Re\left(Y_{22,k}(V_2,\omega)\right) - G_k^c(V_2) \right|^2 \end{cases} \quad (3.14)$$

It is worth noticing that the linear regression not only reduces the impact of measurement noise in data –which significantly affect the performance of the constructed model – as it also minimizes the errors in the equivalent model by providing a best fit of the non-quasi static data into a quasi static model formulation. Then, the large-signal's functions are obtained for a range of the output voltages, V_2, by integration:

$$\begin{cases} I_K^c(V_2) = \int_{-\Delta}^{V_{DD}+\Delta} G_k^c(V_2)dV_2 \\ Q_K(V_2) = \int_{-\Delta}^{V_{DD}+\Delta} C_k(V_2)dV_2 \end{cases} ; \quad K = L, H \quad (3.15)$$

The model extraction procedure is formulated using an alternative model representation in the frequency domain, providing a methodology which successfully leads to optimal model identification. In fact, the parametric modeling approach [15], [28]-[32] based on nonlinear optimization algorithm identification may involve excessive computational cost and convergence difficulties. Also, it may suffer from inaccuracy due to the noisy measurement data or the tolerance of the characterized electronic sources and devices used to perform laborious measurements.

3.4.2 Model Functions' Extraction Results

The performance of the extraction procedure is illustrated on an inverting and single-ended CMOS driver. It is a 0.25µm driver (power supply: $V_{ss} = 0$ V; V_{DD} =3.3V) [2] in which the transistors are described by the BSIM3v3 model. The S-parameters data for 44 output voltage bias points measured over the frequency range [300MHz, 700Mhz] are used to extract the model's functions as shown in Figure 3.30.

The comparison between both types of identification procedure for the nonlinear conduction function shows a very good agreement. Besides, the proposed approach has the advantage of enabling the simultaneous extraction of both the I-V and Q-V functions from data delivered from single equipment (e.g. VNA). This verification proves the validity of the proposed signal model extraction from signal measurements.

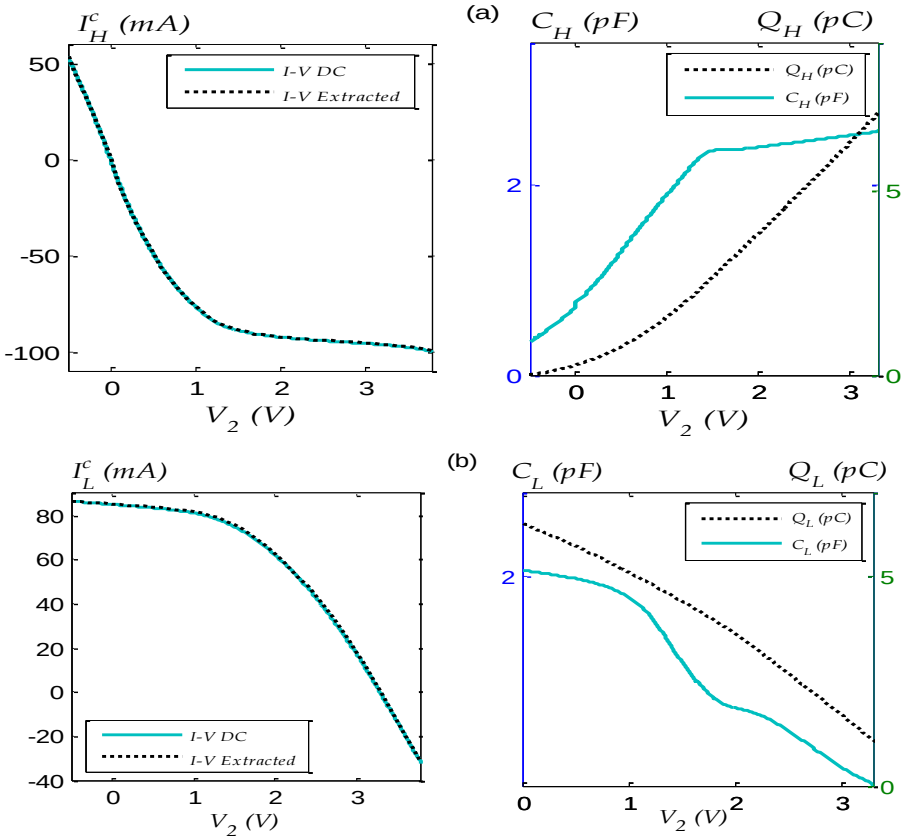

Figure 3. 30. Extraction and comparison of the I-V function with dc measurements at the left side and the Q-V function at the right side. lower (a) and upper (b) devices' functions.

3.4.3 Model Validation Results

The I-V and Q-V functions, along with $w_L(t)$ and $w_H(t)$ StIDF, were stored as LUTs and implemented in ADS as detailed in the previous section. The model's performance is assessed in a crosstalk simulation setup as shown in Figure. 3.31.

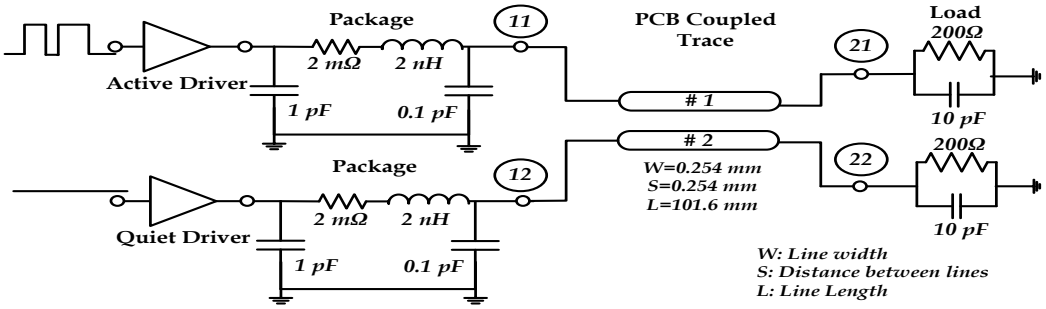

Figure 3. 31. Crosstalk simulation setup used for the I-Q behavioral model validation.

The active and quiet channels comprise the *RLC* network package and the coupled PCB traces (modeled in ADS as a coupled transmission line [12]) which are terminated with a parallel RC load. They are driven by a two-stage CMOS output buffers. The active driver transmits the bit pattern "10010111" where the rise and fall times are equal to 0.7 ns at 270 Mbps data rate while the quiet device behaves as if it were transmitting the "00000000" bit pattern. Figure 3.32 shows the good accuracy of the extracted I-Q model in predicting the signal due to reflections on the active channel (#1). The I-Q behavioral model improves the IBIS model's accuracy by capturing the missing nonlinear dynamics of the digital output buffer upper and lower admittances modeled by charge sources [8], as illustrated in Figure. 3.33.

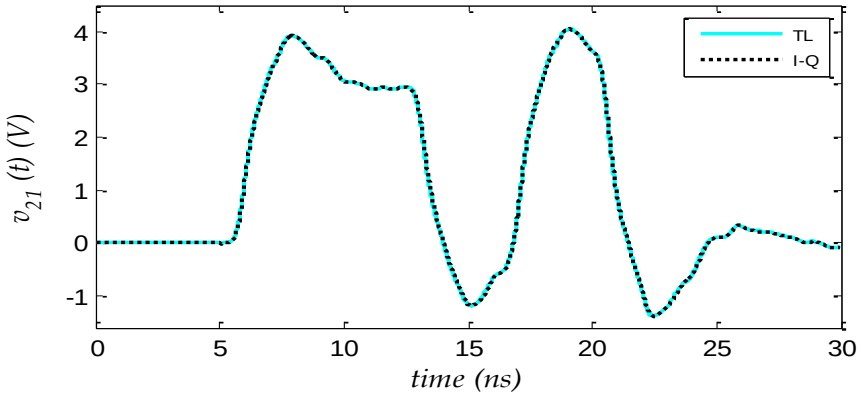

Figure 3. 32. Comparison between the far-end voltage waveform on the active channel. Solid lines: TL model; dashed lines: I-Q model.

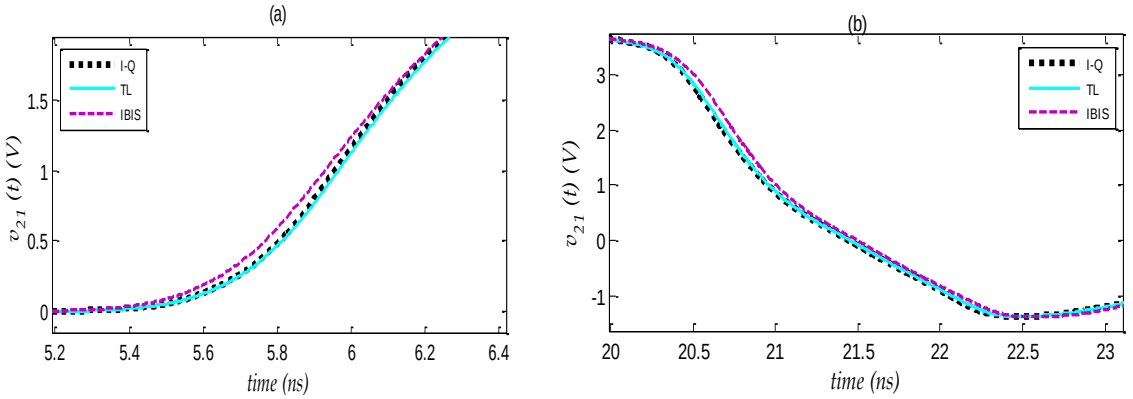

Figure 3. 33. Comparison between the IBIS and I-Q behavioral models against the TL model. Zoomed view of the far-end voltage waveform: (a) the first up output's transition, and (b) the last down output's transition.

Additionally, at the rising/falling edges the aggressor trace (#1) induces currents in the adjacent trace (#2) due to their capacitive and inductive coupling. The near-end voltage wave-form transmitted in the quiet adjacent channel trace due to the crosstalk was also captured and compared with the TL and IBIS models along with the voltage's error and shown in Figure 3.34.

The voltage error of the IBIS model reaches 50.5 mV, while it was smaller than 28.5 mV for the I-Q behavioral model. This result confirms the improvement introduced by the dis-placement currents captured by the voltage-dependent capacitance or charge. Besides, the predictive capability of both behavioral models is illustrated in Figure 3.35. Moreover, the NMSE (3.5) is used for quantifying the accuracy between simulated and predicted signals of each behavioral model as shown in Table 3.4.

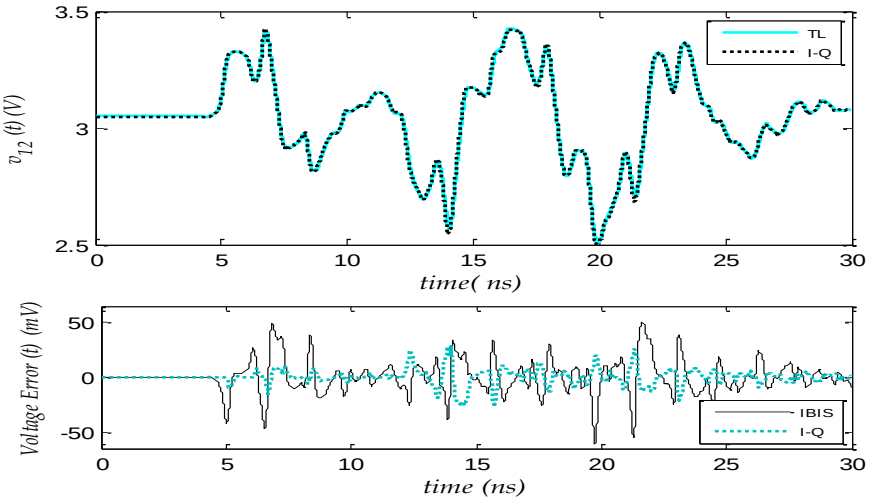

Figure 3. 34. Validation of the I-Q behavioral model. The near-end voltage waveform on the quiet channel and the voltage error of the IBIS and I-Q behavioral models.

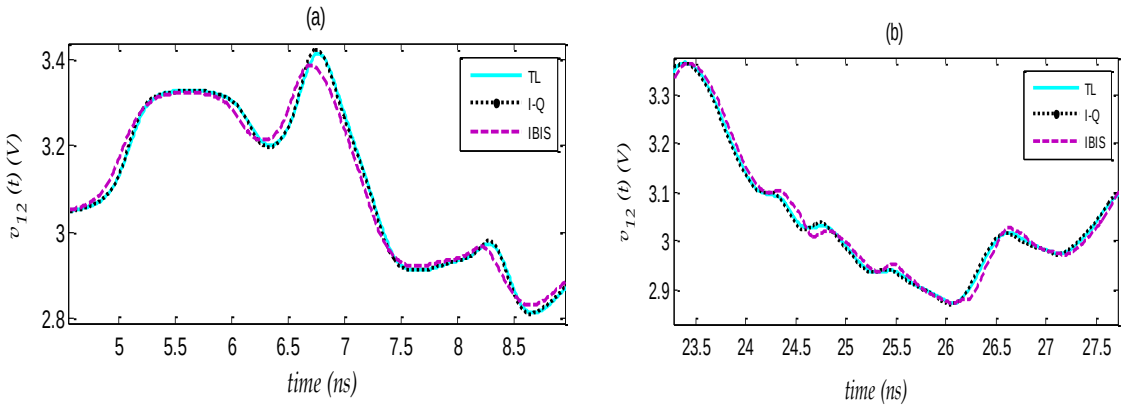

Figure 3. 35. Comparison between IBIS and I-Q behavioral models against the TL model in predicting the noise on the quiet channel. Zoomed view of the near-end voltage waveform: (a) the first up output's transition. (b) the last down output's transition.

Table 3. 4. Performance of the simulation of the TL, IBIS, and the I-Q models for the setup of Figure 3.32.

Model	$NMSE_{v_{21}}$ (dB)	$NMSE_{v_{12}}$ (dB)	CPU time (s)
TL	-	-	20.29
I-Q	-35.5	-51.1	6.92
IBIS	-27.1	-38.6	6.64

As seen from Table 3.4, the extracted I-Q model improves the predictions of the far-end voltage waveform on the active channel by 8.5 dB and for the near-end voltage waveform on the quiet channel by 12.5dB without sacrificing the IBIS model computational efficiency. This good agreement between the physical and the I-Q behavioral model, under high termination mismatch between the driver's output admittance and the PCB traces characteristic, confirms the validity of the extraction method for transient simulation under trapezoidal excitations.

3.4.4 Summary

The bias-dependent small-signal admittance data, recorded from the circuit-level model by simulation, or from the actual device's laboratory measurements, are used to construct the best fit of the behavioral model for the driver last stage over a wide frequency range of operation. The combination of the extracted I-Q model and the StIDF can be effectively used for nonlinear design of digital interconnected systems. In fact, the measurement-based and table-driven behavioral model, implemented as LUTs, maintains high accuracy and computational efficiency as it is an extension of the IBIS model structure by modeling the nonlinear stored charge effect accountable for the displacement current.

3.5 Two-port Solution for Overclocking Simulation

Nowadays, IC and PCB designers are willing to operate their digital interconnected systems at higher data rates, running them faster than the specified clock frequency, an operation condition known as "overclocking" [27]. In fact, by overclocking lower-priced components, but still keeping the specified bit-error-rates, the digital equipment manufacturers can sell their products with higher profit margins. As happens with the normal clocking condition, the assessment of the SI performance of the interconnected digital system designs under overclocking is usually carried out by simulation. This relies on the availability of a reliable CAD behavioral model [28]-[32], [50]-[53]. In fact, and as shown in Figure 3.36, the I/O buffer is an active device that comprises two parts: the predriver stage, which processes the input signal so that its output voltage meets the timing and amplitude requirements of the driver's last stage, and this wide CMOS inverter, responsible for providing the chips' interconnect current. Therefore, finding a behavioral model for these I/O buffer interfaces capable of offering the accuracy and the predictive capabilities of the TL model, but still keeping the

aforementioned properties of model generality and computational efficiency, is of paramount important for the SI analysis of modern digital systems operating in both the normal and overclocking conditions.

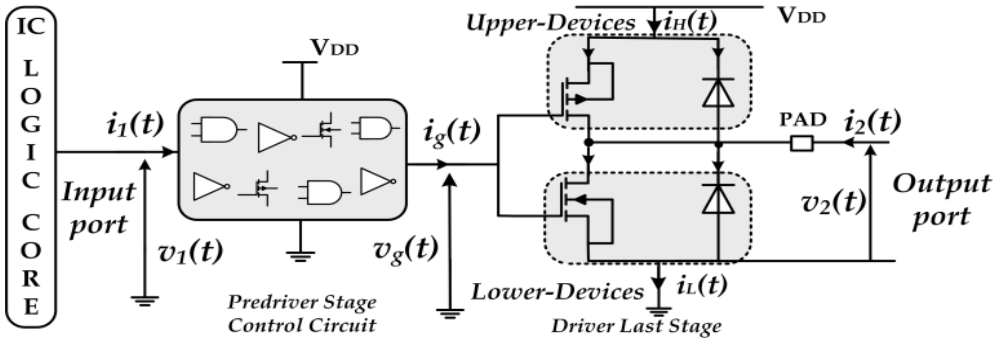

Figure 3. 36 Generic digital I/O buffer electrical structure with its relevant electrical variables.

Recent advancements in I/O buffers' behavioral modeling, as the table-based extensions of IBIS [52], [53], or the parametric models of [28]-[32], [51] have been focused on the improvement of the one-port output stage network of the output buffers/drivers. So, these previous approaches share the same methodology for capturing and implementing the nonlinear dynamic behaviors of the predriver's input stage, presenting fixed table-based timing signals. Consequently, they cannot provide complete models capable of predicting the I/O buffers' distortion behaviors when the designer overclocks these CAD representations [28]-[32], [51], [53] i.e. when the bit duration is less than the extracted timing signals window [54], [57]. In fact, under overclocking operation, the last stage's gate voltage, $v_g(t)$, (please refer to Figure. 3.37) has not enough time to complete the state transitions, i.e., to reach the steady-state. Therefore, the last stage's transistors are no longer fully saturated, which impairs the output drive current capability and capacitance, causing additional I/O buffer's dynamics and waveform distortion. This problem is recognized by the IBIS committee since the circuit's simulation leads to inaccurate results [57]-[62], which is mainly due to the mixed-mode implementation algorithm of the model that relies on the time juxtaposition of predefined timing signals.

This work presents the first solution to the correct simulation of digital devices subject to overclocking conditions, proposing and validating a new two-port I/O buffer's behavioral model. The adopted modeling methodology follows the physics-based approach to efficiently construct a table-based empirical model for the driver's input port that captures the nonlinear dynamic behaviors of the pre-driver logic stage, this way complementing the existing output port's analog part. The developed two-port

model can be understood as an extension of the IBIS in the model format, its extraction and the implementation algorithms. For achieving this, the outcome of an overclocked IBIS model is discussed and the physical mechanisms causing its failure are identified and thoroughly analyzed. Then, the two-port behavioral model formulation and its function's extraction procedure are described. In addition, the implementation details and the validation results for assessing the performance of a high-speed digital link are presented.

3.5.1 IBIS Model in Overclocking Conditions

As described in the previous chapter, the standard two-piece implemented behavioral model structure, which is shared by the state-of-the art models to capture the I/O buffers' behavior, is (2.17). The various implementation alternatives of the one-port's large signal currents, $i_L(.)$ and $i_H(.)$, can be achieved using equivalent-circuit macro-models, artificial neural networks (ANNs) [28]-[32], or directly by means of LUTs [25], [52]-[53]. On the other hand, the StIDFs – that encapsulate all the nonlinear dynamic behavior associated to the pre-driver's stages are loaded and stored as time dependent files in the simulator. Based on the elementary analog StIDFs, the signals that represent the input bit pattern are processed in real-time by a state machine algorithm implemented in the simulator (e.g. analog mixed signal language) or computed offline to scale the output currents as illustrated in Figure 3.20.

Because the StIDFs are only dependent on the present input state transition, regardless of any previous ones, this implemented mixed-mode behavioral model assumes time concatenation of the successive transients determined by the different input state transitions. That is, since any posterior state transition should only appear after the I/O buffer has reached its steady-state, this modeling strategy is condemned to fail when the buffer is overclocked.

In order to illustrate these negative overclocking effects on the IBIS model, a 0.25µm non-inverting CMOS driver (power supply: $V_{ss} = 0\ V; V_{DD}$ =3.3V), in which the transistors are described by the BSIM3v3 model [2], is considered. According to the specification, this device operates up to a 270 Mbps data rate (*DR*). The IBIS behavioral model was extracted according to the procedure determined in [14]. The usual channel reflection simulation setup shown in Figure 3.37 is used to compare the far-end voltage waveforms, $v_{far-end}(t)$, predicted by IBIS and the TL model in both normal and overclocking operation conditions.

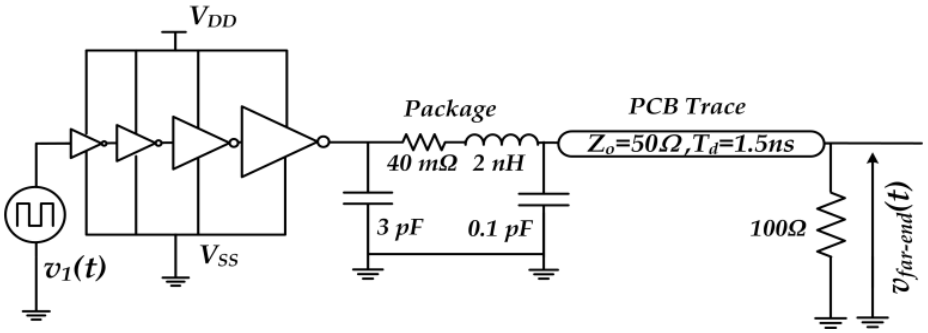

Figure 3. 37. SI evaluation setup for IBIS model under overclocking conditions.

The results of both models are shown in Figure 3.39 when the buffer is driven by the bit pattern "010101000" with equal rise/fall times $t_r = t_f = 1ns$. As seen in Figure 3.38.(a) there is a good agreement between the IBIS and the TL model responses. However, as the device is overclocked (the data rate has almost doubled) the IBIS model's response starts to deviate from the reference model and thus fails to produce accurate results as shown in Figure 3.38.(b).

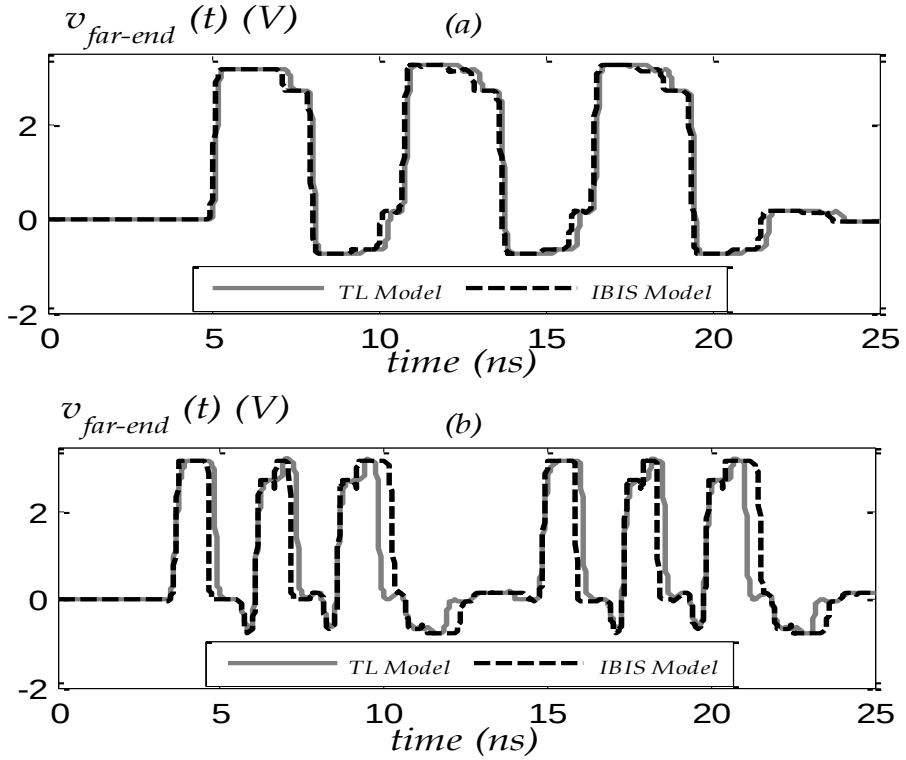

Figure 3. 38. Comparison between the $\boldsymbol{v_{far-end}(t)}$ of the IBIS and TL models. (a) normal operation at a bit-rate of DR=350 Mbps and (b) overclocking operation at DR=800 Mbps.

As expected, the cause of this model failure is due to the *if…then* structure of the AMS algorithmic processing which builds the IBIS output as a succession of the same elementary analog StIDFs, regardless of their separation in time [57]-[58]. Besides, each simulator differs in how they handle turn-on/turn-off timing, even with correctly timed IBIS waveform data [59]-[62]. In addition, this *if…then* algorithmic structure generates

discontinuities in the analog waveforms, which may induce convergence instability in the time-step integration simulator. To prevent these instabilities, smoothed transitions of analog variables must be used and, if possible, digital events should be slightly shifted in time [62], [64].

Based on these observations and analysis, we concluded that the previous modeling methodologies suffer from inaccuracy and convergence issues in overclocking condition and that this is mainly due to the fixed IBIS model format adopted for its StIDF timing signals. So, in the following sections is presented a two-port behavioral model's formulation and extraction procedure that, no longer relying in pre-determined timing signals, but capturing instead the actual input associated nonlinear dynamics, is thus capable of correctly accommodating successive input digital transitions, regardless of their time separation.

3.5.2 Proposed Two-Port Behavioral Model

❖ Model Formulation

Based on TL simulations and StIDFs' computation [11]-[15], we have realized that the intrinsic I/O buffer and the pre-driver's responses under step excitation have an over damped monotonic response as shown in Figure 3.39. According to the output buffer's stages arrangement (see Figure 3.37), there are mainly three physical mechanisms responsible for this behavior. Firstly, there is the static behavior of the nonlinear voltage-current transfer characteristics, $i_H(v_g)$ and $i_L(v_g)$, of the last stage's PU and PD network, respectively. The second interaction to consider is the memoryless nonlinear voltage-current $i_{g,L}(v_1)$ and $i_{g,H}(v_1)$ characteristics of the pre-driver's stage PU and PD devices, respectively. Finally, there is the linear dynamics due to the low-pass characteristics of the pre-driver's controlling logic gates and the loading gate-source capacitor of the large transistors of the buffer's last stage.

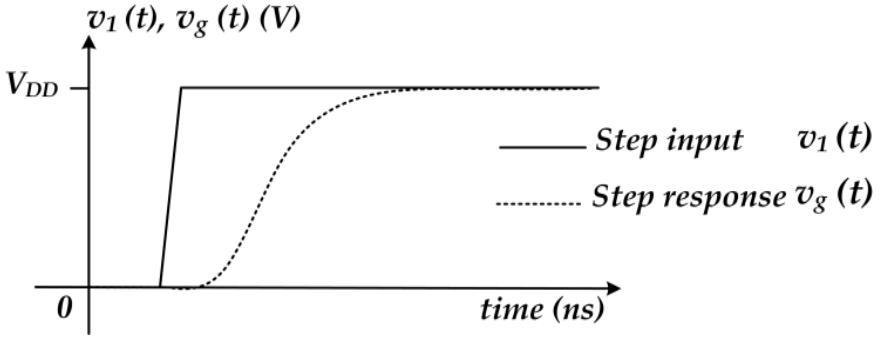

Figure 3. 39. Step response characteristics of the pre-driver stage.

Based on these observations and physical operation analysis, the constructed two-port model is an analog behavioral description of the nonlinear dynamic characteristics of the driver's input and output port. In fact, instead of the IBIS algorithmically processing of fixed elementary StIDFs, a physics-based nonlinear dynamic behavioral model of the driver's input port is proposed as represented in Figure 3.40. This new model allows to continuously and accurately predict the gate signals that control the activation of the upper and lower devices of the buffer's output port.

Accordingly, the driver input behavioral model's diagram consists of the cascade of three blocks corresponding to the above mentioned three physical mechanisms. First, the input signal passes through the nonlinear static pre-driver's functions $T_j(.)$. Then, the linear dynamic filter transfer functions $H_j(.)$ that capture the dynamics of the output stage's gate-voltage behavior:

$$\begin{cases} v_{z,j}(t) = T_j\big(v_1(t)\big) \\ v_{g,j}(t) = \int_0^t h_j(\rho) v_{z,j}(t-\rho) d\rho \end{cases} ; j = L, H \qquad (3.16)$$

where h stands for the filter's impulse response. This filter simulates the voltage that controls the activation of the driver's last stage in which the I-Q model is used to capture the output port nonlinear dynamic effects for a fixed input logic state. Finally, the static gate nonlinearity functions $G_j(.)$ that control the upper and lower devices' output currents complete the model

$$\begin{aligned} i_2\left(v_g(t), v_2(t)\right) = G_L\left(v_{g,L}(t)\right) i_L\left(v_2(t), \frac{dv_2(t)}{dt}\right) \\ + G_H\left(v_{g,H}(t)\right) i_H\left(v_2(t), \frac{dv_2(t)}{dt}\right). \end{aligned} \qquad (3.17)$$

The procedures to extract the three blocks of the proposed model for the driver's input behavior will be described as follows.

❖ Last Stage Gate Functions' Identification

The large signal voltage-current characteristics, $i_H(v_g)$ and $i_L(v_g)$, are extracted through dc voltage sweeps of the gate voltage, v_g, while the dc output node, v_2, is successively connected to the power supply V_{SS} or to the ground V_{DD}, respectively, as shown in Figure 3.41.

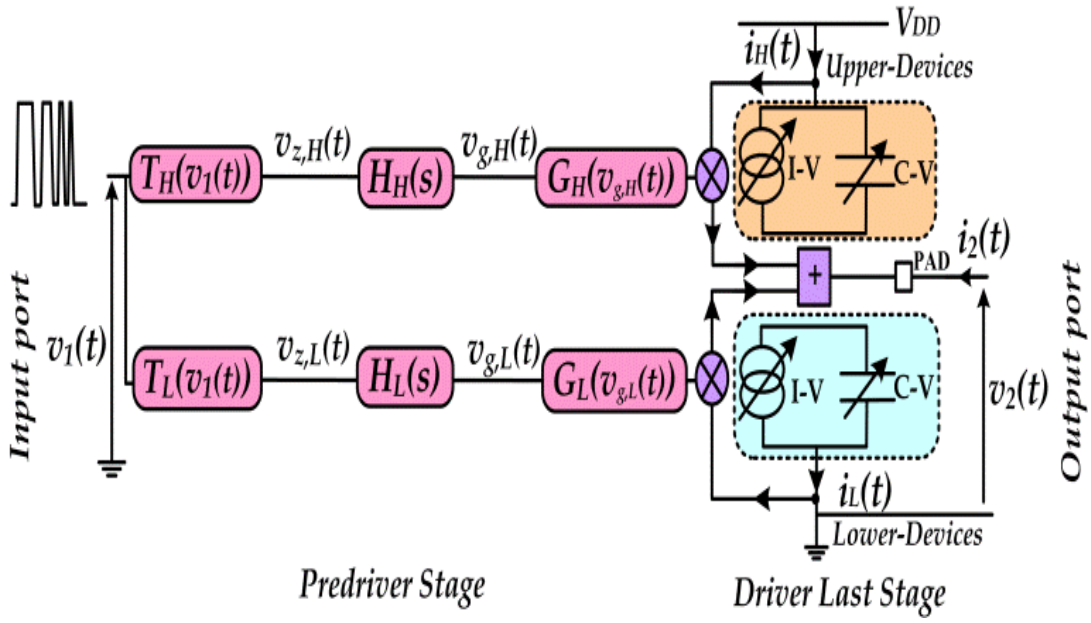

Figure 3. 40. Two-port circuit implementation of the digital output buffer.

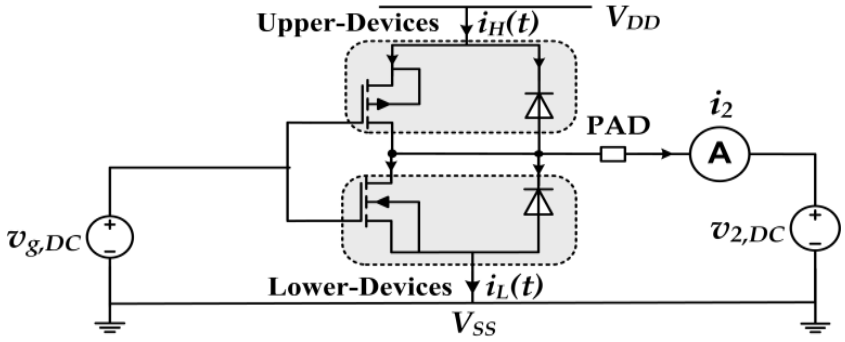

Figure 3.41. Driver's last stage simulation setup for the voltage-current gate effect identification.

In order to have a consistent model formulation for the output port that describes the PU and PD transistors' behavior, the identified nonlinear gate effect of the driver's last stage functions are normalized to generate dimensionless outputs such as:

$$\begin{cases} G_H(v_g) = \dfrac{i_H(v_g, v_2 = V_{SS})}{i_H(v_g = V_{SS}, v_2 = V_{DD})} \\ G_L(v_g) = \dfrac{i_L(v_g, v_2 = V_{DD})}{i_L(v_g = V_{DD}, v_2 = V_{SS})} \end{cases} . \tag{3.18}$$

The single-valued functions $G_j(.)$ can be fitted by ANNs using various basis functions such as the Gaussian, the sigmoid, etc., or can be directly implemented as LUTs.

❖ Pre-driver's Model Functions' Identification

As explained by the physical mechanisms, the adopted model for the pre-driver must have a static nonlinearity followed by a linear filter, the structure known as the

Hammerstein two-box is shown in Figure 3.42. Thus, the model extraction consists in identifying the normalized $T_L(.)$ and $T_H(.)$ nonlinearities and the linear filter characteristics $H_L(s)$ and $H_H(s)$ for the lower and upper pre-driver networks, respectively.

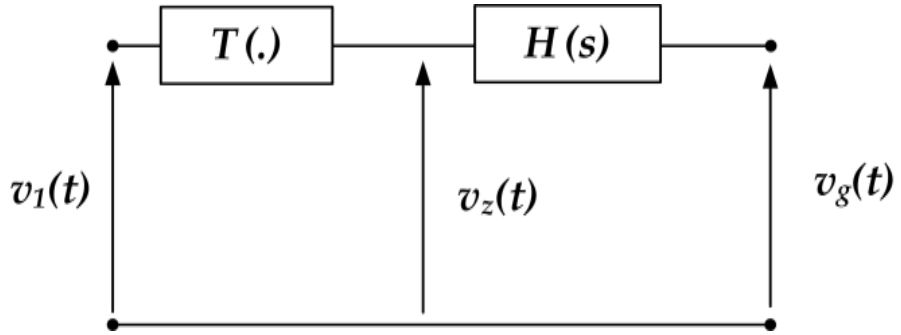

Figure 3. 42.System's representation of the Hammerstein model of the pre-driver's stage.

Firstly, the voltage-current's functions are identified via dc sweeps of the input voltage v_1, recording the output current $i_{g,L}(.)$ and $i_{g,H}(.)$ while the load dc voltage source, $v_{g,DC}$, is connected to the power supply V_{DD} and to the ground V_{SS} , respectively, as shown in Figure 3.43. Then, the $T_j(.)$ nonlinear functions are obtained by normalizing the voltage-current functions, $i_{g,j}(.)$, with respect to the saturation current, as described in (3.18). They exhibit a very narrow transition zone and can be implemented as ANNs or LUT models.

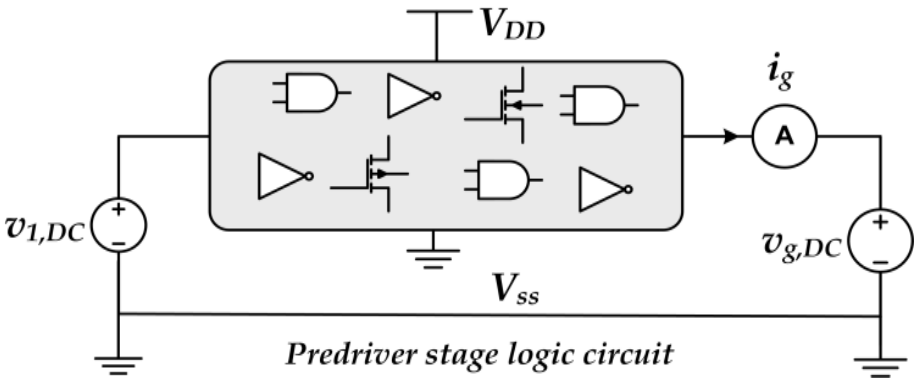

Figure 3. 43. Simulation setup for the identification of $T_L(.)$ and $T_H(.)$.

Secondly, the parameters describing the finite impulse response of the filters that will reflect the monotonic step response of the pre-driver stage circuit are extracted. In fact, the transient data used for the filter identification can be obtained from the StIDFs calculated by linear inversion for up and down transitions (3.4) or by recording the input-output identification signal for a step excitation, while the load V_{DC} voltage is connected to the power supply V_{DD} or to the ground V_{SS}, as shown in Figure 3.44.

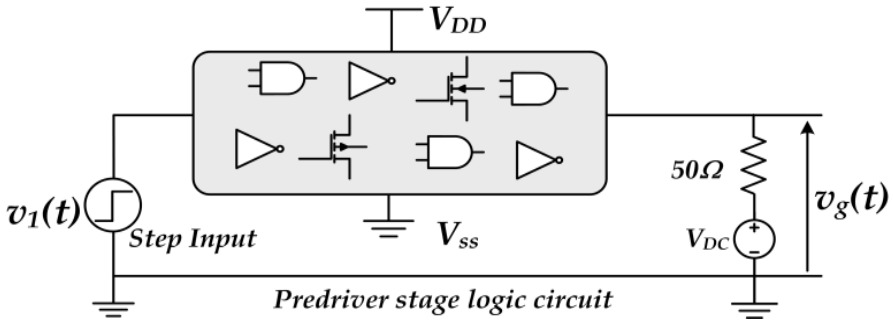

Figure 3. 44. Simulation setup for recording the transient identification signal for the filter parameters estimation.

As seen in Figure 3.40, the pre-driver's step response has a low pass characteristic over a time delay, **σ**, between the input and the pre-driver's transitions. This observed delay can be physically explained by considering a set of *m* cascaded inverters and logic gates, where each one behaves as a low pass filter. In such a case, the smaller time constants work together to produce a lag that acts as a pure dead time [65]

$$e^{-\sigma s} = \lim_{m\to\infty} \frac{1}{\left(1+\frac{\sigma}{m}s\right)^m} \tag{3.19}$$

Therefore, the behavior of this element can be determined by the dc gain of the filter, k_o, and the combination of a dead time, σ, and an apparent time constant, τ, used as the first order approximation for its low pass filter behavior (i.e., we simply assume a resistive path feeding the large C_{gs} input capacitance of the driver's last stage). These physical effects can be accurately captured by the first order plus dead time (FOPDT) model whose Laplace transfer function is

$$H(s) = \frac{V_g(s)}{V_z(s)} = \frac{k_o e^{-\sigma s}}{1+\tau s}. \tag{3.20}$$

Both the graphical method based on engineering heuristics and the evolved statistical method based on the least-squares can be used to estimate the FOPDT parameters. In the first case, the static gain k_o is obtained from the steady state of the observed I/O data. The interception of the tangent to the step response that has the largest slope with respect to the horizontal axis gives the value of the delay σ. The time constant τ is determined from the difference between σ and the time when the step response reaches the value of 0.63 k_o [64]. This method is simple but quite sensitive to large measurement noise [65]. The least-squares estimation of the filter's parameters can outperform this identification method and is more resilient to measurement noise.

The basic idea is to formulate the model so that linear regression can be used to evaluate the filter's parameters. By differentiating the $V_g(s)$ response of (3.20) to a step ($V_z(s) = 1/s$), with respect to the complex frequency, s, we obtain:

$$(\tau s^2 + s)\sigma V_g(s) + (2\tau s + 1)V_g(s) + (\tau s^2 + s)\frac{dV_g(s)}{ds} = 0 \quad (3.21)$$

The division by s^2 of (3.21) allows the elimination of all time-domain differentiations of $v_g(t)$. So, the inverse Laplace transform of (3.21) yields [66]:

$$m_1(t)\tau + m_2(t)\sigma + m_3(t)\theta = m_4(t) \quad (3.22)$$

where the auxiliary variable $\theta = \tau\sigma$, and the signals $m_i(t), i = 1,2,3,4$ are defined by

$$\begin{cases} m_1(t) = 2\int_0^t v_g(l)dl - tv_g(t), \\ m_2(t) = \int_0^t v_g(l)dl, \\ m_3(t) = v_g(t), \\ m_4(t) = -\int_0^t \int_0^l v_g(q)dqdl + \int_0^t lv_g(l)dl. \end{cases} \quad (3.23)$$

By collecting all the signals of at time instants $0, T_s, \ldots nT_s$, where $(n+1)$ is the number of samples, it is possible to write (3.23) as a system of linear equations $\Psi X = \Upsilon$, where $X = [\tau \quad \sigma \quad \theta]^T$

$$\Psi = \begin{bmatrix} m_1(0) & m_2(0) & m_3(0) \\ m_1(T_s) & m_2(T_s) & m_3(T_s) \\ \vdots & \vdots & \vdots \\ m_1(nT_s) & m_2(nT_s) & m_3(nT_s) \end{bmatrix} \quad (3.24)$$

$$\Upsilon = \begin{bmatrix} m_4(0) \\ m_4(T_s) \\ \vdots \\ m_4(nT_s) \end{bmatrix}. \quad (3.25)$$

The model's parameters are then extracted from the estimate $\hat{X}$ of X using the least-squares method as [67]

$$\hat{X} = (\Psi^T\Psi)^{-1}\Psi^T\Upsilon. \quad (3.26)$$

The referred noise sensitivity is avoided using the linear regression of (3.26). This only involves the identification of the time constant, τ, and the delay, σ, from the set of

equations (3.23), which are based on integrations of the output signal during the observation time. Although, it may seem to be a fair assumption to apply the same extracted parameters for $T_L(.)$ and $T_H(.)$, and for $H_L(s)$ and $H_H(s)$, it is better to repeat the identification process for each of these parameters because the predriver circuit usually does not present a symmetric behavior for the high and low states.

3.5.3 Model's Computational Complexity

While the recursive and direct models' formulation of ANNs and memory polynomials [8]-[11] demonstrate that it is possible to approximate the driver's last stage's nonlinear dynamic behavior with a given dynamic order or number of basis functions, the computational complexity of the adopted behavioral modeling strategy is worth to be analyzed.

In this study, the computational cost of the proposed model is determined by the number of calculations that is performed at each time step, when the implemented model is simulated within the CAD tool. For that, the number of floating point operations (FLOPs) is used as a metric to evaluate the number of additions, subtractions, and multiplications, as shown in the operation-FLOP conversion of Table I. Indeed, the number of FLOPs is sufficiently accurate to make a fair evaluation of the computational complexities of behavioral models [26].

Table 3.5 Number of FLOPs for Different Operations [45]

Mathematical Operation	Number of FLOPs
Delay	0
Addition	1
Multiplication	1
Derivative	2

An efficient computational table-based I-Q behavioral model implementation, for the driver's last stage upper and lower devices, with a reduced number of FLOPs, is presented in [52], [53]. The adopted LUT alternative not only reduces the memory used for storing the coefficients of the nonlinear models (i.e. ANNs or polynomial expansions) as it also reduces the computational cost by using a less number of FLOPs in generating the signal from nonlinear stored LUT functions. For instance, in the case of linear interpolation, 2 FLOPs are required to generate the signal from the nonlinear function. However, 11 FLOPs are required to generate the signal from a third order

polynomial function [12]. In general, the complexity of a nonlinear dynamic behavioral model can be written as the sum of the nonlinear function and filter complexities.

$$C_p = C_{NLF} + C_F. \tag{3.27}$$

where C_p represents the behavioral model's total complexity, C_{NLF} and C_F represents the nonlinear function and filtering complexities, respectively.

Based on the model formulation and the operation-FLOP described in Table I, the number of FLOPs of the two-port behavioral model is calculated. In fact, the upper horizontal branch of the model described in (3.16) and (3.17) presents 4 nonlinear functions implemented as LUT which are linearly interpolated. Therefore the C_{NLF} for the model two branches is 16 FLOPs. In addition, the filter complexity depends on the memory length M of the finite impulse filter (FIR) implemented as FOPDT filter. For instance, a FIR filter with memory length *M* requires *M* multiplication and *M-1* addition [45]. Taking in consideration the derivative operator required for the I-Q model's formulation of the output port [7], the C_F of the model is equal $4 * M + 2$ FLOPs.

Since the formulation of (3.17) presents a multiplication between the predicted signals issued from the pre-driver's stage and the driver's last stage and due to the addition between the I-Q model's functions [52] and the addition between the two branches, the total complexity, C_T, of the implemented behavioral model is

$$C_T = C_p + 5 = 4 * M + 23 \tag{3.28}$$

The model's total FLOPs is in the same order of the IBIS's required FLOPs [14] and it is significantly less demanding in computational resources than the previous non-linear parametric approaches [28], [32], in both simulation time and allocated memory .

3.5.4 Model Implementation and Validation

In this section, the performance of the proposed model is evaluated in the context of the characterization of a commercial high-speed non-inverting and single-ended CMOS output buffer from Austria Microsystems. The BU1P_3B is a 0.35µm technology driver from c35 IOLIB cells (power supply: $V_{ss} = 0\,V; V_{DD} = 3.3\,V$). This device operates at 270 Mbps (maximum switching frequency specified by the vendor). The simulation of this driver's TL model will be used for the two-port behavioral model generation as well as for constructing the reference curves necessary for the model validation. Moreover, the IBIS model for this driver is extracted according to its

specification [25] and it is implemented in the ADS simulator using the IBIS signal integrity component.

❖ Model Extraction and Implementation

Firstly, the large-signal output port characteristics $i_L(.)$ and $i_H(.)$, for fixed input logic levels, are extracted as explained in [53]. In fact, they consider single-valued I-V and Q-V functions for the drivers' last stage PU and PD networks. Then, the nonlinear voltage-current of the driver's last stage $G_L(.)$ and $G_H(.)$ as well as the pre-driver's stage $T_L(.)$ and $T_H(.)$, are extracted following the previous section's description, resulting in the characteristics shown in Figures. 3.45 and 3.46.

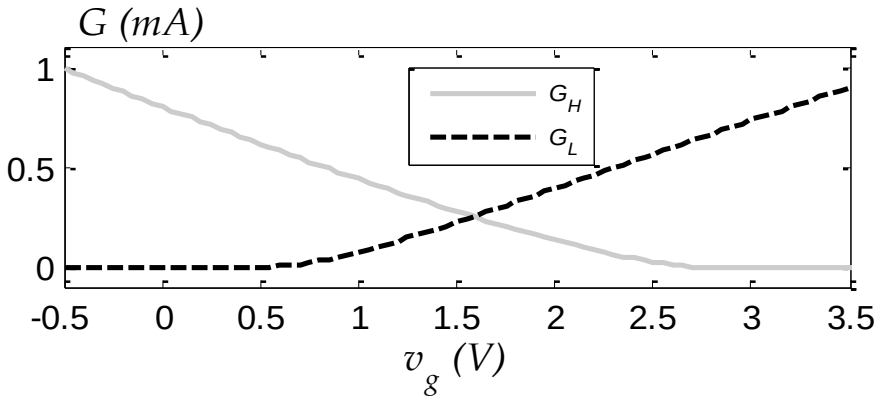

Figure 3. 45. Nonlinear voltage-current functions for the output port PU and PD networks.

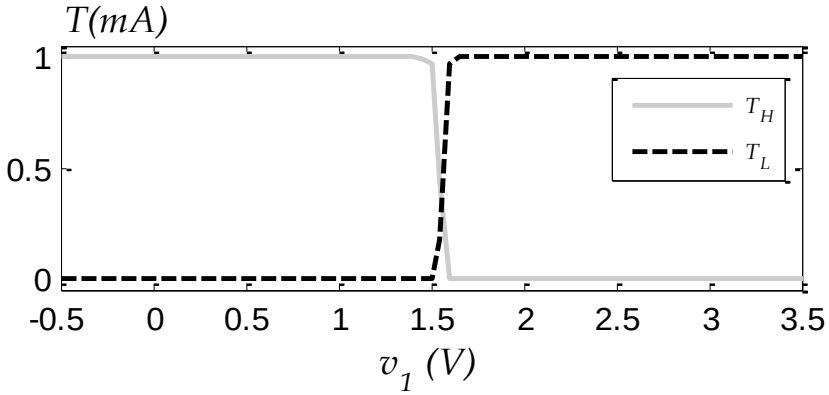

Figure 3. 46. Nonlinear voltage-current functions for upper and lower pre-driver's stage.

The highly nonlinear predriver's functions present a sharp transition at 1.65 V. This confirms that it is converting the input voltage into an output square wave-like waveform regardless of the input voltage waveform shape. This is a consequence of the high voltage gain during the switching operation, when both NMOS and PMOS transistors are simultaneously on, and in saturation. Now we move to the parameters' extraction of the FOPDT filters, which are implemented as the low-pass RC filters shown in Figure 3.47.

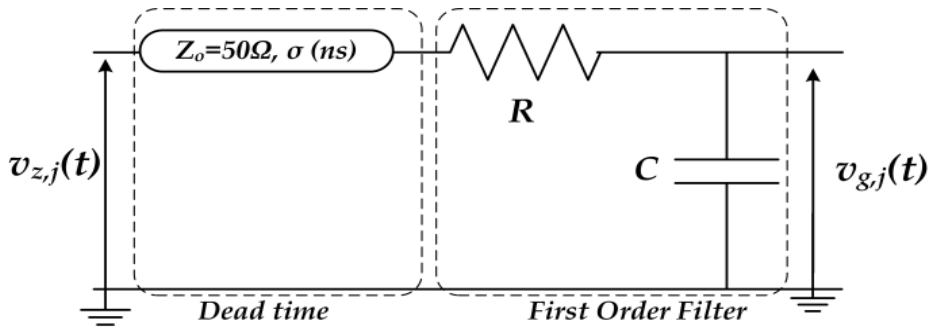

Figure 3. 47. Circuit implementation of the FOPDT filters.

The dead time can be inserted directly in the random bit sequence source, or using an ideal transmission line in which the delay is equal to the filter's dead time. The last alternative was the adopted implementation in the considered output buffer example. The values of the resistance *R* and capacitor *C* were set to verify the estimated time constant τ equals the product *RC*. For the buffer under test, the extracted filter parameters were: steady-state gain $k_{o,H}$ =$k_{o,L}$=1; dead times σ_H=0.772 ns, σ_L =0.791 ns, and time constants τ_H=0.116 ns, τ_L=0.118 ns.

❖ Model Simulation and Validation

The validation test consists of the crosstalk simulation setup depicted in Figure 3.48. It will highlight both the model prediction for the active channel reflection (on PCB trace #1) and the importance to construct an accurate nonlinear dynamic buffer output admittance model to predict the propagated signal into the coupled quiet channel (on PCB trace #2).

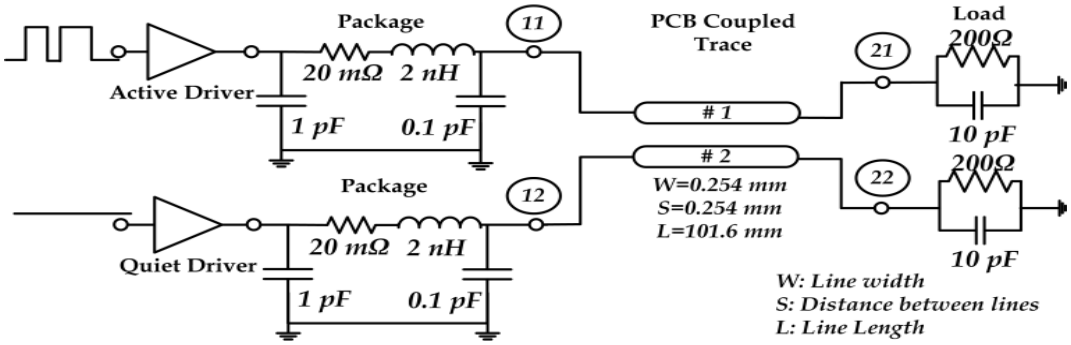

Figure 3. 48. Crosstalk simulation setup used for the two-port behavioral model validation.

Moreover, in order to assess the prediction performance of each behavioral model, qualitative visual inspection and the quantitative NMSE metric will be used as waveform similarity assessments. The validation procedure considers the simulation of the implemented model for boundary conditions that were never tested during the model extraction procedure, for three different test cases described in the following text.

Test Case 1: As a first test the buffer was driven in normal operation by a bit sequence at the input v_1 with data pattern "011001010", data rate *DR*=300 Mbps and with equal rise and fall times of $t_r = t_f = 0.5ns$. The obtained waveforms are shown in Figure. 3.49 and the numerical performances are reported in Table 3.6. Figure 3.50 clearly shows a very good agreement between the two-port behavioral model and the TL simulation. Also, there is only a slight visual difference between the IBIS results and the developed model, although the improvement in NMSE was about 13 dB. In terms of computational efficiency, it was observed an improvement factor on the order of 12 with respect to the TL model.

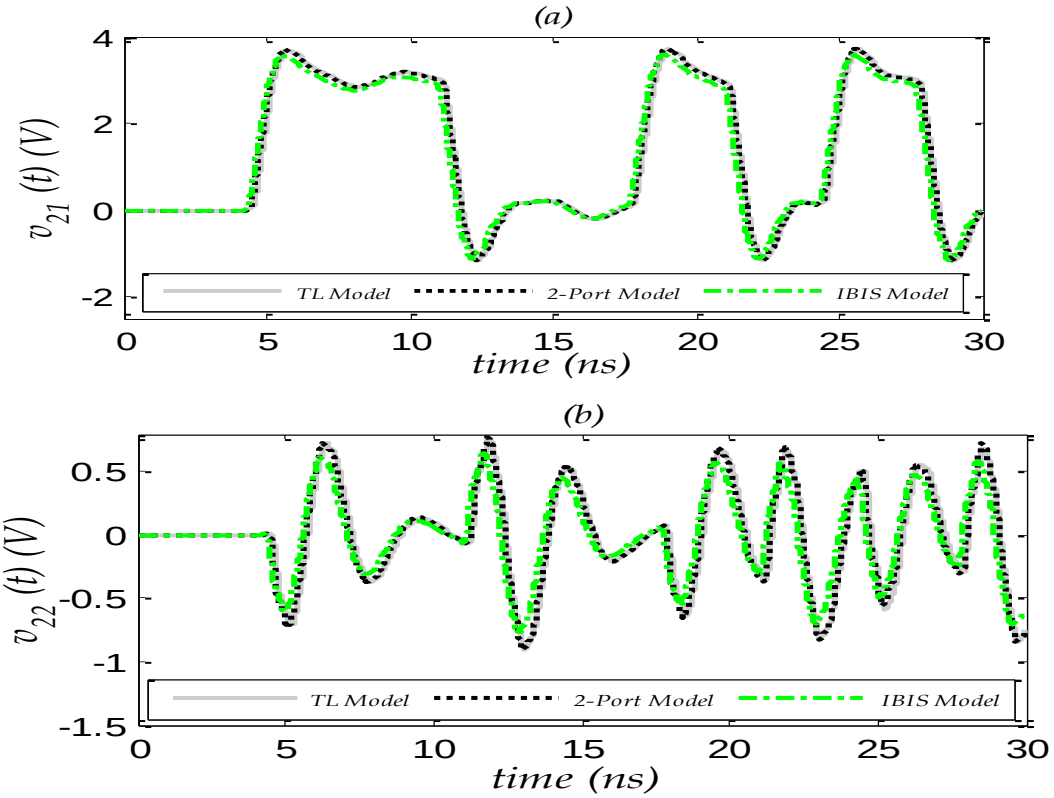

Figure 3. 49. Validation of the two-port behavioral model for the test case #1, (a) $v_{21}(t)$ on PCB trace #1 and (b) $v_{22}(t)$ on PCB trace #2.

Table 3. 6. Performance of the behavioral model's simulation of the test case #1.

Model	$NMSE_{v_{21}}$ (dB)	$NMSE_{v_{12}}$ (dB)	CPU time (s)
TL	-	-	74
Two-Port	-37.42	-47.94	5.32
IBIS	-24.31	-31.15	4.64

Test Case 2: in the second test the input excitation is a bit sequence with the same data pattern "0110010100", but now *DR*=800 Mbps and $t_r = t_f = 1ns$. During the transient IBIS model simulation in this overclocking condition two warning messages

appear in the simulation window saying: "A falling IBIS trigger happens in the middle of a rising transition" and "A rising IBIS trigger happens in the middle of a falling transition". The resulted waveforms are shown in Figure 3.50 and the simulation performances are quantified in Table 3.7.

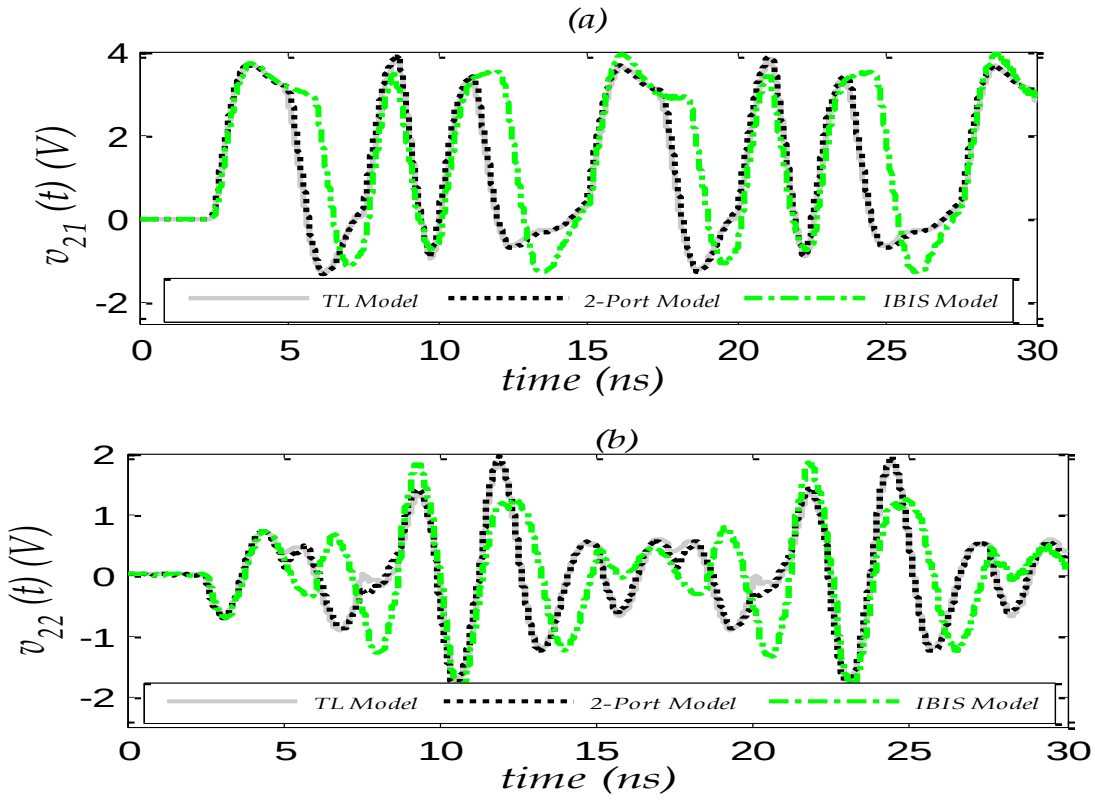

Figure 3. 50. Validation of the two-port behavioral model for the test case #2, (a) $v_{21}(t)$ on PCB trace #1 and (b) $v_{22}(t)$ on PCB trace #2.

Table 3. 7. Performance of the behavioral model's simulation of the test case #2.

Model	$NMSE_{v_{21}}$ (dB)	$NMSE_{v_{12}}$ (dB)	CPU time (s)
TL	-	-	78
Two-Port	-34.47	-40.30	5.42
IBIS	-2.13	-6.73	5.87

The IBIS model now fails to follow the TL waveforms in both the active and quiet channels. The delay errors in this overclocking condition arise from the failure of the IBIS algorithm to compute the exact timing signals that excite the driver's last stage. On the contrary, the proposed two-port behavioral model is still able to provide accurate results. As shown in Figure. 3.51 is the prediction of the controlling gate voltage that switches the driver's output port's model, confirming the high accuracy of the proposed model.

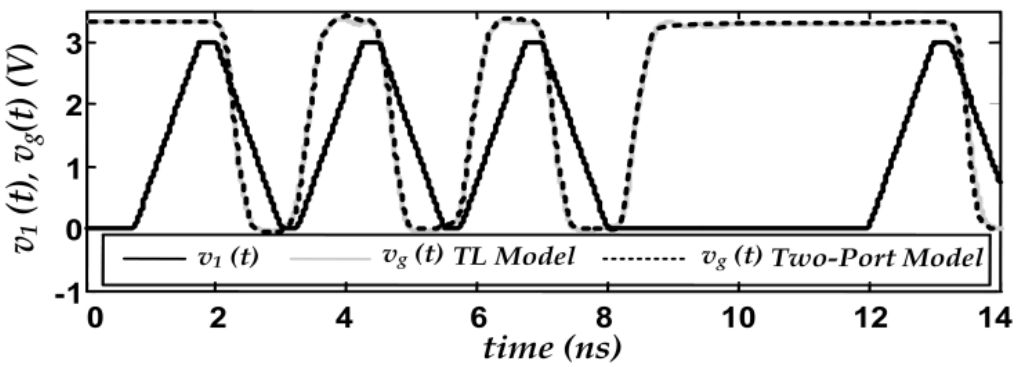

Figure 3. 51. Comparison between the gate voltage waveform of the TL model and the one predicted by the pre-driver's behavioral model for the test case #2.

Test case 3: The aim of this final test is to assess the model accuracy for a 1024-bit-long random input sequence at DR=800 Mbps with a bit duration equal to 1.48 ns. The eye diagram [32] of the far-end voltage waveform on the active channel of Figure 3.48, $v_{21}(t)$, is generated by the TL, the IBIS, and the two-port model, and compared in Figure 3.52. From visual inspection it is clear that the IBIS model fails to predict the channel distortion effects under overclocking operation. However, the comparison between the TL and the two-port I-Q model simulations shows a high correlation.

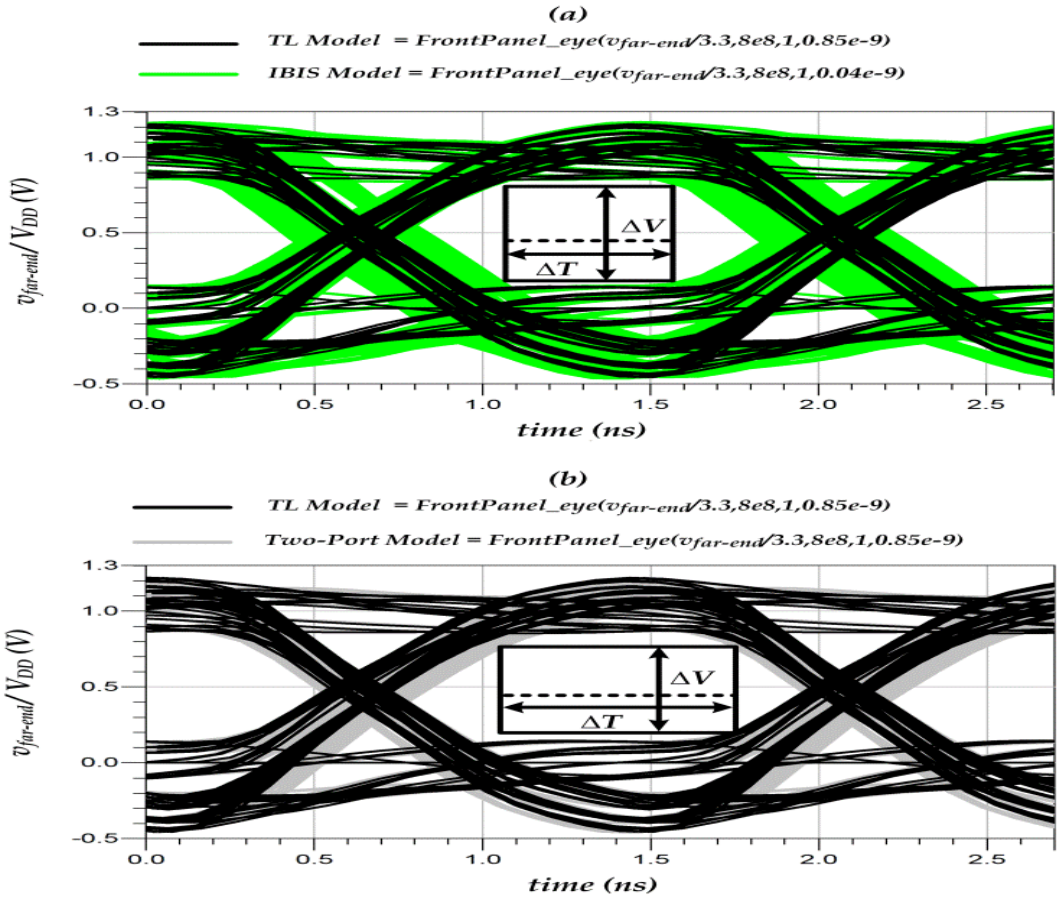

Figure 3. 52. Eye diagram derived from the $v_{21}(t)$ waveform of Figure 3.49 and the definition of the eye opening parameters ΔV and ΔT.

This is confirmed by computing the eye width aperture ΔT for various eye height opening ΔV to quantify the error in the eye opening introduced by the IBIS and the two-port behavioral model. The corresponding scatter plot is shown in Figure 3.53. The error in the eye diagram openings resulting from the two-port model is almost within 3% from that of the TL model, however, it reaches 11% in the IBIS model for the simulation of the entire input bit sequence. Finally, Table 3.8 shows a comparison of CPU time required by the Spectre simulator in Cadence and the implemented two-port behavioral model in ADS, when the output buffer is driven by the 1024 bit sequence.

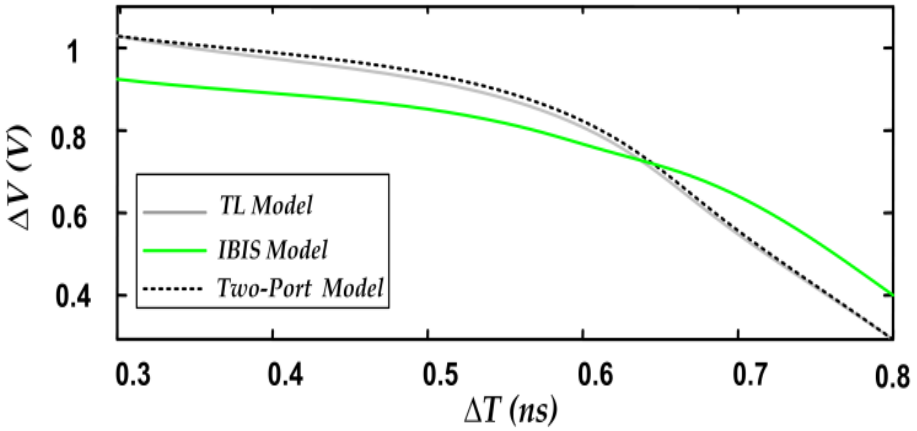

Figure 3. 53. Eye opening parameters of the waveform $v_{21}(t)$ for the TL , IBIS model, and two-port behavioral model.

Table 3. 8. Computational efficiency of the model's simulation of the test case #3.

Model	CPU time
TL	18.66 min
Two-Port	46.27 s
IBIS	41.19 s

These validation examples demonstrate that the implemented two-port model is general and accurate, indeed resolving the modeling difficulties of previous modeling approaches under overclocking conditions, without compromising the computational efficiency. As indicated by the CPU time results of Tables 3.6 to 3.8, the efficiency improvement factors introduced by the two-port behavioral model, with respect to the full TL model, are still on the order of 10 to 25 , if multiple buffers are simultaneously simulated, or whenever long bit streams are simulated for assessing the high-speed channel perform.

3.5.5 Summary

The new developed two-port behavioral model formulation, along with its extraction procedure and implementation, provides a general, accurate and reliable simulation alternative for the digital I/O buffer in normal and overclocking conditions.

The identification of the nonlinear dynamic input port functions that capture the behavior between the digital input signal and the gate voltage controlling the driver's last stage substitute the concatenated fixed StIDFs of the previously published approaches for the buffer's behavioral model. The resulting general model can be seen as a physics-based refinement of this modeling methodology within which stands the industry-standard IBIS model. Moreover, this is accomplished without exposing in the model any specificity of the buffer circuit implementation, thus protecting the industrial property of the buffer manufacturer.

As was demonstrated by the validation examples, the implemented model overcomes the accuracy limitations that the IBIS (and other parametric approaches that rely on the concatenation of fixed StIDFs) suffer in the SI assessment in an overclocked high-speed digital link. Furthermore, the proposed gray-box model did not introduce any significant increase in CPU and memory resource consumption when compared to its behavioral models predecessors.

CHAPTER IV:

Conclusions and Future Work

The objective of this research work was to a create a reduced-order and physically inspired black-box model for any TL driver circuit by taking into account the prior knowledge of the driver's physical properties and internal circuitry design. These properties are reflected in the behavioral model generation algorithm at the construction and the extraction steps in order to optimize the model's identification and running complexities. The generated driver's behavioral models run faster and consume less CPU memory compared to driver's TL driver's circuits while maintaining high accuracy and do not suffer from any convergence issues when implemented in CAD tools repertoires.

4.1 Conclusions

The physically inspired model's computational cost, stability, and accuracy are the multiple criterions that were selected as started specifications of the developed behavioral models in this PhD work. During the behavioral modeling generation steps, all these factors were considered to construct an optimized behavioral model that provide a general, accurate and reliable SI simulation.

Firstly, the main focus of was to efficiently enhance the one-port driver's last stage behavioral model steps. In fact, an optimized generation procedure for a reduced-order of the nonlinear parametric model's based on equivalent circuit approach and system identification is presented. Then, a new linear least-squares model extraction from time-domain data is developed and measurement-based model is derived from frequency-domain data. In fact, the linear least-squares extraction method outperforms the nonlinear optimization algorithm used in the previous nonlinear parametric modeling approaches [11], [12]. Moreover, the LUTs implementation alleviates the computational complexity associated with the driver's behavioral model identification and implementation steps to capture the overclocking behavior of drive's circuit.

Due to the fact that the parametric black-box models are converted into an equivalent circuit-level representation in order to be implemented and used in the CAD libraries, this serves to highlight that if a physically-based equivalent circuit template

that describes the distortion effects of the device is adopted from an early stage of model generation would be appealing in easing and speeding up the process of identifying and constructing a transparent and accurate model structure.

Nevertheless, both black-box and gray-box approaches have their own strengths and weaknesses in the modeling generation steps. We have investigated the optimization of each approaches by merging the features of each methodology in order to generate an efficient behavioral model that improve the industry standards IBIS for I/O buffer simulations.

4.2 Future Work

The developed gray-box two-port behavioral models should be extended to multiple ports to capture the effect of power and ground bouncing voltages on the driver output signal. Capturing these relations can lead to the accurate modeling of nonlinear and memory effects caused by the SSN when multiple drivers are switching.

Modern high-speed digital I/O interfaces have turned to low-voltage differential signaling (LVDS) because of their numerous advantages over single-ended signaling. Differential signals have lower voltage swings than single-ended signals. Differential signals have a reduced electromagnetic interference (EMI) effect and crosstalk coupling. A modeling methodology based on an equivalent-circuit approach that extend the IBIS model structure could be proposed and extracted to model differential drivers with and without the pre-emphasis effect.

A gray-box two model for the mixed signal behavior of the receiver circuits could be proposed (i.e. the input of the receiver is analog in nature and the output is digital). Then the modeling technique could be extended to multiple-ports to include the effect of power supply voltages fluctuations on the receiver input and output characteristics. The accuracy and the computational speed-up of the developed I/O buffer's behavioral models proposed in this future work will be compared to transistor-level circuits for various test cases to accurately capture signal and power integrity distortions such as the case of SSN.

4.3 Publications

✓ IEEE JOURNAL TRANSACTIONS

[1] W. Dghais, T. R. Cunha, and J. C. Pedro "Reduced-Order Parametric Behavioral Model for Digital Buffers/Drivers with Physical Support", I*EEE Trans. on Components, Packaging and Manufacturing Technology*, vol. 2, no. 12, pp. 1-10, Dec. 2012.

[2] W. Dghais, H. M. Teixeira, T. R. Cunha, and J. C. Pedro "Novel Extraction of Table-Based I-Q Behavioral Model for High-Speed Digital Buffers/Drivers", *IEEE Trans. on Components, Packaging and Manufacturing Technology* March 2013.

[3] H. M. Teixeira, **W. Dghais**, T. R. Cunha, and J. C. Pedro "Measurement Setup for RF/Digital Buffers Characterization" I*EEE Trans. on Instrumentation and Measurement*, March 2013.

[4] W. Dghais, T. R. Cunha, and J. C. Pedro "A Novel Two-Port Behavioral Model for I/O Buffer Overclocking Simulation" *IEEE Trans. on Components, Packaging and Manufacturing Technology*, October 2013.

✓ IEEE CONFERENCES

[1] W. Dghais, T. R. Cunha, and J. C. Pedro "Behavioral Model for High-Speed Digital buffer/Driver", *IEEE Integrated Nonlinear Microwave and Millimeter-Wave Circuits*, pp. 110–113, Apr. 2010.

[2] W. Dghais, H. M. Teixeira, T. R. Cunha, and J. C. Pedro "Efficient Table-Based I-Q Behavioral Model for High-Speed Digital Buffers/Drivers" *16th IEEE workshop on Signal and Power Integrity (SPI)*, pp.95-96 May 2012.

[3] W. Dghais, T. R. Cunha, and J. C. Pedro "A Mixed-Domain Behavioral Model's Extraction for Digital I/O Buffers", *21st IEEE conference on electrical performance of electronic packaging and systems (EPEPS)*, Arizona, October 2012.

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