Universidade de Aveiro Departamento de Electrónica, Telecomunicações e Informática
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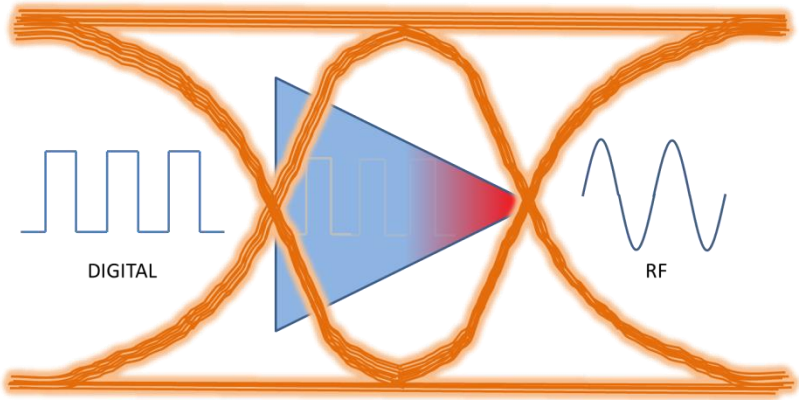
Modelação Comportamental de Dispostivos Não-Lineares (RF-Digital) de Entrada/Saída

Nonlinear Behavioral Modeling of Mixed Signal RF-Digital I/O Devices



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Nonlinear Behavioral Modeling of Mixed Signal RF-Digital I/O Devices

Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Electrotécnica, realizada sob a orientação científica do Doutor José Carlos Pedro, Professor Catedrático do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro e sob a co-orientação científica do Doutor Telmo Reis Cunha, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

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Dedico este trabalho aos meus pais Joaquim e Isabel…por uma vida de sacrifício e dedicação.

o júri

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A todos o meu Muito Obrigado !

palavras-chave

Comportamento não linear, configuração de medição, *buffer* de saída, digital, rádio frequência, modelação, integridade do sinal, integridade do barramento de alimentação.

resumo

Esta tese investiga a caracterização (e modelação) de dispositivos que realizam o interface entre os domínios digital e analógico, tal como os *buffers* de saída dos circuitos integrados (CI).

Os terminais sem fios da atualidade estão a ser desenvolvidos tendo em vista o conceito de rádio-definido-por-software introduzido por Mitola. Idealmente esta arquitetura tira partido de poderosos processadores e estende a operação dos blocos digitais o mais próximo possível da antena. Neste sentido, não é de estranhar que haja uma crescente preocupação, no seio da comunidade científica, relativamente à caracterização dos blocos que fazem o interface entre os domínios analógico e digital, sendo os conversores digital-analógico e analógico-digital dois bons exemplos destes circuitos. Dentro dos circuitos digitais de alta velocidade, tais como as memórias Flash, um papel semelhante é desempenhado pelos *buffers* de saída. Estes realizam o interface entre o domínio digital (núcleo lógico) e o domínio analógico (encapsulamento dos CI e parasitas associados às linhas de transmissão), determinando a integridade do sinal transmitido. Por forma a acelerar a análise de integridade do sinal, aquando do projeto de um CI, é fundamental ter modelos que são simultaneamente eficientes (em termos computacionais) e precisos. Tipicamente a extração/validação dos modelos para *buffers* de saída é feita usando dados obtidos da simulação de um modelo detalhado (ao nível do transístor) ou a partir de resultados experimentais. A última abordagem não envolve problemas de propriedade intelectual; contudo é raramente mencionada na literatura referente à caracterização de *buffers* de saída.

Neste sentido, esta tese de Doutoramento foca-se no desenvolvimento de uma nova configuração de medição para a caracterização e modelação de *buffers* de saída de alta velocidade, com a natural extensão aos dispositivos amplificadores comutados RF-CMOS. Tendo por base um procedimento experimental bem definido, um modelo estado-da-arte é extraído e validado. A configuração de medição desenvolvida aborda não apenas a integridade dos sinais de saída mas também do barramento de alimentação. Por forma a determinar a sensibilidade das quantias estimadas (tensão e corrente) aos erros presentes nas diversas variáveis associadas ao procedimento experimental, uma análise de incerteza é também apresentada.

keywords

nonlinear behavior, measurement setup, output buffer, digital, radio frequency, modeling, signal integrity, power integrity.

abstract

This thesis investigates the characterization (and modeling) of devices that perform the interface between the digital and analog domains, such as the output buffers of the Integrated Circuits (ICs).

Modern wireless transceivers are moving towards the software-defined radio (SDR) concept proposed by Mitola. The ideal architecture makes use of powerful digital signal processors (DSP) and extends the digital blocks's operation as close as possible to the antenna. In this way, it is not surprising that there is a growing concern regarding the characterization of the blocks that perform the interface between the analog and digital domains, being the analog-to-digital and digital-to-analog converters (ADCs/DACs) two good examples of these circuits. Within the high speed digital circuits, such as Flash memories, a similar role is played by the output buffers. They act as an interface between the digital (logic core) and the analog radio frequency domains (package/printed circuit board), determining the signal integrity of the transmitted data. In order to speed up the signal integrity analysis, at the design stage, it is fundamental to have models that are simultaneously computationally efficient and accurate. Typically, the extraction/validation of models for output buffers is performed by using characterization data obtained from either the simulation of the transistor level model (if available) or from measurements. The latter approach is not sensitive to intellectual property issues but is rarely addressed in literature referred to output buffers' characterization.

Therefore, this thesis addresses the development of a novel measurement setup for the characterization and modeling of high speed output buffers, naturally extendable to switched-mode RF-CMOS amplifiers. Based on a well-defined experimental procedure, a state of the art model is extracted and validated. The developed measurement setup addresses not only the integrity of the output signals (signal integrity) but also of the power supply voltages (power integrity). In order to determine the sensitivity of the estimated quantities (voltage and current) to the errors in the different variables of the experimental procedure, an uncertainty analysis is presented.

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List of Acronyms

ADC	Analog-to-Digital Converter
AMS	Analog Mixed-Signal
ANN	Artificial Neural Network
AWG	Arbitrary Waveform Generator
BT	Bias Tee
CAD	Computer Aided Design
CF	Coupling Factor
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
EIA	Electronics Industry Alliance
EM	Electromagnetic
FFIB	Flash Fast Interface Board
FWC	Forward Wave Coupler
GPS	Global Positioning System
IBIS	Input/Output Buffer Information and Specification
IC	Integrated Circuit
IEC	International Electrotechnical Commission
I/O	Input/Output
LS	Large Signal
MM	Memory Module
MOCHA	MOdelling and CHAracterization for SiP – Signal and Power Integrity Analysis
NMOS	N-Type Metal-Oxide-Semiconductor
PCB	Printed Circuit Board

PMOS	P-Type Metal-Oxide-Semiconductor
PWL	Piece-Wise Linear
RBFN	Radial Basis Function Networks
SDD	Symbolic Defined Device
SDR	Software Defined Radio
SFWFTD	Spline Function With Finite Time Difference
SiP	System in Package
SMD	Surface Mount Device
SPICE	Simulation Program With Integrated Circuit Emphasis
SSO	Simultaneous Switching Outputs
SWA	Switching Activity
TL	Transistor Level
VNA	Vector Network Analyzer
WP	Work Package

Chapter 1 - Introduction

Nowadays, modern wireless transceivers integrate an increasing number of functionalities such as: MP3 player, video camera, GPS, etc. In order to obtain a highly reconfigurable terminal, the radio frequency (RF) circuit design paradigm is changing towards the software-defined-radio (SDR) concept proposed by Mitola [1]. The idea is to pass most of the analog functional blocks of the wireless transceiver to the digital (software programmable) domain, pushing the digital blocks as close as possible to the antenna. In this way, it is not difficult to predict that, in the future wireless terminals, the baseband complementary metal-oxide semiconductor (CMOS) and the modern RF-CMOS will be mixed, in an undistinguishable manner, with the digital signal processing blocks. Moreover, the Moore's law continues (surprisingly) to prevail, where a huge number of transistors can be incorporated in a single die. The emergence of the System in Package (SiP) concept, where a single package holds several dies, either in a vertical or horizontal arrangement, is just a consequence of this trend. As an example, Fig. 1.1 presents the constitutive blocks (Digital and RF) of a 1st generation mobile phone. On the right side of the figure, the SiP concept is illustrated for the baseband blocks.

The increasing heterogeneity (mixed-signal) of modern wireless terminals will demand for new computer aided design (CAD) tools. If, on the one hand, this will require more efficient circuit simulation methods [3], on the other hand this will demand for reduced order models, or system behavioral models [4], of both digital and analogue RF circuits. Moreover, for SiP devices, the situation is even worst. The proximity of distinct dies increases significantly the electromagnetic interaction between the several electrical signals propagating through the integrated circuit (IC) lines (traces, bond-wires, …) which causes interference problems that are very difficult to predict (and thus to model) at the design stage of the SiP device.

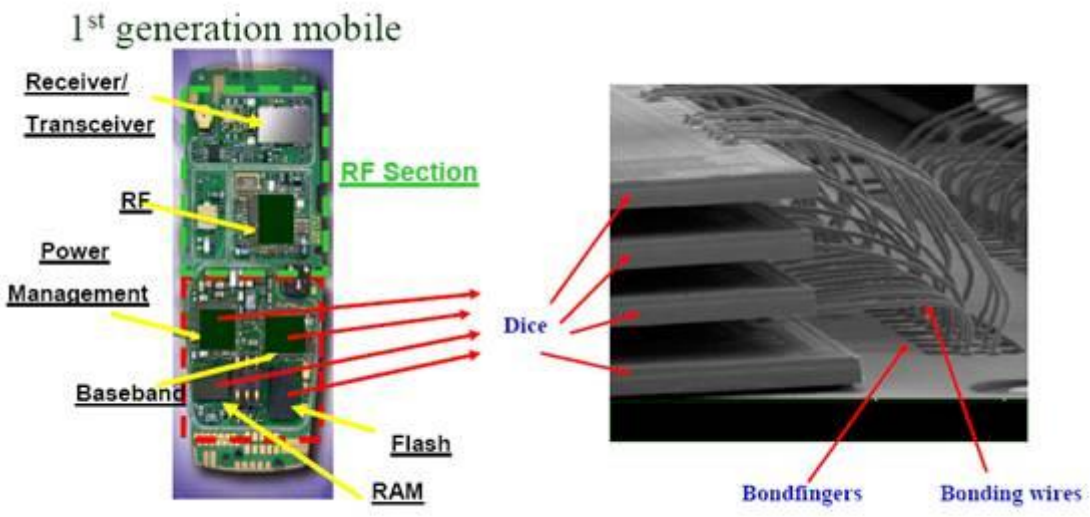

Fig. 1.1 – The 1st generation mobile phones are migrating towards the SiP concept (source: [2]).

From the set of blocks that constitute a wireless transceiver, the RF power amplifier (PA) [5] and the circuits that perform the interface between the digital and analog domains, such as digital-to-analog (DAC) and analog-to-digital converters (ADC) [6], deserve special attention. Within the high speed digital circuits, such as a Flash memory (see Fig. 1.1), a similar role is played by the Input/Output (I/O) buffers [7]. They act as an interface between the digital (logic core) and the analog RF domains (package/printed circuit board), determining the signal characteristics of the transmitted data.

In fact, seen from the analog circuit level point of view, one immediately realizes that there should be no fundamental difference between a high-speed digital CMOS buffer and a class-D push-pull switched mode RF power amplifier when they are both applied to a certain load via the corresponding high-speed interconnect. Therefore, it is expectable that an input/output buffer imposes similar challenges in terms of behavioral modeling representation; behaving as a continuous time/continuous amplitude ("analog") highly nonlinear and dynamic circuit [8], [9].

The I/O buffers' behavior is strongly affected by the poor stabilization of the power supply voltage. In a SiP device, in the worst case scenario, it is possible that all the buffers switch at the same time. In this case of simultaneous switching outputs (SSO) [10], the voltage drop, mainly associated to the long bond wires inductance, may cause several artifacts in the output signal that are difficult to predict, or may even lead to a complete system failure. The majority of the state of the art models for I/O buffers only allow

limited variations of the power supply voltage, on the order of 10-15% of the nominal power supply voltage.

Concerning the extraction and validation of the I/O buffer model, two approaches are normally followed. The characterization data can be obtained from detailed simulations of the transistor level-model (TL model) or from laboratory measured data. However, either because of the possible unavailability of the TL model (usually hidden under intellectual property protection), or of the need to accurately account for the device-PCB mounting parasitics, it is desirable – and thus of recognized importance for the industry – that the model extraction from laboratory measurements is performed on packaged devices.

1.1 Motivation and Problem Statement

As described in the previous section, the trend to mix digital and analog components in telecommunications transmitter/receiver devices determines that the design of such devices needs to simultaneously consider models of digital and analog elements. Naturally, the bottleneck for this digital-analog integration will be in those blocks that perform the interface between the two domains. From the digital domain perspective this role is played by the I/O buffers. Moreover, for SiP devices, the increasing switching frequency, density (two or more dies per package) and power, as well as decreasing size and reduced logic voltage level, make it fundamental to predict (and thus to model), at the design stage, the integrity not only of the output signals but also of the power networks that supply the buffers. The accuracy of the obtained models is strongly dependent on the used characterization data and chosen measurement setup. Nevertheless, the literature referring to the experimental characterization of digital I/O buffers is quite scarce. Moreover, the existing approaches [11], [12], [13] present some drawbacks that limit their use in high speed applications (this issue is discussed in more detail in Section 1.2.4).

The motivation for this thesis was exactly to consider some of the open issues described in the previous section and, in that way, address the laboratory characterization and model extraction of digital I/O buffers. Therefore, the main objective of this PhD work was to develop a measurement setup for the characterization of I/O digital buffers (extendable to other similar architectures as RF-CMOS switched amplifiers) and, in this way, overcome the limitations presented by the state of the art approaches (see next section).

1.2 Characterization of I/O Digital buffers – State of the Art

This section is dedicated to present the state of the art methods for the characterization of I/O digital buffers and their limitations. Since, typically, the final goal of the characterization methods, and correspondent measurement setups, is the extraction and validation of behavioral models, in this section I start by a brief description of the most important behavioral models for I/O digital buffers.

In Fig. 1.2 is presented the schematic of an output buffer interfacing the logic core (digital domain) and package (plus PCB - RF domain). The output buffer assumes an important role by providing the logic core with the capability to drive large off-chip capacitances (package, PCB, and external devices) and, in this way, minimizing the propagation time. Since the output buffer is a nonlinear dynamic device, operating in highly nonlinear regimes, adequate models for its behavior are significantly complex and difficult to extract. In the reception side, a similar interface role is provided by an input buffer. Nevertheless, in what respects signal integrity analysis, it is far more important the study of the I/O buffer as an output device than as an input one, because the signal it generates suffers from the non-ideal behavior of the output buffer circuit, which other ICs will interpret as logical levels. Moreover, the output circuit must supply higher currents than the input circuit (implying larger transistors) and, as a consequence, the impact of the non-idealities of the input buffer are very reduced when compared to those of the output buffer. So, in this section, and in the remaining of this document, only the output buffers are addressed. The modeling of input buffers is well explained in [14] and [15].

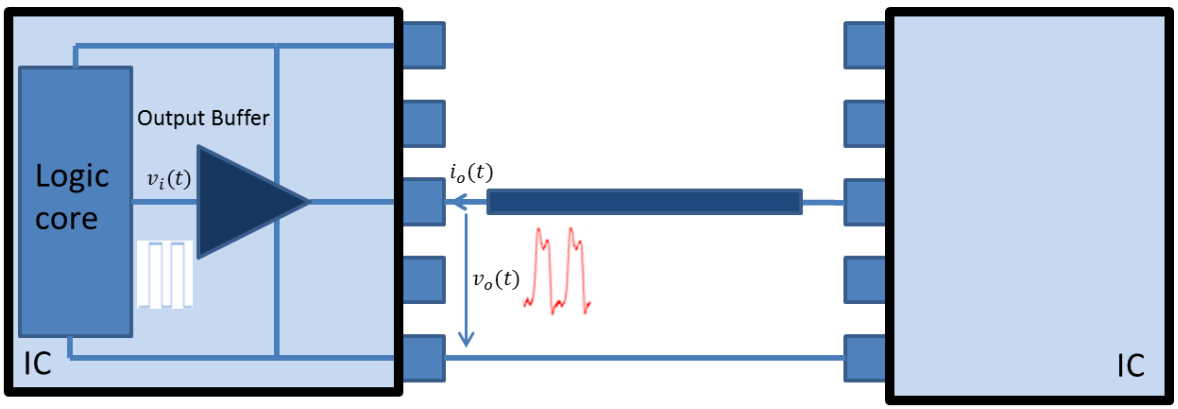

Fig. 1.2 - Output Buffer interfacing the digital and the analogue (RF) domains.

1.2.1 The IBIS Model

The first model to be described is the Input/Output Buffer Information and Specification (IBIS) [16], from the Electronics Industry Alliance (EIA). IBIS is a simple table-based model that describes the electrical characteristics of the digital inputs and outputs of a device through Voltage/Current (V/I) and Voltage/Time (V/T) data without disclosing any proprietary information. The IBIS model can be obtained for three different corners: typical, slow (weakest drive, slowest edge) and fast (strongest drive, fastest edge). These corners are generally determined by the environmental (temperature and power supply) conditions under which the silicon is expected to operate, the silicon process limits, and the number of simultaneous switching outputs.

An IBIS model for output buffers is shown in Fig. 1.3. This model takes into account: DC steady-state I/V characteristics of the pull-up and pull-down transistors, I/V characteristics of the power and ground clamps, die capacitance (C_{die}) and package parameters (R_{bond}, L_{bond} and $C_{package}$). To generate the pull-up and pull-down curves, voltage sources are connected at both the driver input (In) and output (Out). The input voltage source guarantees that only one transistor, type-P Metal Oxide Semiconductor Field Effect Transistor (PMOS) or type-N MOSFET (NMOS) is active at a certain time while the output voltage is swept from $-V_{dd}$ to $2V_{dd}$ (this range accounts for possible reflections in the transmission line that normally loads the output), where V_{dd} is the supply voltage. It should be noted that the pull-down data is relative to GND, whereas pull-up data is relative to V_{dd} since the output current depends on the voltage between the output (Out) and V_{dd}.

Regarding the power and ground clamp curves, these can be generated when the output is in a high impedance state (tri-state). The ground clamp is active when the output is below ground, and the power clamp is active when the output is above V_{dd}. The ground clamp is extracted when the output is swept from $-V_{dd}$ to V_{dd}, while for the power clamp the sweeping range varies between V_{dd} and $2V_{dd}$. These curves have to be subtracted from the pull-up and pull-down data, so that the simulator does not take them into account twice. Note that, for the model of Fig. 1.3, the circuitry necessary to put the device in the tri-state mode is not represented. It is also true that not all devices have this option, which makes

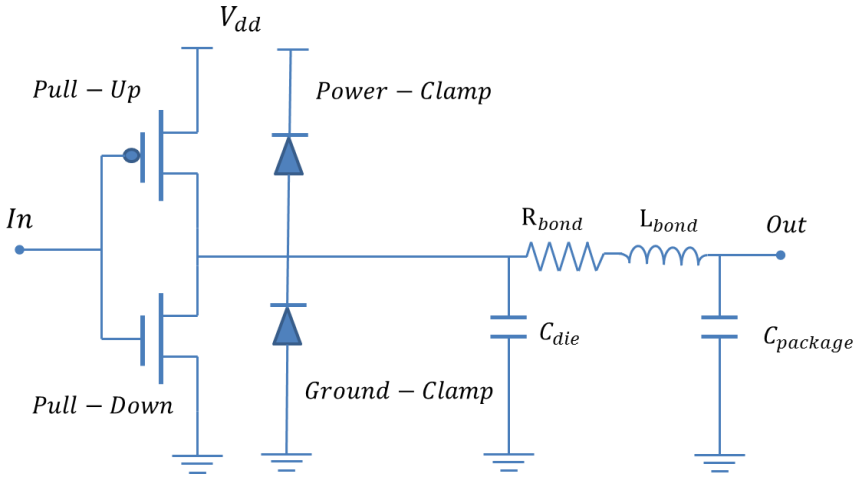

Fig. 1.3 - IBIS: output buffer model schematic [16].

difficult, in this situation, to separate the power/ground clamp and the pull-up/pull-down curves.

Beyond the components presented in Fig. 1.3, a typical IBIS file for output buffers also includes timing information, such as the ramp rate and the transition waveforms. The ramp rate (*dV*/*dt*) describes the transition time when the output of the buffer is switching from the current logic state to another logic state. The ramp rate is measured at the 20% and 80% points when the buffer is terminated with a 50 Ω load. On the other hand, the transition (falling and rising) waveforms show the time it takes the device to go from high to low and from low to high when driving a resistive load connected to ground and to V_{dd}. In both situations (ramp rate and transition waveforms) the die capacitance is included but the package effects are not considered.

Analog SPICE behavioral model

In order to simulate the behavior of a digital output buffer using the information provided by the IBIS file, an equivalent analog SPICE (Simulation Program with Integrated Circuit Emphasis) behavioral model is needed [17]. The pull-up (i_H), pull-down (i_L), power clamp (i_{pc}) and ground clamp (i_{gc}) curves can be represented by voltage controlled current sources. Moreover, two time dependent coefficients, $w_H(t)$ and $w_L(t)$, allow to model the switching behavior of the pull-up and pull-down transistors. The equivalent intrinsic (without the package) SPICE behavioral model, together with the standard loads for the determination of the transition waveforms, is represented in Fig. 1.4.

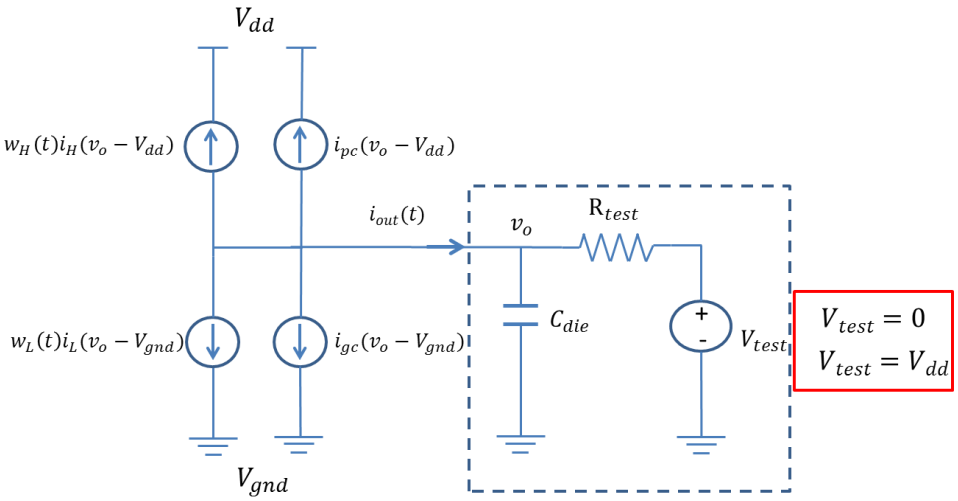

Fig. 1.4 – IBIS: equivalent model for SPICE simulations together with the standard loads for measuring the transition waveforms.

The values of $w_H(t)$ and $w_L(t)$ can be extracted from the transition waveforms provided in the IBIS file. Let us consider, for example, a rising waveform in the output. By assuming the current flowing directions of Fig. 1.4, equation (1.1) can be obtained. Since v_o is typically given for two different loads (transition waveforms), it is possible to obtain a system of two equations in two unknowns $[w_{H_r}(t), w_{L_r}(t)]$ for the rising waveform. The corresponding values for i_H, i_L, i_{pc} and i_{gc} can be determined by using piecewise linear interpolation of the static IV tables. Regarding $i_{out}(t)$, it is determined by considering the simulation of the boundary condition (dashed line in Fig. 1.4). If a similar procedure is applied for the falling waveform, the time dependent coefficients for both transitions (rising/falling) are obtained.

$$-i_{out}(t) = w_{H_r}(t)i_H(v_o - V_{DD}) + w_{L_r}(t)i_L(v_o - V_{gnd}) + \cdots \\ \ldots + i_{pc}(v_o - V_{DD}) + i_{gc}(v_o - V_{gnd}) \quad \textbf{(1.1)}$$

IBIS worked well for the technology of the 1990s, and during 5 years (1993 to 1998) enjoyed the status of the standard digital I/O model format. However, high frequencies brought new phenomena and it became clear that adding more complexity to the existing standard was not the answer to model new technologies such as the gigabit serial links. A possible solution to this problem was to revert back to the days before IBIS, which called for netlisting the I/O, encrypting the netlist and simulating in proprietary SPICE.

Unfortunately, this solution is non-portable (each SPICE vendor has its own encryption technique), is complex (it required PCB designers to understand difficult SPICE syntax) and it is non-public (as there is not a single SPICE standard). The IBIS committee had recognized these problems and ratified the IBIS 4.1 in 2004, which has multilingual support. The IBIS 4.1 allows to wrap traditional encrypted SPICE models, which make the SPICE models easier to use; unfortunately the time-efficiency problem of the SPICE models was not solved. An important achievement of the multilingual wrapper is the possibility to use the AMS (Analogue and Mixed Signal) language. The AMS models can be written so that they keep only the essential information from the I/O buffer and leave behind all the unnecessary transistor-level details. In this way AMS models can run faster (hundreds of times!!!) than SPICE models, without compromise the accuracy.

1.2.2 The Mπlog Model

The limitations faced by IBIS also originated the development of several black box approaches where the buffer's behavior is described in an abstract mathematical formulation. A possible structure to describe the behavior of a general RF-digital buffer can be given by (1.2), where f is a nonlinear dynamic analytical function. For the specific case of a digital output buffer, the modeling process becomes more difficult since the input, $v_i(t)$, (see Fig. 1.2) is not normally accessible. In order to overcome this difficulty, the majority of behavioral models for digital output buffers followed the two-piece model approach first introduced by IBIS (see Fig. 1.4). The structure of (1.3) was obtained, where i_H and i_L are sub-models accounting for the device behavior in the logic HIGH and LOW states, respectively, and $w_L(t)$, $w_H(t)$ are weighting functions that describe the switching between the logic states. The d/dt input argument in i_H and i_L represent the dependency also on the successive time-derivatives of $v_o(t)$ (indicating that the functions also incorporate the device's dynamic behavior).

$$i_o(t) = f\big(v_o(t), v_i(t)\big) \tag{1.2}$$

$$i_o(t) = w_H(t) i_H\left(v_o(t), \frac{d}{dt}\right) + w_L(t) i_L\left(v_o(t), \frac{d}{dt}\right) \tag{1.3}$$

Different approaches have been used to model i_H and i_L, in a dynamic way. The first approach was tried by Stievano *et al.* [18] and uses Radial Basis Functions Networks (RBFN). A RBFN is a particular case of the direct ANN, in which the nonlinear mapping depends on the distance between the input vector and the centre vector,

$$i_n(\theta_n, x(k)) = \sum_{j=1}^{M} \theta_{nj} \Phi(|x - c_{nj}|, \beta); n = H, L \quad \textbf{(1.4)}$$

In (1.4) the discrete time sub-models i_H and i_L are expressed as summations of radial basis functions, where M is the number of basis functions needed to accurately model i_H and i_L; Gaussian, multi-quadric and thin-plate spline are some of the RBFs normally used. In (1.4) Φ is the asymptotically increasing or decreasing basis function and θ_{nj} is the weight of the basis function. The centres of the basis functions are defined by c_{nj} and the width or the spread parameter is defined by β. The regressor vector x in (1.4) can be represented by (1.5) where the parameter r is the dynamic order of the model and the sample k is obtained at integer multiples of the sampling period (T_s)

$$x(k) = [i_o(k-1), \dots, i_o(k-r), v_o(k), \dots, v_o(k-r)]. \quad \textbf{(1.5)}$$

In order to estimate i_H and i_L, Stievano *et al.* [18] uses a piece-wise linear (PWL) voltage waveform, as it is shown in Fig. 1.5, connected at the buffer's output. These waveforms are composed of some level transitions (normally 4 to 10), spanning the range of operating voltages, $[V_{ss} - \Delta, V_{DD} + \Delta]$ where Δ is the accepted overvoltage. Typical values of Δ are (0.1-0.2)V_{DD}. The flat parts of the waveforms last for sufficient duration to allow the port to reach steady state operation and the edges have transition times comparable to the switching times of the port. The estimation of the parameters θ_1 and θ_2 is achieved by applying the algorithms of [19], [20] to the sampled identification signals. Once the sub-models i_H and i_L are estimated, the weighting coefficients w_H and w_L are obtained from a second set of identification signals. Such identification signals are the voltage and the current responses recorded during state transitions for two different load conditions, as it is shown in Fig. 1.6.

For a single LOW to HIGH transition and for two different loads (a) and (b), the sequences $\left(i_a^u(k), v_a^u(k)\right)$ and $\left(i_b^u(k), v_b^u(k)\right)$ are recorded, which leads to (1.6).

$$\begin{cases} i_a^u(k) = w_1^u(k) i_H\left(\theta_1, x_{1a}(k)\right) + w_2^u(k) i_L\left(\theta_2, x_{2a}(k)\right) \\ i_b^u(k) = w_1^u(k) i_H\left(\theta_1, x_{1b}(k)\right) + w_2^u(k) i_L\left(\theta_2, x_{2b}(k)\right) \end{cases} \quad \textbf{(1.6)}$$

Then, the elementary weight sequences, $w_1^u(k)$ and $w_2^u(k)$, describing the transition, can be obtained by simple linear inversion of the former equation, as described in (1.7).

$$\begin{bmatrix} w_1^u(k) \\ w_2^u(k) \end{bmatrix} = \begin{bmatrix} i_H\left(\theta_1, x_{1a}(k)\right) & i_L\left(\theta_2, x_{2a}(k)\right) \\ i_H\left(\theta_1, x_{1b}(k)\right) & i_L\left(\theta_2, x_{2b}(k)\right) \end{bmatrix}^{-1} \begin{bmatrix} i_a^u(k) \\ i_b^u(k) \end{bmatrix} \quad \textbf{(1.7)}$$

The same procedure, repeated for the HIGH to LOW transition, allows to compute two additional elementary sequences $w_1^d(k)$ and $w_2^d(k)$. Finally, a proper concatenation of $w_1^u(k)$, $w_1^d(k)$, $w_2^u(k)$ and $w_2^d(k)$ produces the final form of the weight coefficients for a given bit pattern. In principle, there are no restrictions on loads (a) and (b), which can also be real sources stimulating the output port. The best loads would be those allowing $\{i_a, v_a\}$ and $\{i_b, v_b\}$ to explore the widest possible region of the regressor space. Within the class of resistive circuits, the typical choices are: a resistor for load (a) and the series connection of a resistor and a V_{dd} battery for load (b); these loads are also used in IBIS.

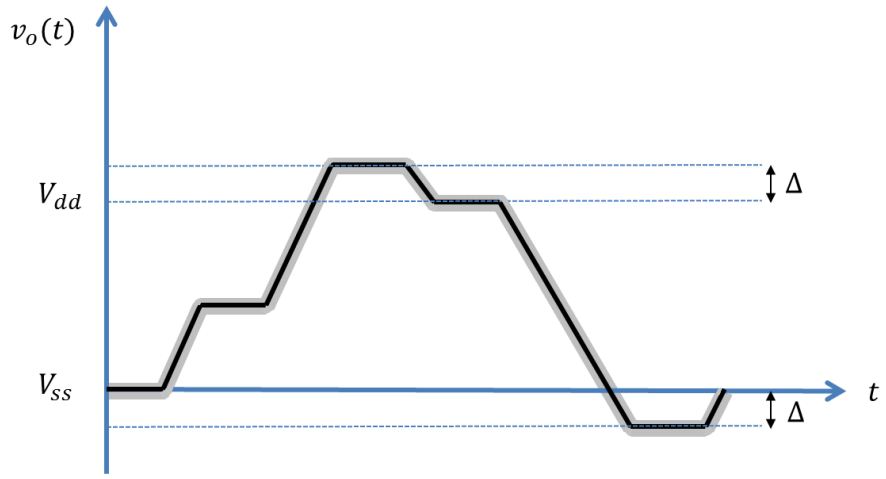

Fig. 1.5 - General multilevel driving waveform $v_o(t)$. Thin black line: noiseless waveform; thick gray line: superimposed noisy signal [18].

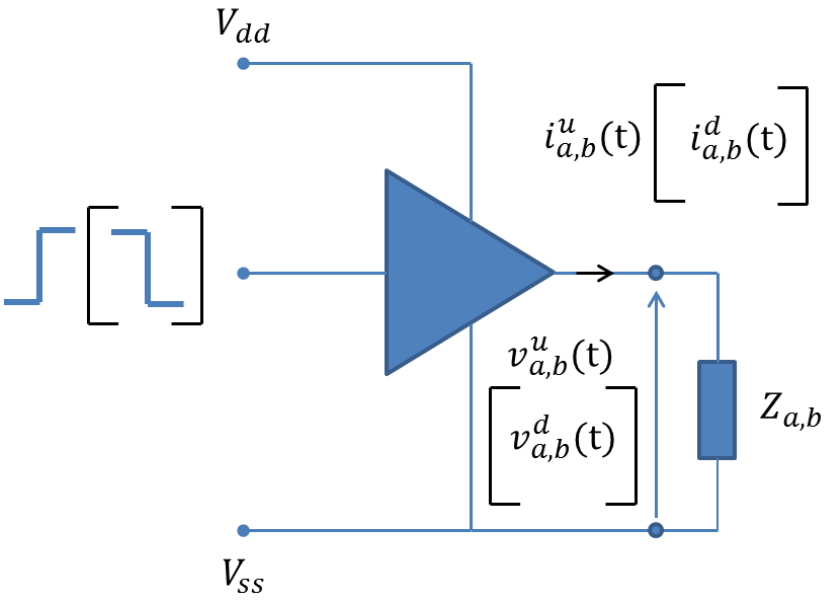

Fig. 1.6 - Ideal setup for the generation of the identification signals for the weight coefficients w_1 and w_2. The port current and voltage waveforms are recorded while the port is loaded by two different loads and is driven to perform an up (or a down) state transition. Z_a represents a load resistor, and Z_b is the series connection of a resistor and a V_{dd} battery [18].

1.2.3 The SFWFTD Model

Another possible approach to model digital output buffers was defined by Mutnury *et al.* [21] and assumes that $i_H(.)$ and $i_L(.)$ in (1.3) can be represented using Spline Functions With Finite Time Differences (SFWFTD), as it is described in (1.8) and (1.9), where now $i_{H/L,s}(k)$ is a polynomial function (static approximation) that relates the output current (i_o) and the output voltage of the driver (v_o).

$$i_H(k) = i_{H,s}(k) + p * i'_{oh} + q * i''_{oh} + \cdots \quad \textbf{(1.8)}$$

$$i_L(k) = i_{L,s}(k) + r * i'_{ol} + s * i''_{ol} + \cdots \quad \textbf{(1.9)}$$

The constants p, q, r and s can be estimated by calculating the error between $i_{H/L,s}(k)$ and the transistor level output current for the inputs HIGH and LOW. The effect of the dynamic behavior when the driver input is HIGH is captured in (1.10) (and in the higher order derivatives),

$$i'_{oh} = \frac{i_{H,s}(k) - i_{H,s}(k-1)}{h_t} \quad \textbf{(1.10)}$$

while the dynamic behavior when the driver input is LOW is captured in (1.11) (and in the higher order derivatives); in (1.10) and (1.11) h_t is the sampling time.

$$i'_{ol} = \frac{i_{L,s}(k) - i_{L,s}(k-1)}{h_t} \quad \textbf{(1.11)}$$

There is no limitation on the number of previous output current instances that can be added to the static sub-models. In general, SFWFTD approximation models need one previous time instance to accurately model the output buffers' current characteristics. Regarding the determination of the weighting functions, $w_H(t)$ and $w_L(t)$, a procedure similar to the one presented in Section 1.2.2 is used.

1.2.4 Test Fixture for Output Buffers' Characterization

As it was referred in the introduction of this document it is highly desirable to characterize the buffers' behavior based on laboratory measurements instead of considering the simulation of the detailed transistor-level model, usually hidden under intellectual property protection. The determination of the buffer's output (and supply) current is fundamental for the characterization (and modeling) of these devices.

A possible technique to measure the buffer's output (and supply) current makes use of a magnetic probe [13]. The current flowing through a conductor generates a magnetic field. The voltage that is induced at the probe is proportional to variation of the magnetic flux with time and hence to the current flowing in the conductor. Fig. 1.7 presents an example of a 120 MHz bandwidth magnetic probe (TCP0030) from Tektronix. In order to use this probe to measure the current, it is necessary to close and lock the probe's jaw around the conductor of interest. This makes difficult to use this type of probes in a coaxial or a microstrip environment. Moreover, for this specific case, the limited bandwidth (120 MHz) restricts its use for low frequency applications and, in this way, it is not suitable for the characterization of high speed digital buffers.

Another popular approach that allows measuring the power supply current of digital circuits is the so called 1-Ω method [13]. This technique employs a 1 Ω current probe whose schematic is presented in Fig. 1.8. Basically, it consists of a coaxial cable that is matched at both sides (R_p=1 Ω, R_a=49 Ω). Typically, the port 2 of the current probe is connected to a spectrum analyzer (R_{sa}=50 Ω) that is protected against DC current by the decoupling capacitor C_{sa}. Assuming ideal passive components, with C_{sa}=∞ and a coaxial cable with a linear phase and no losses, the magnitude of the current spectrum ($|I_{RF}|$) can be given as follows,

$$|I_{RF}| = \frac{R_p + R_a + R_{sa}}{R_{sa}R_p}|V_{sa}|. \quad \textbf{(1.12)}$$

In practice the passive components of the current probe are affected by fabrication tolerances and parasitic elements which demands for a calibration procedure. A similar method [12], called Direct Method, has been used for the characterization of digital buffers. In this approach the power supply current is determined by measuring the voltage drop directly over a low inductive 1 Ω resistor. Now a wideband oscilloscope is used whereas the voltage drop is determined by placing the voltage probe tip and the ground lead at the two terminals of the resistor. A similar strategy was followed by Stievano *et al.* [11] to measure the buffer's output current and extract the Mπlog model presented in section 1.2.2. In the remaining of this section the experimental procedure of [11] is discussed in detail.

The equivalent circuit of the developed measurement setup is presented in Fig. 1.9, where the passive probes of the oscilloscope (whose internal impedance can be modeled as a very high resistor $R = 1\,M\Omega$ in parallel with a capacitor $C_p = 14.1\,pF$) connect to terminals T and T_2. The output buffer current, $i_o(t)$, is indirectly determined from the differential measurement of the voltage drop across the surface mount device test resistor, as it is shown in (1.13); in this case $R_s = 100\ \Omega$.

$$i_o(t) = C_p\frac{dv_o(t)}{dt} + \frac{[v_o(t) - v_2(t)]}{R_s}. \quad \textbf{(1.13)}$$

Fig. 1.7 – TCP0030 - Tektronix Magnetic probe (120 MHz).

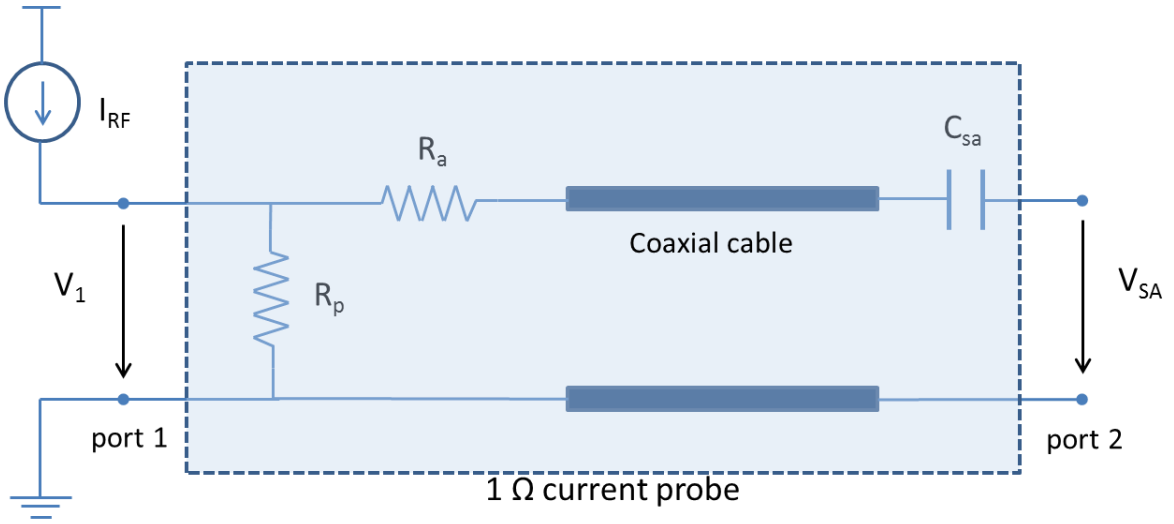

Fig. 1.8 – Schematic description of the 1 Ω current probe.

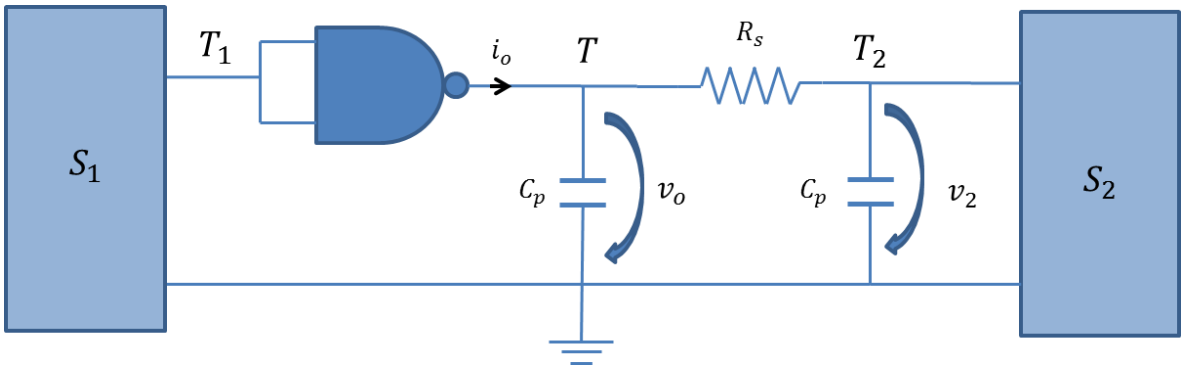

Fig. 1.9 - Measurement setup of [11] – equivalent circuit $C_p = 14.1\,pF$, $R_s = 100\Omega$.

In order to extract the sub-models i_H and i_L of (1.3) a multifunction generator (S_2) is used to obtain a multilevel waveform (see Fig. 1.5) in the buffer's output, whereas the logic state is set via the source (S_1).

Regarding the determination of the weights $w_H(t)$ and $w_L(t)$, the procedure previously presented is followed. For that reason, the port is driven (via S_1) to produce a rising and a falling transition in the buffer's output and the resulting $\{i_{oA,}v_{oA}\}$ and $\{i_{oB,}v_{oB}\}$ are measured.

According to its authors, this measurement setup has some drawbacks that limit its use at low frequencies. As mentioned in [11], for higher frequencies, the resistor R_s should be characterized with a network analyzer. Therefore, the determination of the buffer's output current is much more complicated than what is described in (1.13), as this R_s may have to be treated as an actual dynamic impedance.

Regarding the chosen value for R_s, some additional comments have to be made. If, on the one hand, a low value is desirable to minimize the impact on the buffer's behavior; on the other hand, a high value resistor is needed to increase the voltage drop $(v_o - v_2)$ and guarantee a certain signal-to-noise-ratio, necessary for the desired measurement accuracy. Thus, the choice of the resistance value (R_s) represents a compromise, which is, quite often, difficult to solve. A possible solution to this problem makes use of a differential probe, potentially useful with comparably smaller resistances. However, this type of probes is usually expensive and so normally not available in the measurement laboratories.

Another issue that should not be overlooked is the parasitic capacitance (C_p) of the oscilloscope's passive probes. For high frequencies, not only these parasitic capacitances add an undesired load to the output buffer, as their low impedance completely distorts the measured voltage (and thus current) waveforms.

1.3 Objectives and Thesis Outline

As it was possible to observe (see section 1.2), the modeling of digital I/O buffers starting from measured data is making its first steps. The importance of this topic attracted the attention of the industrial companies which motivated the development of the MOCHA (MOdelling and CHAracterization for SiP – Signal and Power Integrity Analysis)

European project [2] for which I have also contributed. This two year project started on the 1st January 2008 and was developed in collaboration with several companies and research institutes, such as: Micron Semiconductor Italy S.r.l (Italy), Politecnico di Torino (Italy), Cadence Design System (Germany), Agilent Technologies (Belgium), Instituto de Telecomunicações of Aveiro (Portugal) and Microwave characterization center (MC^2 – Technologies, France). So, together with the development of the measurement setup (the core of the work), the following topics constitute the framework of this PhD thesis:

- Characterization and modeling of the power supply networks (IC Core and I/O) of high speed memories ;
- Determination of the power supply fluctuations and its impact on the buffers' behavior;
- Definition of an experimental procedure, together with its calibration details, to extract/validate state of the art models for RF-digital buffers;
- Development of an uncertainty analysis for the proposed experimental procedure.

Therefore, in order to fulfill the above mentioned objectives, this document is organized as follows. Chapter 1 provides the motivation for this work and the state of the art approaches for the characterization (and modeling) of high speed digital I/O buffers. The drawbacks of the existing solutions, namely on what concerns the characterization procedure based on measurements (Section 1.2.4), are highlighted. The most relevant contributions achieved during this PhD thesis are included in Section 1.4 which concludes Chapter 1. Chapter 2 describes the main contributions that this work has produced for the MOCHA project. This project was much broader than what is presented here, being constituted by several work-packages. In this document is only described the impact that the developed work has produced in the progress of the MOCHA project. Therefore, Chapter 2 mainly focuses on the developed experimental procedures to characterize the power supply networks (IC Core and I/O) of the high speed memories that normally constitute a wireless transceiver (Flash, RAM, etc.). Both on-die (on-wafer) and in-package measurements were considered. Chapter 3 presents the constitutive blocks of the novel measurement setup and, based on the considered test-fixture, an experimental

procedure (together with its calibration details) was defined to extract a state of the art model for a commercial packaged high speed digital buffer. An uncertainty study for the proposed experimental procedure is presented in Chapter 4. This assumes a relevant role in this PhD thesis since any measurement procedure (or setup) must provide an indication of the level of accuracy associated to its final results, setting their level of reliability and usefulness. This analysis is seldom observed in previous publications in this field. Finally, Chapter 5 concludes this PhD thesis and discusses possible ideas to improve the developed work in a near future.

1.4 Main Contributions

The main achievements of this PhD work were published in international peer-reviewed journals and conferences, as listed below. These journals and conferences are considered the most relevant in this field. The work developed for the MOCHA project (see Chapter 2) is well documented in [J3] and [J4] while the material addressed in Chapters 3, 4 resulted in the publications [C1] and [J1]. The publications [C1] and [J1] are attached to the end of this document.

Papers in International Journals

- **[J1] H. M. Teixeira**, W. Dghais, T. R. Cunha, and J. C. Pedro "Measurement Setup for RF/Digital Buffers Characterization*", IEEE Transactions on Instrumentation and Measurement,* vol. 62, no. 7, pp. 1892-1899, Jul. 2013.

- **[J2]** W. Dghais, **H.M. Teixeira**, T.R. Cunha, J. C. Pedro, "Novel Extraction of a Table-Based I-Q Behavioral Model for High-Speed Digital Buffers/Drivers", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol.3, no.3,pp. 500-507, March 2013.

- **[J3]** I.S. Stievano, L. Rigazio, F. G. Canavero, T. R. Cunha, J. C. Pedro, **H. M. Teixeira**, A. Girardi, R. Izzi, and F. Vitale, "Behavioral modeling of IC memories from measured data", *IEEE Transactions on Instrumentation and Measurement*, vol. 60, no. 10, pp. 3471-3479, Oct. 2011.

- **[J4]** T. R. Cunha, **H. M. Teixeira**, J. C. Pedro, I. S. Stievano, L. Rigazio, F. G. Canavero, R. Izzi, F. Vitale, and A. Girardi, "Validation by measurements of an IC modeling approach for SiP applications", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 8, pp. 1214-1225, Aug. 2011.

Papers in International Conferences

- **[C1]** **H.M. Teixeira**, T.R. Cunha, J.C. Pedro, "Large Signal Characterization of High Speed Digital Buffers for Signal Integrity Analysis of Software-Defined-Radio Applications", accepted for presentation in the European Microwave Conference, Oct. 2013.

- **[C2]** W. Dghais, **H.M. Teixeira**, T.R. Cunha, J.C. Pedro, "Efficient table-based I-Q behavioral model for high-speed digital buffers/drivers", Proceedings of 16th IEEE Workshop on Signal and Power Integrity, SPI 2012, Sorrento, Italy.

- **[C3]** I.S. Stievano, I.A. Maio, L. Rigazio, F.G. Canavero, R. Izzi, A. Girardi, T. Lessio, A. Conci, T. Cunha, **H.M. Teixeira**, J.C. Pedro, "Characterization and modelling of the power delivery networks of memory chips", 13th IEEE Workshop on Signal Propagation on Interconnects, Strasbourg 2009.

Chapter 2 - Contributions to the MOCHA Project

This chapter is devoted to present the most important contributions to the MOCHA project. The main goal of the MOCHA project was the development of reliable modeling and simulation solutions for System in Package (SiP) devices [2]. In order to validate the obtained simulation tools, the project also addressed the development of several measurement platforms. The project was divided into four major work-packages (WP) that are summarily described below:

WP1 – Definition of an experimental procedure to derive reliable and wideband models for the IC power supply distribution networks (IC Core and I/O);

WP2 – Development of an innovative approach to obtain models, either from measurement or simulation results, for the buffers of a SiP device;

WP3 – Development of Electronic Design Automation (EDA) tools for signal and power integrity (SiP) analysis that also included a 3D EM field solver;

WP4 – Design of a measurement platform to allow the characterization of high-speed SiP devices and, in that way, validate the achievements of WP3.

The four WP were not developed independently as they were highly correlated. However, and since my main contribution was focused on WP1, the remaining of this chapter will be dedicated to present the most important achievements inside WP1. Towards the goal previously presented, the WP1 was divided in four main tasks:

T1.1 – Definition of a broadband model for the passive power distribution networks;

T1.2 – Characterization and modeling of the IC core switching activity;

T1.3 – Validation of the models obtained in T1.1 and T1.2;

T1.4 – Design of a high flexible characterization board.

Within a general logic device, such as a Flash memory Integrated Circuit (IC), two main blocks can be identified: the core sub-system that performs the logic operations and the I/O buffers block that performs the interface between the IC core and the outside world (PCB, package, etc.). Usually, the IC core and the I/O drivers are powered by two different networks. In this way, a complete behavioral model should describe: 1) the dynamic

associated to the core power delivery network; 2) the dynamic of the I/O power rail and its impact on the I/O buffers' behavior; and 3) the possible coupling between the core and I/O power rails.

In the next section (Section 2.1) the chosen models for the core power delivery network (VDD/VSS) and I/O buffers' power rails (VDDQ/VSSQ) are presented. The models' extraction procedure is addressed in Section 2.2. Finally, Section 2.3 presents the measurement setup used for the validation of the proposed models. For validation purposes, two particular memory ICs were tested: a 66 MHz 512 Mb NOR Flash memory developed by Numonyx Italy S.r.l. (now Micron Semiconductor Italia S.r.l.) in 90 nm technology (proprietary test-case) and a 133 MHz 512 Mb LPDDR memory manufactured by a third party company (external test-case). This document focuses mainly on the obtained results for the proprietary test-case. Further results, concerning the external test-case, can be found in [24].

2.1 Core and I/O Buffers Models

2.1.1 IC Core Power Network

In order to model the core power delivery network, and its effects on the peripheral circuits, the approach proposed by the International Electrotechnical Commission (IEC) was followed. The IEC proposes a standard model called Integrated Circuit Electrical Model (ICEM) [26] for simulating conducted and radiated emission of the integrated circuits. In the ICEM model the IC core power network is represented by a Norton equivalent where the impedance accounts for the passive interconnect structure and the short-circuit current generator accounts for the internal switching activity of the device. Moreover, due to the complexity of the IC core circuitry, a piecewise linear (PWL) source is normally assumed for the current generator.

For the specific cases of the memories mentioned above, the power/ground pads are distributed along the core power rail (VDD/VSS). Therefore, the ICEM model was slightly modified to take this issue into account, as it is shown in Fig. 2.1. The resulting model was obtained after performing electromagnetic simulations on structures similar to those present in the referred memories. From the obtained simulation results it was observed that the dominant effects were that of a longitudinal resistance and a transversal capacitance.

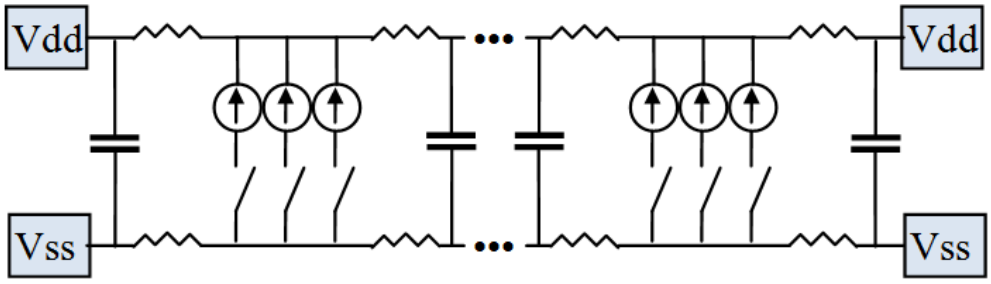

Fig. 2.1 - Adopted topology to model the IC core network; copied from [22].

Regarding the short-circuit current generator, it was split in three different independent generators where the specific operation (erase, program and burst) is activated/deactivated by turning on/off some switches.

2.1.2 I/O Buffers Power Rail

The I/O buffers power rail presents a much more simple structure than the core power rail. Basically a set of straight lines connect multiple VDDQ/VSSQ pads pairs where each couple VDDQ/VSSQ typically supplies a single buffer.

An approach similar to the one presented in the previous section was followed for the dynamic characterization of the I/O power rail and its impact on the buffers' behavior. The resulting model is presented in Fig. 2.2, where the model adopted for consecutive pairs of VDDQ/VSSQ pads consists of both series (Zs) and shunt (Zp) impedances. The loading effect imposed by the I/O buffer circuit in the I/O power rail is dominantly capacitive (C_B). Finally, additional impedance was considered to model the die substrate impact on the power rail.

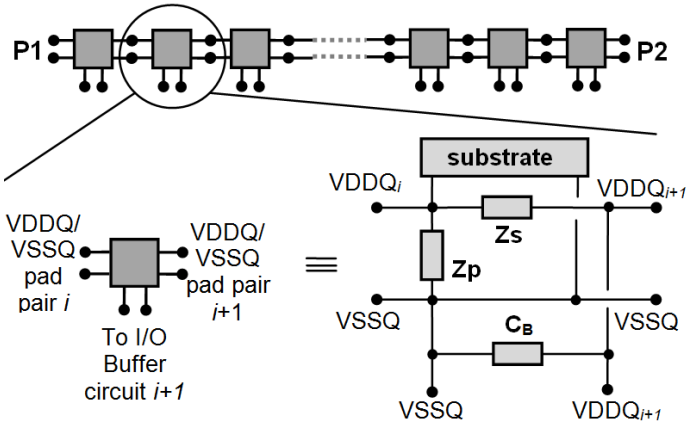

Fig. 2.2 - Adopted topology to model the IC I/O buffers power rail; copied from [22].

2.2 Models Extraction Procedure

The extraction of the models presented in the previous sections demands for a procedure to estimate (preferably from measurements) not only the IC core switching activity but also the passive structures that constitute the core and I/O buffers power rails. Towards the measurement of the IC core switching activity, two test-boards (one for each memory) were developed. In both boards the voltage drop over a 1 Ω resistor was used to indirectly determine the core's current. The details of the test boards' implementation are well documented in [23] and are not addressed in this document.

The extraction of the passive models for the I/O and core power rails is based on the collection of several on-wafer S-parameters measurements that were performed on the RF laboratory of Instituto de Telecomunicações (IT-Aveiro). The measurement setup of Fig. 2.3 represented my first contact, at the early stage of the PhD, with the characterization of state of the art output buffers. In this way, the MOCHA project assumed an important role by providing me the initial experience, needed to the development of the PhD work. The developed measurement setup consists of a probing station that holds the wafer (one for each memory device) constituted by several dies. The RF probes, which connect to a vector network analyzer (VNA), touch different VDD/VSS and VDDQ/VSSQ pads. In order to completely characterize the power rails' behavior, all possible combinations of pads' pairs were tested and the effect of the bias supply was also considered.

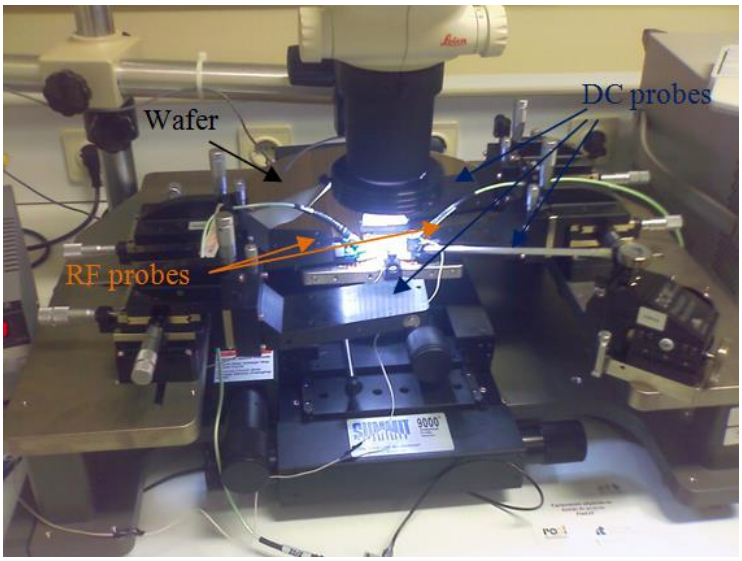

Fig. 2.3 - On-wafer measurement setup used for IC power rails characterization (with the die being externally biased, in this case); copied from [22].

The bias voltages can be injected either by using external bias-tees in the RF probes or by on-wafer landing of DC needles (DC probes).

In Fig. 2.4 is shown the used configuration for on-die characterization of the VDDQ/VSSQ power supply rail (proprietary test-case). The two RF probes are connected to the first and to the last couples of the VDDQ-VSSQ pads. The respective measured S-parameters are presented in Fig. 2.5 for both biased and unbiased situations.

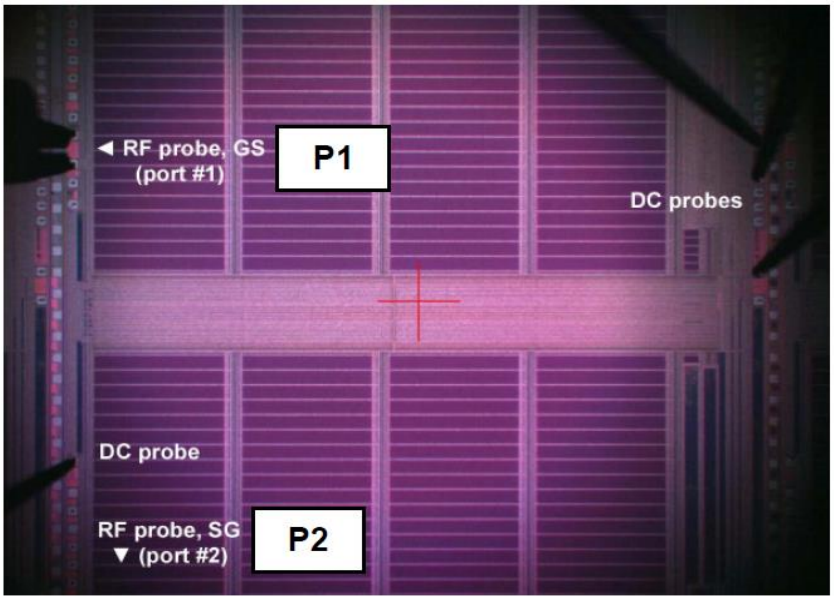

Fig. 2.4 - Setup for collection of the two-port S parameters of the VDDQ-VSSQ power supply structure of the proprietary test chip from on-die measurements; copied from [27].

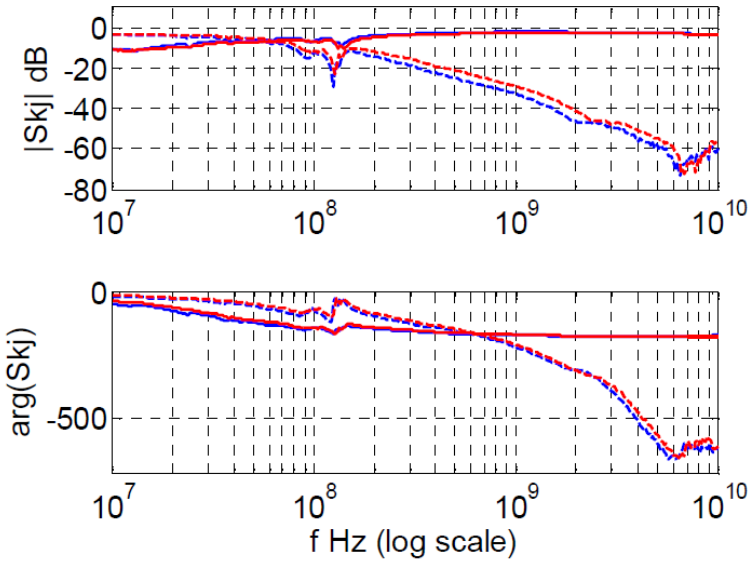

Fig. 2.5 - Set of S-parameter measurements obtained between the two farthest pairs of VDDQ/VSSQ pads, for the proprietary test-case; solid line-S11, dashed line-S21; red – with DC bias applied, blue – without DC bias applied; copied from [27].

As it is possible to verify in Fig. 2.5, the bias influence on the dynamic behavior of the VDDQ/VSSQ power rail is negligible. Based on the measured S-parameters, the lumped model of Fig. 2.2 can be extracted by considering a least squares error minimization. The extracted values for the proprietary and external-test cases are presented in Table 1. Once the spatial distribution of the VDDQ/VSSQ pads is not exactly uniform, the estimated values can be slightly different from basic cell to basic cell. On the other hand, since the buffers' capacitance (C_B), due to its substantially higher value, makes the shunt impedance (Z_B) effects negligible, the latter impedance was not considered in the final model. Moreover, it was verified that the series impedance (Z_S) could be reasonably approximated by only considering a resistive component. As a further simplification, the possible substrate contributions were not considered. In Fig. 2.6 the measured results, for two non-consecutive pads, are compared against the simulation results (proprietary test-case) obtained with the lumped model previously described.

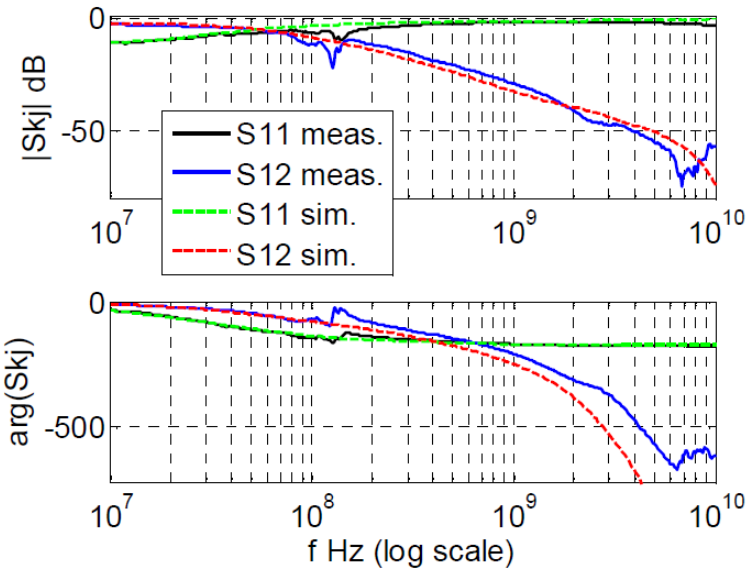

Fig. 2.6 - Fitting the measured S-parameters with the lumped elements' model, for two non-consecutive VDDQ/VSSQ port; copied from [27].

Test-case	Z_S (Ω)/basic cell	Z_P (Ω)/basic cell	C_B (pF)/basic cell
Proprietary	1.6	--------	6.3

Table 1 – Extracted lumped elements for the VDDQ/VSSQ power rail.

As it is possible to observe, even considering the aforementioned approximations for the resulting model, the fitting results are quite reasonable.

A similar approach was followed in order to determine the lumped model for the core power supply passive network. The measurement results presented in Fig. 2.7 reflect a dominant capacitive behavior of the VDD/VSS power rail. Note that for this power rail the differences between the biased (grey curves) and unbiased (blue curves) curves are more visible (about 2-3 dB in the low frequency range) than those obtained for the VDDQ/VSSQ power rail. A total capacitance of 2 nF was extracted for the proprietary test-case. The comparison between measured and simulation results, for the proprietary test-case, is presented in Fig. 2.8. As it is possible to observe, this simple model, that only considers a shunt capacitor, predicts reasonably well the dynamic behavior of the core power supply passive network. However, if it is desirable to increase the accuracy of this model, more complex structures can be considered [27]. It is worth to say that the apparently high values obtained for the shunt capacitor are coherent with the fact that the VDD/VSS power rails typically supply a huge number of transistors that cover most of the area of the die. In order to study the cross coupling between the VDD/VSS and VDDQ/VSSQ power supply rails additional S-parameters measurements were performed. For that, an external bias-T was associated to each VNA port. It was verified that the coupling between the two rails was negligible; for the majority of measured frequencies, the S21 magnitude presents values that are below -40 dB (see Fig. 2.9).

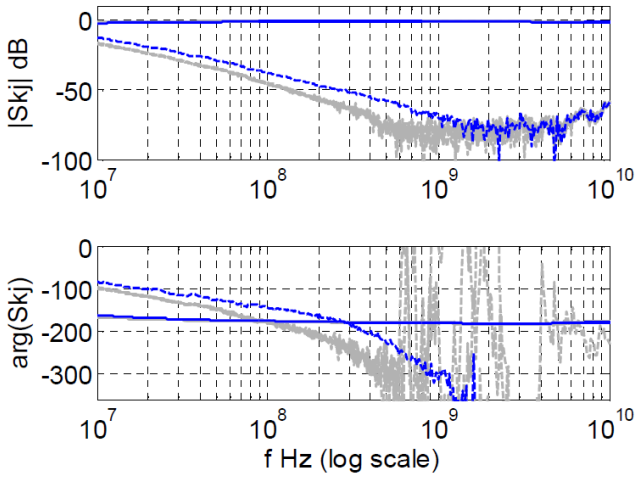

Fig. 2.7 -Selection of the scattering responses on the VDD-VSS network. Solid lines - S11, dashed lines - S21. The grey and the blue curves represent measurements on different biased and unbiased dies, respectively; copied from [27].

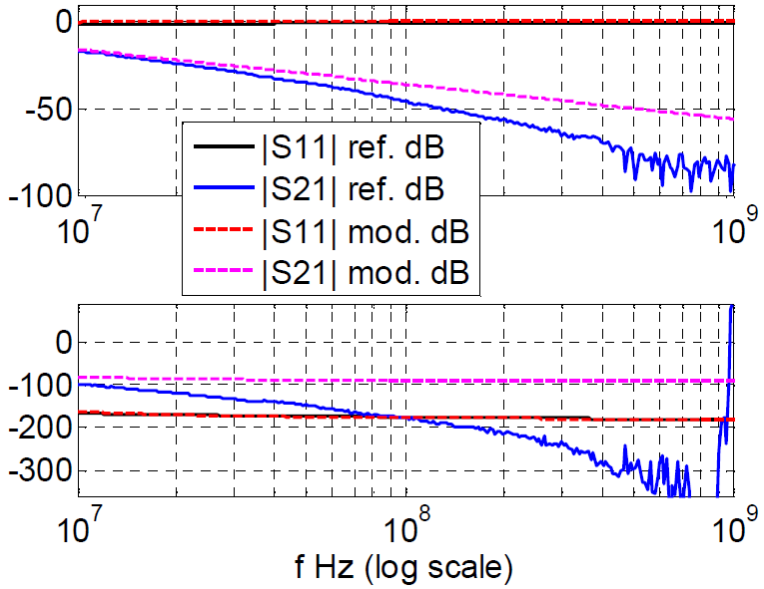

Fig. 2.8 - Selection of scattering responses of the VDD-VSS structure. Solid lines – reference measured responses, dashed lines – responses of the model that considers a shunt capacitor (C=2 nF); copied from [27].

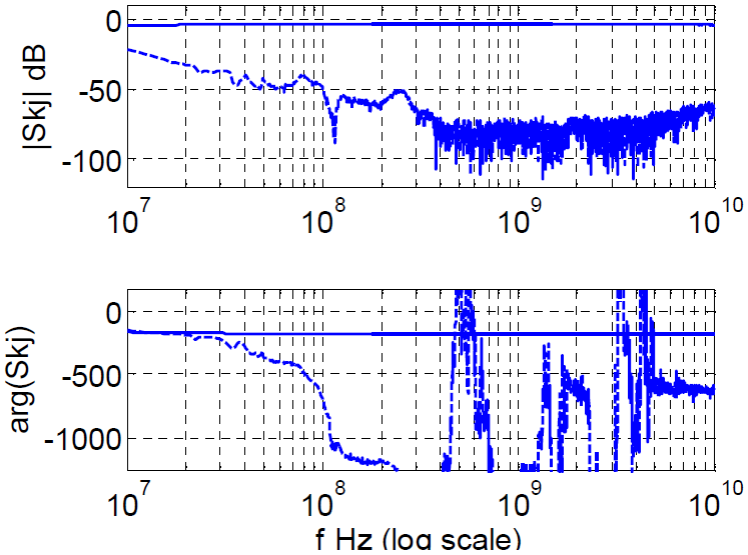

Fig. 2.9 - Selection of the scattering responses for the coupling of the VDDQ-VSSQ (Port P1) and of the VDD-VSS (Port P2) structures. Solid lines – S11, dashed lines – S21. Port P1 is defined by the VDDQ-VSSQ couple of pads surrounding the DQ11; copied from [27].

2.3 Measurement Setup and Validation Results

In order to validate the whole power integrity model, interfacing PCB boards were developed to connect the two test-cases. For both test-cases, the same design approach was followed where a motherboard, denominated Flash Fast interface board (FFIB), holds a daughterboard (memory module - MM) in which the memory die is assembled. The FFIB and MM boards are presented in Fig. 2.10 and Fig. 2.11, respectively. The memory dies are glued to the MM and bonded, through gold bond-wires, to the MM bond-fingers (see Fig. 2.12). On the other hand, the MM connects to the FFIB via QTE connectors. Therefore, the testing of different memories only requires the design of the MM board.

In order to measure the voltage waveforms, the RF probes connect to the desired bond-fingers (DQx and power pads) while the inputs are switching in a controlled way by the firmware loaded into the field programmable gate array (FPGA) of the FFIB. Moreover, the RF probes signals were measured using a real time oscilloscope (Tektronix TDS3052B) whose input impedance is nearly 50 Ω over the whole frequency range (0-500MHz). Since this impedance value was too low for loading the IC I/O output buffers, surface mount devices (SMD) series resistors were added to the measurement setup (120 Ω, 270 Ω or 330 Ω), as it is shown in Fig. 2.13.

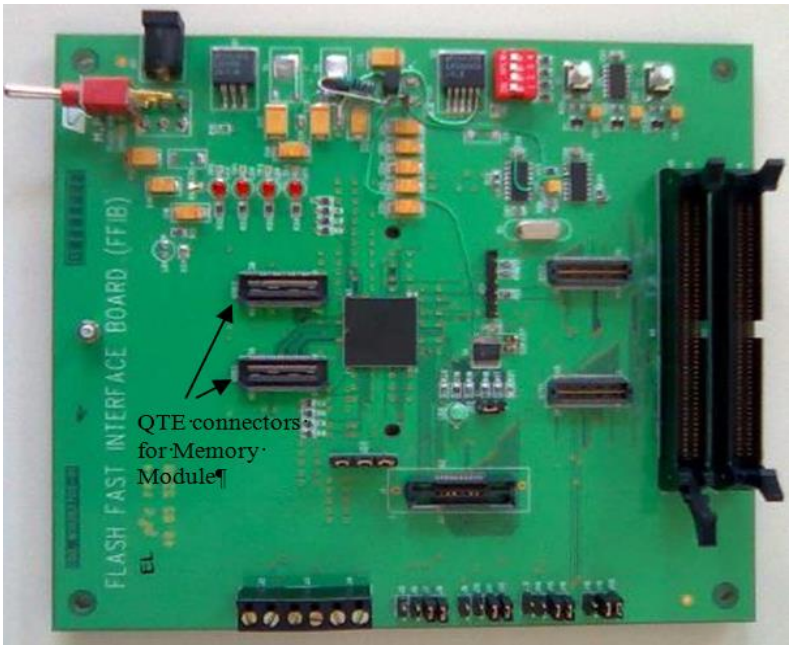

Fig. 2.10 - Image of the FFIB control board; copied from [22].

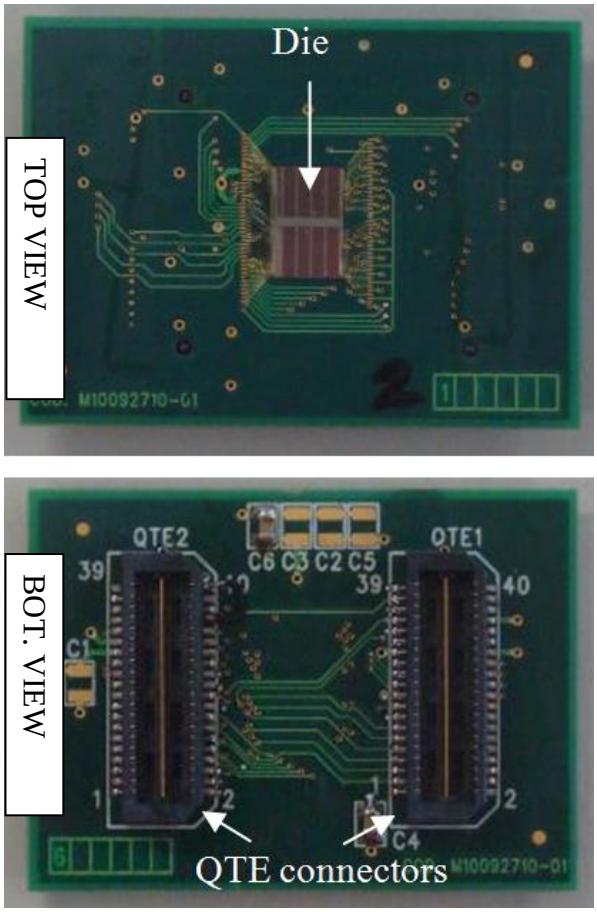

Fig. 2.11 - Image of the MM of the proprietary device; copied from [22].

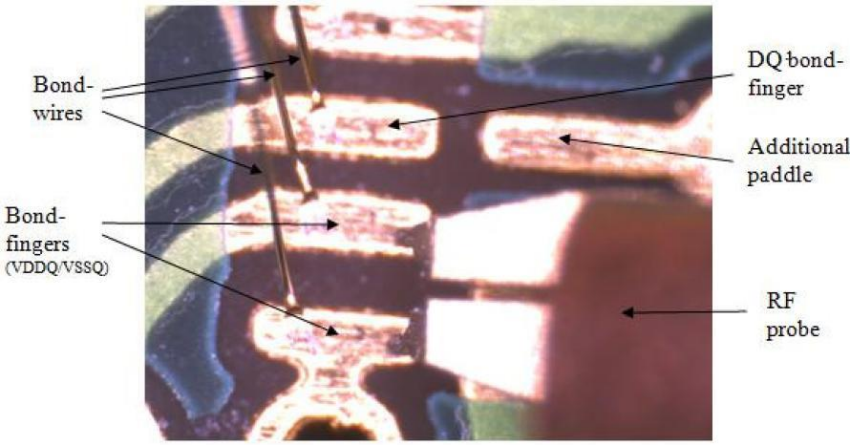

Fig. 2.12 - Image of the extended bond-fingers and additional paddles for the external test-case MM; copied from [22].

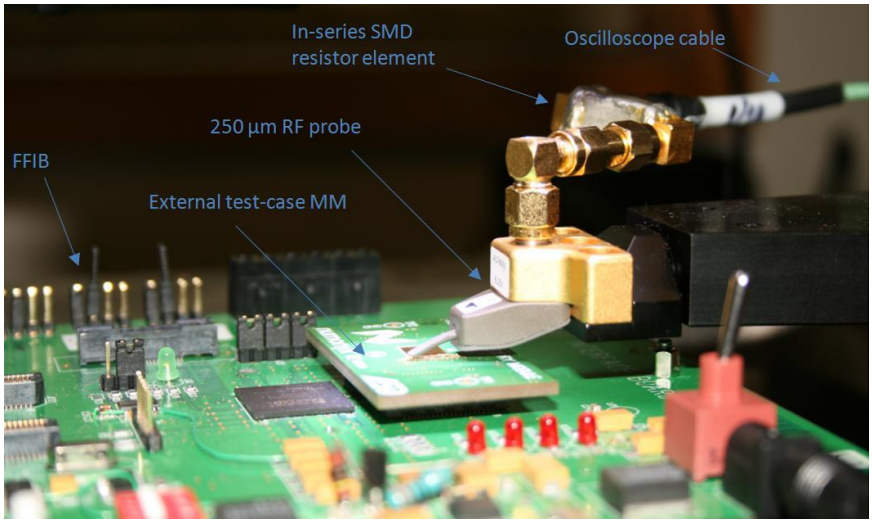

Fig. 2.13 - Image of the developed oscilloscope probe, with an in-series SMD resistor mounted before the RF probe tip; copied from [22].

In order to remove the non-ideal effects of the measurement setup, a de-embedding procedure was applied. For that, using a swept frequency sine wave, the linear transfer function from the probe tips to the monitor of the oscilloscope was determined and its effect removed from the measured voltages. In Fig. 2.14 are presented the measured output voltages obtained in the outputs of four buffers (DQ0-DQ3) of the proprietary device that was programmed in order to guarantee simultaneous switching conditions. In this worst-case scenario, the I/O buffer (VDDQ-VSSQ) and core (VDD-VSS) supply voltages were also measured in order to correlate their results with those obtained by the implementation of the full simulation model.

The full simulation model should include, for accurate correlation results, not only the whole power integrity model previously extracted, but also the FFIB and interface boards effects that were obtained via S-parameters measurements and electromagnetic simulations. Moreover, since the SPICE netlists of the I/O buffer circuits were available for both test-cases, these were used to model the I/O buffer behavior. Nevertheless, when that is not the case, other behavioral models can be indeed used. In [23] the details of the extraction, either from measurements or simulations, of a state of the art model for I/O buffer circuits are presented.

In Fig. 2.15 some simulation and measurement results are reported for the I/O signal and power noise. Regarding the core switching activity (swa) extraction, two approaches were followed: one using IC core simulation data and another that considers the current measured through a 1 Ω resistor [23]. As it can be observed, the full model predicts very

well the behavior of the proprietary test-device, namely the bouncing associated to the low-high and high-low transitions. In this way, the power integrity model was considered validated. Despite of the fact that the MOCHA project is much more embracing than what was described in the previous sections, my goal within this chapter was to present my main contributions to that project, which mainly focused on characterization by measurements of the structures interconnecting the IC core and buffer circuits (the power supply rails and the signal rails). Further documentation related to the MOCHA project can be found online [24].

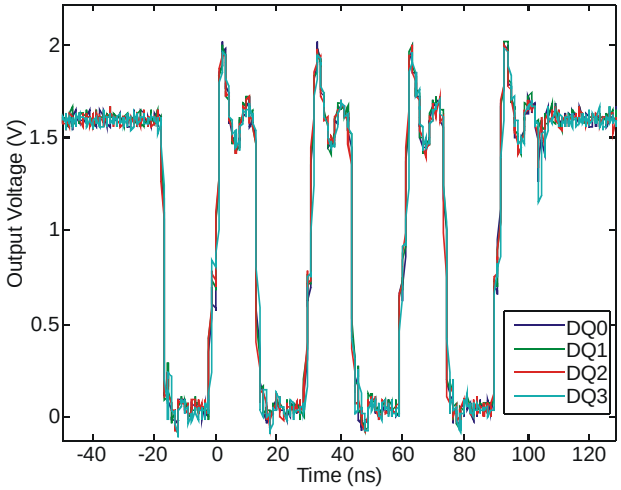

Fig. 2.14 - Example of four measured I/O buffer output voltage signals for the proprietary test-case; copied from [22].

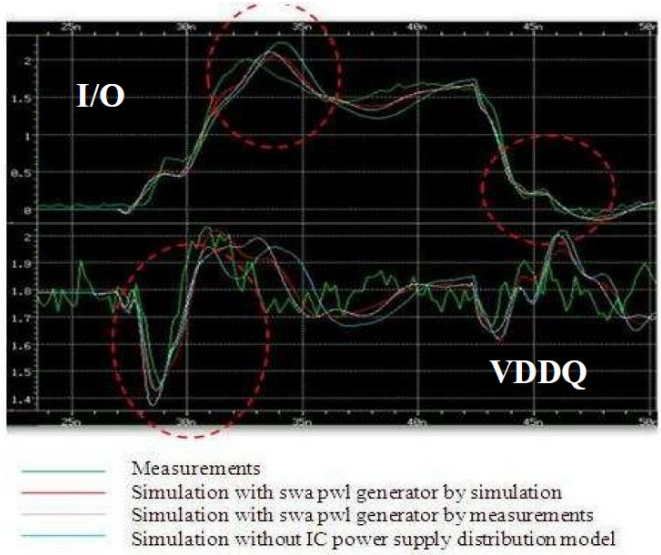

Fig. 2.15 - Benchmark between SSO simulation and measurement results for the proprietary test-case; copied from [25].

Chapter 3 - The Novel Measurement Setup

As it was mentioned in the previous chapter (Chapter 2), considerable work was performed on characterizing by measurements the power and signal rail interconnects that interface the I/O buffer circuits within their ICs. Complementing such work, the WP2 of the MOCHA project was dedicated to the development of an innovative approach to obtain models, either from measurement or simulation results, for the buffers of SiP devices. The work developed within this PhD had direct impact on the progress of the MOCHA project, both on WP1 and WP2, as it addresses the characterization by measurement of complete I/O buffer structures. Not only was the MOCHA project important in the acquisition of knowledge in this field (from the experience of the industry and academia partners), as was relevant to the project the work developed in the scope of this PhD.

In this chapter the novel measurement setup for output buffers' characterization is presented. In order to show the validity of the proposed setup, a well-defined experimental procedure was defined to extract and validate a state of the art model for a commercial non-inverting output buffer in packaged format.

3.1 Proposed Measurement Setup and Calibration

In Fig. 3.1 is presented the proposed measurement setup. Instead of using a test resistor (SMD) to indirectly measure the switching output current, $i_o(t)$, it makes use of a Forward Wave Coupler (FWC). This device has 3 ports and allows sampling the incident (forward) wave in a transmission line (main-line) - in this case the incident wave moves towards the load (Z_L). It is worth to say that there are several FWC in the market, with different coupling factors (CF). However, the chosen directional coupler has a CF of -20 dB which guarantees a minimal impact on the buffer's operation but is still capable of producing accurate measurements. The setup also includes: bias-Ts in the input (BT1) and output (BT2) of the buffer which permit to control the static operating point of the device; a high speed oscilloscope (SCOPE) to monitor the forward wave; and an arbitrary

waveform generator (AWG) that controls the buffer's switching operation. A vector network analyzer (VNA) and a voltage source with current sink capability complete the measurement setup (not shown in the picture). Table 2 presents the commercial components that were used during the several experiments.

For the determination of the buffer's output current (i_o) and voltage (v_o), based on the coupled measured voltage (port 2), the system of equations of (3.1), that contains the S-parameter description of the three port network (BT_2 and FWC) together with the boundary conditions in ports 2 and 3, was considered. Although it is possible to solve numerically the full system of linear equations, some simplifications were considered so that the proposed characterization procedure could be explained making use of closed form expressions.

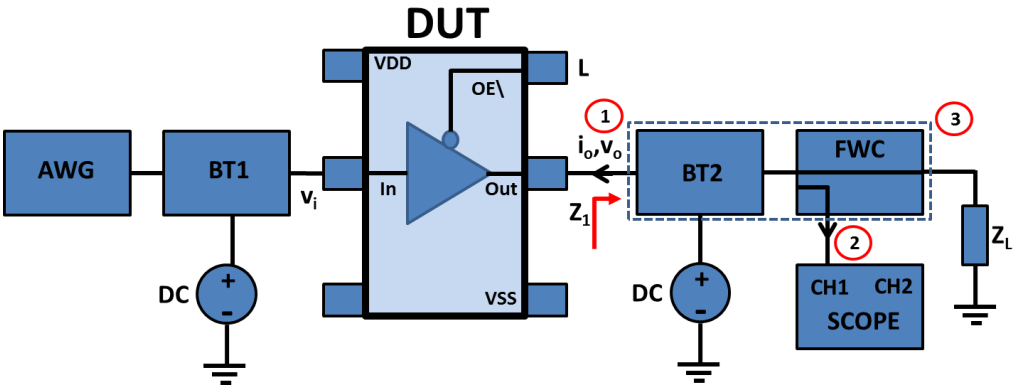

Fig. 3.1 - Proposed measurement setup – block diagram.

Forward Wave Coupler (FWC)	ZFDC-20-5 (0.1 to 2000 MHz) – Mini Circuits
Bias-Tee (BT1 and BT2)	ZFBT-6GW (0.1 to 6000 MHz)- Mini Circuits
High Speed Oscilloscope (SCOPE)	DPO72004B – 20 GHz – Tektronix
Arbitrary Waveform Generator (AWG)	VSG-SMU-200A – Rohde&Schwarz
Voltage Source (with sink capability)	HP6634A-100V-1A
Vector Network Analyzer (VNA)	E8361C PNA from Agilent Tech.

Table 2 – Description of the main commercial components that constitute the measurement setup.

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3 \\ b_2 = S_{21}a_1 + S_{22}a_2 + S_{23}a_3 \\ b_3 = S_{31}a_1 + S_{32}a_2 + S_{33}a_3 \\ a_2 = \Gamma_i b_2 \\ a_3 = \Gamma_L b_3 \end{cases} \quad \textbf{(3.1)}$$

Accordingly, since the high-speed oscilloscope (SCOPE) that was connected to the coupling port (port 2) presented nearly 50 Ω over the entire measurement bandwidth, it was assumed that $a_2 \approx 0$, in a system with characteristic impedance $Z_o = 50\ \Omega$; a_2 is the reflected wave in the oscilloscope input or the incident wave in port 2 of the FWC. Moreover, the set formed by the FWC and BT2 was characterized, using the VNA specified in Table 2, in the range of 0.1 MHz - 2000 MHz and a quite reasonable directivity ($S_{23} \approx -30\ dB$) was observed. In this situation, the system of equations of (3.2) is enough to describe the set formed by the FWC and BT2. In the next chapter (section 4.3), the error associated to the aforementioned approximations is quantified.

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{13}a_3 \\ b_2 &= S_{21}a_1 \\ b_3 &= S_{31}a_1 + S_{33}a_3 \\ a_3 &= \Gamma_L b_3 \end{aligned} \quad \textbf{(3.2)}$$

So, based on the Mason's rule [28], it is possible to determine the voltage transfer function from port 1 (output port) to port 2 (coupled port), as it is presented in (3.3). Then, by using the inverse transfer function (TF^{-1}) the test fixture effects from port 2 to port 1 are de-embedded. The obtained output voltage and current, in the frequency domain, are given by (3.4) and (3.5), respectively, where Z_1 represents the measured impedance looking into port 1 when port 3 is terminated by the desired load (Z_L) and port 2 is connected to the high speed oscilloscope (see Fig. 3.1). Finally, to recover the time domain signals, an inverse Fourier transform is applied. The picture of the whole measurement setup is presented in Fig. 3.2, which presents the device under test (DUT) mounted on a dedicated test fixture (the Anritsu Model 3680 K).

$$\frac{V_2}{V_1} = TF = \frac{S_{21}(1 - S_{33}\Gamma_L)}{1 + S_{11} - S_{33}\Gamma_L - S_{11}S_{33}\Gamma_L + S_{13}S_{31}\Gamma_L} \quad \textbf{(3.3)}$$

$$V_1 = V_2 . TF^{-1} \quad \textbf{(3.4)}$$

$$I_1 = \frac{V_1}{Z_1} \quad \textbf{(3.5)}$$

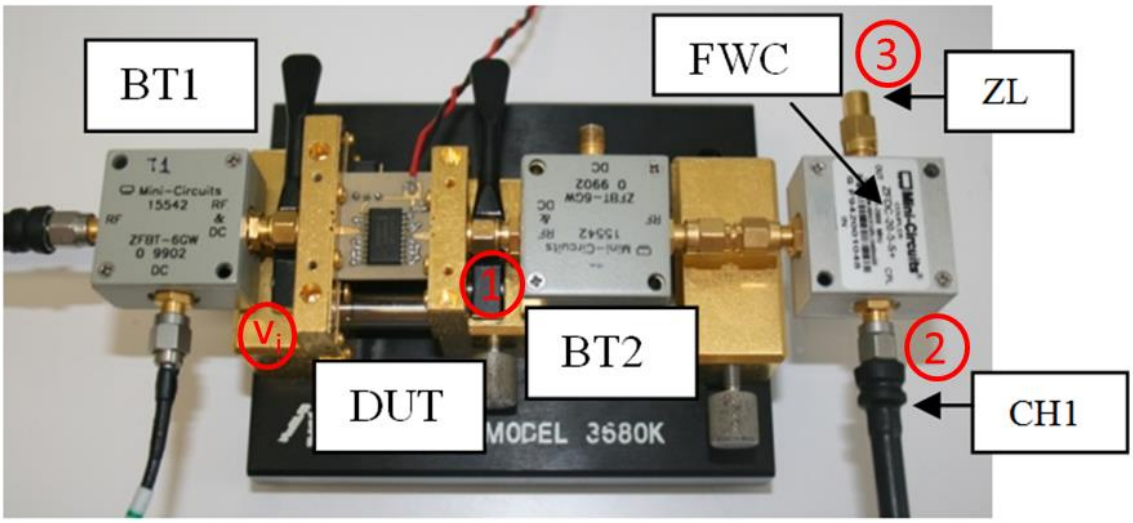

Fig. 3.2 - Measurement setup used for the characterization of the 74LVC244 output buffer.

3.2 Model Extraction and Validation

After presenting the novel measurement setup, together with its calibration details, this section is dedicated to describing the experimental procedure necessary to the extraction and validation of a state of the art model. The used test device was the 74LVC244 output buffer from NXP. The 74LVC244 is a non-inverting buffer (VDD_{max}=6.5 V and f_{max}=150 MHz) with 3-state outputs. As already addressed in Chapter 1 (Section 1.2) the state of the art models, for output buffers, share the structure of (1.3).

The next sub-sections describe the steps necessary to estimate, from measurements, the pull-down (i_L) and pull-up (i_H) sub-models as well as the weighting functions (w_H, w_L).

3.2.1 Pull-Down (i_L) and Pull-Up(i_H) Networks Extraction

Similarly to what is assumed in the IBIS model, a static behavior was considered for the pull-up (i_H) and pull-down (i_L) networks. For the extraction of these sub-models DC voltage sources were connected at both buffer input (BT1) and output (BT2) and no signal was applied. It is worth to say that the voltage source associated to the BT2 needs to have the capability to sink (from the pull-up) and source (to the pull-down) current. This is the case of the HP6634A-100V-1A source presented in Table 2. For the i_H sub-model, the

buffer's input (v_i) has to be in the HIGH logic state (VDD=3.3V) while the output is varied, in a static way, in the range -0.5 to 3.8 V. These conditions guarantee that the clamping diodes are not activated. A similar procedure should be used for the extraction of the i_L sub-model, but for this case the input should be in the LOW logic state.

In Fig. 3.3 and Fig. 3.4 are represented the measured pull-down and pull-up curves, respectively. The same figures also include the data provided in the IBIS file for the same commercial test device. As it is possible to observe, the measured curves (dotted) are bounded by the IBIS MAX and IBIS MIN curves, which accordingly to [29], validates the measured static behavior of the pull-down and pull-up networks.

3.2.2 Weighting Functions Extraction, $w_H(t)$ and $w_L(t)$

Now, it remains the determination of the weighting functions, $w_H(t)$ and $w_L(t)$. For that, typically, the buffer's switching behavior for two different loads is determined. The recommended loads by the IBIS consist of a resistor (50 Ω) and a series connection of a resistor and a VDD battery. Then, the weighting functions are extracted as it is described in (3.6), where waveforms $\{i_{oA}, v_{oA}\}$ and $\{i_{oB}, v_{oB}\}$ are the switching signals recorded for the two loads. Nevertheless, in order to avoid an ill-conditioned matrix resulting from noisy measured data [30], only one load (50 Ω) was used for the determination of the weighting functions. In this case the approximation $w_H(t) = 1 - w_L(t)$ is required.

$$\begin{bmatrix} w_H(t) \\ w_L(t) \end{bmatrix} = \begin{bmatrix} i_H(v_{oA}(t)) & i_L(v_{oA}(t)) \\ i_H(v_{oB}(t)) & i_L(v_{oB}(t)) \end{bmatrix}^{-1} \begin{bmatrix} i_{oA}(t) \\ i_{oB}(t) \end{bmatrix} \quad \textbf{(3.6)}$$

Towards the measurement of the switching waveforms (voltage and current), a sine wave (100 MHz) was applied in BT1 which, together with a DC level of 1.4 V, guaranteed a square voltage waveform with 50 % duty cycle in the buffer's output. After using the procedure presented in Section 3.1 for the determination of the voltage (v_o) and current (i_o), based on the sampling voltage of the directional coupler (FWC), the weighting functions of (3.6) were extracted for $Z_L = 50\ \Omega$ (see Fig. 3.5).

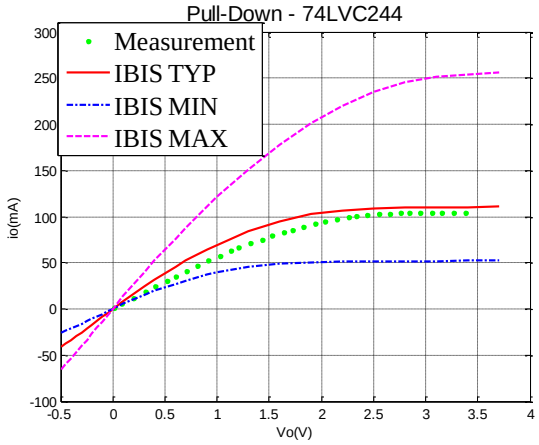

Fig. 3.3 - Pull-down curves for the 74LVC244 digital buffer (IBIS file vs LAB data).

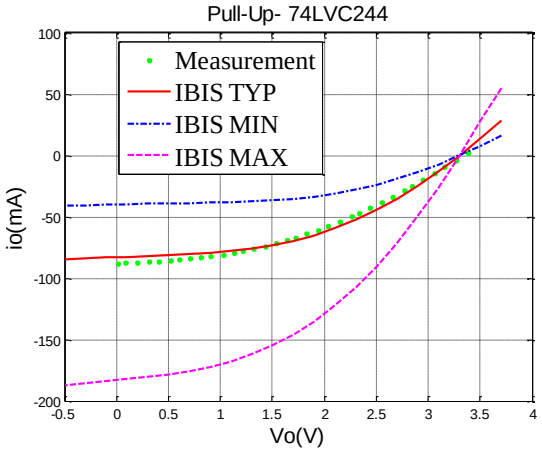

Fig. 3.4 - Pull-up curves for the 74LVC244 digital buffer (IBIS file vs LAB data).

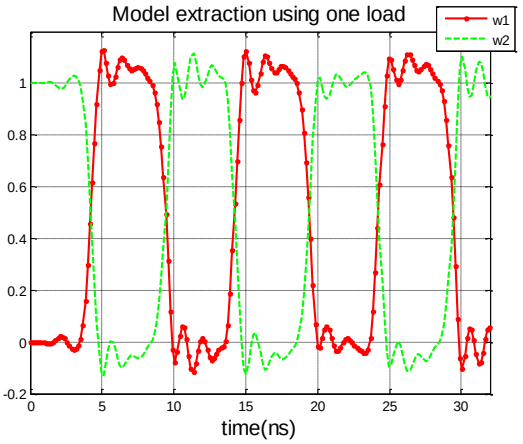

Fig. 3.5 - Weighting functions obtained for $Z_L = 50\ \Omega$.

3.2.3 Model Implementation and Validation

The resulting model was implemented in Advanced Design System, from Agilent Technologies Inc., as shown in Fig. 3.6. Two Symbolic Defined Device [32] (SDD 2-port) were used, one for i_L and another for i_H, where $w_H(t)$ and $w_L(t)$ were applied, as look-up-tables, to the inputs of the SDDs. The SDD allows the creation of equation based, user-defined, nonlinear components specifying algebraic relationships between port voltages, currents, and their derivatives. The implemented model also includes the S-parameters of the set FWC-BT2 (FWC_S3P.S3P) and the one port S-parameters of the used load (LOAD_S1P.S1P) and high speed oscilloscope (SCOPE_S1P.S1P). The measured and simulation results were compared for three different loads: Z_L=50 Ω (used for the extraction), Z_L=100 Ω and Z_L=470 Ω; the obtained results are presented in Fig. 3.7, Fig. 3.8 and Fig. 3.9, respectively. As it is possible to observe from Table 3, the considered model is quite accurate for the extraction load, however, its prediction capability degrades as we move away from its value [33]. This is certainly related to the considered approximation for the weighting functions. If it is possible to extract the model for two different loads, the model will become more accurate for a wider range of loads.

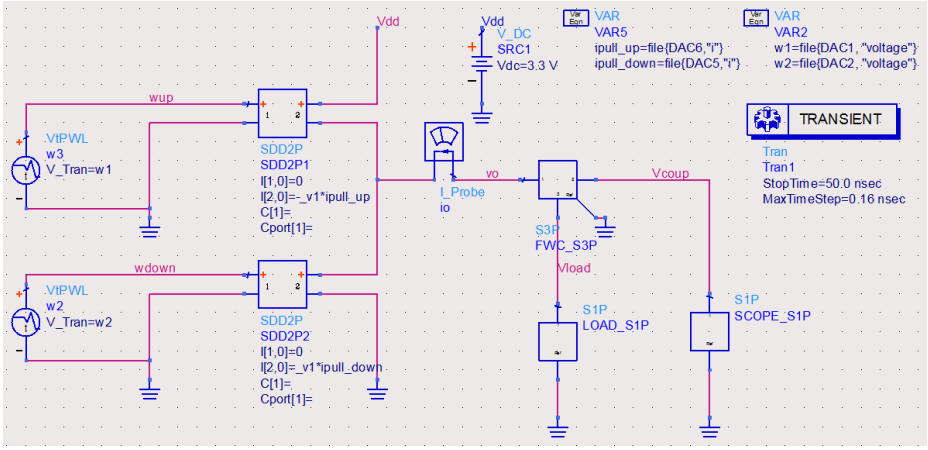

Fig. 3.6 - Model implementation in ADS using SDDs

Z_L(Ω)	*NMSE* (dB)
50	-33.4
100	-28.7
470	-23.4

Table 3 – NMSE [31] values for the different loads.

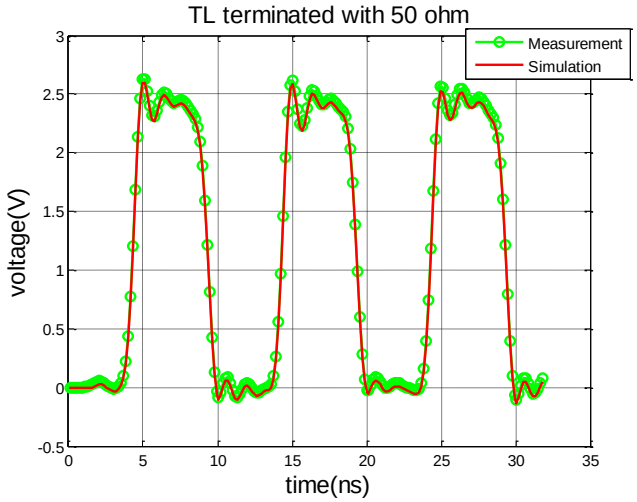

Fig. 3.7 - Measured and simulated voltage curves for R_L=50 Ω.

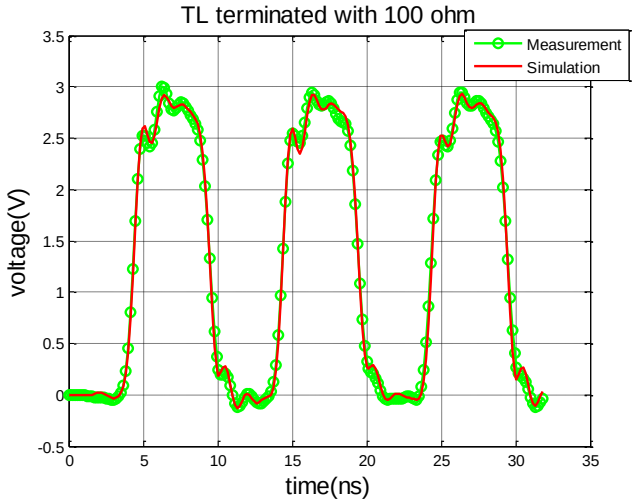

Fig. 3.8 - Measured and simulated voltage curves for R_L=100 Ω.

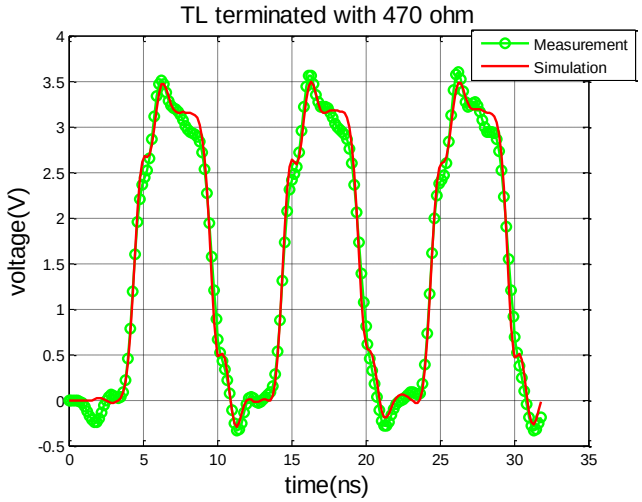

Fig. 3.9 - Measured and simulated voltage curves for R_L=470 Ω.

3.3 Pull-Down (i_L) and Pull-Up (i_H) – Dynamic Characterization

In the previous section (Section 3.2), the characterization data for the estimation of the sub-models $i_H(t)$ and $i_L(t)$ was based on a static voltage DC sweep at the output, $v_o(t)$, and, in this way, the package dynamic effects were not taken into account in these sub-models. Herein, the proposed measurement setup of Fig. 3.1 is extended for the characterization of $i_H(t)$ and $i_L(t)$ under large signal (LS) [34], [35] conditions. In this way, the necessary number of measurement points, as well as the measurement time, is reduced (in comparison with the static approach) and the buffer's dynamic effects are exposed for the situations where the input (v_i) is already in the steady state.

Fig. 3.10 presents the block diagram of the extended measurement setup. In order to measure the LS incident wave, a bi-directional coupler (Bi-Dirc) was used, instead of a single FWC. Regarding the excitation signal (LS), a sine wave (VSG-SMU-200A generator) was chosen since, besides it is readily available in the laboratory, it excites the buffer's dynamic behavior. Nevertheless, the characterization procedure herein presented is not limited to sinusoidal signals.

Now, the high speed oscilloscope (SCOPE) needs to simultaneously measure the incident and reflected waves. In the bias-T (BT2) a DC level was applied in order to guarantee that the LS spans the whole operating range (0-V_{DD}). Since the sub-models $i_H(t)$ and $i_L(t)$ are determined when the input (In) is at a fixed logic level, the arbitrary waveform generator can be substituted by a constant DC voltage source. Both generator and high speed oscilloscope were synchronized by a 10 MHz reference.

Now, for the determination of the buffer's output voltage and current (port 1), for both logic states, a 4 port S-parameter description is needed,

$$b_i = \sum_{j=1}^{4} S_{ij} a_j \quad , \quad i = 1, \dots, 4. \tag{3.7}$$

Once again, some simplifications were considered so that the characterization procedure could be explained making use of closed form expressions. Accordingly, it was assumed that, for the typical operating frequencies of most high speed digital buffers, the

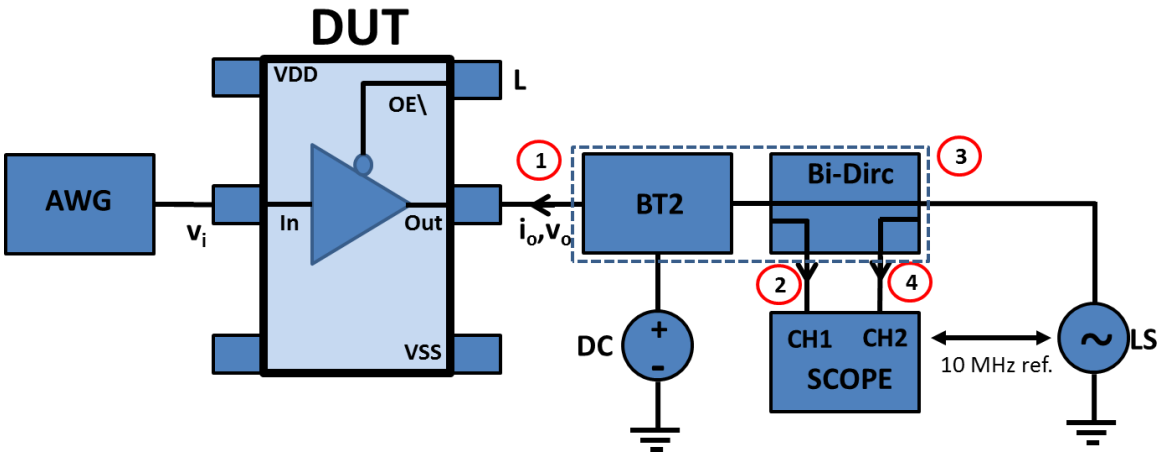

Fig. 3.10 – Measurement setup for the dynamic characterization of the pull-up/down networks.

broad bandwidth oscilloscope (SCOPE) presents an input impedance of nearly 50 Ω, which implies that $a_2, a_4 \approx 0$ in a system with characteristic impedance, $Z_o = 50\ \Omega$.

In this situation, the 4-port S-parameter matrix reduces to:

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{13}a_3 \\ b_2 &= S_{21}a_1 + S_{23}a_3 \\ b_3 &= S_{31}a_1 + S_{33}a_3 \\ b_4 &= S_{41}a_1 + S_{43}a_3. \end{aligned} \tag{3.8}$$

After some mathematical manipulations, the voltage and current at port 1, in the frequency domain, can be easily determined as shown in (3.9) and (3.10), respectively.

$$V_o = \left(\frac{b_2 - S_{23}a_3}{S_{21}}\right).(1 + S_{11}) + S_{13}a_3 \tag{3.9}$$

$$I_o = \left(\frac{b_2 - S_{23}a_3}{S_{21}Z_o}\right).(1 - S_{11}) - \frac{S_{13}a_3}{Z_o} \tag{3.10}$$

Since b_2 can be obtained from the time domain voltage that is monitored in the channel 1 of the broad bandwidth oscilloscope only a_3 is left to be determined. If it is considered that S_{41} is negligible ($S_{41} \approx -60\ dB@100\ MHz$) then the incident wave in port 3 (a_3) can be determined from the monitored voltage in the second channel of the high speed oscilloscope, as shown in (3.11).

$$a_3 = \frac{b_4}{S_{43}} \tag{3.11}$$

Finally to obtain the time domain signals at the buffer's output, $i_o(t)$ and $v_o(t)$, (thus, with the effect of the measurement setup de-embedded) the inverse Fourier transform is applied to (3.9) and (3.10).

For illustrative proposes, this experimental procedure was applied in the characterization of $i_H(t)$ and $i_L(t)$ for the same commercial buffer mentioned in the previous section (NXP-74LVC244, V_{DD}=3.3 V). A 100 MHz LS was considered and the averaging mode was chosen for the high speed oscilloscope with a sampling frequency of 6.25GS/s. The measured dynamic output current for the pull-up (i_H) and pull-down (i_L), as a function of the output voltage (v_o), are represented in Fig. 3.11 and Fig. 3.12, respectively. These figures also include the static characteristics of the IBIS model provided by the manufacturer, for the pull-up and pull-down. As observed, the measured dynamic I/V characteristics cover reasonably well the trajectories followed by the static characteristics of the IBIS model. Furthermore, the package and printed circuit board (PCB) parasitic effects are taken into account and, in this way, the output dynamic behavior of the buffer is characterized for the cases where the input (In) is at fixed logical level. It is important to remember that reflections may occur even when the input (In) is already in the steady state, and that is the reason why a dynamic characterization of the pull-up and pull-down networks is highly desirable.

In the next section, the measurement setup of Fig. 3.10 is extended to consider possible fluctuations of the supply voltage. This issue assumes a relevant role in SiP devices (see Chapter 2) where fluctuations on the order of 30/40 % of the nominal value (V_{dd}) can be obtained.

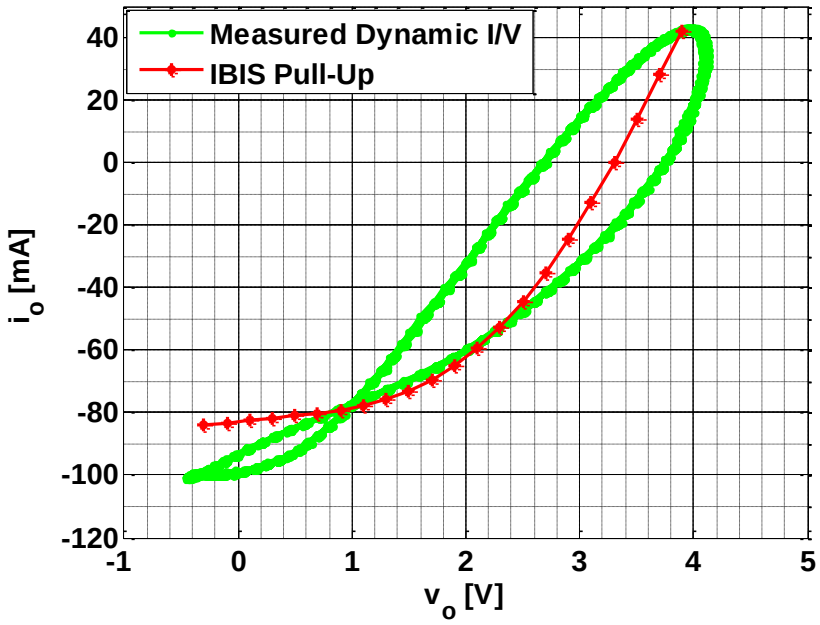

Fig. 3.11 – Measured pull-up dynamic I/V characteristics and simulated IBIS static pull-up.

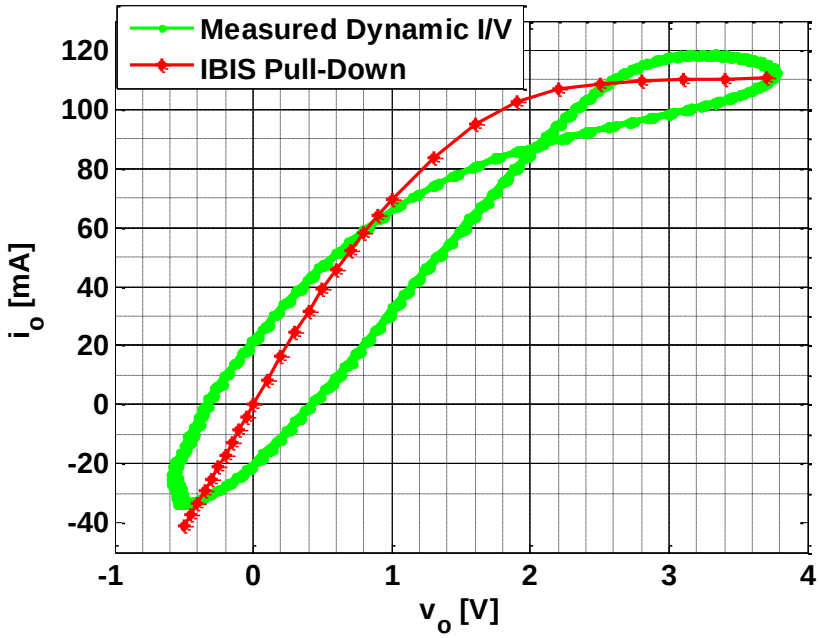

Fig. 3.12 – Measured pull-down dynamic I/V characteristics and simulated IBIS static pull-down.

3.4 Multi-Port Extension

In Chapter 2 was already highlighted the importance of the characterization of the buffers' power supply rail. In the case of SiP devices the long bond-wires, associated with the high data rates, make extremely difficult to guarantee the integrity of the power supply voltages. In this way, any fluctuation of the power supply network may affect the device's overall performance leading to bit errors or even to a complete system failure. Therefore, it is highly desirable that a measurement setup for the characterization of high speed digital buffers also has the capability to estimate the voltage and current waveforms in the power supply port.

The most straightforward approach for this purpose would be to use an additional commercial directional coupler, such as the ZFDC-20-5 [36] from Mini Circuits. However this device blocks the DC current in the main arm, which is unacceptable for the V_{dd} port. To overcome this difficulty, a directional bridge was designed. This device (see Fig. 3.13) is based on the resistive Wheatstone bridge concept [37]. A coupling factor of 20 dB and an insertion loss of 1 dB were specified for the design. These values guarantee a minimal impact on the buffer's operation providing, at the same time, accurate measurement results.

The full block diagram of the developed measurement setup is presented in Fig. 3.14. So, in order to completely define the experimental procedure needed to remove the test fixture effects from the measured data, only the power supply port remains to be addressed.

3.4.1 Power Integrity Calibration

Herein, the same approach of Sections 3.1 and 3.3 is considered to remove the linear effects of the test fixture. Based on the voltage (coupling port) measured by the high speed oscilloscope (CH1 in Fig. 3.14) it is possible to determine the power supply current (i_{Vdd}) and voltage at port 3. For that, let us consider the full S-parameters matrix describing the directional bridge. The system of equations of (3.12) also includes the boundary conditions for ports 1 and 2, where Γ_{SCOPE} represents the reflection coefficient of the high speed oscilloscope (in this case channel 1), and $\Gamma_{V_{dd}}$ is the reflection coefficient associated with the source connected to port 1. Once again, it is assumed that the used high speed oscilloscope (DPO72004B – Tektronix – 20 GHz) presents an input impedance that is nearly 50 Ω, which results in a reflection coefficient $\Gamma_{SCOPE} \approx 0$, in a system with

characteristic impedance $Z_o = 50\ \Omega$. Moreover, the DC source that is connected to port 1 presents a reflection coefficient $\Gamma_{V_{dd}} \approx -1$, and in this way $a_1 \approx -b_1 + V_{dd}\delta(\omega)$, where $\delta(\omega)$ is the Dirac delta function; a well-designed DC voltage source is a short-circuit for signal components.

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3 \\ b_2 = S_{21}a_1 + S_{22}a_2 + S_{23}a_3 \\ b_3 = S_{31}a_1 + S_{32}a_2 + S_{33}a_3 \\ a_2 = \Gamma_{SCOPE}b_2 \\ a_1 = \Gamma_{V_{dd}}b_1 + \dfrac{1-\Gamma_{V_{dd}}}{2}\ V_{dd}\delta(\omega) \\ V_{CH1} = a_2 + b_2 \end{cases} \quad \textbf{(3.12)}$$

After some mathematical manipulations, it is possible to obtain the voltage and current (in the frequency domain) as a function of the voltage measured by the high speed oscilloscope (CH1). This is described in (3.13), (3.14), (3.15) and (3.16).

$$a_3 = \frac{S_{21}V_{dd}\delta(\omega) - (1+S_{11})b_2}{S_{21}S_{13} - S_{23}(1+S_{11})} \quad \textbf{(3.13)}$$

$$b_3 = \frac{S_{31}V_{dd}\delta(\omega)}{1+S_{11}} + a_3\left(S_{33} - \frac{S_{31}S_{13}}{1+S_{11}}\right) \quad \textbf{(3.14)}$$

$$V_3 = a_3 + b_3 \quad \textbf{(3.15)}$$

$$I_3 = \frac{a_3 - b_3}{Z_o} \quad \textbf{(3.16)}$$

Then, after applying an inverse Fourier Transform to (3.15) and (3.16), it is possible to recover the time domain signals. The final developed test fixture is presented in Fig. 3.15. Please note the presence of the dual-coupler used for large signal characterization (Section 3.3) and of the designed directional bridge. To show the validity of the developed setup for power integrity characterization, it follows now the estimation of the voltages and currents at the V_{dd} port for different frequencies and loads. Although not addressed in this document, the characterization data obtained for the V_{dd} port can be used afterwards to

extract models that also consider the fluctuations of the power supply voltage [38], [39] and [40].

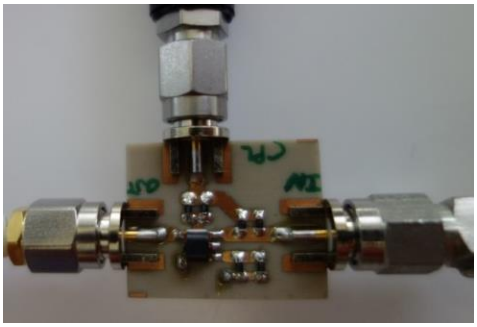

Fig. 3.13 – Designed directional bridge for the V_{dd} port characterization.

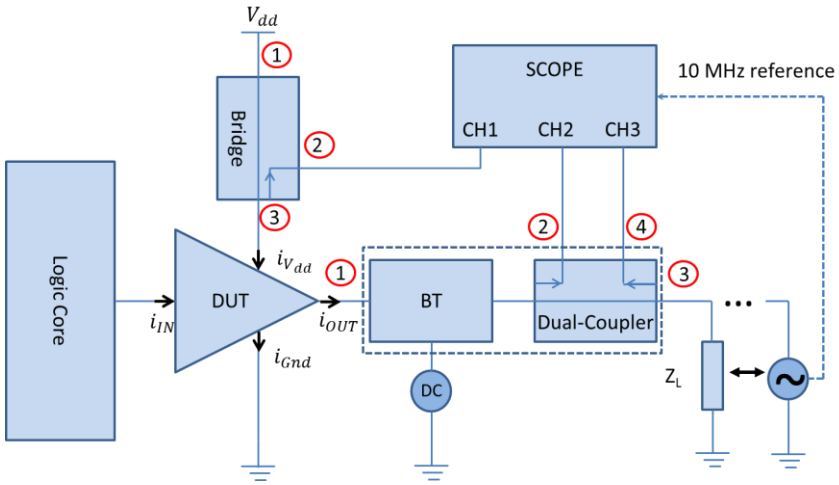

Fig. 3.14 – Measurement setup for signal and power integrity characterization of high-speed digital buffers – block diagram.

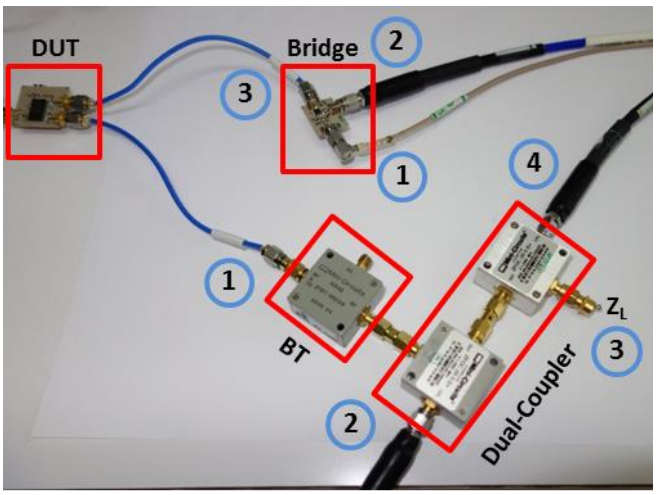

Fig. 3.15 – Measurement setup for signal and power integrity characterization of high speed digital buffers.

3.4.2 Measurement results

First the considered DUT (74LVC244 from NXP) was forced to switch with a fundamental frequency of 10 MHz. This low frequency value was chosen since it allowed performing a direct comparison against the results obtained using an available magnetic probe [41], which has a maximum specified bandwidth of 120 MHz. The determined current in port 3 of the bridge (i_{Vdd}) was compared to the current measured by the magnetic probe for two different loads, that is, $Z_L = 50\ \Omega$ and $Z_L = 100\ \Omega$. The obtained results are presented in Fig. 3.16 and Fig. 3.17. In both figures it is possible to observe that, globally, the two methods give similar results. The difference between the curves was quantified, in terms of NMSE, for the two considered loads. The obtained NMSE values for $Z_L = 50\ \Omega$ and $Z_L = 100\ \Omega$ were, respectively, -19.7 dB and -18.5 dB.

Based on the developed experimental procedure it is also possible to estimate the voltage in the V_{dd} port of the DUT (port 3). In order to get large fluctuations, on the order of 40 % of the nominal value (V_{dd} = 3.3V), a 100 MHz switching frequency was chosen. The measured voltages in the V_{dd} port, together with the output voltages, are presented in Fig. 3.18 and Fig. 3.19. In the case of $Z_L = 50\ \Omega$ is still possible to obtain an approximately square waveform at the buffer's output. However, for $Z_L = 470\ \Omega$ the power supply fluctuations severely affect the output waveform.

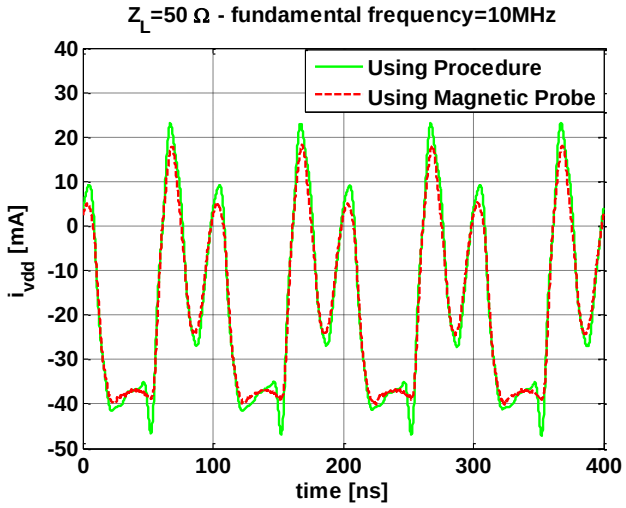

Fig. 3.16 – Measured current in the V_{dd} port using presented experimental procedure (solid line) and using magnetic probe (dashed line), Z_L=50 Ω.

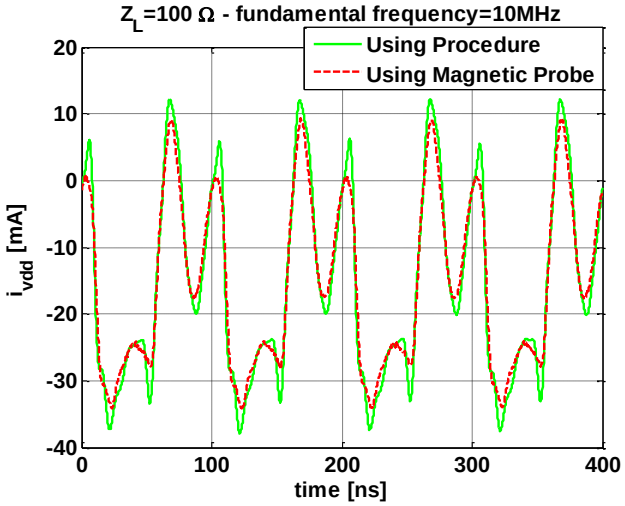

Fig. 3.17 - Measured current in the V_{dd} port using presented experimental procedure (solid line) and using magnetic probe (dashed line), Z_L=100 Ω.

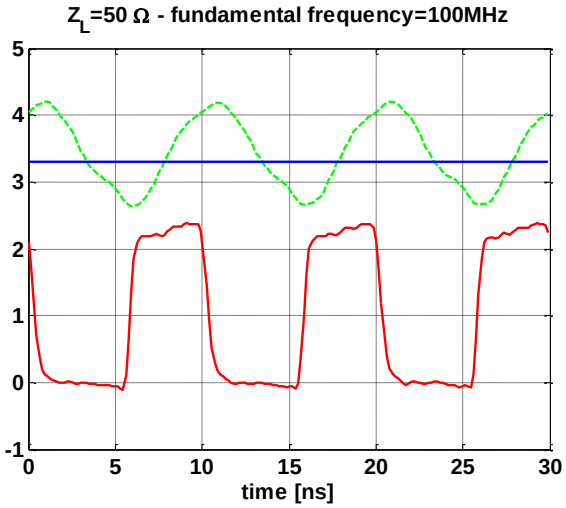

Fig. 3.18 – Measured voltages in the output port (solid line) and V_{dd} port (dashed line), Z_L=50 Ω.

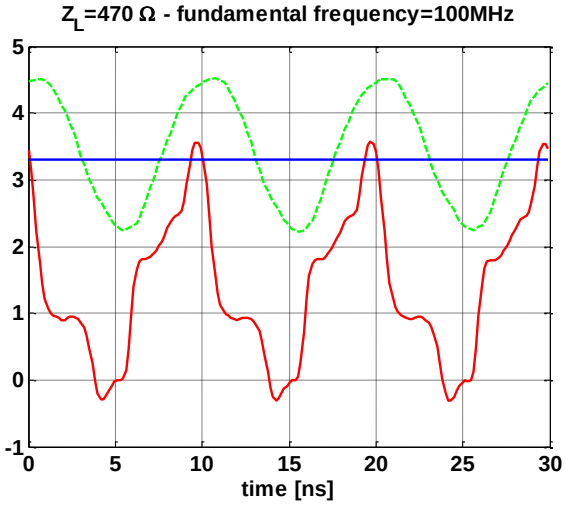

Fig. 3.19 - Measured voltages in the output port (solid line) and V_{dd} port (dashed line), Z_L=470 Ω.

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Chapter 4 - Error and Uncertainty analysis

"We may at once admit that any inference from the particular to the general must be attended with some degree of uncertainty, but this is not the same as to admit that such inference cannot be absolutely rigorous, for the nature and degree of the uncertainty may itself be capable of a rigorous expression."

R. A. Fisher (1966, 8th ed., p. 4) *The Design of Experiments*

The result of a measurement is only an approximation (or estimate) of the value of the specific quantity subject to the measurement, that is the measurand. Since the measurement error is never known, due to the lack of knowledge of the *true* value, the measurement result is complete only when accompanied by a quantitative statement of the uncertainty. So, the main goal of this chapter is to quantify the uncertainty associated to the developed measurement setup. The uncertainty analysis is focused on the proposed setup of Section 3.1, nevertheless, this analysis can be easily extended to the multi-port approach of Section 3.4. The obtained uncertainty results were also compared to the approach of Section 1.2.4, which makes use of a SMD resistor to determine the buffer's output voltage and current. For now, in Section 4.1, the most important concepts that constitute an uncertainty analysis are presented.

4.1 Overview and Terminology

The measurement uncertainty is defined accordingly to the GUM (Guide to the Expression of Uncertainty in Measurement) [42] as the *"parameter, associated with the result of a measurement that characterizes the dispersion of values that could reasonably be attributed to the measurand*".

The measurement error, traditionally, is viewed as being constituted by a combination of systematic and random errors. The random error varies when a measurement is repeated under the same conditions. On the other hand, the systematic

error remains fixed under the same measurement conditions. Fig. 4.1, Fig. 4.2 and Fig. 4.3 illustrate the definitions of error, random error and systematic error. The systematic error can be corrected by calibration. If the calibration coefficient is a value that is added algebraically to the uncorrected measurement result, it is called correction. For the situations where the calibration coefficient multiplies the uncorrected measurement result, the term numerical factor is adopted. Note that since the systematic error cannot be known perfectly, for example due to an incomplete knowledge of the calibration standards, a residual systematic error remains after all known corrections have been applied. In this case the correction or correction factor itself has an uncertainty.

An uncertainty analysis accounts for both systematic and random errors. Usually, a measurand Y is not measured directly but is calculated from other measured quantities $X_1, X_2, \dots, X_N$ through a functional relation f:

$$Y = f(X_1, X_2, \dots, X_N). \quad \textbf{(4.1)}$$

In Fig. 4.4 are presented the different constitutive blocks of a general uncertainty analysis. The next sub-sections will be dedicated to describe each of these blocks.

4.1.1 Classification of Components of Uncertainty (Type A or B)

The measured input quantities $(X_1, X_2, \dots, X_N)$, can be grouped depending on the way that its uncertainty is evaluated:

- **Type A –** evaluation by statistical analysis;
- **Type B –** evaluation by any other means.

For example, if the measured input quantity X_1 is observed M times, under the same conditions of measurement, and its estimate x_1 and uncertainty $u(x_1)$ are evaluated accordingly to (4.2) and (4.3), respectively, the input quantity X_1 is of Type A; X_1^k is the observed value of X_1 at the realization k.

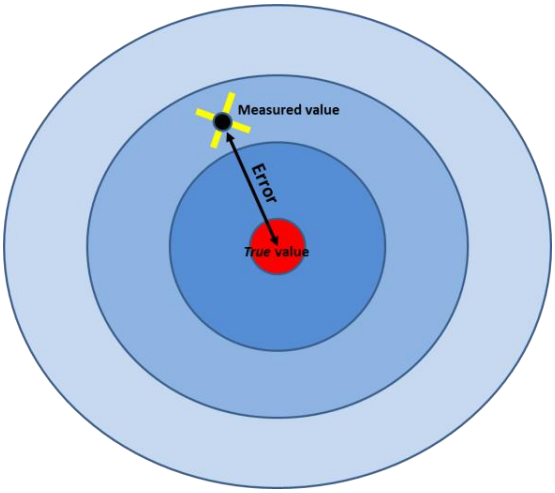

Fig. 4.1 – Illustration of the measurement error concept.

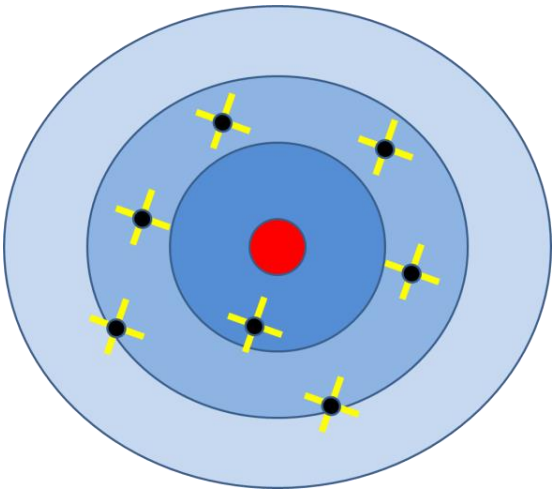

Fig. 4.2 – Illustration of the random error concept.

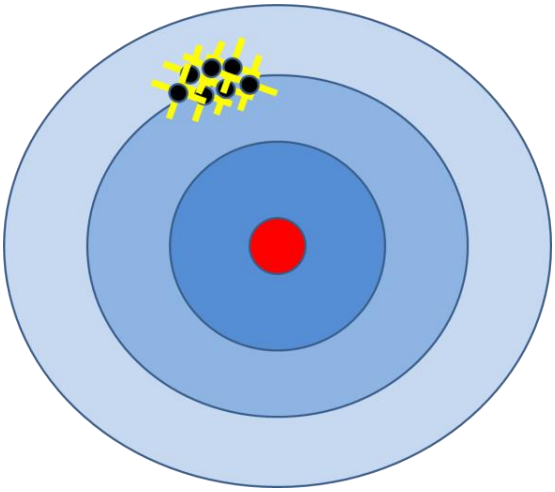

Fig. 4.3 – Illustration of the systematic error concept.

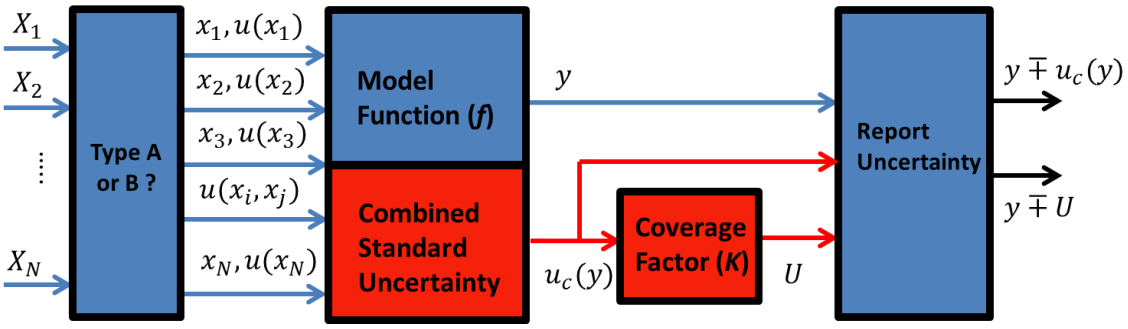

Fig. 4.4 – Flow chart describing the several blocks of an uncertainty analysis.

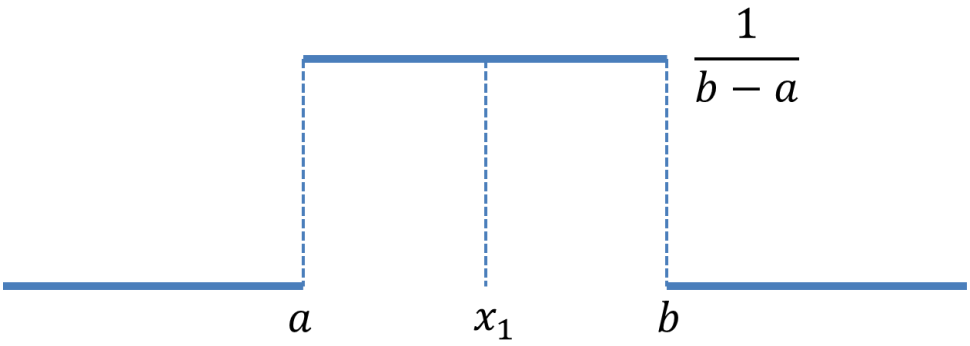

Fig. 4.5 – Uniform Probability Density Function (PDF).

$$x_1 = \overline{X_1} = \frac{1}{M}\sum_{k=1}^{M} X_1^k \tag{4.2}$$

$$u(x_1) = \sigma(X_1) = \left(\frac{1}{M-1}\sum_{k=1}^{M}\left(X_1^k - \overline{X_1}\right)^2\right)^{1/2} \tag{4.3}$$

Now follows an example of a Type B uncertainty. Let us consider that, for some reason, it is not possible to get M samples of the input quantity X_1, preventing statistics calculation, but it is known that X_1 follows a uniform distribution (probability theory) with upper bound b and lower bound a (see Fig. 4.5). In this case the input estimate x_1 and uncertainty $u(x_1)$ can be given, respectively, by the expectation and square root of the variance, as it is shown in (4.4) and (4.5).

The classification of the uncertainties, together with the determination of their values, should be performed for all the input quantities $(X_1, X_2, \ldots, X_N)$ that affect the estimation of the output quantity Y. After the determination of the uncertainty values it is

necessary to somehow combine the different values to determine the uncertainty of the output, $u_c(y)$. This is addressed in detail in the next sub-section.

$$x_1 = E[X_1] = \frac{a+b}{2} \tag{4.4}$$

$$u(x_1) = (E(X_1 - E[X_1])^2)^{1/2} = (E[X_1^2] - E[X_1]^2)^{1/2} = \frac{b-a}{\sqrt{12}} \tag{4.5}$$

4.1.2 Combined Standard Uncertainty

After obtaining estimates $(x_1, x_2, \dots, x_N)$ for the input quantities $(X_1, X_2, \dots, X_N)$, and respective uncertainties $(u(x_1), u(x_2), \dots, u(x_N))$, it is necessary to determine an estimate (y) for the output quantity Y together with its uncertainty value $u_c(y)$. The output estimate is simply given by,

$$y = f(x_1, x_2, \dots, x_n). \tag{4.6}$$

It remains now the determination of the uncertainty associated with the result provided by (4.6). Towards that goal a first order Taylor approximation, at point $(x_1, x_2, \dots, x_n)$, is considered for f,

$$Y = y + \sum_{i=1}^{N} \frac{\partial f}{\partial X_i}(X_i - x_i). \tag{4.7}$$

From (4.7) it is possible to derive the variance of Y, as it follows:

$$var[Y] = E[(Y - E[Y])^2]. \tag{4.8}$$

The expected value of Y, $E[Y]$, can be obtained from (4.9) and (4.10).

$$E[Y] = E[y] + \sum_{i=1}^{N} \frac{\partial f}{\partial X_i}(E[X_i] - E[x_i]) \tag{4.9}$$

$$E[Y] = y + \sum_{i=1}^{N} \frac{\partial f}{\partial X_i} x_i - \sum_{i=1}^{N} \frac{\partial f}{\partial X_i} x_i = y \tag{4.10}$$

Finally, substituting $E[Y]$ in (4.8), and then considering (4.7), it is possible to determine the variance of the output variable Y, as it is presented below [43].

$$var[Y] = E\left[\left(\sum_{i=1}^{N} \frac{\partial f}{\partial X_i}(X_i - x_i)\right)^2\right] \tag{4.11}$$

$$var[Y] = E\left[\sum_{i=1}^{N} \frac{\partial f}{\partial X_i}(X_i - x_i) \sum_{j=1}^{N} \frac{\partial f}{\partial X_j}(X_j - x_j)\right] \tag{4.12}$$

$$\begin{aligned} var[Y] = E\Bigg[&\sum_{i=1}^{N} \left(\frac{\partial f}{\partial X_i}\right)^2 (X_i - x_i)^2 \\ &+ 2\sum_{i=1}^{N-1} \sum_{j=i+1}^{N} \left(\frac{\partial f}{\partial X_i}\right)\left(\frac{\partial f}{\partial X_j}\right)(X_i - x_i)(X_j - x_j)\Bigg] \end{aligned} \tag{4.13}$$

$$var[Y] = \sum_{i=1}^{N} \left(\frac{\partial f}{\partial X_i}\right)^2 u^2(X_i) + 2\sum_{i=1}^{N-1} \sum_{j=i+1}^{N} \left(\frac{\partial f}{\partial X_i}\right)\left(\frac{\partial f}{\partial X_j}\right) u(X_i, X_j) \tag{4.14}$$

Thus, the uncertainty associated with y, $u_c(y)$, is simply given by the square-root of (4.14). Equation (4.14) also highlights that possible correlations between the input variables should be taken into account. The correlations are described by the covariance between the two variables, $u(X_i, X_j)$, which is given by (4.15).

$$u(X_i, X_j) = E\left[(X_i - \bar{X}_i)(X_j - \bar{X}_j)\right] \quad \textbf{(4.15)}$$

The combined standard uncertainty, also known as law of propagation of uncertainty, can be represented in a more compact format [44]. To illustrate this let us consider now the more generic case of two output variables, Y_1 and Y_2, which are related to the N input variables $(X_1, X_2, \dots, X_N)$ as it follows.

$$Y_1 = f_1(X_1, X_2, \dots, X_N) \quad \textbf{(4.16)}$$

$$Y_2 = f_2(X_1, X_2, \dots, X_N) \quad \textbf{(4.17)}$$

In matrix form, the law of propagation of uncertainty states [45],[46], [47]:

$$V(\vec{Y}) = JV(\vec{X})J^T \quad \textbf{(4.18)}$$

where $V(\vec{X})$ and $V(\vec{Y})$ are the covariance matrices of the input and output vectors respectively and J is the Jacobian matrix of the transformations f_1 and f_2. The Jacobian matrix for this case (two output variables and N input variables) is given by (4.19).

$$J = \begin{bmatrix} \frac{\partial f_1}{\partial X_1} & \cdots & \frac{\partial f_1}{\partial X_N} \\ \frac{\partial f_2}{\partial X_1} & \cdots & \frac{\partial f_2}{\partial X_N} \end{bmatrix} \quad \textbf{(4.19)}$$

The covariance matrix of the input vector is an (NxN) matrix which expresses the uncertainty in the N input quantities (including the effect of correlation). It is defined as presented in (4.20). The diagonal elements of the covariance matrix represent squared standard uncertainties (variances) while the off-diagonal elements represent covariance terms. The covariance matrix of the output (see (4.21)) is a (2x2) matrix which expresses the uncertainty in the 2 output quantities (including the correlation effect).

$$V(\vec{X}) = \begin{bmatrix} u^2(X_1) & u(X_1,X_2) & \dots & u(X_1,X_N) \\ u(X_2,X_1) & u^2(X_2) & \dots & u(X_2,X_N) \\ \vdots & \vdots & \ddots & \vdots \\ u(X_N,X_1) & u(X_N,X_2) & \dots & u^2(X_N) \end{bmatrix} \quad \textbf{(4.20)}$$

$$V(\vec{Y}) = \begin{bmatrix} u^2(Y_1) & u(Y_1,Y_2) \\ u(Y_2,Y_1) & u^2(Y_2) \end{bmatrix} \quad \textbf{(4.21)}$$

4.1.3 Coverage Factor and Uncertainty Report

It is common to multiply the combined standard uncertainty, $u_c(y)$, by a factor, k, chosen so that the interval $y \pm ku_c(y)$ has a specified high probability of containing the true value of the measurand. The product $U = ku_c(y)$ is known in GUM as the expanded uncertainty, k is the coverage factor (often $k = 2$ or 3) and the probability that $y \pm U$ contains the true value is called the coverage probability, p.

The final stage of an uncertainty analysis consists of reporting the uncertainty (see Fig. 4.4), either the combined standard uncertainty, $u_c(y)$, or the expanded uncertainty, U. In the latter case the coverage factor (k) should always be stated and, if possible, the approximate coverage probability, p.

4.2 Uncertainty Analysis

After presenting the basic concepts that define an uncertainty analysis, in this section an uncertainty study is presented for both the state of the art experimental procedure of Section 1.2.4 [11] and the novel approach introduced in Chapter 3. A comparison is performed for the two cases. The uncertainty study focused on the estimation of the buffer's output current. The same approach can be easily applied to other measured quantities, such as the output voltage, or even to a multi-port measurement setup.

4.2.1 State of the Art Approach

In Section 1.2.4 [11] the output buffer's current, $i_o(t)$, was estimated, as it follows,

$$i_o(t) = C_p \frac{dv_o(t)}{dt} + \frac{[v_o(t) - v_2(t)]}{R_s}, \quad \textbf{(4.22)}$$

where the current was determined, indirectly, from the differential measurement of the voltage drop across a surface mount test resistor (R_s). Since the result of a measurement is always accompanied with a certainty uncertainty, due to the non-ideal behavior of the instruments, it is natural that the uncertainty associated with the voltage drop will influence the estimation of the buffer's output current. This is not only true for the voltage drop, $v_o(t) - v_2(t)$, but also to any measured quantity affecting, $i_o(t)$, such as R_s or C_p.

Following the procedure of [48], the uncertainty associated with the measured voltage at any instant of time ($\sigma_{v(t_i)}$), can be given by:

$$\sigma_{v(t_i)} = \sqrt{\sigma_v^2 + \left(\frac{dv(t_i)}{dt}\right)^2 \sigma_t^2} \quad \textbf{(4.23)}$$

where σ_t and σ_v represent the standard deviation associated with the horizontal (time) and vertical (voltage) scales, respectively. If it is assumed that the bandwidth of the oscilloscope, used to measure $v_o(t)$ and $v_2(t)$, is much higher than the signal's bandwidth, then the second term in (4.23) can be neglected and the error is independent of time.

As a first approximation, it was considered that the probe's parasitic capacitances (C_p) were negligible. In this case, and assuming that the errors associated with the variables $v_o(t)$, $v_2(t)$ and R_s are statistically independent, the uncertainty associated with the measured output current $i_o(t)$ is given by (4.24), where the uncertainties in $i_o(t)$ due to $v_o(t)$, $v_2(t)$ and R_s are denoted by $\sigma_{i_{o1}}$, $\sigma_{i_{o2}}$ and σ_{i_R}, respectively. This is simply the definition of the combined standard uncertainty for uncorrelated variables (see Section 4.1.2).

$$\sigma_{i_o} = \sqrt{\sigma_{i_{o1}}^2 + \sigma_{i_{o2}}^2 + \sigma_{i_R}^2} \tag{4.24}$$

For example, the uncertainty in the determination of $i_o(t)$ due to the uncertainty in the measurement of $v_o(t)$, $\sigma_{i_{o1}}$, can be determined as is described in (4.25), in which i_o is given by (4.22).

$$\sigma_{i_{o1}} = \frac{\partial i_o}{\partial v_o}\sigma_{v_o} \tag{4.25}$$

In order to have an idea of the uncertainty associated with the determination of the buffer's output current following the approach of [11], the values presented in Table 4, for the various uncertainties, were considered.

It was assumed a constant resistor load, Z_L=50 Ω, for the output buffer and three different test resistors: R_T=100/50/10 Ω. As far as the accuracy test is considered, it was also assumed that the current waveform is constant (see Fig. 4.6), regardless of the test resistor actually used. The value for σ_v (0.02 V) was imported from the specified oscilloscope's DPO72004B "Vertical Noise", which corresponds to 0.77 % of full-scale. In this case, the full-scale has a minimal value of about 2.5V. Regarding R_T, and for keeping similar measurement conditions with the novel approach presented in this document, it was assumed that its value was determined via one-port S-parameters measurements. These could be performed on a vector network analyser, such as the HP8753D [49], and then followed by the usage of (4.26), where Γ_T is the measured reflection coefficient and Z_o the characteristic impedance of the system ($Z_o = 50\ \Omega$).

$$R_T = Z_o \frac{1 + \Gamma_T}{1 - \Gamma_T} \tag{4.26}$$

The uncertainty associated with R_T (σ_{R_T}) can be obtained by propagating the uncertainty in Γ_T (σ_{Γ_T}) into (4.26), using the values of [49], resulting in (4.27).

$$\sigma_{R_T} = \sqrt{\left(\frac{2Z_o}{(1-\Gamma_T)^2}\sigma_{\Gamma_T}\right)^2} \tag{4.27}$$

parameter	value	Term definition
R_T	100 , 50, 10 Ω	Test resistors values
σ_{R_T}	1.91, 0.51, 0.46 Ω	Test resistors uncertainty
σ_v	0.02 V	Scope vertical noise

Table 4 – Uncertainty values for the different test resistors and measured voltage

Fig. 4.7, Fig. 4.8 and Fig. 4.9 present the associated uncertainty, considering the values of Table 4. As it is possible to observe, a maximum uncertainty of about 1.1 mA is obtained for R_T =100 Ω, while this value is slightly reduced for R_T =50 Ω. In this latter case, the uncertainty in the one-port measurement of the test resistor has a minimal value. However, as we move to lower R_T values, the current uncertainty quickly rises and reaches a maximum value of about 3.7 mA for R_T =10 Ω. If the test resistor value is further decreased, the uncertainty severely degrades, which makes this approach unsuitable when it is desirable to minimize the loading impact of the measurement setup.

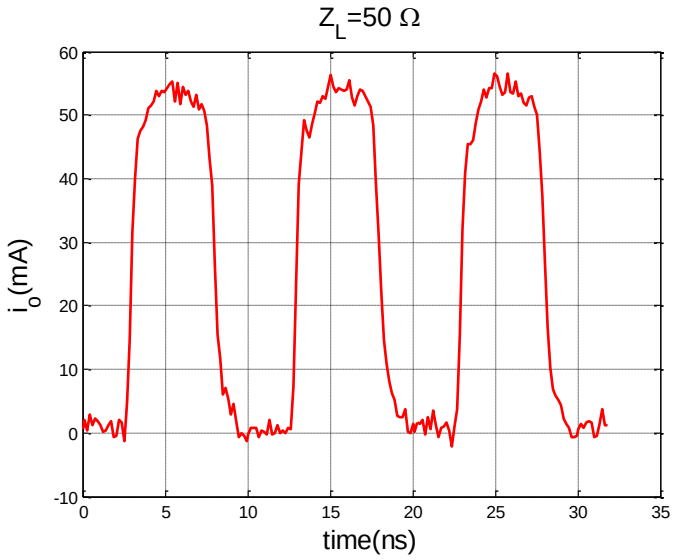

Fig. 4.6 – Measured current waveform, Z_L=50 Ω.

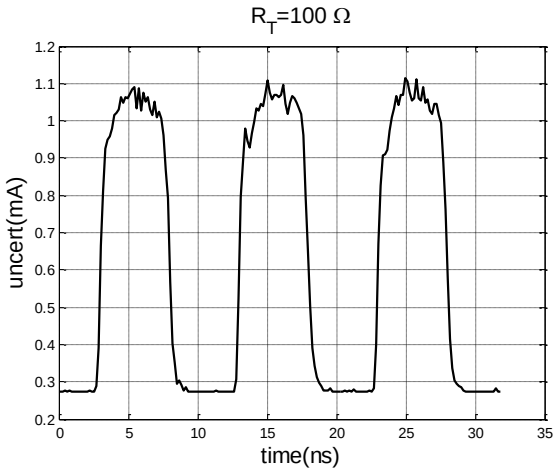

Fig. 4.7 – Output current uncertainty, R_T=100 Ω.

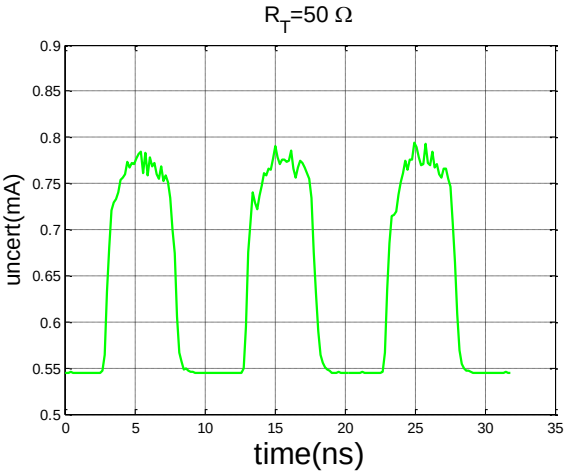

Fig. 4.8 – Output current uncertainty, R_T=50 Ω.

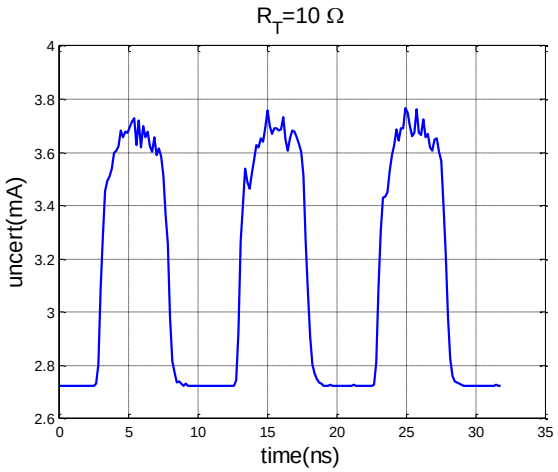

Fig. 4.9 – Output current uncertainty, R_T=10 Ω.

4.2.2 The Novel Approach

In Section 3.1 the buffer's output current was determined accordingly to (4.28), (4.29) and (4.30).

$$\frac{V_2}{V_1} = TF = \frac{S_{21}(1 - S_{33}\Gamma_L)}{1 + S_{11} - S_{33}\Gamma_L - S_{11}S_{33}\Gamma_L + S_{13}S_{31}\Gamma_L} \quad \textbf{(4.28)}$$

$$V_1 = V_2 . TF^{-1} \quad \textbf{(4.29)}$$

$$i_o = IFFT\left(\frac{V_1}{Z_1}\right) \quad \textbf{(4.30)}$$

So, the uncertainties in all the measured quantities have to be propagated through these equations. First, it is important to note that the Fourier transform (and its inverse) is a linear operator, which simplifies the uncertainty propagation analysis [50]. Since the signal was measured on the coupling port of the FWC (20 dB below the main line voltage), and taking into account the assumptions previously made to choose σ_v, the considered value for σ_v was 0.002 V (which guarantees the same relative error).

Regarding the uncertainties associated with the measured S-parameters, the values (transmission and reflection) provided for the HP8753D Network Analyzer [49] were used, where it is assumed that the real and imaginary parts are independent stochastic variables.

In this case, the typical matrix form of the law of propagation of uncertainty of (4.31), which relates the covariance matrices of the input $\left(V\left(\vec{X}\right)\right)$ and output vectors $\left(V\left(\overrightarrow{I_1}\right)\right)$ though the Jacobian matrix (see Section 4.1.2), is greatly simplified, resulting in (4.32) and (4.33),

$$V\left(\overrightarrow{I_o}\right) = JV\left(\vec{X}\right)J^T \quad \textbf{(4.31)}$$

$$\sigma^2\big(real(I_1)\big) = \sum_{i=1}^{n} \left(\frac{\partial f_1}{\partial x_i}\right)^2 \sigma^2(x_i) \tag{4.32}$$

$$\sigma^2\big(imag(I_1)\big) = \sum_{i=1}^{n} \left(\frac{\partial f_2}{\partial x_i}\right)^2 \sigma^2(x_i) \tag{4.33}$$

where f_1 and f_2 represent the mapping from the input variables $x_i(real(S_{11}), imag(S_{11}), \ldots real(V_2), imag(V_2))$ to the real and imaginary parts of I_1, respectively. After propagating the uncertainties associated with the various measured quantities into the time-domain output current, $i_o(t)$, the uncertainty representation of Fig. 4.10 was obtained. Now, for the same output current of Fig. 4.6 (measured with the proposed setup), the maximum uncertainty value is about 0.65 mA. This is close to the average value obtained for R_T=100 Ω using the approach of [11], while measurement setup loading in the buffer's output is minimal. In fact, please note that, using a test resistor of R_T =100 Ω in the approach of [11] means that for being able to measure the current of a 50 Ω load test, the actual load applied to the output buffer is 150 Ω. Before closing this section, a final remark is in order. Since the correlations between the different uncertainties (at different frequencies) were not considered, the standard uncertainty (dashed line in Fig. 4.10) does not follow the shape of the current waveform, but presents instead a nearly constant value. Nevertheless, since, for pulsed signals, neglecting these correlations results in an underestimation of the true uncertainty value (in the transition) and overestimation of it (in the steady state), in average, a reasonable uncertainty estimation is expected to be obtained. This issue was already addressed in [50], [51].

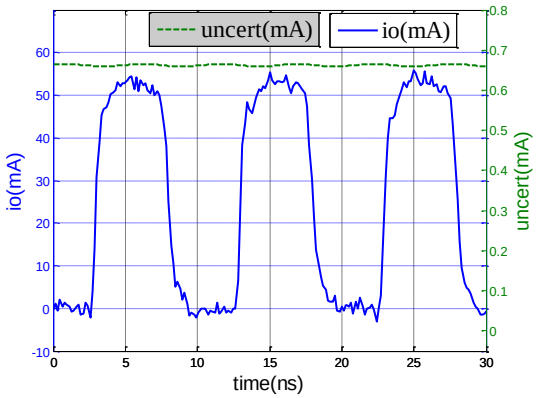

Fig. 4.10 – Output current uncertainty for the proposed approach.

4.3 Error Analysis

Throughout this document, a simplified S-parameter matrix was used for developing the presented experimental procedure. This section is devoted to quantify the error associated to these approximations. For that, this error analysis is focused on the measurement setup of Section 3.1. A similar analysis can also be performed for the multi-port approach of Section 3.4 or for the dynamic characterization of the Pull-Up/Pull-Down (Section 3.3).

In order to quantify the error associated with the approximations (see Section 3.1) performed on (3.2), the full system of (4.34), with the corresponding boundary conditions for the oscilloscope input (Γ_i) and the load (Γ_L), was implement in MATLAB as a signal flow graph, and the detailed voltage transfer function was determined using Mason's rule [28].

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3 \\ b_2 = S_{21}a_1 + S_{22}a_2 + S_{23}a_3 \\ b_3 = S_{31}a_1 + S_{32}a_2 + S_{33}a_3 \\ a_2 = \Gamma_i b_2 \\ a_3 = \Gamma_L b_3 \end{cases} \quad \textbf{(4.34)}$$

This allowed the determination of a_1 and b_1, that are, respectively, the reflected and incident waves at port 1 (the buffer's output port). Then, the frequency domain voltage and current, at the buffer's output, are given by (4.35).

$$\begin{cases} V_o = V_1 = \sqrt{Z_o}a_1 + \sqrt{Z_o}b_1 \\ I_o = -I_1 = \dfrac{b_1}{\sqrt{Z_o}} - \dfrac{a_1}{\sqrt{Z_o}} \end{cases} \quad \textbf{(4.35)}$$

After performing the IDFT of the frequency domain waveforms, the comparison (in terms of *NMSE*) between the voltage (and current) waveforms obtained for the two cases (full and approximated matrix), when the buffer was switching and $Z_L = 100\,\Omega$, is presented in Table 5. From the obtained *NMSE* values it is clear that the error associated with the approximations performed in the system of equations of (3.2) is negligible. In this way, it is confirmed the validity of the followed approach.

	$NMSE_{v,i}$ (dB)
v_o	-38.7
i_o	-36.7

Table 5 – *NMSE* values – Full vs aproximated matrices

Chapter 5 - Conclusions and Future Work

Modern wireless terminals tend to be reconfigurable. This concept demands for an increasing use of digital techniques, leading to highly heterogeneous circuits that combine: analog base-band, analog RF/Microwave and digital blocks. This change of paradigm is exposing the need of new computer aided design (CAD) tools. If, on the one hand, this will require more efficient circuit simulation methods, on the other hand this will demand for reduced order models, or system behavioral models, of both digital and analogue RF circuits.

In the case of SiP devices, the complexity, the large integration and the fast signals require the accurate prediction of the whole system performance in the early stage of the design. This motivated the development of the MOCHA project (see Chapter 2). The MOCHA project focused on the characterization and modeling of high speed memories. Within these devices, the output buffers play a key role since they perform the interface between the logic core (digital) and package/PCB parasitics (analogue/RF). In a SiP device, the long bond-wires associated with the fast transition times cause fluctuations of the power supply voltage that affect the output waveform and are difficult to predict. The situation is even worst when several buffers switch at the same time. In this way, it is fundamental to predict not only the integrity of the output signals (SI) but also of the power supply voltage (PI). So, Chapter 2 presented the test fixtures, developed inside the MOCHA project, for the signal and power integrity characterization (and modeling) of SiP devices. Both on-wafer and on-package measurements were considered. The developed approach was validated for several digital memories.

In the MOCHA project the buffer's output current was measured, indirectly, by considering the differential voltage drop on a test resistor. The chosen value for the test resistor represents a compromise that is difficult to achieve. If, on the one hand, a high value resistor is needed to maximize the signal-noise ratio of the differential voltage measurement, on the other hand, a low value resistor is desirable to minimize the loading impact of the test fixture. Moreover, it is recognized by the scientific community that this

method is only accurate for low frequencies applications ($f < 1\ GHz$). So, in Chapter 3 a novel measurement setup for the characterization (and modeling) of high-speed output buffers was presented. The developed test fixture makes use of a directional coupler, in order to estimate the buffer's output voltage and current, avoiding the use of additional test resistors. Based on a well-defined experimental procedure, a state of the art model for a commercial output buffer was extracted and validated. In Chapter 3 the developed measurement setup was also extended to allow the dynamic characterization of the Pull-Up/ Pull-Down networks (see Section 3.3). Moreover, since for SiP devices the power supply voltage cannot be considered constant, Chapter 3 closed (see Section 3.4) with a multi-port approach that allows estimating the voltage and current waveforms at both output and power ports.

Chapter 4 quantifies the uncertainty associated with the estimation of the output current. The obtained results were compared with those obtained using the test resistor method. It was observed that the developed measurement approach provides better results when it is desirable to minimize the loading effect of the measurement setup on the buffer's output.

So, the main contribution of this thesis was the development of a novel measurement setup for the characterization of devices that perform the interface between the digital and analog (RF) domains, such as the output buffers, contributing at the same time to obtain more accurate and computationally efficient models. Nevertheless, there is still a considerable amount of work to do in this area. If it is true that state of the art models predict very well the output waveforms for small variations of the power supply voltage, the same cannot be affirmed when the power supply fluctuations reach 30-40 % of the nominal value. Another issue that affects all the models that share the two-piece structure presented in Section 1.2 has to do with overclocking. In overclocking simulation, the input of the buffer is switched before the previous transition reach the steady state.

In what concerns the improvement of the developed measurement setup, a topic that should be addressed in the near future is the extraction of the buffer's package characteristics from external measurements. Then, it would be possible to separate the nonlinear dynamic contributions of the intrinsic device from the linear dynamic package effects. This would, for sure, improve the quality of the developed models for high speed digital buffers.

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Measurement Setup for RF/Digital Buffers Characterization

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***Abstract*— This paper presents a measurement setup for digital output buffers' characterization. This is of recognized importance for the integrated circuit industry and has been rarely addressed in literature referred to output buffer modeling. Currently, the model extraction is typically performed by simulating the transistor-level model of the device, which raises important issues regarding intellectual property protection, long simulation times and deembedding inaccuracies of the high-speed device mount parasitics.**

In the presented approach a well-defined experimental procedure is proposed to extract and validate a state-of-the-art model for a commercial non-inverting output buffer in packaged format.

***Index Terms*— Measurement setup, output buffer, signal integrity, behavioral model, system identification.**

I. Introduction

Nowadays, with increasing switching frequency, density and power, as well as decreasing size and reduced logic voltage level in Integrated Circuit (IC) electronic devices, the assessment of signal integrity (SI) and electromagnetic compatibility (EMC) effects is fundamental for the success of new designs. Such analysis is mainly performed by simulating the signal propagation, between the various ICs, through the traces of a printed circuit board (PCB). In this analysis, the communicating input/output buffers play a key role since they shape the signals on the PCB's interconnects, acting as an interface between the digital and the analogue (RF) domains, as shown in Fig. 1.

The most obvious and accurate approach to simulate the output buffers' behavior is based on the transistor-level (TL) model. However, this model requires a large amount of computer memory and simulation time and reveals the proprietary information of the semiconductor device designers. Alternatively, one could opt for a macro-model representation, being the IBIS [1] (Input/Output Buffer Information and Specification) model, the most widely spread and commonly used solution. The IBIS core consists of

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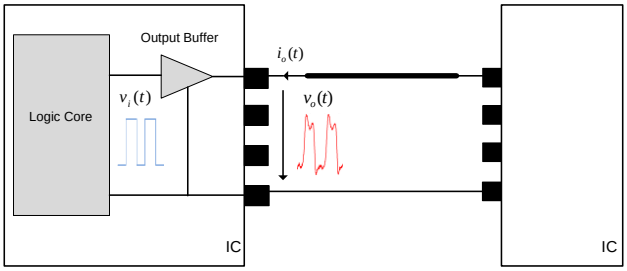

Fig. 1. Output buffer interfacing the digital and the analogue (RF) domains.

several tables (table-based model) with current, voltage and timing information and assumes a simplified equivalent circuit of the IC ports, being widely accepted by several electronic design automation (EDA) tools.

More recently, other approaches to IC macro-modeling have been proposed [2]-[4]. These are based on the estimation of parametric relationships from port voltage excitations and their corresponding current responses to a suitable set of stimuli applied to the IC ports.

For both approaches (IBIS or parametric), the model can be extracted from either simulation (TL model) or measurement results, being the former approach the one that is usually followed. However, either because of the possible unavailability of the transistor level model (usually hidden under intellectual property protection), or of the need to accurately account for the device-PCB mounting parasitics, it is desirable – and thus of recognized importance for the industry – that the model extraction from laboratory measurements is performed on a packaged device.

In [5] this issue was addressed and a dedicated test fixture was designed to extract/evaluate the parametric model of [2] from measurements. The presented extraction/evaluation procedure [5], which was based on a series resistor to indirectly measure the buffer current, was successfully validated for a real device. However, as will be highlighted in the next sections of this paper, for higher frequencies, the inserted resistor and the associated parasitic capacitances of the oscilloscope probes degrade the measurement accuracy as they introduce an undesirable effect in the device load network. Another possibility to measure the buffer current makes use of a magnetic probe [6] that can be placed over the PCB trace of interest.

Accordingly, a novel measurement setup for high-speed output buffer characterization, which indirectly measures the buffer output current and voltage from their corresponding

incident and reflect waves, is presented. The setup, based on an inexpensive directional coupler, covers a large multi-decade bandwidth (0.1 MHz - 2000 MHz) enabling the determination of the voltage and current at the buffer's output, without removing the device from its typical operation environment, as it is the case of a 50 ohm characteristic impedance transmission line.

The remaining of the paper is organized as follows. Section II briefly describes the structure that is shared by most state of the art models and, in this context, discusses the test fixture of [5]. Section III presents the new measurement setup and Section IV estimates the uncertainty associated to the determination of the buffer's output current. Section V shows the extraction and validation results of a state-of-the-art output buffer model for a commercial device. Finally, Section VI presents the conclusions of this work.

II. Typical Output Buffer Model Structure

The majority of behavioral models for output buffers shares the structure of Eq. (1) that relates the output current, $i_o(t)$, and the output voltage, $v_o(t)$ (see Fig. 1). In (1), i_H and i_L are sub-models accounting for the device behavior in the logic HIGH and LOW states, respectively, and $w_L(t)$, $w_H(t)$ are weighting functions that describe the switching between the logic states [1]-[4]. The d/dt representation in (1) indicates model dynamics herein shown as a possible dependence of i_H and i_L on successive time derivatives of $v_o(t)$.

$$i_o(t) = w_H(t) i_H\left(v_o(t), \frac{d}{dt}\right) + w_L(t) i_L\left(v_o(t), \frac{d}{dt}\right) \quad (1)$$

The sub-models i_H and i_L can be represented by either static or dynamic functions. While the IBIS model [1] considers two static look-up-tables (Pull-Up and Pull-Down) to describe the buffer's behavior in the HIGH and LOW logic states, other authors use nonlinear dynamic functions such as Radial Basis Functions (RBF) neural networks [2] and Spline functions [3]. Regarding the weighting functions, $w_H(t)$ and $w_L(t)$, these are obtained by solving (2),

$$\begin{bmatrix} w_H(t) \\ w_L(t) \end{bmatrix} = \begin{bmatrix} i_H(v_{oA}(t)) & i_L(v_{oA}(t)) \\ i_H(v_{oB}(t)) & i_L(v_{oB}(t)) \end{bmatrix}^{-1} \begin{bmatrix} i_{oA}(t) \\ i_{oB}(t) \end{bmatrix} \quad (2)$$

where waveforms $\{i_{oA}, v_{oA}\}$ and $\{i_{oB}, v_{oB}\}$ are switching signals recorded while the output buffer drives two different loads (*A* and *B*). Usually, these loads used during the extraction are those recommended by IBIS: a resistor, and a series connection of a resistor and a V_{dd} voltage source. It is important to note that, for the particular case of the IBIS model, the temporal dependence of the output current ($i_o(t)$) is entirely attributed to the weighting functions.

As mentioned in the previous section, the two-piece model of (1) is usually extracted using simulation results, requiring the availability of a TL model. In [5] it was developed a test fixture that allows model extraction from actual measurements, whose procedure is now analyzed. The equivalent circuit of that measurement setup is presented in Fig. 2, where the passive probes of the oscilloscope (whose internal impedance can be modeled as a very high resistor

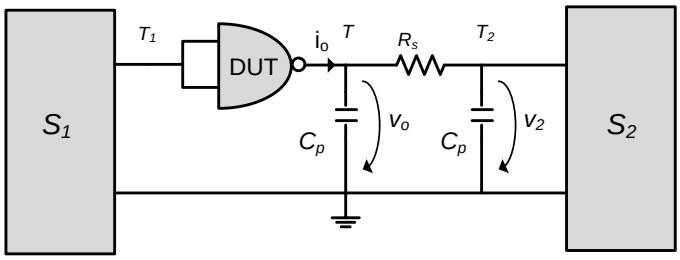

Fig. 2. Measurement setup of [5] - Equivalent circuit - $C_p = 14.1$ pF, $R_s = 100\ \Omega$.

$R = 1\ M\Omega$ in parallel with a capacitor C_p = 14.1 pF) connect to terminals T and T_2. The output buffer current, $i_o(t)$, is indirectly determined from the differential measurement of the voltage drop across the surface mount device (SMD) test resistor ($R_s = 100\ \Omega$), as it is shown in (3).

$$i_o(t) = C_p \frac{dv_o(t)}{dt} + \frac{[v_o(t) - v_2(t)]}{R_s} \quad (3)$$

In order to extract the sub-models i_H and i_L, a multifunction generator (S_2) is used to obtain a multilevel waveform in the buffer's output, whereas the logic state is set via the source S_1.

Regarding the determination of the weights $w_H(t)$ and $w_L(t)$, the procedure previously presented is followed. For that, the port is driven (via S_1) to produce a rising and a falling transition in the buffer's output and the resulting $\{i_{oA}, v_{oA}\}$ and $\{i_{oB}, v_{oB}\}$ are measured.

According to its authors, this measurement setup has some drawbacks that limit its use to low frequencies. As mentioned in [5], for higher frequencies, the resistor R_s should be characterized by means of a network analyzer. Therefore, the determination of the buffer's output current is much more complicated than what is described in (3), as this R_s may have to be treated as actual dynamic impedance.

Regarding the chosen value for R_s, some additional comments have to be made. If, on one hand, a low value is desirable to minimize its impact on the buffer's behavior; on the other hand, a high value resistor is needed to increase the voltage drop ($v_o - v_2$) and so to guarantee a certain signal-to-noise ratio, necessary for the desired measurement accuracy. Thus, the choice of the resistance value (R_s) represents a compromise, which is, quite often, difficult to solve. A possible solution to this problem could make use of a differential probe, potentially useful with comparably smaller resistances. However, this type of probe is usually expensive and so unavailable.

One other issue that should not be overlooked is the parasitic capacitance (C_p) of the oscilloscope's passive probes. For high frequencies, not only these parasitic capacitances add an undesired load on the output buffer, as their low impedance completely distorts the measured voltage (and thus current) waveforms.

In the next section it is presented a measurement setup that overcomes these problems, allowing the determination of the output current, without the need of additional resistances, when the buffer is operating in its typical environment, that is, when it drives a transmission line terminated by a certain load.

III. PROPOSED MEASUREMENT SETUP

In Fig. 3 a novel measurement setup for output buffers' characterization is presented. Instead of using a test resistor to indirectly measure the switching output current, $i_o(t)$, the proposed setup makes use of a Forward Wave Coupler (FWC). This device has 3 ports and allows to sample the incident (forward) wave in a transmission line. For illustrative purposes, the directional coupler used in the performed experiments is the Mini Circuits ZFDC-20–5, whose bandwidth stands from 0.1 to 2000 MHz. It has a coupling factor of -20 dB, a value chosen to guarantee a minimal impact on the buffer's operation, but still capable of producing accurate measurements. The coupling port of the directional coupler (port 2) connects to a high speed oscilloscope (DPO72004B – Tektronix – 20 GHz). The setup also includes bias-tees (ZFBT-6GW-Mini-Circuits - 0.1 MHz to 6000 MHz) in the input (BT1) and output (BT2) of the buffer, which permit to control the static operating point of the Pull-Up and Pull-Down transistors.

The set formed by the FWC and BT2 has been characterized, through a S-parameter matrix, in the range of 0.1 MHz - 2000 MHz, and it has been observed that, although this is a low-cost directional coupler, its directivity (S_{23}) over the specified bandwidth is quite reasonable (-30 dB in the worst case) as we will see by the associated error. Besides that, since the high-speed oscilloscope that is connected to the coupling port presents nearly 50 Ω over the entire measurement bandwidth, the following assumptions can be made: $a_2 = S_{32} = S_{23} = 0$, where a_2 is the incident wave in port 2 of the FWC (therefore, the wave reflected in the oscilloscope input), and S_{32} and S_{23} are the corresponding transmission parameters between the load (port 3) and the measurement port (port 2). In this situation, the system of equations of (4) is enough to describe the set formed by the FWC and BT2:

$$\begin{cases} b_1 = S_{11}a_1 + S_{13}a_3 \\ b_2 = S_{21}a_1 \\ b_3 = S_{31}a_1 + S_{33}a_3 \end{cases} \quad (4)$$

The boundary condition for the load Z_L (port 3) is defined by $a_3 = \Gamma_L b_3$, where Γ_L represents the load reflection coefficient in the characteristic impedance of the system (50 Ω). So, given the system of (4), it is possible to determine the voltage transfer function from port 1 to port 2 (FWC coupling port), as presented in (5).

$$\frac{V_2}{V_1} = TF = \frac{S_{21}(1 - S_{33}\Gamma_L)}{1 + S_{11} - S_{33}\Gamma_L - S_{11}S_{33}\Gamma_L + S_{13}S_{31}\Gamma_L} \quad (5)$$

In this way, the buffer's output voltage and current (port 1) can be determined by *de-embedding* the transfer function *TF*.

This is demonstrated in (6) and (7) for the buffer's output (port 1) voltage and current, respectively. There, Z_1 represents the measured impedance looking into port 1, when port 3 is terminated by the desired load and port 2 is connected to the high speed oscilloscope.

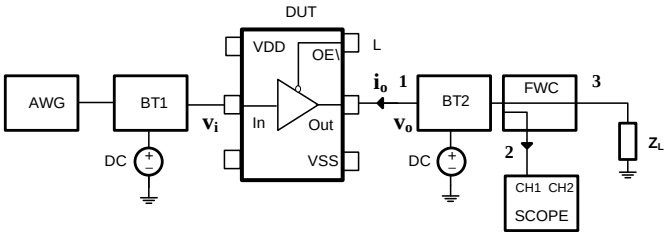

Fig. 3. Proposed Measurement setup – block diagram.

$$V_1 = V_2 . TF^{-1} \quad (6)$$

$$I_1 = \frac{V_1}{Z_1} \quad (7)$$

Finally, to recover the time domain signals, an inverse Fourier transform is applied to (6) and (7).

The error associated with the simplification performed on the S-parameters matrix was quantified. For that, the full system of (8), with the corresponding boundary conditions for the oscilloscope input (Γ_i) and the load (Γ_L), were implemented in Matlab as a signal flow graph, and the detailed voltage transfer function was determined using Mason's Rule [7].

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3 \\ b_2 = S_{21}a_1 + S_{22}a_2 + S_{23}a_3 \\ b_3 = S_{31}a_1 + S_{32}a_2 + S_{33}a_3 \\ a_2 = \Gamma_i b_2 \\ a_3 = \Gamma_L b_3 \end{cases} \quad (8)$$

This allowed the determination of a_1 and b_1 and, consequently, the frequency domain buffer's output voltage, V_o, and current, I_o:

$$\begin{cases} V_o = V_1 = \sqrt{Z_0}a_1 + \sqrt{Z_0}b_1 \\ I_o = -I_1 = \frac{b_1}{\sqrt{Z_0}} - \frac{a_1}{\sqrt{Z_0}} \end{cases} \quad (9)$$

The normalized mean square error (*NMSE* in dB) – defined by

$$NMSE_x = 10log10\left(\frac{\sum_{n=0}^{N}|x(n) - \hat{x}(n)|^2}{\sum_{n=0}^{N}|x(n)|^2}\right). \quad (10)$$

– associated with the voltage (and current) waveforms obtained for the two cases (full and approximated matrix), when the buffer is switching and Z_L=100 Ω, is presented in Table I.

TABLE I

NMSE VALUES – FULL VS APPROXIMATED MATRICES

	$NMSE_{v,i}$ (dB)
v_1	-38.7
i_1	-36.7

From these *NMSE* values it is clear that the resulting approximation error is negligible, which confirms the validity of the followed approach. In the next section, an uncertainty

analysis is presented to estimate the sensitivity of the determined quantities (output voltage and output current) to all the model parameters' errors. A comparison of the uncertainty in the proposed setup to the larger uncertainty in the setup of [5] is also provided.

IV. Uncertainty Analysis

Following the procedure of [8] the total uncertainty in the measured voltage at any instant of time ($\sigma_{v(t_i)}$) can be given by:

$$\sigma_{v(t_i)}^2 = \sigma_v^2 + \left(\frac{dv(t_i)}{dt}\right)^2 \sigma_t^2 \tag{11}$$

where σ_t and σ_v represent the standard deviation associated to the horizontal (time) and vertical (voltage) scales, respectively.

If it is assumed that the bandwidth of the oscilloscope is much higher than the signal's bandwidth, then the second term in (11) can be neglected and the error is independent of time.

For the approach followed in [5], the current is estimated using (3). Let us consider, as a first approximation, that the probes' parasitic capacitances (C_p) are negligible. In this case, and assuming that the errors associated to the variables $v_o(t)$, $v_2(t)$ and R_s are statistically independent, the uncertainty associated to the measured output current $i_o(t)$ is given by (12), where the uncertainty in $i_o(t)$ due to $v_o(t)$, $v_2(t)$ and R_s are denoted by $\sigma_{i_{o1}}$, $\sigma_{i_{o2}}$ and σ_{i_R}, respectively.

$$\sigma_{i_o} = \sqrt{\sigma_{i_{o1}}^2 + \sigma_{i_{o2}}^2 + \sigma_{i_R}^2} \tag{12}$$

For example, the uncertainty in the determination of $i_o(t)$ due to the uncertainty in the measurement of $v_o(t)$, $\sigma_{i_{o1}}$, can be determined as is described in (13),

$$\sigma_{i_{o1}} = \frac{\partial i_o(v_o)}{\partial v_o}\sigma_{v_o} \tag{13}$$

in which $i_o(v_o)$ is given by (3). In order to have an idea of the uncertainty associated to the determination of the buffer's output current following the approach of [5], the values presented in Table II, for the various uncertainties, are considered. We will assume that we wanted to test our output buffer under a constant resistor load of, say, Z_L=50 Ω, and that three different test resistors are to be considered: R_T=100/50/10 Ω. As far as the accuracy test is considered, we will also assume that the current waveform is constant, regardless of the test resistor actually used.

The value for σ_v (0.02 V) was imported from the specified oscilloscope's DPO72004B "Vertical Noise", which values 0.77% of full-scale. In this case, it has a minimal value of about 2.5V. Regarding R_T, and in order to keep similar measurement conditions with the approach presented in this paper, it is assumed that its value is determined via one-port S-parameters measurements. These could be performed on a vector network analyzer such as the HP8753D [10], then followed by the usage of (14), where Γ_T is the measured reflection coefficient and Z_o the characteristic impedance of the system ($Z_o = 50$ Ω).

$$R_T = Z_o \frac{1+\Gamma_T}{1-\Gamma_T} \tag{14}$$

The uncertainty associated to R_T (σ_{R_T}) can be obtained by propagating the uncertainty associated to Γ_T (σ_{Γ_T}) into (14), using the values of [10], resulting in (15).

$$\sigma_{R_T} = \sqrt{\left(\frac{2Z_o}{(1-\Gamma_T)^2}\sigma_{\Gamma_T}\right)^2} \tag{15}$$

Fig. 4 (a) depicts the buffer's output current (solid line), while Figs. 4 (b), (c) and (d) present the associated uncertainty, considering the values of Table II. As it is possible to observe, a maximum uncertainty of about 1.1 mA is obtained for R_T=100 Ω, while this value is slightly reduced for R_T=50 Ω. In this latter case, the uncertainty in the one-port measurement of the test resistor has a minimal value. However, as we move to lower R_T values, the current uncertainty quickly rises and reaches a maximum value of about 3.7 mA for R_T =10 Ω. If we further decrease the test resistor value, the uncertainty severely degrades, which makes this approach unsuitable when it is desirable to minimize the loading impact of the measurement setup.

Now we will consider the determination of the uncertainty propagation into (7) and, subsequently, into the correspondent time domain signal. First, it is important to note that the Fourier transform (and its inverse) is a linear operator, which simplifies the uncertainty propagation analysis [9].

Since the signal is measured on the coupling port of the FWC (20 dB below the main line voltage), and taking into account the assumptions previously made to choose σ_v, the considered value for σ_v is now 0.002 V (which guarantees the same relative error). Regarding the uncertainties associated with the measured S-parameters, the values (transmission and reflection) provided for the HP8753D Network Analyzer [10] are used, where it is assumed that the real and imaginary parts are independent stochastic variables. In this case, the typical matrix form of the law of propagation of uncertainty of (16), which relates the covariance matrices of the input $\left(V(\vec{X})\right)$ and output vectors $\left(V(\overrightarrow{I_1})\right)$ by the Jacobian matrix [11], is greatly simplified, resulting in (17) and (18),

$$V(\overrightarrow{I_1}) = JV(\vec{X})J^T \tag{16}$$

$$\sigma^2\big(real(I_1)\big) = \sum_{i=1}^{n}\left(\frac{\partial f_1}{\partial x_i}\right)^2 \sigma^2(x_i) \tag{17}$$

$$\sigma^2\big(imag(I_1)\big) = \sum_{i=1}^{n}\left(\frac{\partial f_2}{\partial x_i}\right)^2 \sigma^2(x_i) \tag{18}$$

where f_1 and f_2 represent the mapping from the input variables $x_i(real(S_{11}), imag(S_{11}), \ldots real(V_2), imag(V_2))$ to the real and imaginary parts of I_1, respectively.

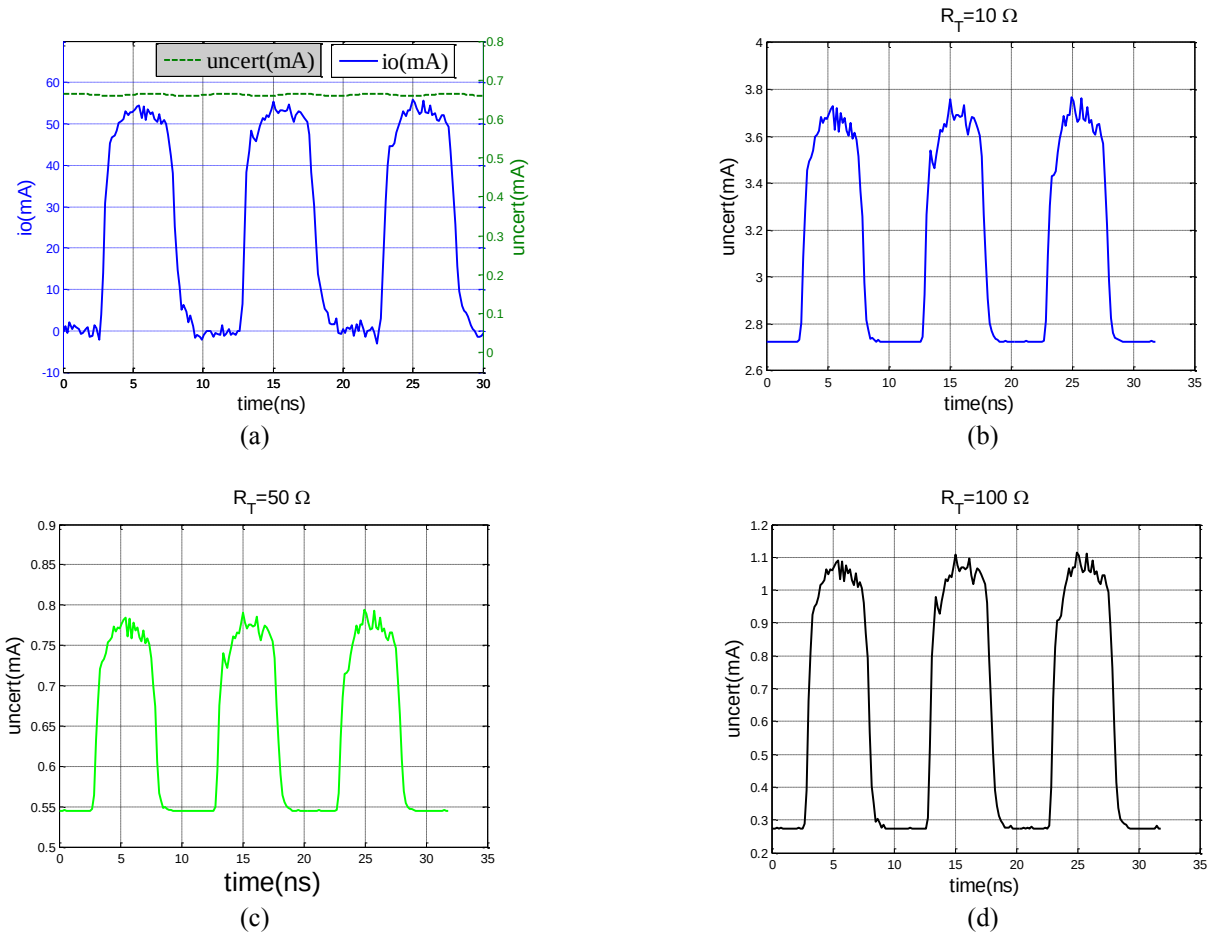

Fig. 4. (a) Output current uncertainty for the proposed approach. (b), (c) and (d) Output current uncertainty for the approach of [5] using 3 different test resistors R_T = 10 Ω, R_T = 50 Ω, R_T = 100 Ω, respectively.

TABLE II
UNCERTAINTY VALUES

parameter	value	Term definition
R_T	$100, 50, 10\ \Omega$	Test resistors values
σ_{R_T}	$1.91, 0.51, 0.46\ \Omega$	Test resistors uncertainty
σ_v	0.02 V	Scope vertical noise

After propagating the uncertainties associated with the various measured quantities into the time-domain output current $i_o(t)$, the uncertainty representation of Fig. 4 (a) is obtained (dashed line). Now, for the same output current of Fig. 4 (a) (measured with the proposed setup), the maximum uncertainty value is about 0.65 mA. This is close to the average value obtained for R_T =100 Ω using the approach of [5], while the measurement setup loading in the buffer's output is minimal. In fact, please note that, using a test resistor of R_T =100 Ω in the approach of [5], it means that for being able to measure the current of a 50 Ω load test, the actual load applied to the output buffer is 150 Ω.

Before closing this section, a final remark is in order. Since the correlations between the different uncertainties (at different frequencies) were not considered, the standard uncertainty (dashed line) does not follow the shape of the current waveform, but presents instead a nearly constant value. Nevertheless, since, for pulsed signals, neglecting these correlations results in an underestimation of the true uncertainty value (in the transition) and overestimation of it (in the steady state), in average, we expect to have a reasonable uncertainty estimation. This issue was already addressed in [9].

V. MODEL EXTRACTION

The measurement setup of Fig. 5 has been used to extract and validate the state of the art model of (1) for the 74LVC244 non-inverting output buffer from NXP Semiconductors. This device has been mounted on a test fixture (Anritsu Model 3680K). It is assumed that the functions that describe the buffer's behavior in the logic HIGH and LOW states are static, similarly to what is considered in the IBIS model. In order to obtain i_H (Pull-Up) and i_L (Pull-Down), DC voltage sources are connected at both the buffer input (BT1) and output (BT2) while no signal is applied. For the i_L sub-model, the buffer's input (In) has to be in the LOW logic state while the output is varied in a quasi-static way over a certain range. The

determination of the i_H submodel follows the same procedure, but now the buffer's input (In) has to be in the HIGH logic state (3.3V). The obtained Pull-Down and Pull-Up curves for the 74LVC244 octal buffer are presented in Fig. 6 and Fig. 7, respectively. The supply voltage of this device is V_{dd}=3.3 V and the output sweeping range (-0.5 to 3.8 V) is chosen to guarantee that the clamping diodes are not activated.

As it can be observed, the measured curves (dotted) are bounded by the IBIS MAX (strongest drive) and IBIS MIN (weakest drive), which, according to [12], is a good criterion to validate the measurement setup for this characteristic. Regarding the measurement equipment, no special requirements are needed, being the output voltage source (HP6634A-100V-1A) the most critical component because it should be able to both sink (pull-up) and source (pull-down) current; SMA adapters and cables complete the setup.

After determining the sub-models i_H and i_L, it remains the determination of the weights $w_H(t)$ and $w_L(t)$. For that, the loads (Z_L) recommended by the IBIS can be used, which consist of a resistor (50 Ω) and a series connection of a resistor and a V_{dd} battery. However, it is here assumed that $w_H(t) = 1 - w_L(t)$ and only the first load (50 Ω) is used during the extraction process. This assumption reduces the probability of obtaining an ill-conditioned matrix [13] during the inverse operation performed in (2). The switching frequency chosen for the buffer was 100 MHz. So, a sinusoidal waveform (VSG-SMU-200A from Rohde&Schwarz) is applied in the input port (through BT1) with a DC level of 1.4 V. This excitation produces a square wave of approximately 50% duty cycle in the buffer's output. After using the procedure presented in Section III for the determination of the voltage (v_o) and current (i_o), based on the sampling voltage of the directional coupler (FWC), the model is extracted for Z_L=50 Ω.

Since the directional coupler has zero transmission for direct current voltages, an offset has to be added to the estimated voltage and current curves. This value can be measured with a voltmeter in the DC port of the BT2. One issue is related with the noise level of the obtained curves. In order to increase the dynamic range of the measurement setup, and thus to observe possible mismatch effects that may be hidden in the noise, a low-pass digital filter with a cut-off frequency much higher than the maximum frequency of interest is applied.

After performing the extraction, the model is implemented in a circuit simulator (Advanced Design System from Agilent) using two SDD [14] (Symbolic Defined Device) blocks; one for i_H and another for i_L, where $w_H(t)$ and $w_L(t)$ are applied, as look-up tables, to the inputs of the SDDs. The measured and simulation results are compared for three different loads: Z_L=50 Ω (used for the extraction), Z_L=100 Ω and Z_L=470 Ω and are presented in Figs. 8, 9 and 10, respectively.

The sampling frequency used for the simulation is equal to the one used for the measurements, that is $f_s = 6.25$ GHz. Regarding the rise/fall times, values around 1 ns are measured. As it can be observed, the considered model is quite accurate for the load used during the extraction process, that is Z_L=50 Ω

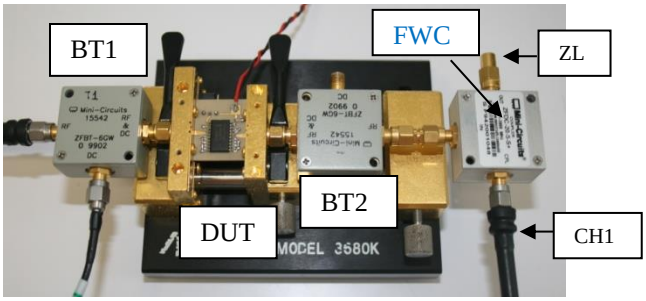

Fig. 5. Measurement setup used for the characterization of the 74LVC244 output buffer.

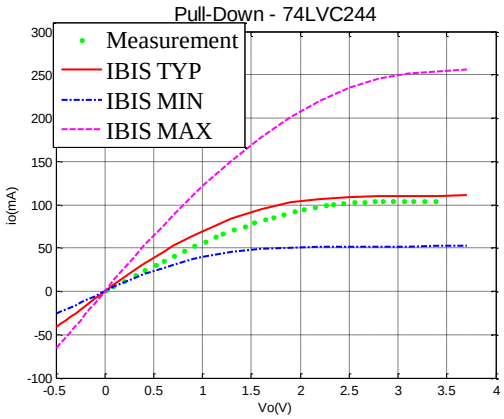

Fig. 6. Pull-Down curves for the 74LVC244 digital buffer (IBIS file vs LAB data)

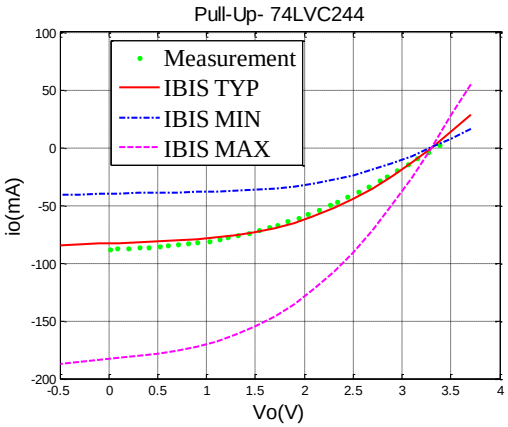

Fig. 7. Pull-Up curves for the 74LVC244 digital buffer (IBIS file vs LAB data).

However, its prediction capability is degraded as we move away from the extraction load. This problem was also observed in [15], where it is stated that the two-piece models predict accurate state transitions for loads close to those used in switching coefficient estimation but may be inaccurate for other loads. The model's load dependence can be reduced by extracting the two weighting functions for two different loads, as it is recommended by the IBIS community. In this way the approximation $w_H(t) = 1 - w_L(t)$ is avoided and the model becomes more accurate for a wider range of loads. The calculated *NMSEs* are presented in Table III.

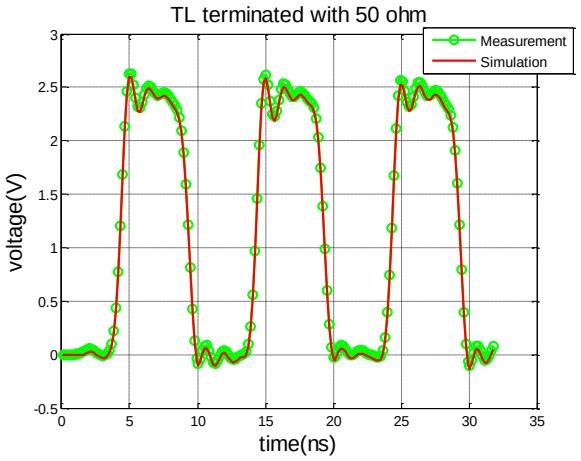

Fig. 8. Measured and simulated voltage curves for R_L=50 Ω.

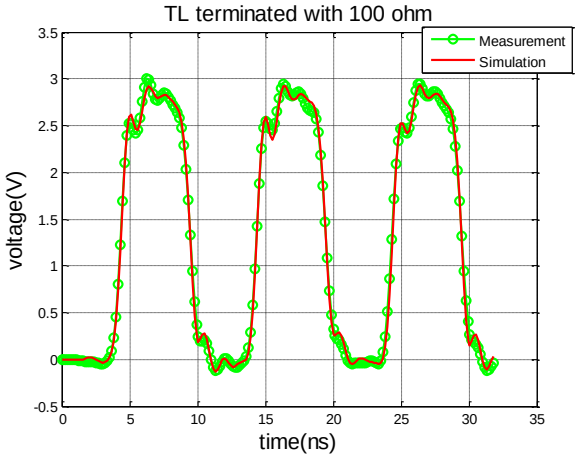

Fig. 9. Measured and simulated voltage curves for R_L=100 Ω.

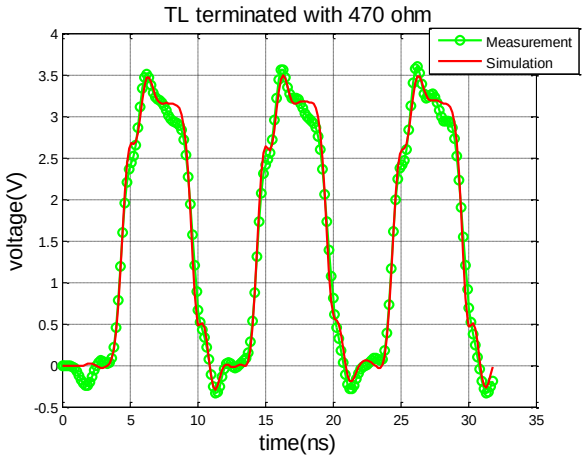

Fig. 10. Measured and simulated voltage curves for R_L=470 Ω.

TABLE III
NMSE VALUES FOR THE DIFFERENT LOADS.

Z_L (Ω)	*NMSE* (dB)
50	-33.4
100	-28.7
470	-23.4

VI. CONCLUSION

In this paper, a novel measurement setup for output buffers' characterization is presented. Currently, the existing approaches face some problems when characterizing high speed output buffers, and their application is limited to low frequencies and slow rise/fall times.

On the contrary, the proposed setup is highly flexible and allows an easy characterization of the static and dynamic behavior of high-speed output buffers. During the dynamic characterization, the buffer drives a transmission line and only a small fraction (-20 dB) of the incident wave is used for the estimation of voltage and current waveforms. In this way, the measurement setup impact on the normal operation of the buffer is minimal. To illustrate its use in a real laboratory environment, the setup was used to extract (and validate) a state-of-the-art buffer model for different loads showing the validity of this approach.

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- **[C1]** **H.M. Teixeira**, T.R. Cunha, J.C. Pedro, "Large Signal Characterization of High Speed Digital Buffers for Signal Integrity Analysis of Software-Defined-Radio Applications", accepted for presentation in the European Microwave Conference, Oct. 2013.

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Large Signal Characterization of High Speed Digital Buffers for Signal Integrity Analysis of Software-Defined-Radio Applications

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***Abstract*— The advent of the software-defined-radio (SDR) concept, has placed many of the traditional analog functions of RF wireless transceivers in the digital domain, attracting an increased interest of the RF community to the characterization and modeling of digital and mixed-mode circuits such as analog-to-digital converters, digital-to-analog converters and input/output digital buffers/drivers. Therefore, this paper presents an experimental procedure to characterize high speed packaged digital buffers under large signal regime. Based on an inexpensive RF broadband bi-directional coupler, the dynamic behavior of the Pull-Down/Pull-Up networks is determined. The test fixture effects are removed through a well-defined de-embedding procedure, allowing the determination of the voltage/current at the buffer's output. The paper also addresses the buffer's characterization under switching conditions.**

Keywords*— Calibration, S-parameters, large signal, measurement setup, output buffer.

I. INTRODUCTION

Modern wireless transceivers are moving towards the software-defined radio (SDR) concept proposed by Mitola [1]. The ideal architecture makes use of powerful digital signal processors (DSP) and extends the digital blocks' operation as close as possible to the antenna. In this way, it is not surprising that there is a growing concern regarding the characterization of the blocks that perform the interface between the analogue and digital domains, being the analog-to-digital and digital-to-analog converters (ADCs/DACs) two good examples of these circuits [2]. Within the high speed digital circuits, a similar role is played by the output buffers/drivers [3-7]. They act as an interface between the digital (logic core) and the analog RF domains (package/printed circuit board), determining the signal integrity of the transmitted data. In fact, these output buffers/drivers dominate the nonlinear dynamic behavior of the digital circuits and their high speed interconnects, demanding for a rigorous signal integrity analysis at the design stage.

In order to speed up the signal integrity analysis, macromodels are commonly used to describe the buffers' nonlinear dynamic behavior, being the IBIS model the most popular approach [3]. The IBIS is a table-based model that comprises the static I-V characteristics and the switching V-t tables. IBIS models protect the manufactures' industrial property (IP) and achieve a good compromise between accuracy and simulation speed. More recently, other approaches incorporating equivalent circuit models have been proposed [4], [5]. On the other hand some authors follow a black box approach where the buffer's behavior is described in an abstract mathematical formulation, as is the case of the artificial neural networks and spline functions [6], [7].

Typically the model extraction/validation can be performed by using characterization data obtained from either the simulation of the transistor level model (if available) or from measurements. The latter approach is not sensitive to IP issues but is rarely addressed in literature referred to output buffers' characterization [8], [9]. Moreover, for the existing solutions, either an error-corrected experimental procedure is yet to be defined or a quasi-static characterization is assumed, which neglects the buffer's important high frequency dynamic effects and requires a large number of dc bias points in order to sweep the entire operating range.

This paper presents an experimental procedure that allows to characterize a packaged high-speed digital buffer when it is operating under large signal regime. In this way, the number of required measurements to determine the buffer's behavior can be significantly reduced. After de-embedding the effects of the test fixture used to characterize the buffer, the voltage and current at the buffer's output can be determined.

This paper is organized as follows. Section II briefly discusses the approaches of [8], [9] and presents the structure shared by most state of the art output buffer models. Then, in Section III, the new experimental procedure is presented. Finally section IV presents the conclusions of this work.

II. BUFFER CHARACTERIZATION –EXISTING APPROACHES

The majority of behavioral models for output buffers share the structure of (1) that relates the output current, $i_o(t)$, and the output voltage, $v_o(t)$. In (1), i_H (Pull-Up) and i_L (Pull-Down) are sub-models accounting for the device behavior in the logic HIGH and LOW states, respectively, and $w_L(t)$, $w_H(t)$ are weighting functions that describe the switching between the logic states [3-7]. The d/dt representation in (1) indicates

$$i_o(t) = w_H(t) i_H\left(v_o(t), i_o(t), \frac{d}{dt}\right) + w_L(t) i_L\left(v_o(t), i_o(t), \frac{d}{dt}\right) \quad (1)$$

model dynamics herein shown as a possible dependence of i_H and i_L on successive time derivatives of $v_o(t)$ and $i_o(t)$.

In [8] a test fixture is presented to measure the buffer's output current, $i_o(t)$, based on the voltage drop on a surface mount device (SMD) test resistor. Since this measurement setup has some drawbacks that restrict its use to low frequencies, in [9] an alternative approach is proposed which makes use of a directional coupler to indirectly determine $i_o(t)$. The latter approach has a minimal impact on the buffer's normal operation and is suitable for the characterization of high-speed digital buffers. Nevertheless, the characterization data for the estimation of the sub-models $i_H(t)$ and $i_L(t)$ is based on a static voltage dc sweep at the output, $v_o(t)$, and, in this way, the package effects are not taken into account in these sub-models.

In the next section, an error-corrected experimental procedure is presented in which it is possible to characterize $i_H(t)$ and $i_L(t)$ under large signal conditions, keeping the buffer in it's typical operation environment, considering the package effects and reducing, at the same time, the necessary number of measurement points.

III. Test Fixture and Experimental Procedure

Fig. 1 presents the block diagram of the proposed test setup to characterize high speed digital buffers. This is similar to the one used in [9] but has been adapted to allow the large signal (LS) characterization of i_H(t) and i_L(t).

In order to measure the LS incident wave, a bi-directional coupler (instead of a single forward wave coupler - ZFDC-20-5-0.1 to 2000 MHz) is now used. Regarding the excitation signal (LS), a sine-wave (VSG-SMU-200A generator) has been chosen since, besides its ready availability in the laboratory, it exposes the buffer's dynamic behavior allowing, in this way, the extraction of state of the art models like the I-Q behavioral model of [5]. However, the characterization procedure herein presented is not limited to sinusoidal signals.

A high speed oscilloscope (DPO72004B – Tektronix – 20 GHz) has been used to measure the incident and reflected waves. In the bias-tee (BT1) a dc level is applied to guarantee that the LS spans the whole operating range (0-V_{DD}). Since the sub-models i_L and i_H are determined when the input (In) is at a fixed logic level, the arbitrary waveform generator (AWG) can be substituted by a constant dc voltage source. Both generator and high speed oscilloscope are synchronized by a 10 MHz reference.

For the determination of the buffer's output voltage and current (port 1), for both logic states at the input, let us assume the S-parameter matrix of (2), describing the four-port network of Fig.1.

$$b_i = \sum_{j=1}^{4} S_{ij} a_j \quad (2)$$

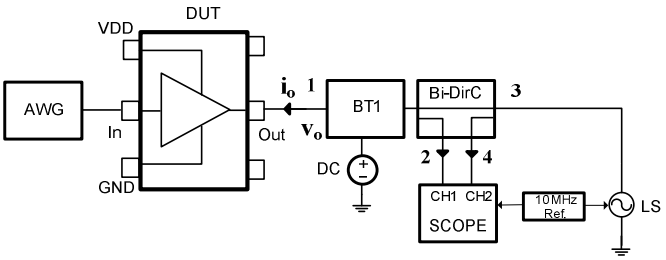

Fig. 1. Test fixture of [9] modified for large signal characterization. BT1 is a Bias-Tee and Bi-DirC a bi-directional coupler.

Although this full 4x4 system of linear equations could be easily solved numerically, we will simplify it so that the proposed characterization procedure can be explained making use of closed form expressions. Accordingly, it was considered that, for the typical operating frequencies of most high speed digital buffers, the broad bandwidth oscilloscope (SCOPE) presents an input impedance of nearly 50 Ω, which implies that $a_2, a_4 \approx 0$ in a system with characteristic impedance, $Z_o = 50\ \Omega$.

In this situation, the voltage and current at port 1, in the frequency domain, can be easily determined as it is shown in (3) and (4), respectively.

$$V_o = \left(\frac{b_2 - S_{23} a_3}{S_{21}}\right).(1 + S_{11}) + S_{13} a_3 \quad (3)$$

$$I_o = \left(\frac{b_2 - S_{23} a_3}{S_{21} Z_o}\right).(1 - S_{11}) - \frac{S_{13} a_3}{Z_o} \quad (4)$$

Since b_2 can be obtained from the time domain voltage that is monitored in channel 1 of the broad bandwidth oscilloscope only a_3 is left to be determined. If we consider that S_{41} is negligible ($S_{41} \approx -60\ dB\ @100\ MHz$) then the incident wave in port 3 (a_3) can be determined from the monitored voltage in the second channel of the high speed oscilloscope, as shown in (5).

$$a_3 = \frac{b_4}{S_{43}} \quad (5)$$

Finally to obtain the time domain signals at the buffer output port, $i_o(t)$ and $v_o(t)$, (thus, with the effect of the measurement setup de-embedded) the inverse Fourier transform is applied to (3) and (4).

For illustrative proposes, this experimental procedure has been applied in the characterization of i_H(t) and $i_L(t)$ of a commercial packaged non-inverting buffer, the NXP-74LVC244 (V_{DD}=3.3V). A 100 MHz LS has been considered and the average mode has been chosen for the high speed oscilloscope with a sampling frequency of 6.25GS/s. The measured dynamic output current for the Pull-Up (i_H) and Pull-Down (i_H), as a function of the output voltage (v_o), are represented in Figs. 2 and 3, respectively. These figures also include the static characteristics of the IBIS model provided by the manufacturer, for the Pull-Up and Pull-Down. As observed, the measured dynamic I/V characteristics cover

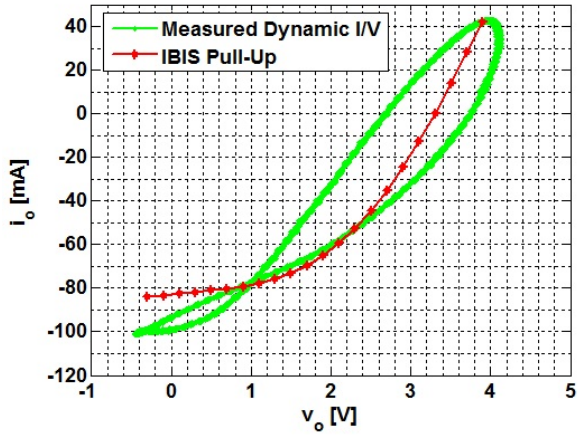

Fig. 2. Measured Pull-Up dynamic I/V characteristics and simulated IBIS static Pull-Up.

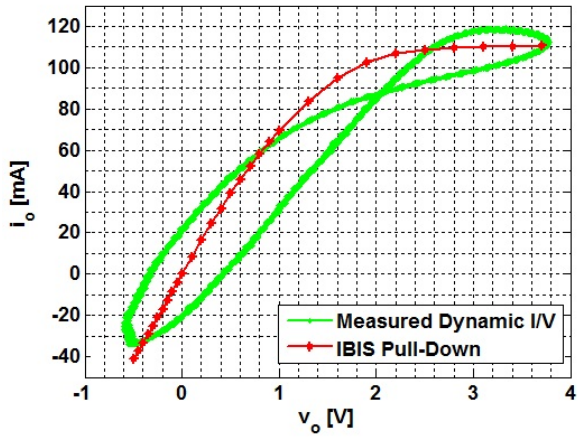

Fig. 3. Measured Pull-Down dynamic I/V characteristics and simulated IBIS static Pull-Down.

reasonably well the trajectories followed by the static characteristics of the IBIS model. Furthermore, the package and printed circuit board (PCB) parasitic effects are taken into account and, in this way, the output dynamic behavior of the buffer is characterized for the cases where the input (In) is at a fixed logical level. It is important to remember that reflections may occur even when the input (In) is already in the steady state, and that is the reason why a dynamic characterization of the Pull-Up and Pull-Down networks is highly desirable.

In order to fully characterize the buffer's behavior, only the switching behavior remains to be determined. In (1) $w_L(t)$ and $w_H(t)$ are weighting functions that describe the switching between the logic states. These can be obtained by solving (6), where waveforms $\{i_{oA}, v_{oA}\}$ and $\{i_{oB}, v_{oB}\}$ are switching signals recorded while the output buffer drives two different loads (*A* and *B*).

$$\begin{bmatrix} w_H(t) \\ w_L(t) \end{bmatrix} = \begin{bmatrix} i_H(v_{oA}(t)) & i_L(v_{oA}(t)) \\ i_H(v_{oB}(t)) & i_L(v_{oB}(t)) \end{bmatrix}^{-1} \begin{bmatrix} i_{oA}(t) \\ i_{oB}(t) \end{bmatrix} \quad (6)$$

For the measurement of the switching waveforms (voltage and current) the procedure presented in [9] is followed in this paper where the large signal generator (port 3 of Fig. 1) is now substituted by the desired loads. If the load reflection coefficient (Γ_L) is measured using a vector network analyzer (E8361C PNA from Agilent Tech.) the bi-directional coupler can be reduced to a forward wave (incident in the load) coupler, resulting in a three port network (bias-tee included). In this case the transfer function from port 1 to port 2 [9] can be given by (7); assuming now $a_2 \approx 0$ and $S_{32} = S_{23} \approx 0$.

$$\frac{V_2}{V_1} = TF = \frac{S_{21}(1 - S_{33}\Gamma_L)}{1 + S_{11} - S_{33}\Gamma_L - S_{11}S_{33}\Gamma_L + S_{13}S_{31}\Gamma_L} \quad (7)$$

The frequency domain voltage and currents are then obtained from (8) and (9), where Z_1 represents the measured impedance looking into port 1 when port 3 is terminated by the desired loads and port 2 is connected to the high speed oscilloscope. Finally, to recover the time domain signals, the inverse Fourier transform is applied to (8) and (9).

$$V_1 = V_2 . TF^{-1} \quad (8)$$

$$I_1 = \frac{V_1}{Z_1} \quad (9)$$

In order to validate the procedure previously presented, a transistor-level model (BSIM3v3 model) of a non-inverting CMOS buffer [10] has been implemented in Advanced Design System (ADS) from Agilent Tech. The implemented buffer has been loaded by the block of measured S-parameters (BT1/Bi-DirC), while a 100 Ω resistor has been chosen for the output load. A switching frequency of 100 MHz and a supply voltage V_{DD}=2.5 V have been considered for the transient simulation. After applying (8) and (9) to the obtained voltage in the coupled port, the resulting voltage (and current) have been compared with the output voltage (and current) using the ADS probes. As it is possible to observe in Fig. 4, the agreement between both curves is very good ($NMSE_{voltage}$ =-42.2 dB, $NMSE_{current}$=-38.96 dB). For illustrative proposes two SMA loads have been chosen (R_L=50 Ω and R_L=100 Ω) for the measurement results. As stated in [9], the presented experimental procedure is not restricted to these loads. Actually the weighting functions' extraction of (6) demands for two loads that avoid ill-condition problems at the time of the determination of the matrix inverse. The same commercial non-inverting buffer (NXP-74LVC244, V_{DD}=3.3V) has been forced to switch at a fundamental frequency of 100 MHz. After measuring the voltage at the coupled port of the directional coupler (port 2), the de-embedding procedure of (8) and (9) has been applied. Finally, after the inverse Fourier transform, it is possible to obtain the switching voltage and currents at port 1 (i_o,v_o) for the two loads. The obtained measurement results for R_L=50 Ω and R_L=100 Ω are presented in Figs. 5 and 6, respectively. As observed, after the rising and falling edges there are ringing effects which are associated to reflections due to impedance mismatches. In a certain way, this reinforces the idea that the Pull-Up and Pull-Down networks should be measured in a dynamic way.

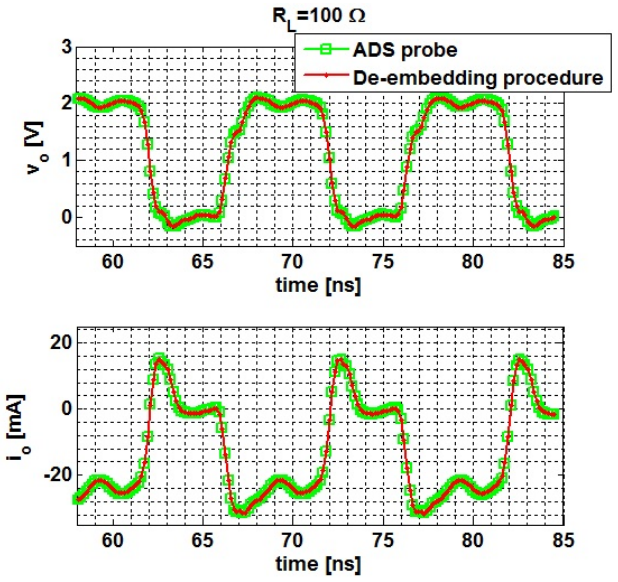

Fig. 4. Transient simulated waveforms using ADS voltage/current probes vs waveforms obtained using the de-embedding procedure.

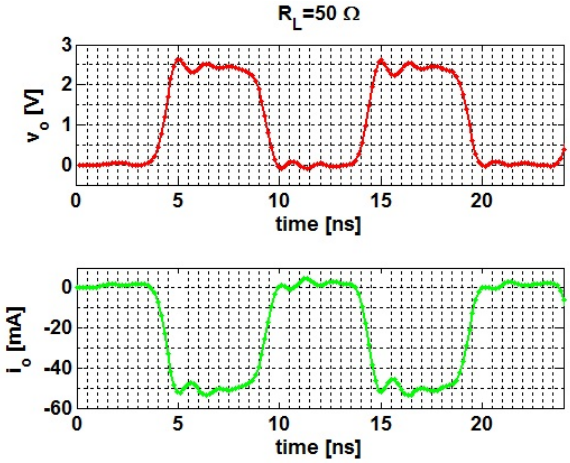

Fig. 5. Measured voltage and current switching waveforms (R_L=50 Ω).

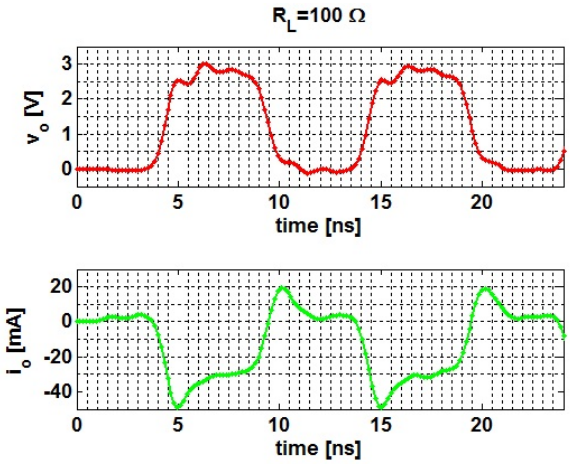

Fig. 6. Measured voltage and current switching waveforms (R_L=100 Ω).

IV. Conclusion

This paper presents an experimental procedure to characterize high speed packaged digital buffers for signal integrity analysis of software-defined-radio applications. A simple large sine wave signal is used to characterize the nonlinear dynamic behavior of the pull-up and pull-down networks, including the package effects. Compared to the quasi-static approach, the minimum number of required measurements can be significantly reduced. The presented de-embedding procedure guarantees that the measurement reference plane is at the buffer's output. Besides the characterization of the Pull-Up and Pull-Down networks, the switching behavior is also characterized by the proposed procedure.

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Curriculum Vitae

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Academic Qualifications

- PhD in Electrical Engineering, University of Aveiro, Portugal (09/2008-Present) under the supervision of Prof. José Carlos Pedro and Prof. Telmo Reis Cunha with a thesis entitled “Nonlinear Behavioral Modelling of Mixed Signal RF-Digital I/O Devices”.

- Master Degree in Electronics and Telecommunications Engineering by University of Aveiro, with a dissertation entitled “Linearizer model for RF power amplifiers”; final classification of fourteen (14) out of twenty (20).

- Final year Project in the antennas area entitled “Broadband antennas for the simultaneous reception of VHF and UHF channels (Analog and Digital)” suported by the company “Sinuta, Antenas Parabólicas Lda”; final classification of seventeen (17) out of twenty (20).

- Degree in Electronics and Telecommunications Engineering by University of Aveiro (October 2000 to July 2006) with a final classification of thirteen (13) out of twenty (20).

- Secondary Studies in Escola Secundária Dr. Manuel Gomes Almeida with a final classification of fifteen (15) out of twenty (20).

Other Courses

- Advanced studies (PhD curricular component) in Electrical Engineering, University of Aveiro (Portugal) with a final grade of fifteen (15) out of twenty (20).

- Spring doctoral school on Measuring, Modelling and Simulation of (Non) linear Dynamic Systems held from 13 May till 7 June 2013 at the Vrije University of Brussels.

Main areas of research

- Behavioral models of RF Power Amplifiers and Linearizers.
- Modelling and characterization of high speed digital buffers.
- Development of accurate RF/Digital measurement setups

Professional Experience

- Researcher in Telecommunications Institute – Aveiro, since September 1st 2006 till 31st August 2008.

Research Projects

- ModEx (Model Behavior Extractor) – 09/2006-06/2007
  - The main objective of this project was to obtain the necessary algorithms and measurement setups for establishing a certain behavioral model format of nonlinear dynamic systems found in common wireless links and its corresponding extraction laboratory bench. Following this study, and after the definition of a feedforward model for RF Power Amplifiers, a linearizer model for these devices was derived. The resultant model can be used to perform digital predistortion. All these models are supported by a well known mathematical tool called Volterra Series. During this period I also got experience with several devices (and measurement instruments) normally found in a RF laboratory.

- MOCHA (MOdelling and CHAracterization for SiP Signal and Power Integrity Analysis) – 01/2008-03/2010.
  - MOCHA – The main goal of the european project MOCHA was to develop reliable modelling and simulation solutions for SiP design verification.
    The final objectives of the project were:
    1) a demonstration of the innovative IC simulation models and their related extraction flows by both simulation and measurement;
    2) the development of an innovative 3D EM field solver;
    3) the development of a performing SiP design and verification EDA platform;
    4) a demonstration of the developed signal integrity measurement techniques.
    The partners of the project were: STMicroelectronics (leader), Agilent Technologies Belgium NV, Cadence Design Systems, Politecnico di Torino, Institute of Telecommunications of Aveiro, and Microwave Characterization Center.

Teaching Experience

- Applicational for Science and Engineering (Matlab), University of Aveiro, 1st semester (2010-2011, 2011-2012, 2012-2013).

Reviewer Activities

- IEEE Transactions on Instrumentation and Measurement (2013).
- IEEE Transactions on Electromagnetic Compatibility (2012).

Papers in Journals [4]

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- **H.M. Teixeira**, T.R. Cunha, and J.C. Pedro “Large Signal Characterization of High Speed Digital Buffers for Signal Integrity Analysis of Software-Defined-Radio Applications”, accepted in European Microwave (EuMW) Conference, October 2013, Nuremberg.
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