Universidade de Aveiro Departamento de
2013 Electrónica, Telecomunicações e Informática

Nelson José Valente da Silva

Transmissores Reconfiguráveis para Rádios Definidos por Software

Reconfigurable Transmitters for Software-Defined Radios

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Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Electrotécnica, realizada sob a orientação científica do Prof. Doutor Arnaldo Silva Rodrigues de Oliveira e do Prof. Doutor Nuno Miguel Gonçalves Borges de Carvalho, Professores do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

Apoio financeiro da FCT e do FSE no
âmbito do III Quadro Comunitário de Apoio.

FCT Fundação para a Ciência e a Tecnologia
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Doutor Pere L. Gilabert
Professor Associado da Universitat Politècnica de Catalunya

Doutor Arnaldo Silva Rodrigues de Oliveira
Professor Auxiliar da Universidade de Aveiro (orientador)

Doutor José Manuel Neto Vieira
Professor Auxiliar da Universidade de Aveiro

agradecimentos / acknowledgements

The challenging road towards a PhD degree is long and winding, where inspiring ideas typically come to light only after a long and sometimes hard research work. Nevertheless, I was fortunate to have the support of so many remarkable people who made my life so much easier.

I would like to thank my supervisors, Prof. Dr. Arnaldo Oliveira and Prof. Dr. Nuno Borges Carvalho, for their day to day support always providing guidance and constructive feedback, and for all the knowledge sharing and friendship. I am also deeply grateful to Prof. Dr. Arnaldo Oliveira for challenging me to pursue a PhD in this scientific field.

To all my friends, colleagues and staff at the Instituto de Telecomunicações and University of Aveiro alumni – in particular to Nuno Rafael, Claudia Camacho, Margarida Fernandes, Rui Fiel, Wonhoon Jang, Manuel Ventura, Alírio Boaventura, Sérgio Pires, Nuno Coutinho, Ricardo Abreu, Pedro Cruz, António Morgado, Nelson Cardoso and André Prata, thanks for many fruitful discussions, mutual support and pleasant times. I would also like to thank to Prof. Dr. José Vieira, Prof. Dr. Nuno Matos, Prof. Dr. Manuel Violas, Ulf Gustavsson and Dr. Jeffrey Pawlan for their friendship, wisdom and help.

I would like to recognize the Instituto de Telecomunicações for financial support and for providing me a rich work environment with notable research conditions. I also acknowledge the Portuguese Foundation for Science and Technology (FCT), the University of Aveiro and the Institute of Electronics and Telematics Engineering of Aveiro (IEETA) for funding and invaluable support.

To my dear friends Domingos Terra, Rui Costa, Daniel Albuquerque, Rui Santos, Nuno Oliveira and Sofia Silva, I have been fortunate to have your friendship, support and so many pleasant moments during all these years.

I would also like to give a special thanks to my family – in particular to my parents, Maria and José, to my sister Patrícia, and to Eugénia and Mário, for all your love, support and encouragement. My hard-working parents have sacrificed their lives for my sister and me and provided unconditional love and care.

Finally, to my beloved Sandra, I truly thank you for your faith in me, for all the encouragement, the unconditional support and the great patience during these last years. You give meaning to my live – words cannot describe how much I love you!

Palavras-chave Arquitecturas Reconfiguráveis, FPGA, Modulação $\Sigma\Delta$, Modulação por Largura de Pulso, Rádio Definido por Software, Transmissores RF Digitais.

Resumo

Transmissores de rádio flexíveis baseados no conceito do Rádio Definido por Software (SDR) estão a receber uma crescente importância de investigação essêncialmente devido à proliferação sem precedentes de novos *standards* de comunicações *wireless* que trabalham em frequências diferentes, usando esquemas de modulação e codificação dissimilares, estando direcionados para os mais diversos fins. Neste novo paradigma de comunicações *wireless*, a camada física do transmissor rádio tem de ser capaz de suportar a transmissão simultânea de sinais provenientes de diferentes *standards*, operando em diferentes bandas de frequências e com diferentes ritmos de transmissão, o que na prática é muito difícil ou muito ineficiente de implementar utilizando abordagens convencionais.

Contudo, os últimos desenvolvimentos nesta área incluem novas arquiteturas de transmissão inteiramente digitais onde o *datapath* do rádio é digital desde a banda base até ao RF. Tal conceito tem uma elevada flexibilidade e representa um passo importante para o desenvolvimento de transmissores baseados em SDR. No entanto, a implementação de tal rádio para cenários de comunicação reais é uma tarefa desafiadora, onde algumas limitações chave estão ainda impedindo uma maior adopção deste conceito.

Esta tese tem como principal objetivo o de investigar algumas destas limitações, propondo e implementando arquiteturas inovadoras de transmissão inteiramente digitais com inerente elevada flexibilidade e integração, e onde melhorar importantes figuras de mérito, tais como a eficiência de codificação, a relação sinal-ruído, a largura de banda utilizável e o ruído dentro e fora da banda também serão abordadas.

Na primeira parte deste trabalho é introduzido o conceito de transmissão de dados RF utilizando uma abordagem totalmente digital, baseada em modulação por impulsos. Uma comparação entre diversas tecnologias de implementação é também apresentada, permitindo afirmar que as FPGAs actuais oferecem um compromisso interessante entre desempenho, eficiência de energia e flexibilidade, tornando-as uma escolha interessante como uma tecnologia de implementação com elevado potêncial para transmissores completamente digitais baseados em moduladores pulsados.

Após esta discussão são apresentados os conceitos fundamentais inerentes aos moduladores pulsados e introduzidos os avanços relativos a transmissores RF modulados por pulsos, juntamente com vários exemplos de arquiteturas do estado da arte encontrados na literatura.

Em seguida, o núcleo desta tese contendo os principais desenvolvimentos alcançados durante este trabalho de doutoramento é apresentado e discutido.

O primeiro contributo fundamental para o estado da arte aqui apresentado consiste no desenvolvimento e integração em FPGA de uma nova arquitetura de transmissão inteiramente digital, baseada em moduladores $\Sigma\Delta$ e dotada de uma elevada flexibilidade e integração, sendo capaz de transmitir dados de multiplos *standards* e em multiplas bandas de RF.

Uma segunda contribuição chave relativa à transmissão simultânea de vários sinais RF é então introduzida, sendo apresentadas e descritas novas arquiteturas de transmissão de sinal RF inteiramente digitais, as quais tiram proveito de serializadores de dados multi-gigabit disponíveis em FPGAs atuais de alto desempenho. Melhorias adicionais a esta abordagem permitiram desenvolver uma arquitetura de transmissão com duas fases de conversão na frequência, a qual permite a transmissão concorrente de sinais *multistandard* e multicanal com ajuste fino na frequência.

Por último, foram ainda investigadas diversas técnicas que visam reduzir duas limitações fundamentais inerentes aos actuais transmissores completamente digitais, nomeadamente, a baixa eficiência de codificação dos moduladores pulsados e o elevado fator de qualidade combinado com elevados requisitos de adaptabilidade na frequencia do filtro de reconstrução do sinal RF a transmitir. A abordagem seguida baseada em multiplos caminhos polifásicos permitiu desenvolver uma nova arquitetura de transmissão integrada em FPGA que melhora de forma significativa importantes figuras de mérito, tais como a eficiência de codificação e SNR, enquanto mantém a elevada flexibilidade que é necessária para suportar a transmissão de dados multimodo e multicanal.

Keywords FPGA, Pulse Width Modulation, $\Sigma\Delta$ Modulation, Reconfigurable Architectures, Software-Defined Radio, All-Digital RF Transmitters.

Abstract

Flexible radio transmitters based on the Software-Defined Radio (SDR) concept are gaining an increased research importance due to the unparalleled proliferation of new wireless standards operating at different frequencies, using dissimilar coding and modulation schemes, and targeted for different ends. In this new wireless communications paradigm, the physical layer of the radio transmitter must be able to support the simultaneous transmission of multi-band, multi-rate, multi-standard signals, which in practice is very hard or very inefficient to implement using conventional approaches.

Nevertheless, the last developments in this field include novel all-digital transmitter architectures where the radio datapath is digital from the baseband up to the RF stage. Such concept has inherent high flexibility and poses an important step towards the development of SDR-based transmitters. However, the truth is that implementing such radio for a real world communications scenario is a challenging task, where a few key limitations are still preventing a wider adoption of this concept.

This thesis aims exactly to address some of these limitations by proposing and implementing innovative all-digital transmitter architectures with inherent higher flexibility and integration, and where improving important figures of merit, such as coding efficiency, signal-to-noise ratio, usable bandwidth and in-band and out-of-band noise will also be addressed.

In the first part of this thesis, the concept of transmitting RF data using an entirely digital approach based on pulsed modulation is introduced. A comparison between several implementation technologies is also presented, allowing to state that FPGAs provide an interesting compromise between performance, power efficiency and flexibility, thus making them an interesting choice as an enabling technology for pulse-based all-digital transmitters.

Following this discussion, the fundamental concepts inherent to pulsed modulators, its key advantages, main limitations and typical enhancements suitable for all-digital transmitters are also presented. The recent advances regarding the two most common classes of pulse modulated transmitters, namely the RF and the baseband-level are introduced, along with several examples of state-of-the-art architectures found on the literature.

The core of this dissertation containing the main developments achieved during this PhD work is then presented and discussed. The first key contribution to the state-of-the-art presented here consists in the development of a novel $\Sigma\Delta$-based all-digital transmitter architecture capable of multiband and multi-standard data transmission in a very flexible and integrated way, where the pulsed RF output operating in the microwave frequency range is generated inside a single FPGA device.

A fundamental contribution regarding the simultaneous transmission of multiple RF signals is then introduced by presenting and describing novel all-digital transmitter architectures that take advantage of multi-gigabit data serializers available on current high-end FPGAs in order to transmit in a time-interleaved approach multiple independent RF carriers. Further improvements in this design approach allowed to provide a two-stage up-conversion transmitter architecture enabling the fine frequency tuning of concurrent multichannel multistandard signals.

Finally, further improvements regarding two key limitations inherent to current all-digital transmitter approaches are then addressed, namely the poor coding efficiency and the combined high quality factor and tunability requirements of the RF output filter. The followed design approach based on poliphase multipath circuits allowed to create a new FPGA-embedded agile transmitter architecture that significantly improves important figures of merit, such as coding efficiency and SNR, while maintains the high flexibility that is required for supporting multichannel multimode data transmission.

List of Publications

[1] N. V. Silva, A. S. R. Oliveira, and N. B. Carvalho, "Design and Evaluation of a Fine Tunable Multichannel All-Digital RF Transmitter Using 3-level Sigma-Delta Modulators," in *IEEE Transactions on Microwave Theory and Techniques*, Submitted.

[2] N. V. Silva, A. S. R. Oliveira, and N. B. Carvalho, "Novel Fine Tunable Multichannel All-Digital Transmitter," in *IEEE MTT-S International Microwave Symposium Digest (MTT)*. IEEE, June 2013, Accepted.

[3] W. Jang, N. Silva, A. Oliveira, and N. Carvalho, "Designing Harmonic-Controlled Drivers for Switching Power Amplifiers," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 5, pp. 247–251, 2013.

[4] N. V. Silva, A. S. R. Oliveira, and N. B. Carvalho, "Design and Optimization of Flexible and Coding Efficient All-Digital RF Transmitters," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 1, pp. 625–632, 2013.

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[7] N. V. Silva, A. S. R. Oliveira, U. Gustavsson, and N. B. Carvalho, "A Novel All-Digital Multichannel Multimode RF Transmitter Using Delta-Sigma Modulation," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 3, pp. 156–158, 2012.

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[10] N. Silva, A. S. R. Oliveira, and N. B. Carvalho, "Towards a New Baseband Processing Architecture for Next Generation Software-Defined Radio," *Electrónica e Telecomunicações*, vol. 5, no. 2, pp. 167–171, June 2010.

[11] N. Silva, A. S. R. Oliveira, and N. B. Carvalho, "Reconfigurable Architectures for Next Generation Software-Defined Radio," in *REC'2010: VI Jornadas sobre Sistemas Reconfiguráveis*, February 2010, pp. 41–44.

Mathematical Notation

η	Drain efficiency
η_c	Coding efficiency
ω	Angular frequency
$D_n(z)$	Dither noise
$E_{ns}(z)$	Noise shaping error
$E_q(z)$	Quantization error
f	Frequency
$F(z)$	$\Sigma\Delta$ loop-filter
fs	Sampling frequency
$G(z)$	$\Sigma\Delta$ loop-filter
$H(z)$	Noise shaping loop-filter
P_s	Signal power
P_{tot}	Total power
$Q(z)$	Output signal
R	Resistance
$X(z)$	Input signal
z	z-domain operator

Abbreviations

ACLR	Adjacent Channel Leakage Ratio
ADC	Analog-to-Digital Converter
ASIC	Application-Specific Integrated Circuit
ASSP	Application-Specific Standard Product
CR	Cognitive Radio
C/N	Carrier-to-Noise ratio
CIFB	Cascade-of-Integrator with distributed FeedBack
CRFF	Cascade-of-Resonators with distributed Feed-Forward
DC	Direct Current
DAC	Digital-to-Analog Converter
DCM	Digital Clock Manager
DSP	Digital Signal Processing
DSP	Digital Signal Processor
DUC	Digital Up-Conversion
EVM	Error Vector Magnitude
FET	Field Effect Transistor
FPGA	Field-Programmable Gate Array
GSPS	Giga-Samples Per Second
ICs	Integrated Circuits
IF	Intermediate Frequency
LCM	Least Common Multiple

LNA Low-Noise Amplifier

LP SDM Low-Pass ΣΔ Modulation

LSB Lower SideBand

LSb Least Significant bit

LUT Look-Up Table

MAC Medium Access Control

MER Modulation Error Ratio

MGT Multi-Gigabit Transceiver

MIMO Multiple-Input Multiple-Output

MSb Most Significant bit

NTF Noise Transfer Function

OSR OverSampling Ratio

OFDM Orthogonal Frequency-Division Multiplexing

PA Power Amplifier

PAPR Peak-to-Average Power Ratio

PHY Physical Layer

PQN Pseudo Quantization Noise

PWM Pulse Width Modulation

QAM Quadrature Amplitude Modulation

RAM Random Access Memory

RDCM Reconfigurable Digital Clock Manager

RF Radio Frequency

RISC Reduced Instruction Set Computer

SDR Software-Defined Radio

SSB Single-SideBand

SMPA Switched-Mode Power Amplifier

SNDR Signal-to-Noise and Distortion Ratio

SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
SQNR	Signal-to-Quantization Noise Ratio
STF	Signal Transfer Function
USB	Upper SideBand
VSA	Vector Spectrum Analyzer
WiMAX	Worldwide Interoperability for Microwave Access

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Chapter 1

Introduction

Outline

This chapter starts by providing the scope and the main motivation for performing this work. Then, the thesis contribution is presented and finally, the chapter concludes with the presentation of the document organization.

1.1 Scope and Motivation

The unprecedented attention given to wireless communications over the last years led to the proliferation of new wireless standards operating at different frequencies, using dissimilar coding and modulation schemes, and targeted for different ends. Such vast proliferation pushes an additional research effort towards the development of new flexible radios, capable of adapting to different communication scenarios. However, the exponential use of wireless devices leads to a further use of the electromagnetic spectrum. In this sense, improving RF spectrum management as well as using it in a very efficient way is also increasingly vital.

Nowadays, the spectral efficiency of a radio transmitter is commonly improved by generating signals with a high Peak-to-Average Power Ratio (PAPR), as well as by using Multiple-Input Multiple-Output (MIMO) systems. While MIMO techniques typically require one Radio Frequency (RF) front-end for each antenna in the array, transmitting high PAPR signals requires both high linearity and high dynamic range constraints, thus making harder the design of such RF front-end. On the other hand, from the power efficiency perspective, the higher the PAPR is, the harder it gets to design an efficient transmitter.

Currently, a significant portion of the energy is literally wasted in the transmission path of the RF front-end. In fact, considering the total power consumption of a cellular network, over 60 % is consumed by the base stations [SNB12], which have an overall power efficiency of about 5 to 10 % [Kar03, Chu04]. Moreover, considering the total power budget of a typical base station, over 50 % is used in the transmission path [Kar03, FBZ$^+$10, SNB12], thus making a clear point that improving the power efficiency of the RF front-end is fundamental.

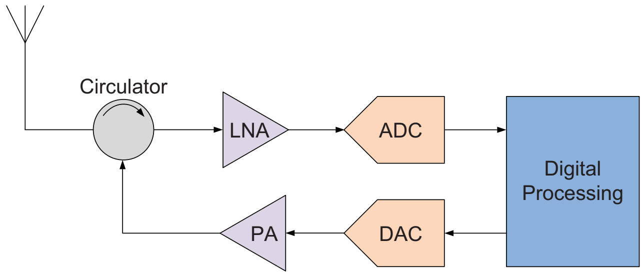

Figure 1.1: Simplified block diagram illustrating the architecture of an ideal SDR transceiver.

Moreover, due to its high contribution in terms of overall power consumption on a cellular network, it is also clear that even small power efficiency improvements in the RF transmission path will have a significant power consumption impact in the overall network, allowing to substantially reduce the environmental footprint.

In this new wireless communication paradigm, the Software-Defined Radio (SDR) concept [Mit92, Mit95] holds the potential for implementing the supreme universal radio, that is, a fully reconfigurable radio that has the flexibility to adapt its own communication parameters in order to meet the user demands as well as the channel and the network conditions.

In an ideal SDR, all the processing is done in the digital domain using powerful Digital Signal Processing (DSP) techniques, while the analog components are reduced to the minimum and are mainly used as signal conditioning and as data bridging between the analog and the digital domain, see Fig. 1.1.

In fact, shifting the radio processing architecture towards the digital domain has an extreme potential since the major signal processing can now be done by using Digital Signal Processor (DSP) or Field-Programmable Gate Array (FPGA) devices, thus making easier configuring and controlling the radio transmitter, and therefore, allowing the radio to adapt to different communication scenarios in an easier way, while also facilitating improvements in terms of spectral management.

Moreover, the continuous technology evolution fosters the development of smaller Integrated Circuits (ICs) with improved power efficiency and having massive transistor densities that provide unparalleled integration. However, while digital ICs have a better performance as they get smaller, the same does not apply to analog ICs [NA05], where it is well known that the analog properties get worse as the transistor size gets smaller. In this sense, it seems clear that transmitter designs having predominantly digital datapaths provide higher integration and cope better with the IC technology evolution.

For all the above mentioned reasons, it becomes evident that further research leading to the development of innovative transmitters based on flexible digital radios such as the SDR concept is increasingly crucial. The latest advances in this field include the development of novel all-digital transmitters [YGM07a, HHNG08, Gha10a], where its datapath is digital from the baseband up to the RF stage, see Fig. 1.2. Such concept has inherent high flexibility and poses an important step towards the development of SDR transmitters. Moreover, this

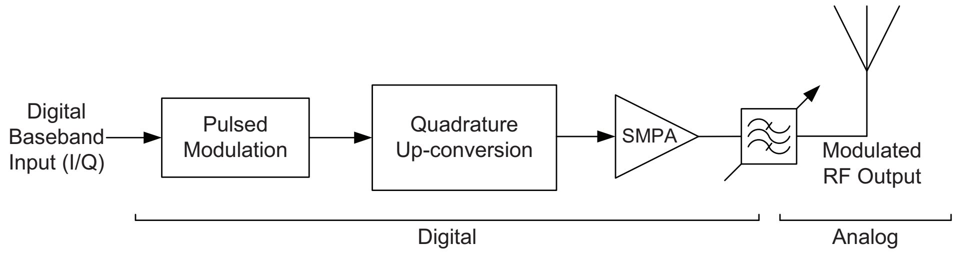

Figure 1.2: Simplified structure of a conventional all-digital transmitter.

new approach enables the use of FPGA devices for implementing the digital datapath of such RF transmitters, which provides additional flexibility as well as field upgradeability.

	DSP	ASIC	ASSP	FPGA*
DSP Speed	●●○	●●●	●●◐	●●◐
Power Efficiency	●◐○	●●●	●●◐	●●○
Reprogrammability	●●◐	◐○○	◐○○	●●○
Design Flexibility	●○○	●●●	◐○○	●●◐
Area Efficiency	●◐○	●●●	●◐○	●◐○
Development Savings	●●○	◐○○	●●○	●○○
DSP Tools Support	●●●	◐○○	◐○○	●●○

Table 1.1: Summary comparison of DSP implementation technologies, partially adapted from [Ber06, HSM03, SPI08]. *DSP-enhanced FPGA.

As shown in Table 1.1, DSP-enhanced FPGAs provide an interesting compromise between performance, power efficiency and flexibility, which makes FPGAs an interesting choice as an enabling technology for SDR transmitters. In fact, current FPGAs have an equivalent logic capacity of millions of logic gates in addition to large RAM blocks, embedded processors, DSP modules and multigigabit I/O standards. If efficiently explored, these valuable resources can be used to enable the development of agile all-digital transmitters.

1.2 The Problem

Innovative all-digital transmitters using a pulsed representation of the desired signal combined with switched-mode power amplification have been proposed for several years as highly adaptable radio architectures allowing the RF transmission of multi-standard and multi-band signals [HHNG08, Gha10a, KAI10, TOGN11, RAM12]. This approach is believed for awhile as a possible candidate for enabling the development of compact and highly efficient RF transmitters where a key motivation for using pulsed signals is the fact that Switched-Mode Power Amplifiers (SMPAs) have the potential of providing considerably higher power efficiencies when compared to linear amplifiers [Cho01, JS06, HG09].

However, the truth is that converting the desired signal into a two-level pulsed representation is typically a very inefficient process where a significant amount of energy containing unwanted noise is produced. In fact, since the hole RF signal including the undesirable noise is amplified by the SMPA, the overall power efficiency of the radio transmitter will be substantial lower than what could be initially expected when considering only the efficiency of the amplifier [HRLA07, GHA+10b, HKTF11].

Moreover, from the point of view of flexibility, current state-of-the-art all-digital transmitter architectures still have a few key limitations that are preventing a wider adoption of this concept. In fact, although they allow multi-standard and multi-band signals, they typically do not support the simultaneous transmission of more than one RF carrier, require very high-quality filters to remove the RF out-of-band noise as well as they commonly support only very narrow-band signals. Furthermore, conventional all-digital transmitters typically have a coarse frequency tuning and where the RF digital up-conversion stage is commonly implemented using expensive external multiplexers.

A key challenge for achieving a new communications paradigm based on all-digital transmitters involves the development of a very flexible physical layer that should support the concurrent transmission of multi-band, multi-rate and multi-standard signals while providing high power efficiency, which in practice is very hard to achieve using conventional approaches. This thesis aims precisely to address some of these limitations by proposing and implementing innovative all-digital transmitter architectures with inherent higher flexibility and integration.

1.3 The Hypothesis

The main research work done in the scope of this PhD was devoted to support the following theory: *Innovative all-digital transmitter architectures allowing the concurrent transmission of multi-band, multi-rate and multi-standard signals can be designed and implemented in a compact and highly integrated approach using recent digital reconfigurable hardware.*

1.4 The Thesis

Given the presented hypothesis, the remaining chapters of this manuscript will be focused in the validation of the following thesis: *Novel all-digital transmitter architectures capable of simultaneously transmitting two or more multi-standard, multi-band, multi-rate RF signals with fine frequency tuning for each carrier and where the RF output signal operating in the microwave frequency range is generated inside a single FPGA are feasible and require a reduced amount of FPGA area when the logic resources commonly available on recent high-end FPGAs are properly explored.*

1.5 Original Contributions

The idea of having an entirely digital transmitter is not new. However, the truth is that implementing such radio for a real world communications scenario is a challenging task, where a few key limitations are still preventing a wider adoption of this concept. This PhD work aims precisely to address some of these limitations by proposing and implementing innovative all-digital transmitter architectures with inherent higher flexibility and integration, and where improving important figures of merit, such as coding efficiency (η_c), Signal-to-Noise Ratio (SNR), usable bandwidth and in-band and out-of-band noise will also be addressed. This manuscript is based on work presented in five papers published in top journals and conferences in the field of this thesis and containing original contributions to the state-of-the-art.

Paper A proposes a novel $\Sigma\Delta$-based all-digital transmitter architecture capable of multichannel, multiband and multi-standard data transmission, where the pulsed RF output operating in the microwave frequency range is generated inside a single FPGA device. In this sense, this paper contributes to the state-of-the-art by presenting a $\Sigma\Delta$-based architecture that combines multichannel multimode data transmission in a very flexible and integrated way, which is possible by the full embedding of the digital datapath into FPGA technology.

Having in mind a better characterization of the effects introduced by typical pulsed modulation schemes, an agile RF transmitter using both $\Sigma\Delta$ and PWM was prototyped using FPGA technology. This design approach permitted to analyze the specific trade-offs of each modulation technique and in turn allowed to improve the SNR of the carrier as well as to reduce the filtering requirements of the RF reconstruction filter, as shown in Paper B.

Further improvements are shown in Paper C, where a dynamically reconfigurable RF transmitter is presented and evaluated. In comparison with Papers A and B, it adds runtime flexibility provided by the dynamic reconfiguration of the Digital Clock Manager (DCM), and adds software programmability by having a microprocessor executing control tasks.

In Paper D, two key limitations inherent to current all-digital transmitter approaches are addressed, namely the poor coding efficiency and the combined high quality factor and tunability requirements of the RF output filter that significantly limit the practical usability and dissemination of these new flexible RF transmitters. This paper also contributes to the state-of-the-art by presenting a novel FPGA-embedded agile transmitter architecture that significantly improves important figures of merit, such as coding efficiency and Error Vector Magnitude (EVM) while maintains the support for multichannel multi-standard data transmission and where the RF output carriers operating in the GHz frequency range are still generated inside a single FPGA device.

A new architecture enabling the fine frequency tuning of concurrent multichannel multi-standard signals in presented in Paper E. In comparison to the previous work, this paper contributes to the state-of-the-art by presenting a pulse-based multi-rate, multi-band, multi-standard transmission architecture that significantly minimizes the output frequencies restrictions of current approaches by allowing fine frequency tuning for channel selection.

1.6 Document Organization

In addition to this introductory chapter, the manuscript is organized as follows:

- **Chapter 2 - Fundamentals of Oversampling Pulsed Converters -** Pulsed converters are a key element when designing SMPA-based all-digital transmitters. This chapter provides the background concepts inherent to pulsed converters by briefly describing the operation principle and the key advantages and main limitations of PWM and $\Sigma\Delta$-based modulators.
- **Chapter 3 - Review of Pulse Modulated RF Transmitters -** as the name suggests, the recent advances regarding pulsed all-digital transmitters are discussed in this chapter. At this point, novel transmitter topologies will be presented as well as a comparative analysis containing important figures of merit will be given.
- **Chapter 4 - Enhancement Techniques for All-Digital RF Transmitters -** This chapter presents in a modular and structured way the main achievements reported in the appended papers. In that sense, this chapter details the key developments made during this thesis regarding the development of new FPGA-based all-digital transmitters with improved figures of merit, such as usable bandwidth, SNR, coding efficiency, out-of-band noise emission and EVM.
- **Chapter 5 - Conclusions and Future Work -** The main conclusions and possible future research work in this field are presented in this chapter.

Chapter 2

Fundamentals of Oversampling Pulsed Converters

Outline

This chapter provides key concepts inherent to pulsed converters that are fundamental when designing SMPA-based all-digital transmitters. In that sense, the operation principle of PWM and $\Sigma\Delta$-based modulators, as well as its key advantages, main limitations and typical enhancement techniques will be addressed in this chapter.

2.1 Pulse Width Modulation

Perhaps one of the oldest types of pulsed conversion is the PWM [Pol61]. In a conventional approach, a time varying input signal is compared with a sawtooth reference signal. As a result of this comparison, a 2-level pulsed signal is generated, where a higher input signal amplitude will result in a higher width of the pulsed output, see Fig. 2.1.

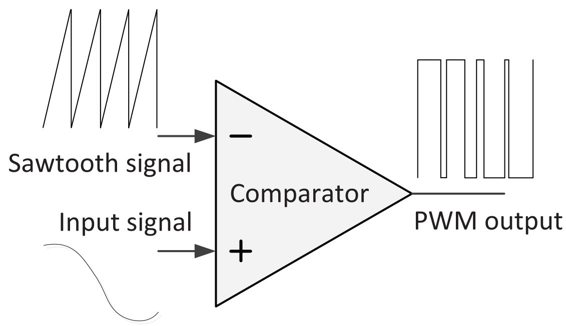

Figure 2.1: Block diagram illustrating the PWM operation principle.

The massification of digital ICs containing a very large number of transistors enables the proliferation digital PWM circuits for a very wide range of applications, including AC-DC power converters [ARH11], control of actuators in industrial processes [vVB97], as well as in audio [LKK05] and in telecommunications [CSV11].

In this scenario, a digital input signal is typically oversampled before its conversion into a pulsed representation. This means that the PWM converter will be able to operate at a higher sampling rate, and consequently it will receive a signal that is changing slower over each sample. This is fundamental since the minimal pulse duration of the PWM signal is determined by the OverSampling Ratio (OSR) of the signal, hence a higher OSR allows the PWM converter to provide a better representation of the desired signal.

Despite the large potential of PWM-based applications using digital ICs, the true is that conventional approaches have limitations in terms of low SNR and high quantization noise that limit its wider dissemination. In fact, it is well known that the PWM conversion process introduces quantization noise due to the finite resolution of the digital representation of the signal, as also the finite sampling frequency introduces out-of-band harmonic distortion.

In Fig. 2.2 it is shown an overlapped spectrum illustration comparing a synthetic signal (orange) with its representation using only 5 bits (yellow) and after converting into a PWM representation where a 5-bit input signal was converted to a 2-level PWM word containing 32 pulses (blue).

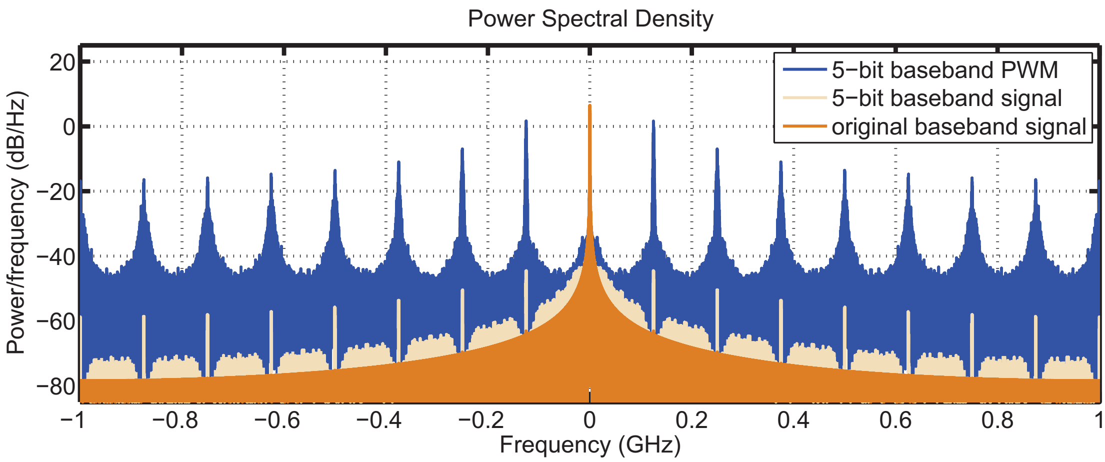

Figure 2.2: Overlapped spectrum illustration comparing a synthetic baseband signal with a sampling frequency of 125 MHz for the following scenarios: a) original signal interpolated by 16 and formatted to the Matlab 64-bit floating-point representation, b) baseband signal upsampled by a factor of 16 and converted into a 5-bit fixed point representation and c) baseband signal upsampled by a factor of 16 and converted into a 5-bit PWM representation.

As can be seen, the noise of the yellow signal is slightly higher than the original representation, which is mainly due to the reduced number of bits used in the quantization process. Moreover, the yellow signal was also up-sampled by a factor of 16, which allows to illustrate the out-of-band harmonics appearing at multiples of the sampling frequency. At last, the PWM representation shown in blue is clearly the one presenting higher unwanted noise, which is mainly due to the 2-level pulsed representation that introduces significant higher quantization noise as well as out-of-band harmonic distortion peaks. This also means that only a part of the energy related to the coding of the input signal was effectively converted by the PWM modulator while the remaining energy appears as noise. In this sense, the coding efficiency, denoted as η_c can be defined as the ratio of the desired signal power (P_s) over the total power (P_{tot}). In general, the coding efficiency is given by:

$$\eta_c = \frac{P_s}{P_{tot}}. \tag{2.1}$$

In the scope of SMPA-based all-digital transmitters, the overall power efficiency is directly proportional to the coding efficiency. Hence, if a low coding efficiency approach is used, the overall transmitter efficiency will be severely limited. Observing the PWM spectrum shown in Fig. 2.2, it is clear that a conventional PWM-based approach has a poor coding efficiency.

Moreover, conventional PWM approaches typically provide the desired pulsed signal with low SNR. This is a particularly important limitation when implementing RF transmitters where transmitting signals high SNR is always desirable, either by allowing a longer coverage or by enabling transmitting at higher data rates. In this sense, several approaches can be used in order to shift the unwanted quantization noise to outside the band of interest, so that the desired signal has less inband noise. Regarding the out-of-band harmonics, the high power that is concentrated on those peaks is also very undesirable and requires the use of filters for attenuating or even removing such components.

The subsections below present well known techniques that can be used to improve the PWM conversion stage, either by allowing to reduce the minimum pulse duration of the PWM converter without SNR degradation of the desired signal, or by reducing the PWM harmonic distortion peaks.

2.1.1 Noise Shaping

The concept of noise shaping has been suggested in [TH78, Gol91] as a way to reduce the number of bits of a given signal without sacrificing SNR over a given bandwidth. In fact, the use of noise shaping allows shifting the quantization noise further away from the desired signal, so that it is possible to reduce the power of the noise in a limited portion of bandwidth, as can be seen in Fig. 2.3.

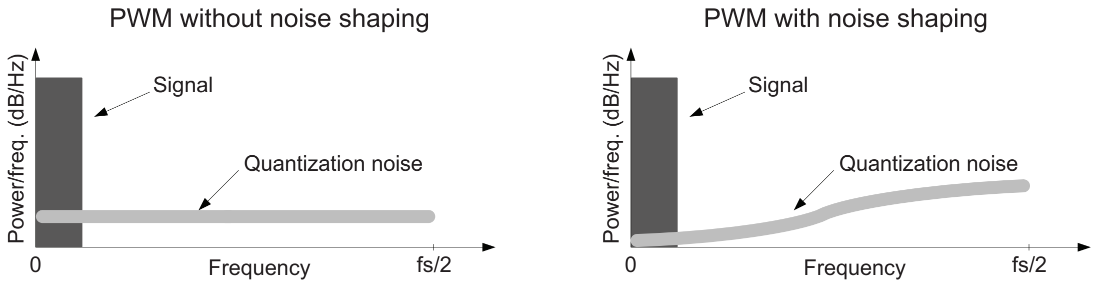

Figure 2.3: Power spectral density illustrations of a PWM-based signal when a) no noise shaping is used, shown on the left, and b) noise shaping is used, shown on the right.

The general model of a noise shaper in shown in Fig. 2.4, where $X(z)$ is the input signal quantized with n bits, $Q(z)$ is the m-bit output signal, $E_{ns}(z)$ is the noise shaping error, $E_q(z)$ is the error introduced by the quantizer and $H(z)$ is the noise shaping filter.

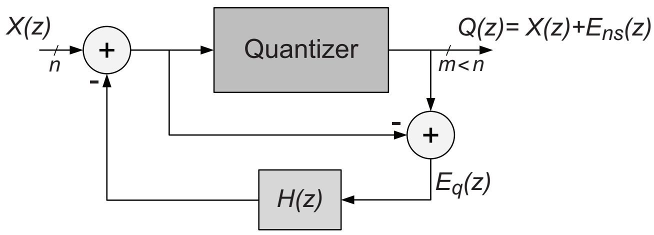

Figure 2.4: Block diagram illustrating the general model of a noise shaper.

In this model, the output signal is given by:

$$Q(z) = X(z) + E_{ns}(z), \tag{2.2}$$

and the error introduced by the quantizer can be expressed as:

$$E_q(z) = Q(z) - [X(z) - H(z)E_q(z)] = E_{ns}(z) + H(z)E_q(z). \tag{2.3}$$

Using a linearized approach, it is possible to describe the noise shaper in terms of a Noise Transfer Function (NTF) that can be defined as the transfer function from $E_q(z)$ to $Q(z)$, as long as $X(z)$ is kept at zero. The NTF can be defined as:

$$\mathrm{NTF}(z) = \left.\frac{Q(z)}{E_q(z)}\right|_{X(z)=0} = \frac{E_{ns}(z)}{E_q(z)} = \frac{E_q(z) - H(z)E_q(z)}{E_q(z)} = 1 - H(z). \tag{2.4}$$

In a conventional PWM conversion approach a n-bit input signal is typically centered at the baseband. Hence, if noise shaping is used, the loop-filter $H(z)$ should be designed to produce a high-pass NTF so that the quantization noise is shifted to the higher frequencies. The NTF equation that is typically used [TH78, LKK05, NPAM08] in noise shaping-based PWM converters can be expressed as:

$$\mathrm{NTF}(z) = (1 - z^{-1})^N, \tag{2.5}$$

where N is the order of the high-pass filter.

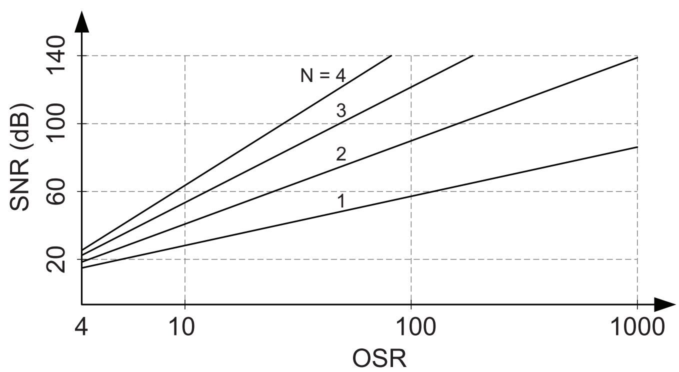

Figure 2.5: Illustration of the relationship between SNR and OSR for different orders of the noise shaping filter, adapted from [MUIK89].

One characteristic that is common to digital pulsed converters is that a higher OSR generally allows to shift further away the unwanted noise which in turn allows to improve the SNR of the desired signal. Moreover, higher orders of the noise shaping filter also contribute for improving the SNR, as can be seen in Fig. 2.5.

2.1.2 Dithering

It is well known that the PWM conversion stage introduces undesirable noise peaks spaced at multiples of the PWM sampling frequency. In fact, every time that the resolution of a signal is reduced, undesirable artifacts will appear due to the truncation error inserted by the quantizer. In this sense, dithering can play an important role by allowing to reduce such undesirable artifacts.

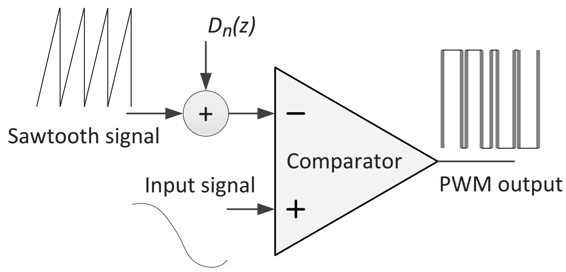

Figure 2.6: Block diagram illustrating the PWM operation principle when dithering is used.

The concept of dithering consists in adding random noise (*dither*) to the waveform in order to disperse the statistical determinability of the resulting signal. In Fig. 2.6, the concept of dithering applied to PWM is illustrated. This approach effectively allows reducing the PWM harmonics by spreading its noise. However, it is important to point out that dithering does not reduces the overall noise, in turn it spreads the energy of undesirable artifacts, which results in a smoother signal, as can be seen in Fig. 2.7.

Although historically it was mostly used in applications involving image [Rob62] and audio [Ble78] processing, dithering is now becoming an important technique in the telecom-

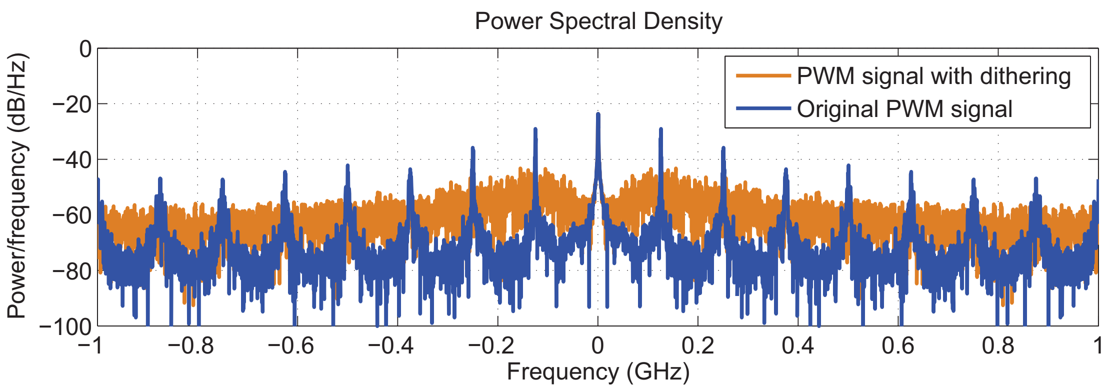

Figure 2.7: Overlapped spectrum illustration comparing the PWM representation of a synthetic baseband signal when a) no dithering is used, depicted in blue and b) dithering noise added to spread the PWM harmonics, shown in orange.

munications field, allowing to improve the transmitting signal [SG12] as well as reducing the radio interference [CRR06].

2.2 ΣΔ Modulation

The ΣΔ modulation concept was originally proposed by Cutler [Cut54] in a patent filed in 1954. Since then, ΣΔ modulators have gained massive popularity, specially in the digital communications field. The underlying idea of ΣΔ modulators consists in using feedback as a way to effectively reduce the quantization error introduced by a low-resolution quantizer. In this sense, ΣΔ converters behave as noise shaping modulators, where an improved dynamic range is achieved by suppressing the error over a given bandwidth.

Over the past years, a large amount of research work containing theory and design improvements, as well as new simulation and implementation techniques have been proposed. While it is out of the scope of this thesis to provide such a comprehensive analysis, more information can be found in [NST96] and [ST04]. This section will contain an overview to the typical tools and methodologies used in the design, simulation and analysis stages of ΣΔ modulators.

2.2.1 The Linear Model

The highly non-linear behavior of ΣΔ modulators makes harder to analyze its functioning in a deterministic way. In this sense, a common way to design and analyze ΣΔ modulators consists in describing its linear model in the frequency domain where the non-linear operator, the quantizer, is replaced by the addition of a Pseudo Quantization Noise (PQN) approximation, see Fig. 2.8. This approach allows the use of linear theory to show that it is possible to separate the spectrum of the input signal from the noise introduced by the quantizer, as well as to estimate the ΣΔ performance in terms of Signal-to-Quantization Noise Ratio (SQNR) and shaping of the quantization noise.

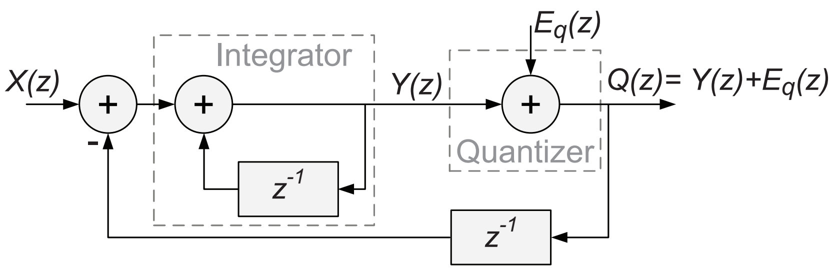

Figure 2.8: Illustration of a z-domain linear model for a first order low-pass ΣΔ modulator.

In this model, the output signal is given by:

$$Q(z) = Y(z) + E_q(z). \tag{2.6}$$

Therefore,

$$\begin{aligned} Q(z) &= X(z) - z^{-1}Q(z) + z^{-1}Y(z) + E_q(z) \\ &= X(z) + E_q(z) - z^{-1}[Q(z) - Y(z)] \\ &= X(z) + E_q(z) - z^{-1}E_q(z) \\ &= X(z) + [1 - z^{-1}]E_q(z). \end{aligned} \tag{2.7}$$

The equation shown in (2.7) can be rewritten into the following general form:

$$Q(z) = \mathrm{STF}(z)X(z) + \mathrm{NTF}(z)E_q(z), \tag{2.8}$$

where in this case the NTF describes a high-pass filter given by $\mathrm{NTF}(z) = 1 - z^{-1}$, and where the Signal Transfer Function (STF) is equal to one. This equation also shows that the output signal consists of two independently filtered components, the desired signal and the quantization noise, and where the contribution of each component is described by a specific transfer function.

In terms of SQNR performance, it is shown in [ST04] that each time the OSR is doubled, there is a ≈9 dB gain, given by the following equation:

$$SQNR = \frac{9 \times \mathrm{M}^2(\mathrm{OSR})^3}{2\pi^2}, \tag{2.9}$$

where M is the peak amplitude of the input signal. This means that if a high SQNR is desired, that can only be achieved if an extremely high OSR is used. In fact, if M is unitary, an OSR of more than 600 is required for producing an SQNR of 80 dB. This way, depending on the bandwidth of the desired signal, using the current technology for implementing a first-order ΣΔ modulator with such high SQNR requirements may be a challenging task or even unfeasible. A possible approach to overcome such limitation consists in using a higher order ΣΔ modulator where achieving the same SQNR requires a lower OSR.

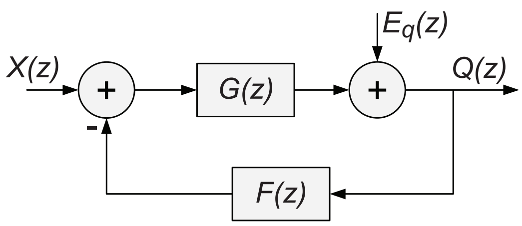

Figure 2.9: General linear model of a ΣΔ modulator illustrating the filters $G(z)$ and $F(z)$.

A general linearized model representation of a N^{th} order ΣΔ modulator is shown in Fig. 2.9, where $G(z)$ and $F(z)$ are the loop filters, $E_q(z)$ is the quantization noise, $X(z)$ is the input signal and $Q(z)$ is the resulting output signal.

Using this general model makes it possible to describe a N^{th} order ΣΔ modulator as a system containing two independent transfer functions, one for the noise and another for the signal. Again, the NTF that can be described as the transfer function from $E_q(z)$ to $Q(z)$, as long as $X(z)$ is kept at zero. The NTF can be given by:

$$\mathrm{NTF}(z) = \left.\frac{Q(z)}{E_q(z)}\right|_{X(z)=0} = \frac{1}{1+G(z)F(z)}. \tag{2.10}$$

On the other hand, the STF can be defined as the transfer function from $X(z)$ to $Q(z)$, as long as $E_q(z)$ is kept at zero. The STF can be calculated as:

$$\mathrm{STF}(z) = \left.\frac{Q(z)}{X(z)}\right|_{E_q(z)=0} = \frac{G(z)}{1+G(z)F(z)}. \tag{2.11}$$

This way, it is possible to use conventional linear optimization techniques in order to synthesize the desired NTF from which the filter coefficients can be computed. There are several commercially available toolboxes that perform the $\Sigma\Delta$ modulator analysis and simulation, such as [Sch00] and [Bri02], where it is possible to view the quantization noise shape as well as to have an estimate of the SQNR performance.

2.2.1.1 Nonmonotonic Frequency Response

The above described low-pass $\Sigma\Delta$ modulators are typically implemented using filters having one or more poles at DC, which provides a high-pass noise transfer function, and zeros at high frequencies in order to improve the stability of the modulator. Those modulators have a monotonic frequency response in the range of 0 to $f_s/2$ and are specially interesting when it is fundamental to maximize the SQNR of a DC-centered signal.

However, when the desired signal is not centered at DC or it is important to have low quantization noise over a wider band, then a possible alternative technique consists in changing the location of the poles by placing them through the signal band. This approach produces a nonmonotonic frequency response where the correct placement of the poles allows to lower the in-band noise and where the resulting NTF has a more rectangular high-pass shape.

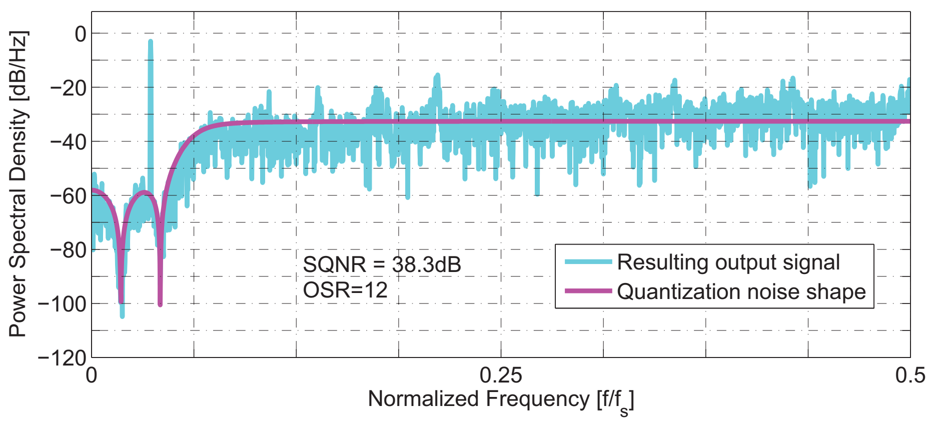

Figure 2.10: Illustrative example containing the frequency response of a given NTF and the spectrum of the resulting output signal for a 4^{th} order $\Sigma\Delta$ modulator and when the specified OSR is 12.

A nonmonotonic frequency response example of a 4^{th} order ΣΔ modulator with a 2-level quantizer is shown in Fig. 2.10. The use of such approach exposes a very important design compromise between the usable bandwidth, where the quantization noise is low, and the quality of the desired signal in terms of SQNR performance. In fact, for the same operating frequency, maximizing the usable bandwidth of a ΣΔ modulator will lead to a poor SQNR performance, while improving the quality of the desired signal will result in a narrower usable bandwidth.

Nevertheless, the inherent higher flexibility of this approach allowed by specifying the best location for the poles and zeros in the system makes it possible to optimize the ΣΔ modulator design for each specific application.

2.2.2 Stability Analysis

As above stated, using a linear model to describe the ΣΔ functioning allows designing and analyzing its behavior in the frequency domain, making possible to simulate the frequency response of the quantization noise as well as the SQNR performance of the desired signal.

However, observing eq. (2.8) where the output of the modulator is given in terms of its input signal and the quantization error may lead to modeling mistakes since it does not clearly shows that the noise is signal dependent. In fact, just by applying an amplitude gain to the input signal will result in a different noise spectrum and may lead to an unstable operation [NST96].

Furthermore, the linear model approximation does not provide an exact representation to the highly non-linear behavior of ΣΔ modulators, thus making hard to analyze the ΣΔ stability with very high precision, specially for higher order modulators [LS87] where its complexity is even higher. For the same OSR, it is clear that using a higher order filter for realizing the NTF provides a sharper frequency response and allows further reduction of the in-band quantization noise. However, orders higher than three require a careful system stability consideration and are usually hard to implement in practice [CNLS90, NST96].

A well known empirical rule for predicting a priori stability using the linear approximation was suggested by Lee et. al. [CNLS90]. Through extensive simulations, the authors were able to place an upper boundary to the gain at higher frequencies that a NTF should have in order to maintain a stable operation. The Lee rule states that for a single bit quantizer, a necessary condition for stable operation of the ΣΔ modulator is given by:

$$\|\mathrm{NTF}(\omega)\|_\infty < 2. \tag{2.12}$$

This simple rule provides acceptable a priori stability predictions and is typically taken into account when designing the NTF loop filter [KALB04]. However, determining the stability behavior of a highly nonlinear system is a complex task where applying the Lee criteria should be made very carefully since it helps in designing the NTF loop filter but it does not ensures the system stability.

The next chapter will present a succinct review containing the recent advances of all-digital RF transmitter architectures based on oversampling pulsed converters.

Chapter 3

Review of Pulse Modulated RF Transmitters

Outline

All-digital RF transmitters based on oversampling pulsed modulators can be split into two main classes, RF or baseband, depending on the clock rate and the level at which the single bit quantization is made. This chapter provides a succinct description containing the recent advances within these two classes, where several examples of state-of-the-art RF pulsed transmitter architectures are given.

3.1 Introduction

The exponential proliferation of mobile wireless communications pushes an additional research effort towards the development of new flexible radios, which should be capable of adapting to different communication scenarios and not least important, should be very efficient in terms of power consumption.

In this regard, the use of pulse modulated data combined with switched-mode power amplification is believed for awhile as a feasible approach for enabling the development of compact and highly efficient RF transmitters [Cho01, JS06, HG09, Gus11].

In this approach, the transistor performing the power amplification behaves as a switch where only two operation regions are desired, the saturation region where full output power is delivered and the cut-off region where the transistor is fully off. These two operation regions are the states where Field Effect Transistors (FET) dissipate less power and therefore efficient power conversion is achieved.

Recent advances involving pulsed RF transmitters include the development of novel all-digital architectures where the radio datapath is digital from the baseband up to the RF stage. Such concept has inherent high flexibility and poses an important step towards the development of software-defined transmitters [Mit95] where a significant portion of the radio hardware can be integrated inside a single digital chip.

3.2 RF-level Pulsed Architectures

As the name suggests, RF-level pulsed transmitters perform the single bit quantization directly at RF rates. In this approach, a m-bit digital RF input signal is typically re-quantized into a 2-level binary representation by means of $\Sigma\Delta$ or PWM schemes. The 2-level pulsed representation is then fed to a high efficiency SMPA and then reconstructed by using a bandpass filter. A highly simplified block diagram illustrating a general RF-level pulsed transmitter is depicted in Fig. 3.1. In this architecture the clock applied to the pulsed modulator is required to have an integer relation to the desired RF carrier, where N is typically higher than one.

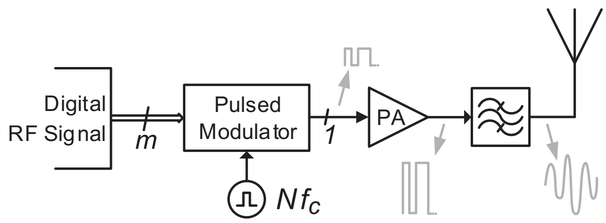

Figure 3.1: High level block diagram illustrating the architecture of an RF transmitter where a pulsed modulator typically operating in the GHz frequency range is used in order to produce a 2-level representation of the desired signal. The bandpass filter after the SMPA provides the reconstruction of the original waveform by removing the undesirable out-of-band noise.

There are several state-of-the-art pulsed transmitters found on the literature that fall within this operation principle, where the amplitude and phase of the RF carrier is shaped using PWM [NL08, OJA$^+$11, PJ12, OAE$^+$12], bandpass $\Sigma\Delta$ modulators [JS06, JS08] or both techniques in a hybrid approach [PDCF09].

At this point it should be noted that RF-level pulsed transmitter architectures are commonly implemented using Application-Specific Integrated Circuit (ASIC) technology since in this approach, the pulsed modulator is typically operating at a rate of 4 times the RF carrier, which consequently results in a significant and undesirable high power consumption.

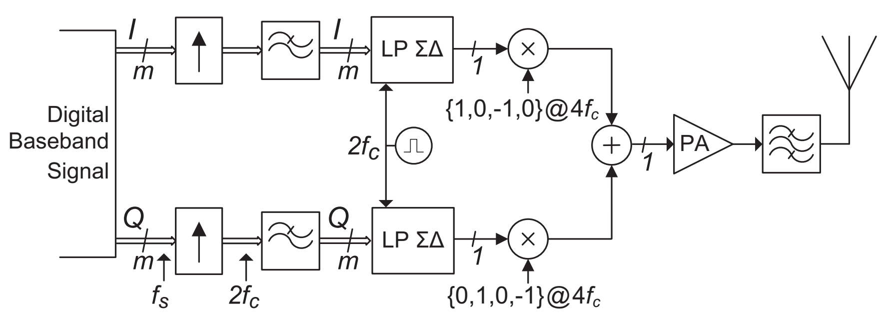

Figure 3.2: Simplified illustration of a 2-level pulsed transmitter where the quadrature baseband signals are firstly interpolated to RF and then shaped using LP $\Sigma\Delta$ modulation. The resulting signals are then digitally up-converted and combined in a time interleaved approach so that the resulting signal is still a 2-level waveform suitable for switched-mode amplification.

An alternative approach that allows reducing such high-speed operation requirements consists in re-quantizing the desired signal into a 1-bit pulsed representation before performing the frequency shift to RF. Such approach typically uses Low-Pass (LP) $\Sigma\Delta$ modulation to encode the baseband input signal into a 2-level representation and then performing a Digital Up-Conversion (DUC) directly to the desired carrier frequency, see Fig. 3.2.

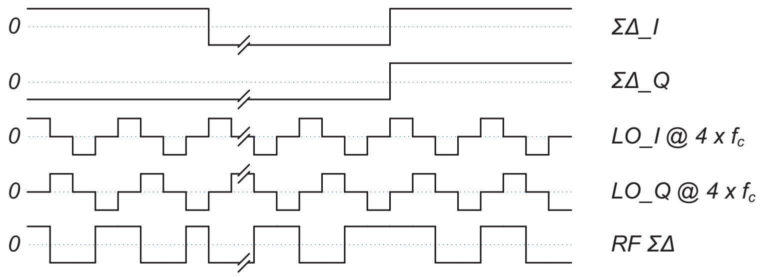

Figure 3.3: Timing diagram illustrating the DUC to RF where the resulting output signal remains a 2-level pulsed waveform suitable for switched-mode amplification.

However, taking advantage of efficient switching-mode amplification requires an unconventional DUC technique where the resulting up-converted signal is still a 2-level pulsed representation. In this approach, the In-phase (I) pulsed signal is multiplied by a digital waveform that is either 1, 0 or -1, as the Quadrature (Q) pulsed signal is multiplied by a 90^o phase shift of the same waveform. After adding both components the resulting 2-level signal will include the desired carrier centered at f_c and also odd harmonics centered at multiples of f_c. Those undesirable harmonics are typically removed by the RF reconstruction filter but can also be removed by means of a low pass filter before or after the PA. A detailed timing diagram illustrating the used DUC process in shown in Fig. 3.3.

On the scientific literature there are a few pulsed transmitters using this operation principle, where two LP $\Sigma\Delta$ modulators typically operating at a rate of $2f_c$ shape the quadrature baseband signals [FFK$^+$06, JS07, FSF$^+$08, FFS$^+$09]. Although reduced to half when compared with the previous RF-level transmitter approach, the required operating rate is still challenging for implementations based on a more flexible technology such as the FPGA.

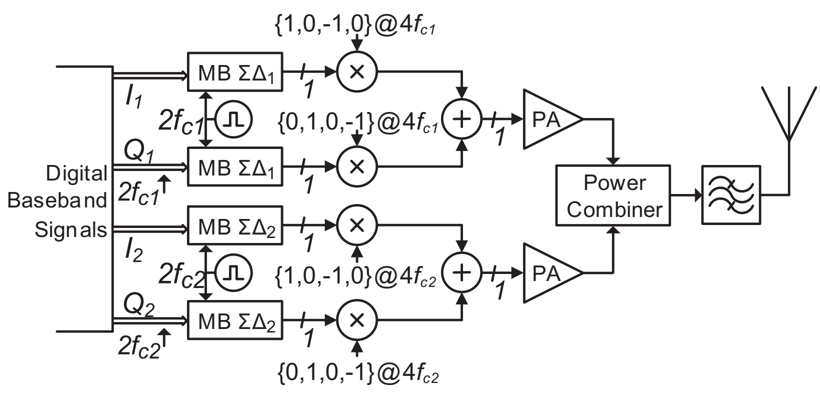

Figure 3.4: Simplified block diagram illustrating a concurrent multi-standard, multi-channel pulsed transmitter architecture based on MB $\Sigma\Delta$ modulation.

The last RF-level pulsed transmitter architecture that is going to be described here consists of a less common approach but also found on the literature [KAI10, KI10], where Multi-Band (MB) ΣΔ modulators are used in order to enable a concurrent multi-channel multi-standard RF transmission, see Fig. 3.4. In this approach, the quadrature components of each baseband signal are noise shaped by ΣΔ modulators containing multiple passing bands in the NTF, one for each carrier. This way, due to the lower noise energy at those frequencies, the pulsed RF signals can be combined with minimal SNR degradation.

However, this approach also requires ΣΔ modulators running at a very high sampling frequency in order to deal with the wide frequency range of operation. Furthermore, a higher number of concurrent bands requires more poles in the NTF and therefore makes it harder to prototype a stable modulator.

3.3 Baseband-level Pulsed Architectures

A common alternative approach that is typically used in order to overcome the strident operating rates of RF-level pulsed transmitters consists in performing the single bit quantization at baseband rates and then up-sample and up-convert the baseband signal to the desired RF carrier. In this approach, each m-bit component of the quadrature baseband signal is typically re-quantized into a 2-level binary representation by means of LP ΣΔ modulation. The pulsed representation is then simultaneously up-sampled and digitally up-converted to RF by means of a multiplexer that is toggling at a rate of f_c between a non-inverted and inverted representation of the input signal. This process is identical for both components of the quadrature baseband signal and finally, a third multiplexer operating at $2f_c$ generates the desired RF output signal by combining both RF components in a time-interleaved approach.

A simplified block diagram illustrating a general baseband-level pulsed transmitter is shown in Fig. 3.5. In this architecture the clock applied to the digital multiplexers is required to have an integer relation to the baseband sampling frequency, where N specifies the up-conversion factor required to produce an RF carrier centered at f_c. A further clarification of the DUC process used in this baseband-level pulsed transmitter is provided in Fig. 3.6.

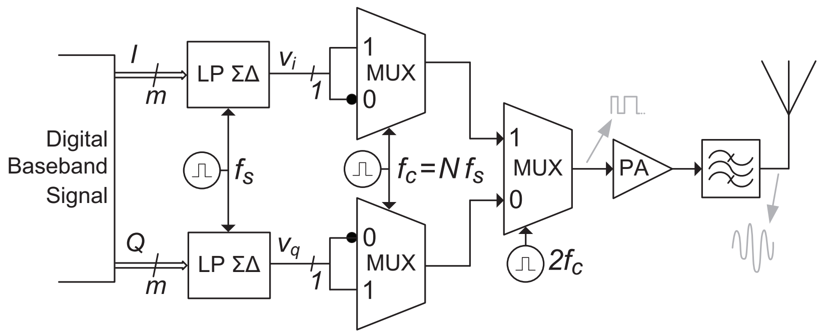

Figure 3.5: Simplified architecture of a baseband-level pulsed transmitter where the DUC is performed by a set of three multiplexers operating in the RF frequency range.

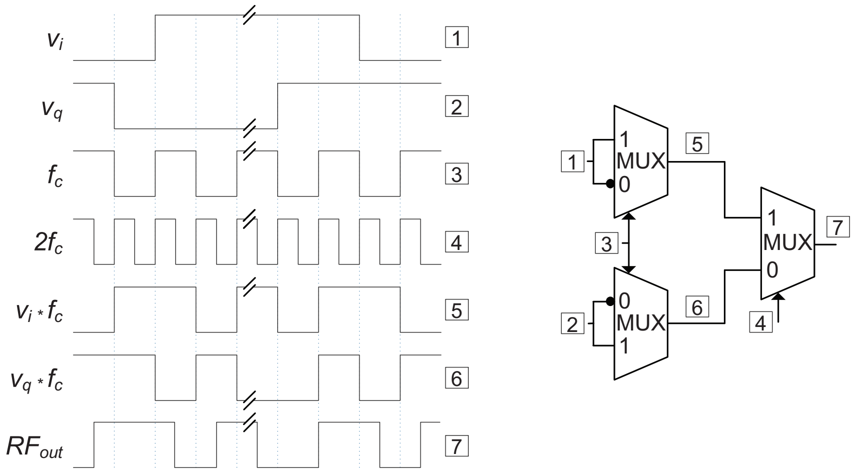

Figure 3.6: Timing diagram illustrating a digital up-conversion process where a set of three multiplexers performs a frequency shift directly to RF.

Due to the lower operating frequency requirements of the pulsed modulators, this approach is typically prototyped in FPGA devices where external multiplexers or high speed serializers are commonly used to shift the baseband signal to f_c [SADERH08, HHNG08, Gha10a, GHA$^+$10b]. However, if the $\Sigma\Delta$ modulators are set to operate at a very low frequency, the resulting OSR will be necessarily low, which ultimately results in a pulsed signal representation with a poor SNR or only very narrow-band operation is allowed.

So far the desired carrier frequency (f_c) is related by an integer ratio (N) to the sampling frequency of the pulsed modulator (f_s), which in practice may be undesirable and even restrictive when a fine frequency tuning for channel adjustment is required.

An alternative baseband-level pulsed transmitter architecture that can be implemented in order to overcome such limitation consists in using a first up-conversion stage to shift the baseband signal into a low IF prior to the pulsed modulation, and then performing the final up-conversion to RF, see Fig. 3.7. This way, it is possible to fine tune the desired

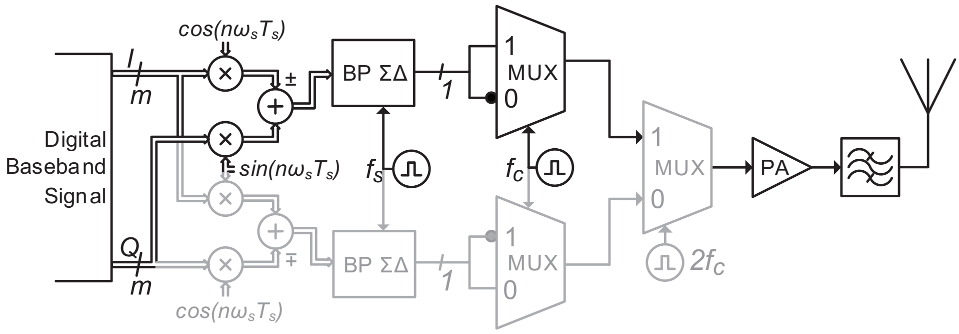

Figure 3.7: High-level illustration of a two-stage pulsed transmitter where two sets of quadrature mixers perform the first up-conversion stage to IF and three multiplexers perform the final up-conversion to RF. In this approach, the optional gray components perform the IF image rejection so that a Single-SideBand (SSB) RF carrier is produced at the output of the rightmost multiplexer.

channel frequency by slightly varying the IF local oscillator. Moreover, if only one of the RF sidebands is desired, a digital mixing based on the Weaver modulator [DKW56] can be implemented in order to generate a quadrature IF signal that will reject the undesired image if both components are combined after the RF up-conversion stage.

Although not widely adopted, there are a few pulsed transmitters found on the literature that use this approach for having higher control on the output carrier frequency [WS08, YP09, SGL10, EHG13]. Additionally, this transmitter is slightly more complex than the previous one and requires a careful design of the Weaver modulator since timing delays between the quadrature IF components or an insufficient number of quantization bits will result in a poor image rejection at the RF output.

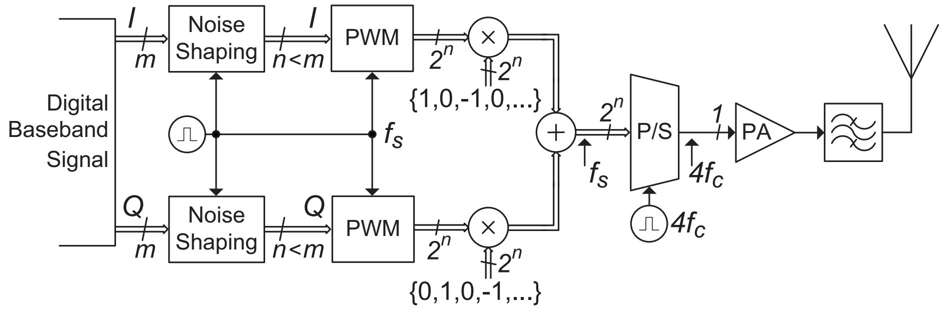

Figure 3.8: Simplified block diagram illustrating the architecture of a PWM-based pulsed transmitter where noise shaping is used to reduce the number of bits of the baseband input signal and a serializer before the SMPA is used to generate a 2-level RF output signal.

A PWM-based pulsed transmitter architecture is shown in Fig. 3.8, where an initial noise shaping stage allows reducing the bit-rate of the transmitting signal and where the entire digital processing up to the serializer is performed at baseband-level. In this approach, the up-conversion to RF is preprocessed in a similar way as in the architecture previously illustrated in Fig. 3.2, but performed at baseband and in a parallel manner. The desired RF carrier centered at f_c is produced by serializing the preprocessed signal at a bit-rate of $4f_c$.

Due to the lower operating frequency requirements and high integration capacity, this approach is very well suited for hardware implementations based on recent FPGA devices where the entire digital datapath up to the amplification stage can be implemented inside a single FPGA [YGM07b].

3.4 Discussion

All the above presented approaches provide an RF pulsed representation of the desired signal that allows taking advantage of efficient switching-mode amplification before transmitting data over the air.

However, current pulsed transmitters still have a few key limitations that prevent its wider dissemination. In fact, almost all the above cited transmitters do not support simultaneous multi-band operation, others are only able to generate low RF frequencies or require expensive high-speed multiplexers for the RF up-conversion, some have carriers with low SNR and most of them require very high-quality filters to remove out-of-band noise.

The next chapter will address some of these limitations by presenting and describing innovative FPGA-based pulsed all-digital transmitter architectures with inherent high flexibility and integration, as well as with improved key figures of merit, such as coding efficiency, SNR, usable bandwidth and in-band and out-of-band noise.

Chapter 4

Enhancement Techniques for All-Digital RF Transmitters

Outline

This chapter provides a succinct description of the main developments achieved during this PhD work plan. In that sense, each section contains a modular description of a specific key enhancement that when combined allow the development of new FPGA-based all-digital transmitters with improved figures of merit including SNR, coding efficiency, usable bandwidth, out-of-band noise emission and EVM. Most of this key achievements are presented and discussed in the several attached papers.

4.1 Transmitter Integration and Flexibility Improvements

In this section, the idea behind the proposed architecture for creating an FPGA-based System-on-Chip (SoC) containing an all-digital pulsed RF transmitter operating in the gigahertz frequency range is explained.

The proposed architecture enables the transmission of RF carriers having different standards, frequencies, modulations and spectral masks, and provides an integrated solution where the DUC to the gigahertz RF range is embedded into a single FPGA, see Fig. 4.1.

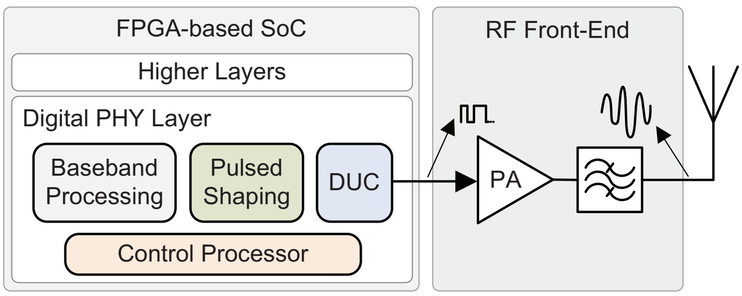

Figure 4.1: High-level block diagram of the proposed FPGA-integrated RF transmitter.

The envisioned architecture includes a digital PHY implemented in reconfigurable hardware, and an embedded control processor. This way, it becomes possible to dynamically change the hardware configuration accordingly to a software program running in the control processor. Moreover, besides out of the scope of this thesis, the used technology enables the integration of other higher layers, such as the Medium Access Control (MAC) in addition to the digital physical layer (PHY).

The proposed architecture also has the potential of enabling wireless data transmission with high power efficiency, if the digital RF output signal is fed to a SMPA [GHA+10b]. At last, the bandpass filter insertion just before transmitting the signal via the antenna allows to remove unwanted frequencies and simultaneously converts the digital RF bitstream into an analog RF signal, thus making it more suitable to be transmitted [SSBH09].

The core of this architecture is the reconfigurable up-conversion engine, presented in Fig. 4.2. This module is responsible for shaping the input data into a pulsed representation and digitally up-convert it in order to obtain the desired RF output signal.

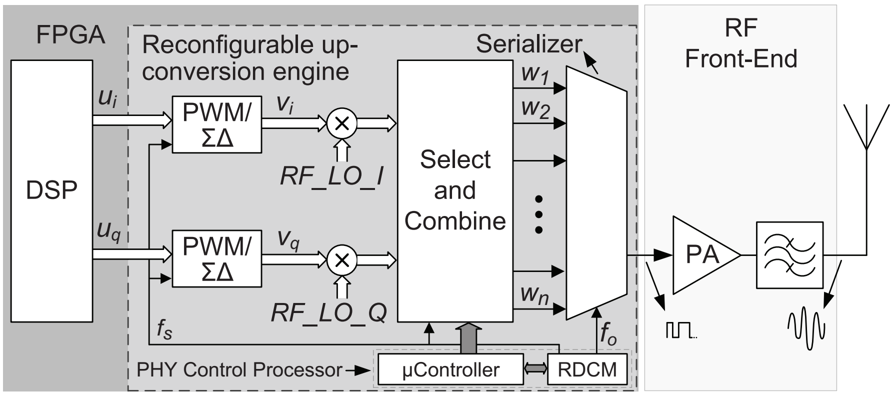

Figure 4.2: Block diagram detailing the FPGA-based up-conversion engine.

The proposed transmitter generates RF carriers by serializing a parallel word (W) at a very high data rate, see Fig. 4.2. In this transmission approach, the 2-level pulsed representation of each component is firstly multiplied by the corresponding *RF_LO* signal. The *RF_LO_I* vector is equal to (+1,0,-1,0,+1,...) and the *RF_LO_Q* is equal to (0,+1,0,-1,0,...), both having the width of the parallel word W. Then, the *Select and Combine* block will add the parallel *RF_I* and the *RF_Q* signals, resulting in a vector containing the four components of the desired signal ($+v_i$, $+v_q$, $-v_i$, $-v_q$, ...), with the dimension of W. The serialization of this vector at a high speed rate given by $4 \times f_c$ will generate an RF carrier centered at f_c.

This way, it is possible to generate and transmit an RF carrier centered in the gigahertz frequency at the FPGA outputs, while inside the required frequencies are still within the FPGA logic fabric operating range. The allowable output carrier frequency is given by:

$$fc = N \times fs, \text{ where } N \in \mathbb{N}. \tag{4.1}$$

Regarding the PHY control processor, it includes an embedded soft-core microcontroller for software programmability with low hardware overhead, interconnected to a dynamically

Reconfigurable Digital Clock Manager (RDCM). This way, it is possible through software programming to configure the FPGA-based up-conversion engine in order to generate the desired RF output.

4.1.1 Prototype Validation

The proposed RF transmitter was prototyped in an *ML605* development board containing a *Virtex6 VLX240T* FPGA. For the purpose of this proof-of-concept, the digital datapath shown in Fig. 4.2 was implemented up to the serializer and its digital RF output was directly connected to a Vector Spectrum Analyzer (VSA), model Rohde & Schwarz FSQ, see Fig. 4.3.

The validation was carried out using two second-order Low-Pass (LP) $\Sigma\Delta$-modulators operating at 125 MHz. Further details regarding the implemented $\Sigma\Delta$-modulators can be found on the appended paper A. Moreover, the proposed architecture is intended to transmit one RF carrier containing a 1.25 MHz WiMAX signal centered at 1 GHz. For that, the serializer was configured to generate an output line rate of 4 Gbps and the *Select and Combine* block was configured to produce the following 32-bit parallel output word (W):

$$W = [+v_i, +v_q, \text{-}v_i, \text{-}v_q, +v_i, +v_q, \text{-}v_i, \text{-}v_q, +v_i, +v_q, \text{-}v_i, \text{-}v_q, +v_i, +v_q, \text{-}v_i, \text{-}v_q,$$
$$+v_i, +v_q, \text{-}v_i, \text{-}v_q, +v_i, +v_q, \text{-}v_i, \text{-}v_q, +v_i, +v_q, \text{-}v_i, \text{-}v_q, +v_i, +v_q, \text{-}v_i, \text{-}v_q].$$

In this prototype the VSA measurement instrument was locked to the FPGA's on-board clock and the baseband signal data was stored inside the FPGA's internal memory. The spectrum of the FPGA-integrated architecture when transmitting a WiMAX signal centered

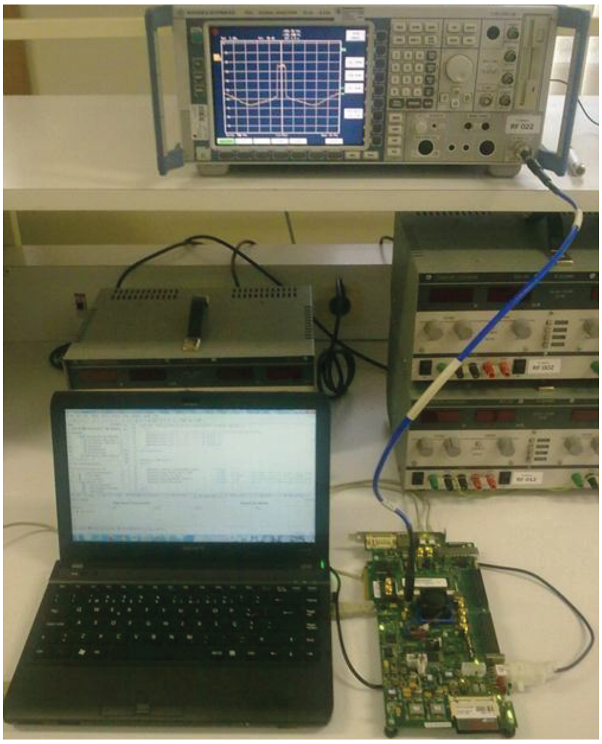

Figure 4.3: Setup illustration of an FPGA-integrated all-digital transmitter.

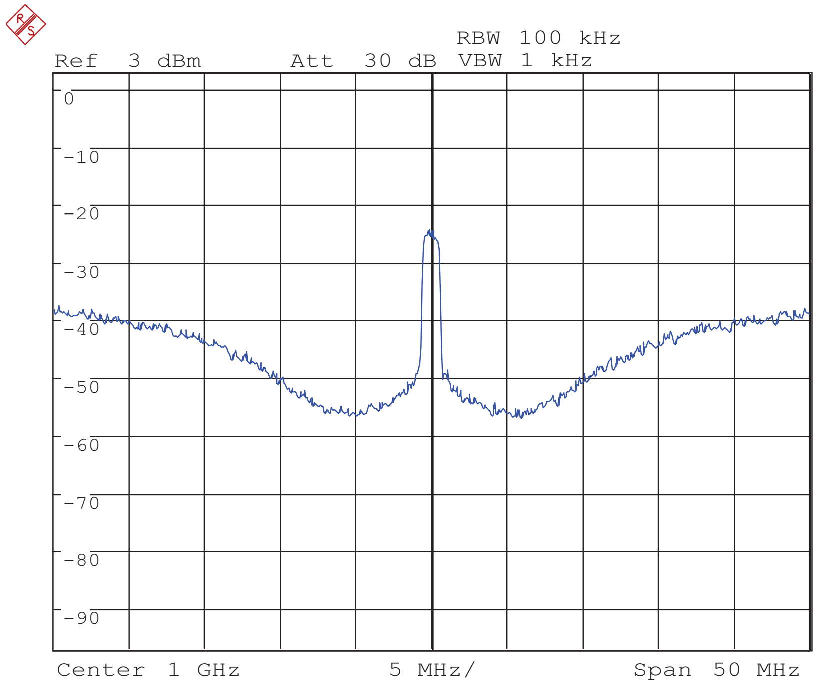

Figure 4.4: Output spectrum of a pulse-based architecture when transmitting a WiMAX signal centered at 1 GHz.

at 1 GHz is shown in Fig. 4.4. As can be seen, the prototyped flexible transmitter allows a usable bandwidth of ≈15 MHz and an Adjacent Channel Leakage Ratio (ACLR) of ≈26 dB when the entire digital datapath is still within the FPGA logic fabric operating frequency range.

4.2 Pulse-based Noise Shaping Enhancements

The key optimizations performed on pulsed data converters for improving important figures-of-merit such as the usable bandwidth, SNR and out-of-band noise emission of the previously proposed all-digital transmitter will be discussed in this section.

4.2.1 ΣΔ Design Optimizations

This Subsection details the design and optimization stages of a ΣΔ architecture that was specially optimized for hardware implementations based on FPGA technology. The topology of the designed second-order LP ΣΔ-modulator is a Cascade-of-Integrator with distributed FeedBack (CIFB) type [NST96], as illustrated in Fig. 4.5 by its general representation in the z-domain. The CIFB structure was chosen due to its good stability when used in a low-pass configuration and by its short critical path that allows a higher sampling rate. This is of critical importance since higher sampling rates move away the quantization noise from the desired signal which allows in one hand having wider band signals and in another hand reducing the quality factor of the reconstruction filter.

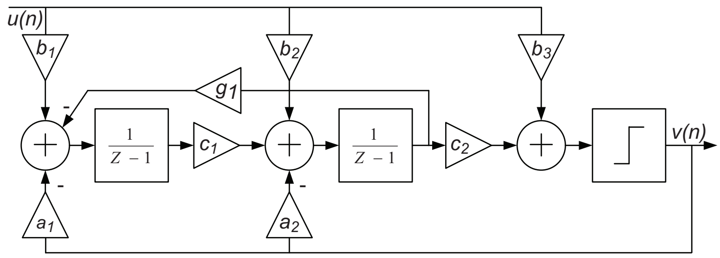

Figure 4.5: General structure of a second-order CIFB ΣΔ modulator.

The ΣΔ coefficients were precomputed using the ΣΔ-toolbox [Sch00], for a sampling rate of $f_s = 250$ MHz and with a bandpass of 20 MHz, resulting in an effective oversampling ratio (OSR) of 12.5. Moreover, in order to obtain a stable NTF, the Lee-criteria was set to $\|\text{NTF}(\omega)\|_\infty < 2$.

Those coefficients were then recomputed using a convergence process where all coefficients are rounded to powers of two or if not suitable, to a two's-complement binary representation using up to eight bits. This approach contributes in further reducing the critical path since coefficients that are powers of two can be implemented using logical shifts, hence without occupying additional hardware resources. The resulting type-2 Chebyshev highpass NTF was then calculated to be:

$$\text{NTF}(z) = \frac{z^2 - 2z + 1.039}{z^2 - 0.875z + 0.315}. \tag{4.2}$$

In Fig. 4.6 the corresponding zero-pole z-plane and the frequency response of the designed ΣΔ modulator are shown. As illustrated in Fig. 4.7, the simulated SNR is ≈40 dBc within the 20 MHz RF bandpass when using a 3.5 MHz bandlimited signal with a Peak-to-Average Power Ratio (PAPR) of 5.4 dB.

ΣΔ-based Transmitter Validation

Concerning the ΣΔ implementation, the chosen topology and optimized coefficients combined with specific design goals and strategies make possible to implement the ΣΔ-modulator at frequencies exceeding the 200 MHz in the current FPGA technology. Fig. 4.8 details the

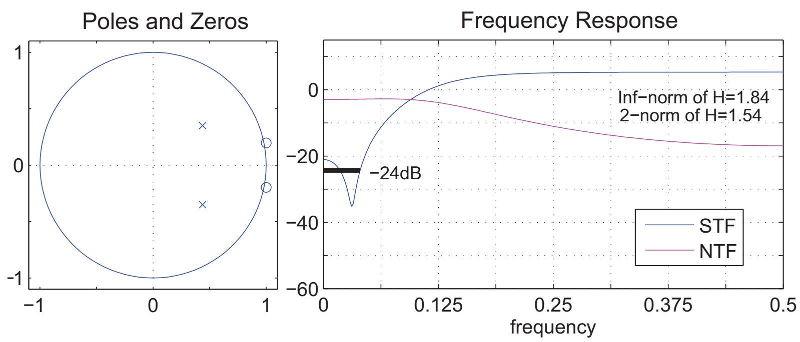

Figure 4.6: Zero-pole z-plane and frequency response of the designed CIFB ΣΔ modulator.

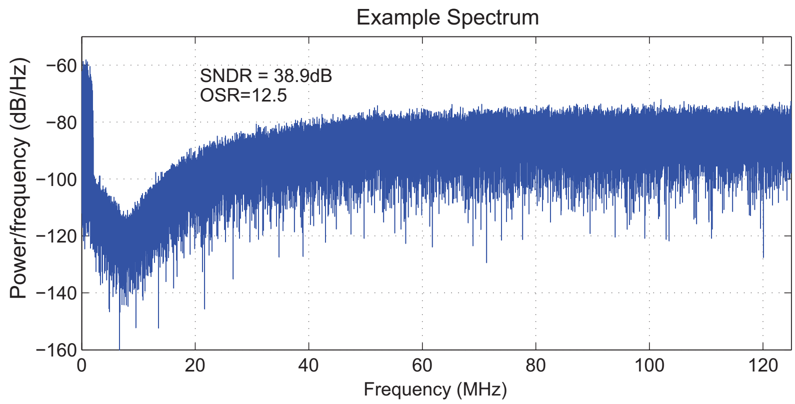

Figure 4.7: ΣΔ modulator output spectrum example for a 3.5 MHz baseband input signal.

implemented ΣΔ illustrating the full datapath and the chosen coefficients.

For the purpose of experimentally validating the designed ΣΔ-modulator, an RF transmitter based on the architecture previously described in Section 4.1 was prototyped in an *ML605* development board. In this sense, the developed ΣΔ-modulator was integrated in an FPGA-based prototype containing the digital datapath shown in Fig. 4.2, where the digital RF output signal was directly connected to a VSA for spectral and vector analysis.

In this experiment, the proposed architecture was configured to perform the transmission of one RF carrier containing a 64-QAM signal centered at 1 GHz. In this sense, the serializer was configured to produce an output line rate of 4 Gbps and accordingly to eq. (4.1) the proposed ΣΔ modulators were set to operate at a sampling frequency of 250 MHz. Again, the baseband I and Q signals were stored inside the FPGA's internal memory.

The *Select and Combine* block was configured to produce the following 16-bit parallel output word (W):

$$W = [+v_i, +v_q, -v_i, -v_q, +v_i, +v_q, -v_i, -v_q,$$
$$+v_i, +v_q, -v_i, -v_q, +v_i, +v_q, -v_i, -v_q].$$

In Fig. 4.9 a 64-QAM signal centered at 1 GHz with a bandwidth of ≈3.5 MHz is illustrated. As can be seen, the high operating frequency of the ΣΔ modulators allows an ACLR

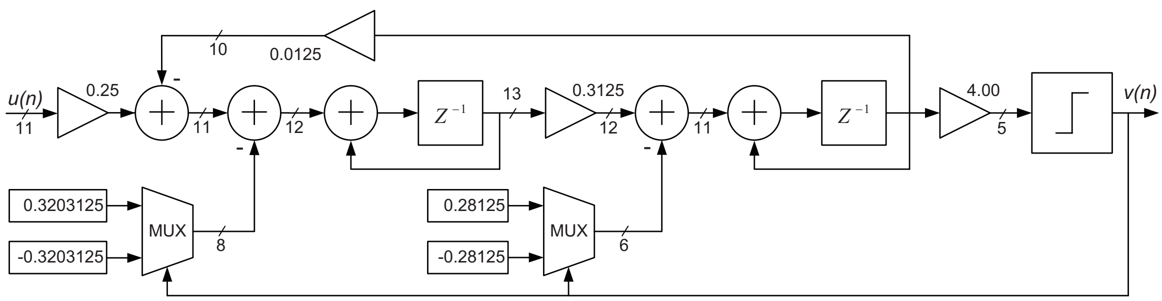

Figure 4.8: z-domain representation of the implemented CIFB second-order ΣΔ modulator.

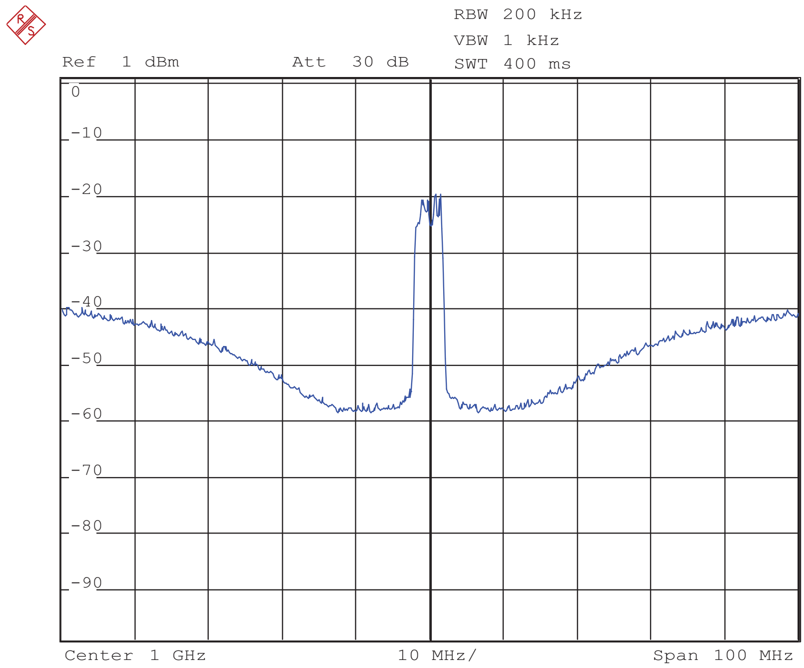

Figure 4.9: Output spectrum of a pulse-based architecture when transmitting a 64-QAM signal centered at 1 GHz.

of ≈35 dB and a usable bandwidth of ≈20 MHz, which is better when compared with the first transmitter prototype described in the previous Section. Also, this higher usable bandwidth significantly contributes in reducing the design complexity of the RF reconstruction filter by allowing filters with lower quality factors.

4.2.2 PWM Harmonic Noise Reduction

This Subsection details the design and optimization stages of a PWM-based all-digital transmitter. In this approach, both In-phase (I) and Quadrature (Q) components of the baseband signal are quantized using 8 bits, which is a good compromise between the quality of the transmitted signal and the design complexity. The 7-bit magnitude data is encoded into a 128-bit PWM word, corresponding to 129 different levels of energy (from 128 bits all zeros up to all ones). This PWM word combined with the signal information will then allow performing the RF up-conversion, see Fig. 4.10. However, if a conventional PWM approach is used, such as when using thermometer coding, each 7-bit input magnitude will match to

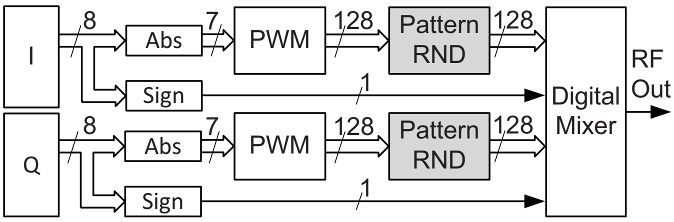

Figure 4.10: Block diagram illustrating the architecture of the PWM-based transmitter with pattern randomization.

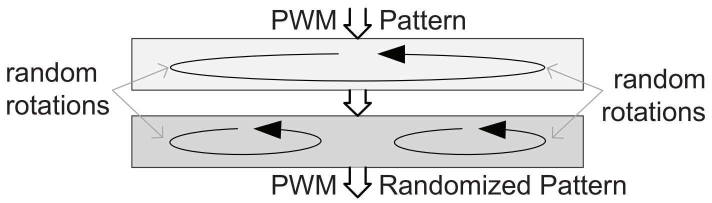

Figure 4.11: Block diagram illustrating the PWM pattern randomization process.

a specific waveform pattern that corresponds to the desired duty cycle. In this scenario, the RF transmitter will generate harmonics spaced at the PWM sampling frequency.

On the other hand, if the desired duty cycle is kept but the waveform changes arbitrarily, then it is possible to spread the energy of these harmonics over the RF spectrum, which in turn enables reducing the RF output filtering requirements. This way, the base architecture of the transmitter was extended by adding a pattern randomization block after the PWM waveform generation, see Fig. 4.10. This block performs several rotations for each sample of the 128-bit PWM word in a pseudo-random manner, see Fig. 4.11.

PWM-based Transmitter Validation

For the purpose of experimentally validating the designed PWM-based transmitter, the digital datapath shown in Fig. 4.10 was prototyped in an *ML628* development board containing a *Virtex6 HX380T* FPGA, where the digital RF output signal was directly connected to a VSA for spectral and vector analysis. Regarding the chosen PWM word length, experimental results show that by increasing from 6 to 8 the number of quantization bits of the baseband

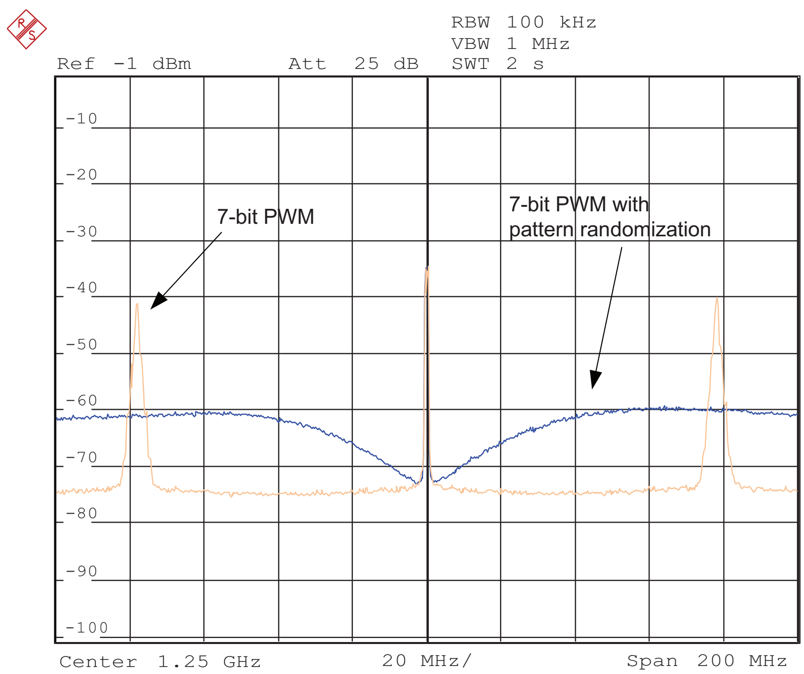

Figure 4.12: Overlapped measurement results comparing the PWM-based transmitter with and without pattern randomization.

signal, that is, using a 128-bit PWM word instead of a 32-bit word, it is possible to increase the SNR of the carrier in approx. 3 dB.

In this experiment, the proposed architecture was configured to perform the transmission of one RF carrier containing a 64-QAM signal centered at 1.25 GHz. As previously stated, at least a bit rate of $4 \times f_c$ is required to produce the desired RF carrier. However, even when used at a baseband-level, the PWM converter produces a wide parallel vector that usually requires very high data rates at the output of the serializer. In this sense, the serializer was configured to twice the minimum required bit rate, that is, 10 Gbps and the PWM modulators were set to operate at a sampling frequency of 156.25 MHz, given by:

$$fs = \frac{8 \times fc}{\text{width}(W)}, \tag{4.3}$$

where fc is the chosen carrier frequency, and width(W) is the width of the word that will be fed to the serializer. In this experiment, the *Digital Mixer* block was configured to generate the following 64-bit output word:

$$\begin{aligned} W = [&+v_i, +v_i, +v_q, +v_q, -v_i, -v_i, -v_q, -v_q, +v_i, +v_i, +v_q, +v_q, -v_i, -v_i, -v_q, -v_q, \\ &+v_i, +v_i, +v_q, +v_q, -v_i, -v_i, -v_q, -v_q, +v_i, +v_i, +v_q, +v_q, -v_i, -v_i, -v_q, -v_q, \\ &+v_i, +v_i, +v_q, +v_q, -v_i, -v_i, -v_q, -v_q, +v_i, +v_i, +v_q, +v_q, -v_i, -v_i, -v_q, -v_q, \\ &+v_i, +v_i, +v_q, +v_q, -v_i, -v_i, -v_q, -v_q, +v_i, +v_i, +v_q, +v_q, -v_i, -v_i, -v_q, -v_q]. \end{aligned}$$

After serializing W it is possible to obtain the spectrum shown in Fig. 4.12. For comparison purposes, the obtained spectrum resulting from the PWM-based RF transmitter with and without pattern randomization is shown overlapped. As can be seen, the noise energy existing at the PWM harmonics is spread across the RF spectrum when using the pattern randomization approach. While this technique does not reduce the total out-of-band noise emission, having lower noise peaks can simplify the design of the RF reconstruction filter. Further details regarding the implemented PWM-based transmitter can be found on the appended papers B and D.

4.3 Concurrent Multi-Standard Data Transmission

This Section contains key achievements regarding the development of FPGA-embedded pulsed RF transmitters operating in the gigahertz frequency range and capable of simultaneously transmitting multiple independent RF signals.

4.3.1 Simultaneous Multi-band Transmitter

The proposed ΣΔ-based architecture described in this Subsection extends previous work by enabling the simultaneous transmission of multiple carriers with different standards, frequencies, modulations and spectral masks in an integrated solution where the digital up-conversion to RF operating in the gigahertz frequency range and the multichannel capacity are embedded into a single digital chip, such as an FPGA.

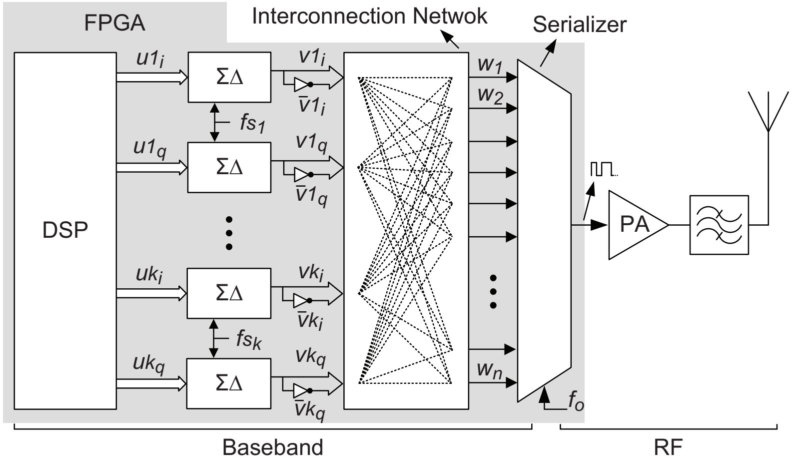

Figure 4.13: Block diagram illustrating the proposed multi-band transmitter.

A block diagram of the proposed concurrent multi-band transmitter architecture is illustrated in Fig. 4.13. In this architecture, each $\Sigma\Delta$ pair is used to process the I and Q data from each channel. The resulting signals of the $\Sigma\Delta$ modulators and its inverted versions are then connected to a multi-gigabit serializer through an interconnection network. This network allows to combine and replicate the output signal of the $\Sigma\Delta$ modulators for generating a parallel output word (W).

The first step to generate W consists of constructing a vector containing the four components of the desired signal ($v_i v_q \bar{v}_i \bar{v}_q$), and then replicating it by the digital up-conversion factor N, given by f_c / f_s. As previously stated, the serialization of this vector at a bitrate of $4 \times f_c$ would generate a single RF carrier centered at f_c.

In a multi-band transmission scenario, this procedure must be done for each carrier. However, since each channel will have a distinct f_c, applying the above described procedure will result in different output bitrates for each channel. Since the multichannel transmission followed in this approach requires all channels operating at the same rate, the Least Common Multiple (LCM) of all output bitstreams is computed and each preconstructed vector is extended so that its waveform is maintained for the new bitrate given by the LCM. Finally, the multichannel transmission is carried out by time interleaving the vectors of each carrier. The allowable output frequencies for each carrier are given by:

$$fc_1 = N_1 \times fs_1 \text{ to } fc_k = N_k \times fs_k \text{ where } N_1 \text{ to } N_k \in \mathbb{N}. \tag{4.4}$$

In this approach the sampling frequencies of all $\Sigma\Delta$ modulators (fs_1 to fs_k) must have an integer relation and the multi-gigabit serializer should produce an output bitrate given by the LCM of the desired carrier frequencies times eight. The digital signal at the output of the serializer can then be fed to a SMPA for efficient amplification.

Multi-band Prototype Validation

For the purpose of experimentally validating the proposed multi-band transmitter, the datapath illustrated in Fig. 4.13 containing the $\Sigma\Delta$ modulators previously detailed in Subsection 4.2.1 was prototyped in an *ML628* development board.

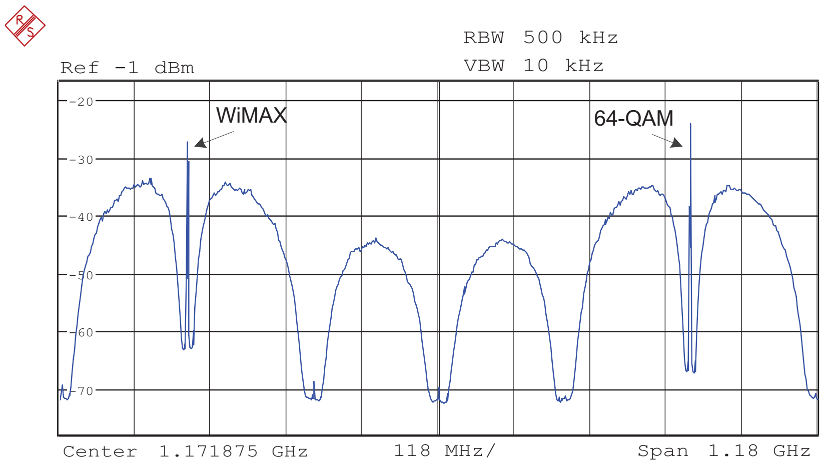

Figure 4.14: Measured spectrum of the proposed concurrent multi-band transmitter.

The proposed architecture was configured to implement the simultaneous transmission of two different carriers, one centered at 1.5625 GHz containing a 64-QAM signal and a second carrier containing a WiMAX signal centered at 781.25 MHz. All $\Sigma\Delta$ modulators were configured to operate at 195.3125 MHz. The interconnection network was configured to generate the following 64-bit output word:

$$\begin{aligned} W = [&v1_i\ v2_i\ v1_q\ v2_i\ \bar{v}1_i\ v2_q\ \bar{v}1_q\ v2_q\ v1_i\ \bar{v}2_i\ v1_q\ \bar{v}2_i\ \bar{v}1_i\ \bar{v}2_q\ \bar{v}1_q\ \bar{v}2_q \\ &v1_i\ v2_i\ v1_q\ v2_i\ \bar{v}1_i\ v2_q\ \bar{v}1_q\ v2_q\ v1_i\ \bar{v}2_i\ v1_q\ \bar{v}2_i\ \bar{v}1_i\ \bar{v}2_q\ \bar{v}1_q\ \bar{v}2_q \\ &v1_i\ v2_i\ v1_q\ v2_i\ \bar{v}1_i\ v2_q\ \bar{v}1_q\ v2_q\ v1_i\ \bar{v}2_i\ v1_q\ \bar{v}2_i\ \bar{v}1_i\ \bar{v}2_q\ \bar{v}1_q\ \bar{v}2_q \\ &v1_i\ v2_i\ v1_q\ v2_i\ \bar{v}1_i\ v2_q\ \bar{v}1_q\ v2_q\ v1_i\ \bar{v}2_i\ v1_q\ \bar{v}2_i\ \bar{v}1_i\ \bar{v}2_q\ \bar{v}1_q\ \bar{v}2_q]. \end{aligned}$$

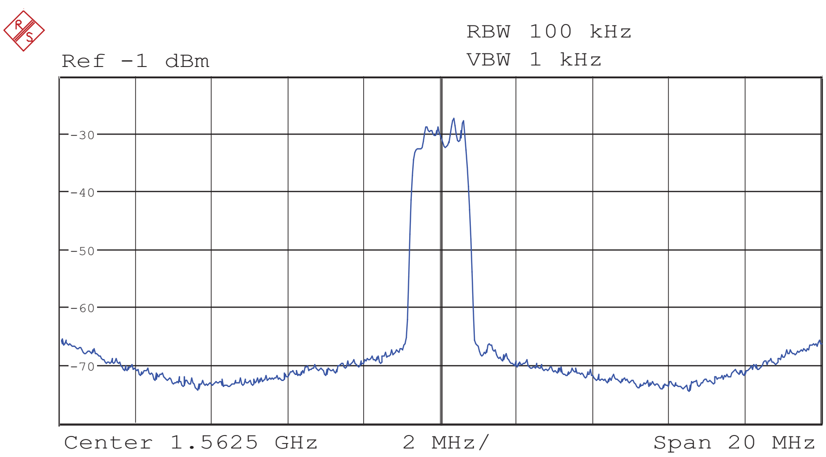

Figure 4.15: Measured spectrum illustration containing a closer view of the 64-QAM signal.

Table 4.1: Modulation accuracy of the 64-QAM signal centered at 1.5625 GHz.

	Measured result	
EVM	1,8	%
Magnitude Error	0,8	%
Phase Error	1,0	deg
SNR (MER)	34,7	dB

In this approach the serializer was set to produce an output bitstream of 12.5 Gbps, that is, eight times the bitrate given by the LCM of the two RF carriers. The obtained spectrum of the multi-band architecture when simultaneously transmitting a WiMAX signal centered at 781.25 MHz and a 64-QAM signal centered at 1.5625 GHz is shown in Fig. 4.14. A closer view of the 64-QAM signal can be found in Fig. 4.15.

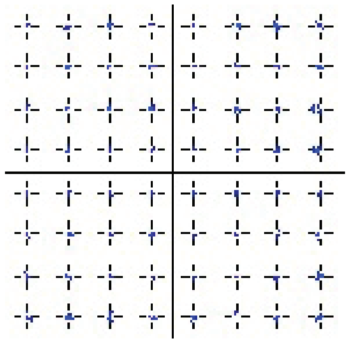

Figure 4.16: Constellation of a 64-QAM signal centered 1.5625 GHz.

The modulation accuracy measurements for a 64-QAM signal centered at 1.5625 GHz are shown in Table 4.1. The obtained results demonstrate the feasibility of this multi-band approach where the low Error Vector Magnitude (EVM) of 1.8% is more than sufficient for enabling a well-defined constellation, as can be seen in Fig. 4.16.

Table 4.2: Main occupied resources of the implemented multi-band all-digital transmitter.

Logic resources	Occupied	Available
Flip-Flops	291	478080
LUTs	496	239040
RAM36E1	14	768
GTHE1_QUADs	1	6

Regarding the occupied resources, the entire datapath takes only about 1% of the FPGA fabric, see Table 4.2, providing a large area available for other system functionalities, as well as a vast grade of integration including for instance, the signal processing of baseband protocols or even higher protocol layers. Further details regarding this concurrent multi-band transmitter can be found on the attached papers A and C.

4.3.2 Fine Tunable Multichannel Transmitter

This Section details the design stage regarding the development of a pulse-based concurrent multichannel transmitter with fine frequency tuning for individual channel selection.

In this new architecture, the fine frequency tuning is achieved by using a two-stage up-conversion approach where IF image rejection is used in order to maximize the usable bandwidth of the RF transmitter. The first up-conversion stage uses a digital Single-SideBand (SSB) signal generation approach based on the Weaver modulator [DKW56], where a set of two multipliers shift the baseband components (b_i and b_q) into an IF signal (u_i) and two other multipliers generate a 90° phase shifted IF signal centered at the same frequency (u_q), as can be seen in Fig. 4.17.

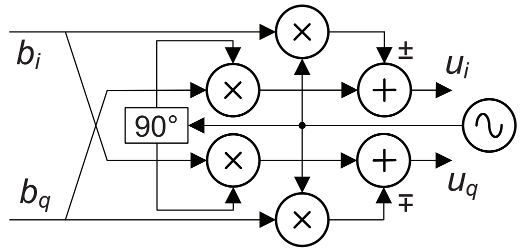

Figure 4.17: Block diagram illustrating the implemented quadrature single-sideband up-converter for IF image rejection.

After the first up-conversion stage, the IF signal is converted into a 2-level representation using ΣΔ modulation. A block diagram detailing the architecture of the proposed fine tunable multichannel transmitter is shown in Fig. 4.18. In this architecture, each channel uses a ΣΔ pair to process the IF components (u_i and u_q) generated by the first up-conversion stage. The resulting signals of the ΣΔ modulators and its inverted versions are then connected to a serializer through an interconnection network.

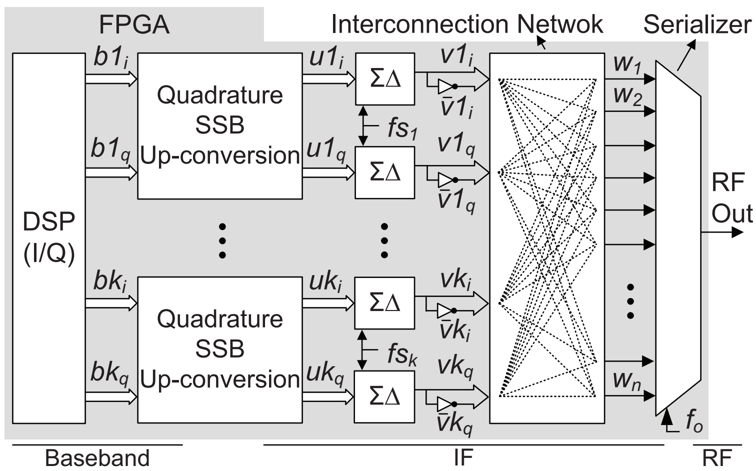

Figure 4.18: Proposed agile transmitter detailing the fine frequency tuning of the multichannel carriers by using a two-stage up-conversion approach combined with SSB signal generation.

As previously described, this network combines and replicates the $\Sigma\Delta$ output signals to generate a parallel output word (W) that contains for each channel, the four components of the desired signal ($v_i v_q \bar{v}_i \bar{v}_q$). Serializing this parallel word will produce a multichannel RF SSB signal where the order given to the four components of the desired signal will determine for each channel, which sideband is generated. For instance, serializing $v_i v_q \bar{v}_i \bar{v}_q$ will generate an RF carrier centered at the Lower SideBand (LSB) and serializing $v_i \bar{v}_q \bar{v}_i v_q$ will result in an RF carrier centered at the Upper SideBand (USB) of the spectrum.

Prototype Validation

As proof-of-concept, the datapath shown in Fig. 4.18 was prototyped in a *Xilinx ML628* development board and its digital RF output signal was directly connected to a VSA. The baseband test signals used in this experiment are one WiMAX (OFDM based) and two 64-QAM signals, all stored inside the FPGA's internal memory.

In a first experiment, the prototyped RF transmitter was configured to simultaneously transmit three independent carriers, one centered at 745.5 MHz containing a Narrow Band (NB) 64-QAM ($\mathrm{b1_{iq}}$), a second one centered at 748.5 MHz containing a Wider Band (WB) 64-QAM ($\mathrm{b2_{iq}}$) and a third one centered at 753.0 MHz, containing a WiMAX signal ($\mathrm{b3_{iq}}$).

For this implementation example, the first up-conversion stage was configured to shift each one of the three baseband signals to a different IF band. The wider 64-QAM signal was up-converted to a 1.5 MHz IF, while the narrow band 64-QAM was shifted to 4.5 MHz, and the WiMAX to 3 MHz. All $\Sigma\Delta$ modulators were set to operate at 187.5 MHz and the interconnection network was configured to generate the following 48-bit word:

$$\begin{aligned} W = [&v1_i\ v2_i\ v3_i\ \bar{v}1_q\ \bar{v}2_q\ v3_q\ \bar{v}1_i\ \bar{v}2_i\ \bar{v}3_i\ v1_q\ v2_q\ \bar{v}3_q\ v1_i\ v2_i\ v3_i\ \bar{v}1_q \\ &\bar{v}2_q\ v3_q\ \bar{v}1_i\ \bar{v}2_i\ \bar{v}3_i\ v1_q\ v2_q\ \bar{v}3_q\ v1_i\ v2_i\ v3_i\ \bar{v}1_q\ \bar{v}2_q\ v3_q\ \bar{v}1_i\ \bar{v}2_i \\ &\bar{v}3_i\ v1_q\ v2_q\ \bar{v}3_q\ v1_i\ v2_i\ v3_i\ \bar{v}1_q\ \bar{v}2_q\ v3_q\ \bar{v}1_i\ \bar{v}2_i\ \bar{v}3_i\ v1_q\ v2_q\ \bar{v}3_q]. \end{aligned}$$

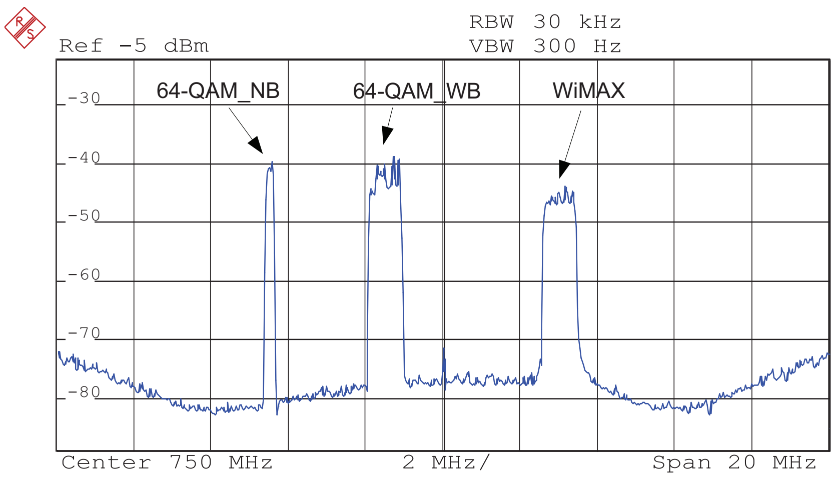

Figure 4.19: Measured multichannel spectrum when the fine tunable RF transmitter is configured to simultaneously generate three independent carriers, one centered at 745.5 MHz, a second one centered at 748.5 MHz and a third one centered at 753.0 MHz.

Serializing W at a rate of 9 Gbps will produce a multichannel RF signal with a 750 MHz central frequency, given by the line rate / (number of channels $\times$ 4). Moreover, the order given in W to the four components $(v_i v_q \bar{v}_i \bar{v}_q)$ of the three channels will impose the two 64-QAM signals appearing at the LSB of the central frequency, while the WiMAX signal will appear at the HSB, as shown in Fig. 4.19.

As a second experiment, the implemented RF transmitter was configured to perform the simultaneous transmission of three carriers, one centered at 373.5 MHz, a second one centered at 378.0 MHz and a third one centered at 753.0 MHz. In this implementation example, all frequencies and data rates are equal to the first experiment, with exception to the narrow band 64-QAM signal that was shifted to a 3 MHz IF in the first up-conversion stage. Again, all $\Sigma\Delta$ modulators were set to operate at 187.5 MHz and the interconnection network was configured to generate the following 48-bit word:

$$\begin{gathered} W = [v1_i\ v2_i\ v3_i\ v1_i\ v2_i\ v3_q\ v1_q\ \bar{v}2_q\ \bar{v}3_i\ v1_q\ \bar{v}2_q\ \bar{v}3_q\ \bar{v}1_i\ \bar{v}2_i\ v3_i\ \bar{v}1_i \\ \bar{v}2_i\ v3_q\ \bar{v}1_q\ v2_q\ \bar{v}3_i\ \bar{v}1_q\ v2_q\ \bar{v}3_q\ v1_i\ v2_i\ v3_i\ v1_i\ v2_i\ v3_q\ v1_q\ \bar{v}2_q \\ \bar{v}3_i\ v1_q\ \bar{v}2_q\ \bar{v}3_q\ \bar{v}1_i\ \bar{v}2_i\ v3_i\ \bar{v}1_i\ \bar{v}2_i\ v3_q\ \bar{v}1_q\ v2_q\ \bar{v}3_i\ \bar{v}1_q\ v2_q\ \bar{v}3_q]. \end{gathered}$$

The serialization of W at a rate of 9 Gbps will generate a multichannel RF signal with a lower central frequency of 375 MHz and a higher central frequency of 750 MHz. Once again, the order given in W to the four components $(v_i v_q \bar{v}_i \bar{v}_q)$ of the three channels will impose the narrow band 64-QAM and the WiMAX signals to appear at the HSB of their central frequencies, while the wider 64-QAM will appear at the LSB. Further details regarding this concurrent multichannel transmitter can be found on the attached paper E.

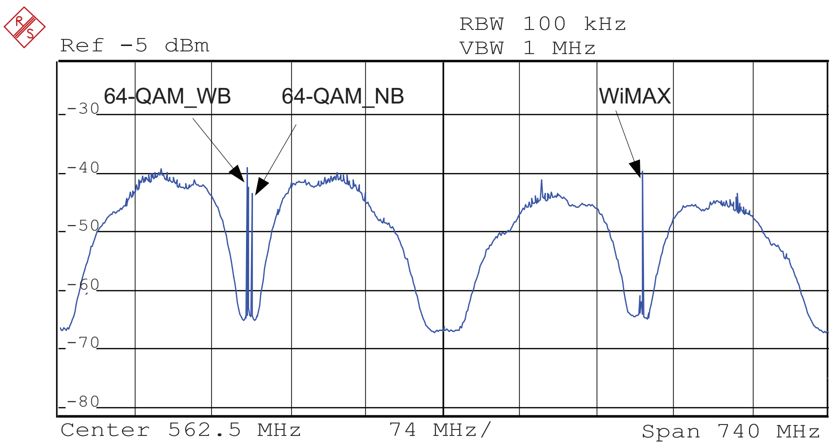

Figure 4.20: Measured multichannel spectrum when the proposed FPGA-based transmitter is configured to simultaneously transmit three independent carriers.

4.4 Coding Efficiency Optimization

This section details the development of a new transmitter architecture that significantly improves the coding efficiency and also reduces the RF filtering requirements while maintaining the inherent flexibility of conventional all-digital transmitters.

A key idea for improving the coding efficiency of this transmitter without sacrificing the flexibility consisted in reducing the overall noise by using polyphase multipath circuits, such as reported in [MKN05, BK10].

The base concept of noise reduction through polyphase circuits relies on having multiple paths where the phase of the desired signal is kept constant but where the unwanted noise has different canceling phases, see Fig. 4.21. This way, when the output signals of the multipath circuits are combined, the energy of the desired signal will grow proportionally to the number of multipath circuits while ideally the noise components will cancel, and therefore it will directly improve the overall coding efficiency of the transmitter. The high level block diagram of the proposed polyphase multipath agile transmitter is shown in Fig. 4.22 where the multichannel operation and a higher number of phases are omitted for the sake of simplicity.

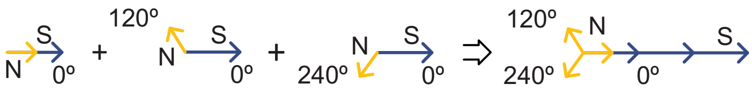

Figure 4.21: Illustration of the noise canceling idea when using polyphase noise.

The proposed transmitter shown in Fig. 4.22 is constituted by two independent paths, one containing noise at 0º and another one where the noise was shifted to 180º. Each independent path applies a specific phase shift to the baseband I and Q components (u_i, u_q). These phase shifted signals are then shaped using PWM or ΣΔ modulation in order to make them suitable for the used RF up-conversion process.

In this transmitter architecture, the first step to generate W requires each pulse modulated component to be multiplied by the corresponding RF_LO signal. However, each RF_LO vector has a specific phase for each independent path. This way, the mixing process also performs a phase shift to the entire signal (both the desired information and the unwanted noise). For the 0º datapath, the $RF\_LO\_I^0$ and $RF\_LO\_Q^0$ vectors should produce a -0º phase shift. In the proposed architecture, these vectors are equal to (+1,0,-1,0,+1,...) and (0,+1,0,-1,0,...), respectively.

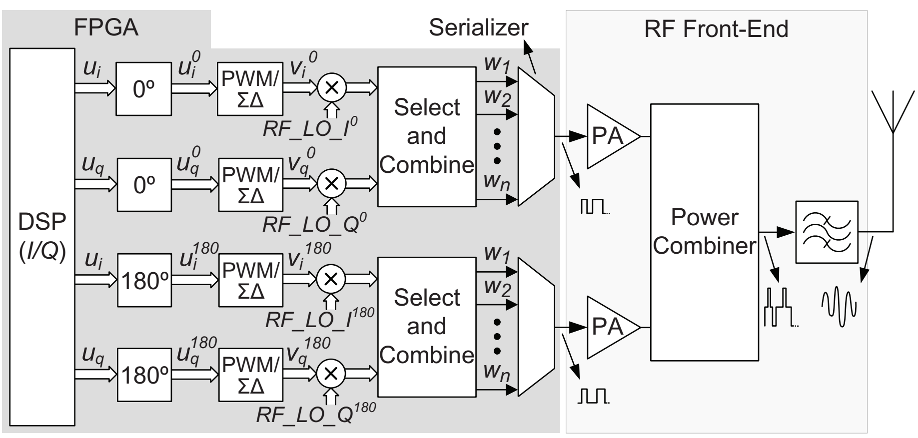

Figure 4.22: Single channel illustration of the proposed polyphase multipath agile transmitter architecture.

The *Select and Combine* block will simply add the RF_I and the RF_Q components, resulting in a vector containing the four components of the desired signal ($+v_i$, $+v_q$, -v_i, -v_q, ...), with the dimension of W. As in previous transmitters, the serialization of this vector at a bitrate of $4 \times f_c$ will generate a single RF carrier centered at f_c.

For the 180º datapath, the $RF\_LO\_I^{180}$ and $RF\_\ LO\_Q^{180}$ vectors should produce a phase shift of -180º. In the proposed architecture, these vectors are equal to (-1,0,+1,0,-1,...) and (0,-1,0,+1,0,...), respectively. After the RF up-conversion stage, the desired signal of all independent paths is now phase aligned while the noise has different phases. This way, it is possible to combine the energy of all RF paths using a power combiner, and consequently improve the SNR of the desired signal.

4.4.1 ΣΔ-based RF Transmitter

This Subsection details the design stage of a ΣΔ-based agile and coding efficient all-digital transmitter. This transmitter extends the proposed architecture shown in Fig. 4.22 by using 90º and 270º phases in addition to the 0º and 180º, see Fig. 4.23. This way it is possible to further improve the SNR of the desired signal.

The designed transmitter uses the same baseband information (I and Q) for each specific path. As a good design trade-off between SNR and the ΣΔ operating speed, each baseband component is quantified using 10 bits. This information is then shifted to the proper phase and then shaped into a 3-level representation using ΣΔ modulation. Then, each specific path will perform the Digital Up-Conversion (DUC) using a proper phase so that all paths have the desired signal shifted to the same phase. The LUT block will convert the 3-level two's complement signal into a 2-bit word where the integers *-2*, *0* and *2* are converted into *00*, *01* and *11*, respectively.

The *Select and Split* block will then send to one serializer a vector containing only the Most Significant bit (MSb) while another vector containing only the Least Significant bit (LSb) will be sent to another serializer, as shown in Fig. 4.23.

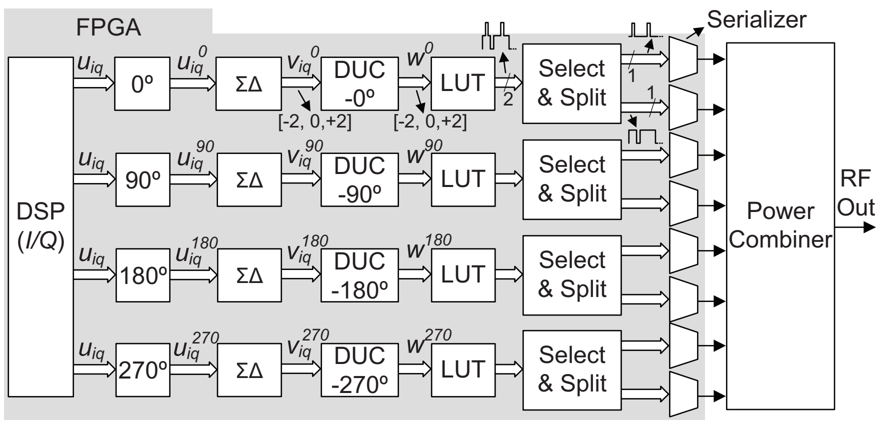

Figure 4.23: High level block diagram illustrating the implemented ΣΔ-based polyphase multipath agile transmitter.

Again, after the serialization process, the desired signal of all independent paths is now phase aligned and centered at fc while the noise has different phases. This way, when all paths are combined, the desired signal will have an improved SNR.

4.4.2 PWM-based RF Transmitter

The design stage details regarding the PWM-based transmitter illustrated in Fig. 4.25 will be given in this Subsection. In this approach, the proposed transmitter requires a baseband signal where each component is quantified using 8 bits, 1 for the signal and 7 for the magnitude. For each individual path, the 7-bit magnitude information is directly translated into a PWM word accordingly to a specific PWM matrix.

For the first two independent paths, the used 128-by-128 PWM matrix can be described as a triangular lower filled with ones, as shown below:

$$PWM_0 = \begin{bmatrix} 1 & & 0 \\ \vdots & \ddots & \\ 1 & \cdots & 1 \end{bmatrix}$$

For the last two independent paths, the used 128-by-128 PWM matrix is a horizontal mirror of the first one, as shown below:

$$PWM_1 = \begin{bmatrix} 0 & & 1 \\ & \iddots & \vdots \\ 1 & \cdots & 1 \end{bmatrix}$$

Since each row of PWM_1 has the same number of ones as in PWM_0, the resulting pulsed signal will have the same energy after the PWM encoding, regardless the used PWM matrix. However, since the ones are placed at different positions for the chosen PWM matrix, the

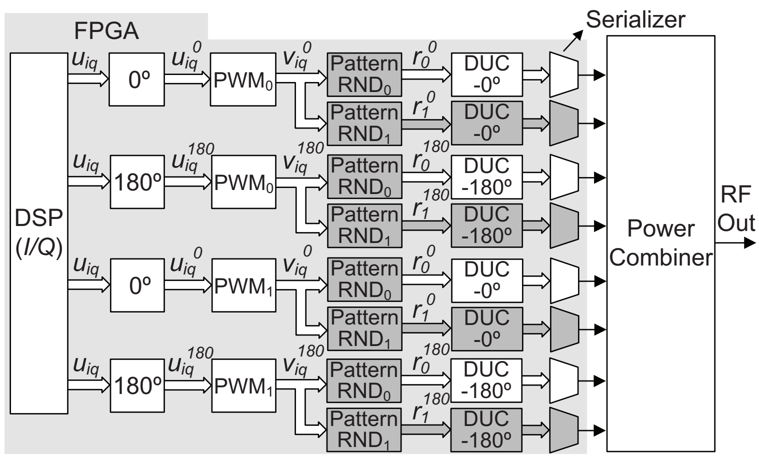

Figure 4.24: High level block diagram illustrating the implemented PWM-based polyphase multipath transmitter. The optional blocks are shown in dark gray.

PWM noise will appear with different phases. This way, when combining all RF outputs, the energy of the desired signal will add in a higher proportion than the unwanted noise.

Additionally, when the optional *Pattern Randomization* block is used, the PWM noise is spread along the RF spectrum, which can be interesting for reducing the RF filter requirements. In this sense, the designed transmitter applies in *Pattern* RND_0 the noise spreading technique detailed in Subsection 4.2.2 where a set of pseudo-random rotations are performed for each PWM word.

In this approach the same random rotations are applied to several PWM samples, as can be seen in Fig. 4.24. On the other hand, since shifting the position of the ones in each PWM word will change the PWM noise phase, the proposed transmitter was expanded to include an additional *Pattern* RND_1. This block will implement a different set of pseudo-random rotations, allowing to duplicate the number of output paths with different phase noise, and therefore improving the SNR of the desired signal.

Prototype Validation

As a proof-of-concept, three different variants of the proposed agile and coding efficient all-digital transmitter were prototyped and experimentally validated. The first variant concerns a ΣΔ-based RF transmitter while the other variants will present PWM-based data transmission with and without pattern randomization.

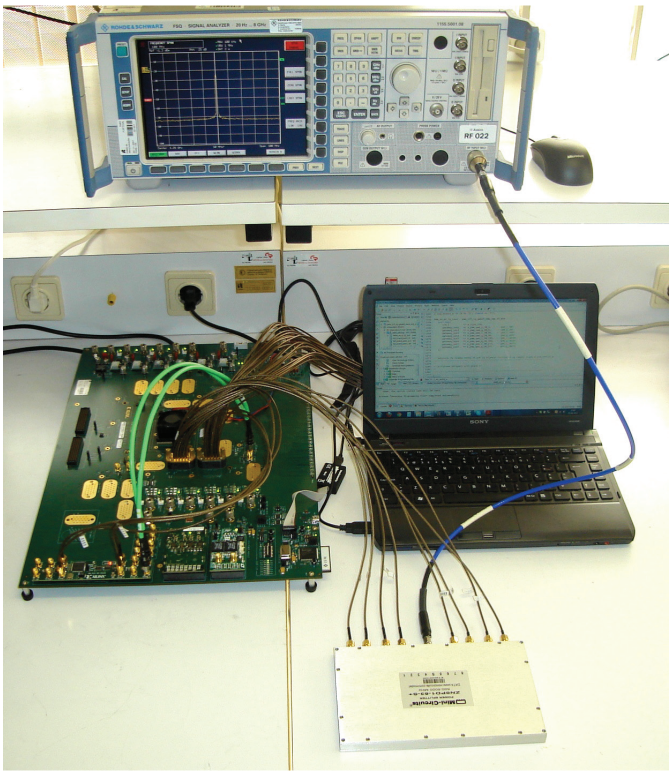

Figure 4.25: Setup of the evaluated FPGA-based all-digital transmitter.

In this experiment, the base datapath shown in Fig. 4.22 was prototyped in a *Xilinx ML628* development board where its digital RF outputs were connected to a *Mini-Circuits* 8:1 RF power combiner model *ZN8PD1-53+*. Finally power combiner was directly connected to a VSA for vector and spectral analysis, as can be seen in Fig. 4.25.

The baseband test signal used in this setup is a 64-QAM signal with a symbol rate of 1.25 MSPS and a Peak-to-Average Power Ratio (PAPR) of approx. 7 dB. Moreover, all baseband signals were stored inside the FPGA's internal memory.

Efficient ΣΔ-based Transmitter

As a first experiment, the implemented RF transmitter architecture illustrated in Fig. 4.23 was configured to perform the transmission of one carrier centered at 1.25 GHz and containing a 64-QAM signal. This implementation used the ΣΔ model previously described in Subsection 4.2.1. The implemented ΣΔ modulators were set to operate at a sampling frequency of 156.25 MHz. For the first independent path, the *RF_LO* vectors and the *Select and Combine* block of the *DUC -0º* were configured to generate the following 32-bit output word:

$$W^{0} = [-v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,].$$

For the second path, the *DUC -90º* was configured to generate the following word:

$$W^{90} = [+v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,].$$

The *DUC -180º* was configured to generate the following 32-bit output word:

$$W^{180} = [+v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,].$$

For the last independent path, the *DUC -270º* was configured to generate the following 32-bit output word:

$$W^{270} = [-v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,\ -v_q,\ +v_i,\ +v_q,\ -v_i,].$$

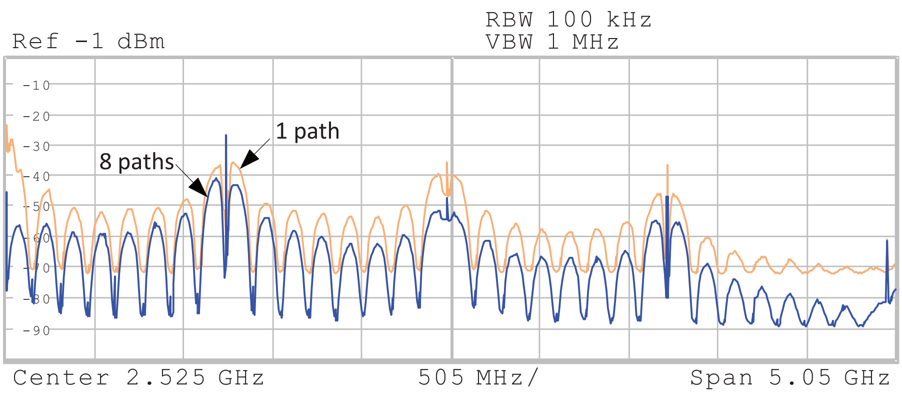

Figure 4.26: Overlapped measurement results for the ΣΔ-based agile transmitter when using 8 paths versus a single path approach with a gain normalized to the 8 paths.

These output words were then converted into a 2-bit representation and split so that each bit is fed to one multigigabit serializer. The serializer must be configured to operate at a line rate that is 4 times the desired carrier frequency. This way, for the 1.25 GHz carrier, the serializer was set to operate at 5 Gbps.

After combining the outputs of the 8 serializers it is possible to obtain the spectrum shown in Fig. 4.26. For comparison purposes, the obtained spectrum resulting from combining 8 paths is shown overlapped with a single path and the gain for the single path was normalized to the 8-path implementation results. As can be seen, for the same energy of the desired signal, the 8-path implementation has clearly less out-of-band noise. This way, the proposed transmitter clearly allows to improve the coding efficiency while maintaining the flexibility inherent to the all-digital transmitter concept.

Efficient PWM-based Transmitter

As a proof-of-concept, two PWM-based variants of the proposed agile and coding efficient all-digital transmitter were experimentally validated. One using a pure PWM-based architecture, while the other combines PWM with a pattern randomizer block.

In both cases the transmitters where configured to implement a 1.25 GHz carrier containing a 64-QAM signal so that it is possible to provide a better comparison with the previously implemented ΣΔ-based transmitter. Accordingly to eq. (4.3), all 7-bit PWM modulators were set to operate at the same sampling frequency of 156.25 MHz. Also, all independent paths perform the DUC in a similar way to the previously implemented ΣΔ-based transmitter.

After combining the outputs of the 4 serializers for the PWM-based transmitter without pattern randomization, it is possible to obtain the spectrum shown in Fig. 4.27. For comparison purposes, the obtained spectrum resulting from combining 4 paths is shown overlapped with a single path. Again, the single path spectrum results were normalized to the 4-path implementation results for an easier comparison.

As can be seen, for the same energy on the carrier, the single path spectrum shows a considerable higher noise. Moreover, the 8-path implementation has a significant PWM

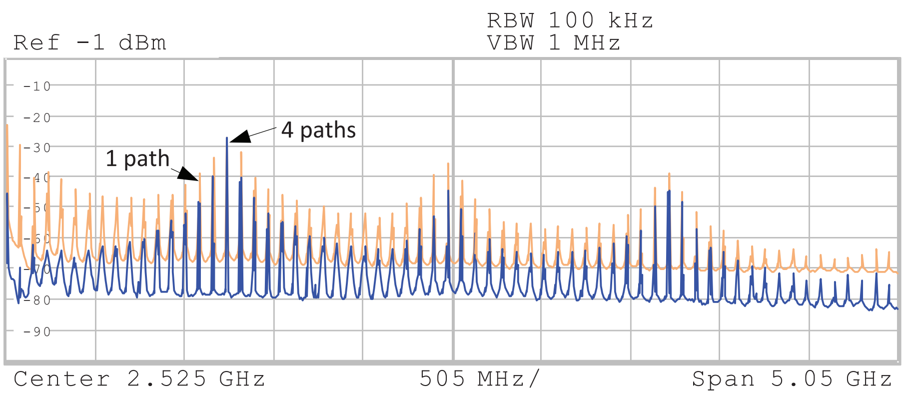

Figure 4.27: Overlapped measurement results for the PWM-based transmitter without pattern randomization when configured with 4 paths vs. a single path with normalized gain.

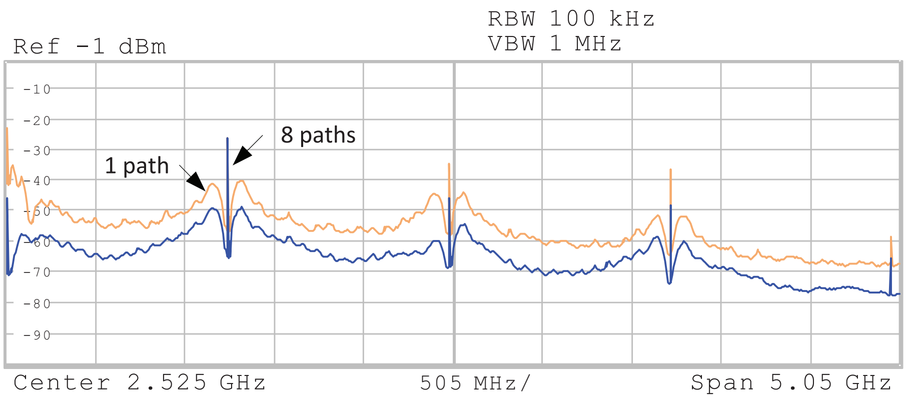

Figure 4.28: Overlapped measurement results for the PWM-based transmitter with pattern randomization when configured with 8 paths versus a single path with a gain normalized to the 8 paths.

noise reduction for the lower frequency harmonics. This way, it is clear that the proposed PWM-based transmitter allows significant improvements in terms of coding efficiency.

The FPGA hardware was then reconfigured to implement the PWM-based transmitter with pattern randomization. In Fig. 4.28 the obtained spectrum is shown overlapped for one implementation where 8 paths are combined with a single path approach with gain normalized to the 8-path implementation. Again, the obtained results show clear improvements in terms of coding efficiency. Moreover, it can be seen that using pattern randomization allows reducing the peak spurious which in turn can be interesting for alleviating the quality factor requirements of the RF reconstruction filter.

Comparative Analysis

The spectrum results for the PWM-based approach with and without pattern randomization and the ΣΔ-based transmitter are shown overlapped in Fig. 4.29 so that a better comparative analysis between the implemented transmitters is possible.

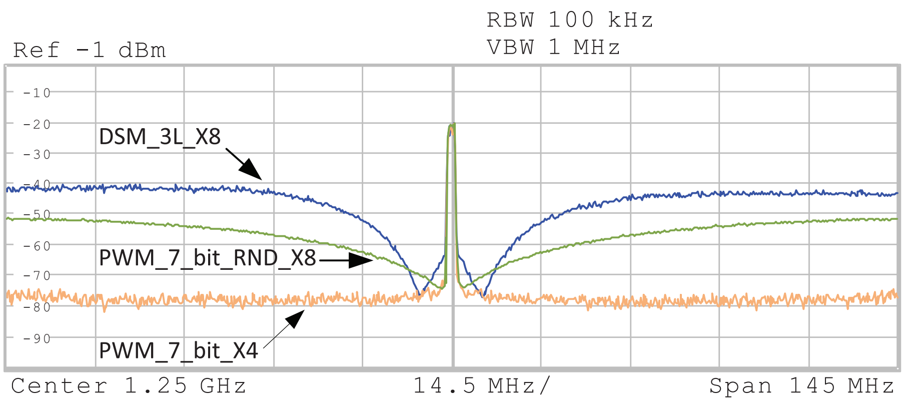

Figure 4.29: Overlapped measurement results comparing the PWM-based approach with and without pattern randomization ant the ΣΔ-based transmitter.

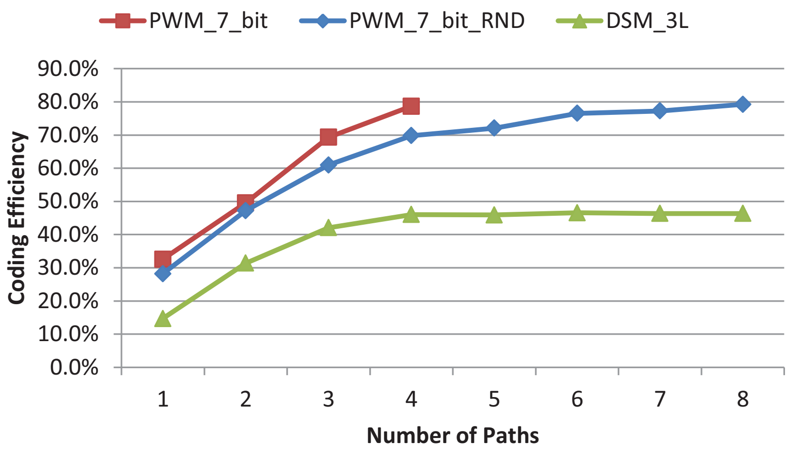

Figure 4.30: Coding efficiency evolution accordingly to the number of used transmission paths for the three implemented transmitters.

As can be seen in Fig. 4.29, the worse implementation in terms of coding efficiency is the ΣΔ-based transmitter, where the quantization noise is clearly higher than in the other approaches. The implementation with lower out-of-band noise within the 145 MHz span is the 7-bit PWM without pattern randomizer. However, this approach generates PWM harmonics with considerable high levels of energy spaced at the PWM sampling frequency. By spreading the PWM noise over the frequency, the 7-bit PWM implementation with pattern randomization successfully eliminates the undesirable PWM harmonics.

The coding efficiency evolution and the modulation accuracy evolution accordingly to the number of used transmission paths for the three implemented transmitters are shown in Figs. 4.30 and 4.31, respectively. As anticipated by the previous results shown in Fig. 4.29, the ΣΔ-based transmitter approach has the lower coding efficiency and lower Error Vector magnitude (EVM). Moreover, the power combining of multiple independent paths with a different phase noise has also less impact in this approach, especially when combining more

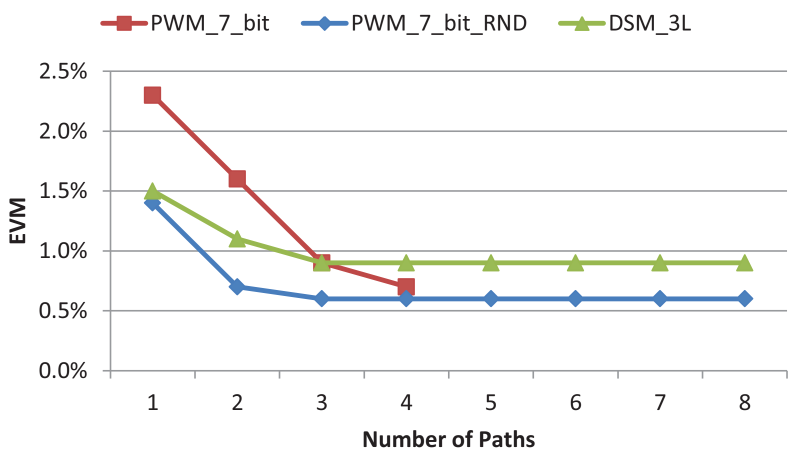

Figure 4.31: Error vector magnitude evolution accordingly to the number of used transmission paths for the three implemented transmitters.

Table 4.3: Comparison with other all-digital transmitter approaches

	[JS06]	[HRLA07]	[GHA+10b]	[SHGB11]	PWM_7_bit	PWM_7_bit_RND	DSM_3L
Signal	W-CDMA	CDMA	WiMAX	N/D	64-QAM	64-QAM	64-QAM
Cod. Eff.	3.4%	32.0%	6.6%	35.0%	78.7%	79.3%	46.3%
SNR	74.5dB	43dB	45dB	N/D	50dB	50dB	45dB
Modulation	2-level ΣΔ	3-level ΣΔ	2-level ΣΔ	3-level ΣΔ	7-bit PWM	7-bit PWM	3-level ΣΔ
Validation	Simulation	Simulation	Hardware	Simulation	Hardware	Hardware	Hardware

than 4 paths. A possible explanation may rely in the fact that in ΣΔ modulation, the variation of the output signal is higher than when using a PWM-based approach. This way, these higher variations at the output of the transmitter combined with non-ideal output waveforms of the serializers and also with small timing mismatches between the independent paths are a possible explanation for this worse performance when combining a higher number of independent paths.

The PWM-based approach with pattern randomization combines the best results in terms of modulation accuracy with a high coding efficiency. In fact, discarding the typical 1.5 dB insertion losses of the power combiner, the total energy resulting from combining the 8 independent paths is only 1.4 dB lower when compared with the ideal addition. This means that almost all energy of the desired signal is adding constructively in this proposed all-digital transmitter. At last, the PWM-based transmitter without pattern randomization has also proven to be an interesting approach when combining multiple independent paths, as can be seen by the obtained high coding efficiency and high modulation accuracy.

A comparison between several state-of-the-art all-digital transmitters is shown in Table 4.3. As can be seen, all the proposed transmitters provide very high coding efficiency and reasonable high SNR, while maintaining the high flexibility inherent to the all-digital pulsed RF transmitters. Further details regarding this coding efficient transmitter can be found on the attached paper D.

4.5 Discussion

The key developments presented in this chapter include the design and prototyping of novel all-digital transmitter architectures supporting the RF transmission of multi-band, multi-rate and multi-standard signals in a highly integrated approach where the RF output signal operating in the microwave frequency range is produced inside a single FPGA device.

In that sense, several main limitations that prevent a wider adoption of conventional pulse-based transmitters were addressed in this chapter by presenting innovative all-digital transmitter architectures with improved figures of merit including coding efficiency, SNR, usable bandwidth and in-band and out-of-band noise.

The above presented enhancements effectively contribute in shortening the gap towards the development of flexible and coding efficient digital radio transmitters where the pulsed representation of the desired RF signal allows taking advantage of efficient switching-mode amplification before transmitting data over the air.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

The work performed in the scope of this PhD thesis included the design and FPGA-based prototyping of innovative all-digital transmitter architectures with superior flexibility and integration, and where improving important figures of merit, such as coding efficiency, SNR, usable bandwidth and in-band and out-of-band noise was also addressed.

In the first part of this thesis, the concept of transmitting RF data using an entirely digital approach based on pulsed modulation was introduced. A comparison between several implementation technologies was then presented, allowing to show that FPGAs provide an interesting compromise between performance, power efficiency and flexibility, making them an interesting choice as an enabling technology for pulse-based all-digital transmitters.

Following this discussion, the fundamental concepts inherent to pulsed modulators, its key advantages, main limitations and typical enhancements suitable for SMPA-based all-digital transmitters were also presented. The recent advances regarding the two most common classes of pulse modulated transmitters, namely the RF and the baseband-level were introduced, along with several examples of state-of-the-art architectures found on the literature.

The core of this dissertation containing the main developments achieved during this PhD work was then presented and discussed. The first key contribute to the state-of-the-art consisted in the development of a novel $\Sigma\Delta$-based all-digital transmitter architecture capable of multiband and multi-standard data transmission in a very flexible and integrated way, where the pulsed RF output operating in the microwave frequency range is generated inside a single FPGA device.

A fundamental contribution regarding the simultaneous transmission of multiple RF signals was then introduced by presenting and describing novel all-digital transmitter architectures that take advantage of multi-gigabit data serializers available on current high-end FPGAs, in order to transmit in a time-interleaved approach multiple independent RF carriers. Further improvements in this design approach allowed to provide a two-stage up-conversion transmitter enabling the fine frequency tuning of concurrent multichannel multi-standard signals. In comparison to the previous work, this approach contributes to the state-of-the-art by proposing a pulse-based multi-rate, multi-band, multi-standard transmission architecture that significantly minimizes the output frequencies restrictions of current approaches by allowing fine frequency tuning for channel selection.

Further improvements regarding two key limitations inherent to current all-digital transmitter approaches were then addressed, namely the poor coding efficiency and the combined high quality factor and tunability requirements of the RF output filter. The followed design approach based on poliphase multipath circuits allowed to create a new FPGA-embedded agile transmitter architecture that significantly improves important figures of merit, such as coding efficiency and EVM, while maintains the high flexibility that is required for supporting multichannel multimode data transmission and where the RF output carriers operating in the GHz frequency range are still generated inside a single FPGA device.

5.2 Future Work

Pulse-based all-digital transmitters currently have an enourmous potential thanks to its high operation flexibility, unmatched integration in reconfigurable hardware and by unlocking further investigation regarding wireless data transmission with superior power efficiency.

However, current FPGA-based all-digital transmitter approaches include pulsed modulators operating only at a few hundreds of megahertz. While lower frequencies are typically desired from a power consumption point of view, the truth is that such operating frequency limits the maximum signal bandwith that can be transmitted, since a smaller oversampling ratio, and consequently a lower SNR, is obtained when using wider band signals.

A possible research direction consists in exploring the concept of time-interleaved $\Sigma\Delta$ modulation where several $\Sigma\Delta$ modulators process the input samples of the desired signal in a parallel manner. This approach has the potential to increase the $\Sigma\Delta$ throughput and consequently improving the SNR of the desired signal.

Another possibilty that worth investigating consists in using fast and low order $\Sigma\Delta$ architectures producing multilevel outputs followed by PWM re-quantization. Such approach produces a 2-level pulsed signal suitable for switched mode amplification while has the potential to improve key figures-of-merit, including SNR, usable bandwidth and coding efficiency.

Lastly, other design approaches involving the FPGA-based development of flexible, multichannel, multistandard digital transmitters with very low out-of-band noise generation should also be considered. One possible approach consists in creating an RF power DAC, where several multigibabit outputs produced from a single FPGA are individually amplified and then combined using an output matching network.

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Appended Papers

Paper A

A Novel All-Digital Multichannel Multimode RF Transmitter Using Delta-Sigma Modulation

Nelson V. Silva, Arnaldo S. R. Oliveira, Ulf Gustavsson and Nuno Borges Carvalho

in *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 3, pp. 156-158, 2012.

The format has been revised.

A Novel All-Digital Multichannel Multimode RF Transmitter Using Delta-Sigma Modulation

Nelson V. Silva, Arnaldo S. R. Oliveira, Ulf Gustavsson and Nuno Borges Carvalho

Abstract

In this letter, we present a new all-digital multichannel multimode transmitter architecture. The main novelty is the development of an agile radio transmitter where the digital up-conversion to RF operating in the gigahertz frequency range and the multichannel transmission capacity are embedded into a single Field-Programmable Gate Array (FPGA) device. Its high flexibility and fast switching of the carriers' frequencies make this transmitter interesting for cognitive radio-based applications.

A.1 Introduction

Wireless communications gained unprecedented attention over the last years leading to the proliferation of different wireless standards and pushing an additional research effort towards the development of new smart radios, capable to adapt to different communication scenarios.

In this sense, the well-known Cognitive Radio (CR) concept [1] holds the potential for implementing the supreme universal radio. However, in order to achieve such a new deployment, the physical layer of CR transmitters must be able to support the simultaneous transmission of multi-band, multi-rate, multi-standard signals, which in practice is very hard or very inefficient to implement using conventional approaches.

Nevertheless, the last developments on this field include novel FPGA-based all-digital transmitter architectures [2, 5, 4, 4], where the datapath is digital from the baseband up to the RF stage. Such concept has inherent high flexibility and poses an important step towards the development of CR transmitters.

In this letter, we extend previous work by combining multi-channel with multiband multistandard data transmission capabilities in a new $\Sigma\Delta$-based all-digital transmitter architecture. To the best of our knowledge, it is also the first digital multichannel implementation where an RF output signal operating in the gigahertz frequency range is generated inside an FPGA.

The remainder of this paper is organized as follows. Section A.2 details the RF transmitter architecture. The experimental results of the proposed multichannel multimode transmitter are reported in section A.3. Section A.4 presents the conclusion.

A.2 Digital RF Transmitter Architecture

This section starts by reviewing a conventional $\Sigma\Delta$-based digital transmitter architecture. Next, the idea behind the proposed architecture for generating a multichannel multimode digital RF transmitter operating in the gigahertz frequency range is explained.

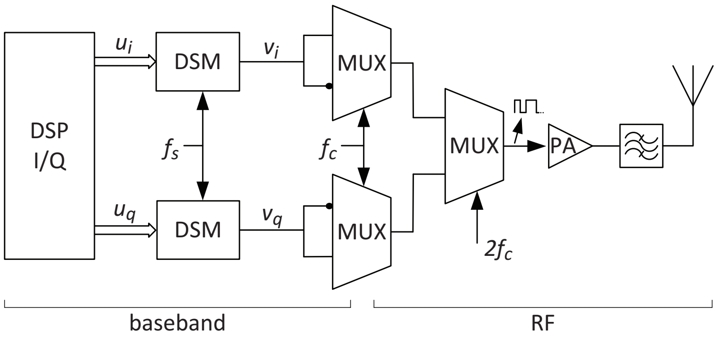

Figure A.1: Block diagram of a conventional $\Sigma\Delta$-based transmitter.

A.2.1 Review of ΣΔ-based Transmitter Architectures

Fig. A.1 presents the architecture of a typical ΣΔ-based all-digital transmitter. Such an architecture uses low-pass ΣΔ modulators operating at the sampling frequency f_s to generate the bi-level outputs v_i and v_q from the baseband In-phase (I) and Quadrature (Q) data, respectively. The three multiplexers are then used to digitally up-convert and mix the bi-level v_i and v_q signals for in order to generate an RF output signal centered at $f_c = N \times f_s$.

In [2, 3, 5, 4, 4], the authors present digital transmitters identical to the presented architecture. However, current state-of-the-art all-digital transmitters are still very restrictive for supporting multichannel data transmission. In [4], the authors present simulation results for a dual-band transmitter using ΣΔ modulators clocked at a frequency of several GHz, which is very hard to implement using current technology. The remaining architectures all fail to transmit two or more different carriers at a time. Moreover, such transmitters are only able to generate low RF frequencies or require external multiplexers for enabling carriers operating in the gigahertz frequency range.

A.2.2 Proposed Multichannel Multimode Transmitter Topology

The proposed ΣΔ-based architecture extends previous work by adding the following two main contributions: a) it enables the simultaneous transmission of multiple carriers with different standards, frequencies, modulations and spectral masks, and b) it provides an integrated solution where the digital up-conversion to RF operating in the gigahertz frequency range and the multichannel capacity are embedded into a single device, such as a Field-Programmable Gate Array (FPGA).

The second-order low-pass ΣΔ-modulator used in this letter is a cascade-of-resonators with distributed feed-forward (CRFF) type [11], as illustrated in Fig. A.2 by its z-domain representation. The feed-forward coefficients were selected using the ΣΔ-toolbox [8]. In the optimization, the sampling rate was set to $f_s = 125$ MHz with an RF pass-band of 10 MHz, resulting in an effective oversampling ratio (OSR) of 12.5. In order to guarantee stability, the Lee-criteria were set to $\|\mathrm{NTF}(\omega)\|_\infty < 2$ in the optimization.

The resulting type-2 Chebyshev highpass Noise-Transfer Function (NTF) was calculated to be:

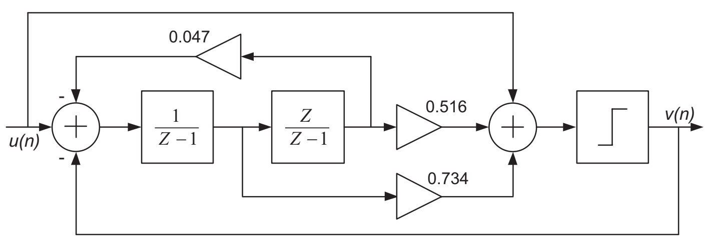

Figure A.2: Representation in z-domain of the implemented ΣΔ modulator.

$$\mathrm{NTF}(z) = \frac{z^2 - 1.953z + 1}{z^2 - 0.703z + 0.266}. \tag{A.1}$$

As shown in Fig. A.3, the simulated dynamic range was > 40 dBc within the 10 MHz pass-band when used with a 1 MHz bandlimited Gaussian noise signal with 9.9 dB Peak-to-Average Power Ratio (PAPR). The calculated NTF is included in the plot for comparison.

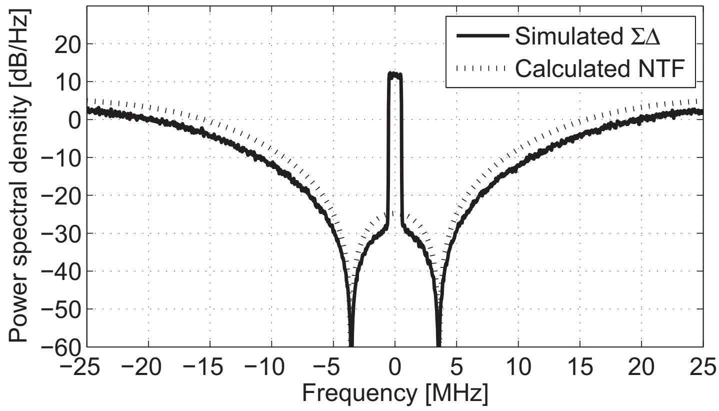

Figure A.3: Baseband power spectral density of simulated ΣΔ-modulator output and calculated NTF.

Concerning the ΣΔ implementation, the chosen second-order CRFF topology has a feedback path shorter than other higher order topologies. This contributes to reducing the critical path, which consequently enables a higher operating frequency. Moreover, through extensive logic optimization involving the binary precision for data representation, combined with specific design goals and strategies, it was possible to implement the ΣΔ-modulator to operate at a maximum frequency of 126 MHz in a Virtex6 VLX240T FPGA.

In Fig. A.4, a block diagram of the proposed multichannel transmitter architecture is shown. In this architecture, each ΣΔ pair is used to process the I and Q data from each

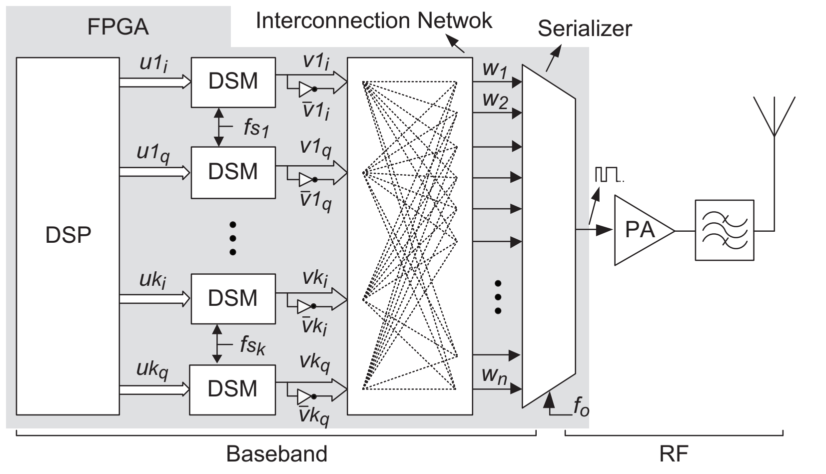

Figure A.4: Block diagram of the proposed multichannel transmitter.

channel. The resulting signals of the $\Sigma\Delta$ modulators and its inverted versions are then connected to a multi-gigabit serializer through an interconnection network. This network allows to combine and replicate the output signal of the $\Sigma\Delta$ modulators for generating a parallel output word (W).

The first step to generate W consists of constructing a vector containing the four components of the desired signal ($v_i v_q \bar{v}_i \bar{v}_q$), and then replicating it by the digital up-conversion factor N, given by $f_c \div f_s$. The serialization of this vector at a bitrate of $4 \times f_c$ would generate an RF carrier centered at f_c.

In a multichannel transmission scenario, this procedure must be done for each carrier. However, since each channel will have a distinct f_c, applying the above described procedure will result in different output bitrates for each channel. Since the multichannel transmission followed in this approach requires all channels operating at the same rate, the Least Common Multiple (LCM) of all output bitstreams is computed and each preconstructed vector is extended so that its waveform is maintained for the new bitrate given by the LCM. Finally, the multichannel transmission is carried out by time interleaving the vectors of each carrier.

The allowable output frequencies for each carrier are given by: $fc_1 = N_1 \times fs_1$ to $fc_k = N_k \times fs_k$ where N_1 to $N_k \in \mathbb{N}$. Moreover, the sampling frequencies of all $\Sigma\Delta$ modulators (fs_1 to fs_k) must have an integer relation.

In order to ensure the proper functioning, the FPGA-embedded serializer should produce an output bitrate given by the LCM of the desired carrier frequencies times eight. Since this serializer operates in both clock edges, it should be clocked at a frequency f_o that is half the output bitrate.

The serializer output signal can then be fed to a switching-mode Power Amplifier (PA). Future PAs suitable for this type of architecture are expected to enable wireless data transmission with high power efficiency.

The filter before the antenna has a dual functionality: a) it shapes the spectral mask by removing unwanted signals and b) it converts the digital bitstream to an analog signal, making it more suitable to be transmitted by the antenna [9].

A.3 Experimental Results

The proposed architecture was implemented in an ML605 development board containing a Virtex6 VLX240T FPGA. For the purpose of this proof-of-concept, we implemented the digital datapath shown in Fig. A.4 up to the serializer and connected its digital RF output directly to a Vector Spectrum Analyzer (VSA), model Rohde & Schwarz FSQ. The entire datapath occupies only about 1% of the FPGA fabric (250 Flip-Flops and 1368 LUTs), providing a large area available for other system functionality and a vast grade of integration. The architecture was configured to implement the simultaneous transmission of two different carriers, one centered at 1 GHz containing a WiMAX signal and the second one centered at 500 MHz and containing a 64-QAM signal. All $\Sigma\Delta$ modulators were set to operate at a sampling rate of 125 MHz. The interconnection network was configured to generate the following 32-bit output word:

$$\begin{aligned} w_o = [&v1_i \; v2_i \; v1_q \; v2_i \; \bar{v}1_i \; v2_q \; \bar{v}1_q \; v2_q \; v1_i \; \bar{v}2_i \; v1_q \; \bar{v}2_i \; \bar{v}1_i \; \bar{v}2_q \; \bar{v}1_q \; \bar{v}2_q \\ &v1_i \; v2_i \; v1_q \; v2_i \; \bar{v}1_i \; v2_q \; \bar{v}1_q \; v2_q \; v1_i \; \bar{v}2_i \; v1_q \; \bar{v}2_i \; \bar{v}1_i \; \bar{v}2_q \; \bar{v}1_q \; \bar{v}2_q]. \end{aligned}$$

The serializer was set to operate at a frequency f_o of 4 GHz, thus generating an output bitstream of 8 Gbps. This output signal was then connected to a VSA for spectral and vector analysis. All measurement instruments were locked to the FPGA's on-board clock and the baseband I and Q of both signals were stored inside the FPGA's internal memory.

In Fig. A.5 the spectrum of the multichannel architecture when transmitting a 64-QAM signal centered at 500 MHz and a WiMAX signal centered at 1 GHz is shown.

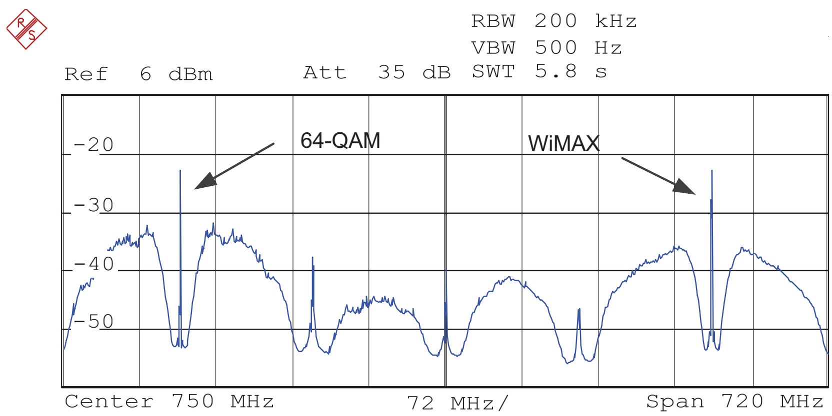

Figure A.5: Measured multichannel spectrum of the proposed transmitter.

Fig. A.6 shows a closer view of the WiMAX signal. As can be seen, the high operating frequency of the $\Sigma\Delta$ modulators allows a usable bandwidth of $\approx$12 MHz. Also, the resulting Signal-to-Noise and Distortion Ratio (SNDR) is $\approx$35 dB.

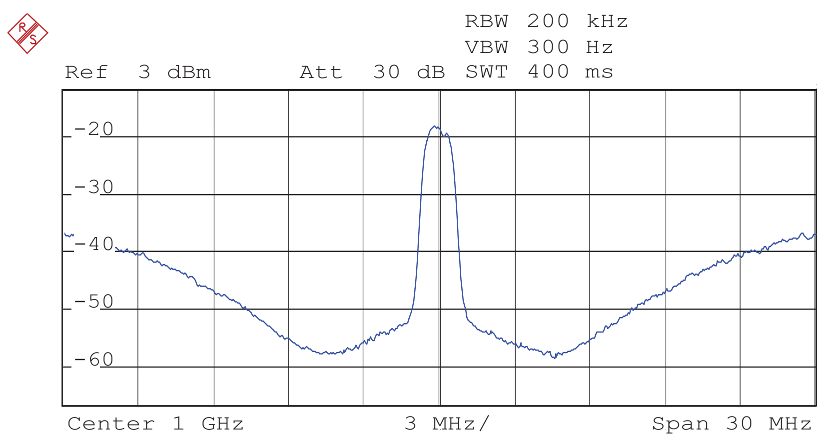

Figure A.6: Output spectrum of the multichannel transmitter for a WiMAX signal.

Table A.1: Modulation accuracy measurements for a 64-QAM signal centered at 1 GHz

	Result	Peak	Unit
EVM	3,050	9,176	%
Magnitude Error	1,128	3,591	%
Phase Error	1,49	5,27	deg
CarrierFreq. Error	1,76		Hz

The high flexibility of this architecture makes it possible to swap the carriers by only changing the interconnection network. In fact, with a latency of one clock cycle, it is possible to place the 64-QAM signal centered at 1 GHz while the WiMAX signal will appear centered at 500 MHz. This flexibility can also be an important feature for improving jamming robustness and for cognitive radio-based applications.

At last, Table A.1 illustrates several modulation accuracy parameters for a 64-QAM signal centered at 1 GHz.

A.4 Conclusion

In this letter, a new multichannel multimode transmitter architecture is presented and validated. The use of a second-order CRFF $\Sigma\Delta$ permits a high operating frequency which consequently enables a higher usable bandwidth and relaxes the quality factor requirements of the RF output filter. Moreover, the use of a switching-mode PA for driving the digital RF output signal of the serializer has the potential for enabling wireless data transmission with higher power efficiency.

At last, the fast switch of the carriers' frequencies makes this transmitter interesting for improving jamming robustness and for cognitive radio-based applications.

Acknowledgment

This work was partially supported by the Portuguese Foundation for Science and Technology (FCT) under project TACCS (ref. PTDC/EEA-TEL/099646/2008) and by the Instituto de Telecomunicações under project DiRecTRadio (ref. LA-LVT-8).

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Paper B

Evaluation of Pulse Modulators for All-Digital Agile Transmitters

Nelson V. Silva, Arnaldo S. R. Oliveira and Nuno B. Carvalho

in *IEEE MTT-S International Microwave Symposium Digest (MTT)*, June 2012, pp. 1-3.

The format has been revised.

Evaluation of Pulse Modulators for All-Digital Agile Transmitters

Nelson V. Silva, Arnaldo S. R. Oliveira and Nuno Borges Carvalho

Abstract

All-digital transmitters are gaining increased access over the last years, mainly due to white space technology needs. In this paper a new FPGA-based multichannel multimode transmitter architecture is presented. The new configuration includes improvements in PWM and $\Sigma\Delta$ Modulators, which are designed in order to optimize important figures of merit for RF transmitters as coding efficiency, usable bandwidth and SNR. The high flexibility of this architecture allows to easily change the frequency of the carriers as also the spectral masks, making it suitable for using in cognitive radio-based applications.

B.1 Introduction

The unprecedented attention given to wireless communications over the last years pushes an additional effort towards the research and development of Cognitive Radios [1], capable of adapting to different communication scenarios in order to meet the channel conditions as well as the network and user demands. However, achieving such a new deployment requires a very flexible physical layer (PHY) in order to support the transmission of multi-band, multi-rate and multi-standard signals, which in practice is very hard to implement using conventional approaches.

Nevertheless, the last developments in this field include novel all-digital transmitters where the PHY path is digital from the baseband up to the RF stage [2, 3, 5, 4]. Such concept has inherent high flexibility and poses an important step towards the development of CR transmitters.

However, current state-of-the-art digital transmitter architectures are still very restrictive. The transmitters reported in [2, 3, 5, 4] fail to transmit two or more different carriers at a time, almost all require very high-quality filters to remove out-of-band noise, others only generate low RF frequencies [2], many require expensive external multiplexers for implementing the RF up-conversion [3, 5] or have carriers with low SNR [4].

In this paper, we extend previous work by presenting an FPGA-embedded agile transmitter based on pulse modulators that supports multichannel, multimode data transmission. This new configuration includes improvements in PWM and ΣΔ modulators, which were designed in order to enhance important figures of merit for RF transmitters, such as coding efficiency, usable bandwidth and SNR.

The remainder of this paper is organized as follows. The ΣΔ modulator design and improvement is detailed in Section B.2. The design and optimization of the Pulse-Width Modulation is discussed in Section B.3. Section B.4 presents the reconfigurable transmitter architecture. The experimental results are reported in Section B.5. At last, Section B.6 presents the conclusion.

B.2 ΣΔ Modulator Design

This Section details the design and improvement stages of a ΣΔ architecture that will be used in order to build a software-defined radio transmitter. The second-order low-pass ΣΔ-modulator used in this paper is a Cascade-of-Integrator with distributed FeedBack (CIFB) type [11], as illustrated in Fig. B.1 by its general representation in the z-domain. The CIFB structure was chosen due to its good stability when used in a low-pass configuration and by its short critical path that allows a higher sampling rate.

The ΣΔ coefficients were precomputed using the ΣΔ-toolbox [8], for a sampling rate of f_s = 250 MHz and with a bandpass of 20 MHz, resulting in an effective oversampling ratio (OSR) of 12.5. These coefficients were then recomputed by a convergence process

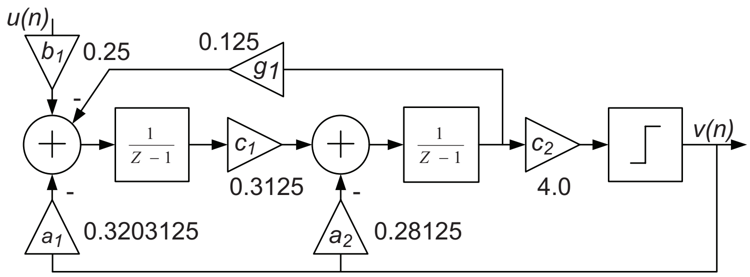

Figure B.1: z-domain representation of the implemented second-order ΣΔ modulator using a 2-level quantizer.

where all coefficients are rounded to powers of two or if not suitable, to a two's-complement binary representation using up to eight bits. This approach contributes to reduce the critical path since powers of two coefficients can be implemented using logical shifts, hence without occupying additional hardware resources.

The spectrum output of the designed ΣΔ-modulator was then analyzed through simulation when using 2-level and 3-level quantizers. The simulation results show that using an extra level on the quantizer allows to increase the Signal-to-Quantization Noise (SQNR) in approx. ≈6 dB.

B.3 Pulse Width Modulator Design

This Section discusses the design and improvement stages of the PWM modulator. In this architecture, the In-phase (I) and Quadrature (Q) components of the baseband signal are quantized, each one using 6 bits. The 5-bit magnitude data is encoded into a 32-bit PWM word, corresponding to 33 different levels of energy (from 32 bits all zeros up to all ones).

This PWM word combined with the signal information will then allow performing the RF up-conversion, see Fig. B.2. However, if a conventional PWM approach is used, for each 5-bit input magnitude there is a specific waveform pattern that corresponds to the desired duty cycle. In this scenario, the RF transmitter will generate harmonics, spaced at the PWM sampling frequency.

On the other hand, if the desired duty cycle is kept but the waveform changes arbitrarily, then it is possible to reduce the generation of harmonics. This way, we extended our

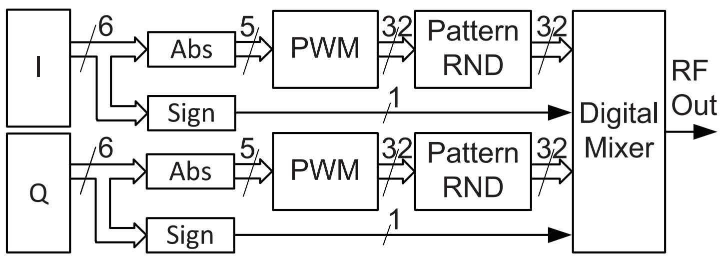

Figure B.2: Block diagram illustrating the architecture of the PWM-based transmitter with pattern randomization.

PWM-based transmitter by adding a pattern randomization block after the PWM waveform generation, see Fig. B.2. This block rotates each sample of the 32-bit PWM word in a pseudo-random manner.

B.4 FPGA-embedded Transmitter Architecture

In this section, we present the multichannel transmitter that will be used to characterize the PWM and ΣΔ modulators used in the scope of RF data transmission.

This transmitter architecture generates RF carriers by serializing a parallel word (W) at a high data rate, see Fig. B.3. The first step to generate W requires each PWM/ΣΔ modulator to be multiplied by the corresponding *RF_LO* signal. The *RF_LO_I* vector is equal to (0,+1,0,-1,0,...) and the *RF_LO_Q* is equal to (-1,0,+1,0...), both having the dimension of the parallel word W. This way, for a single transmission channel, the *Select and Combine* block will simply add the *RF_I* and the *RF_Q* components, resulting in a vector containing the four components of the desired signal ($+v_i$, $+v_q$, $-v_i$, $-v_q$, ...), with the dimension of W. The serialization of this vector at a bitrate of $4 \times f_c$ will generate a single RF carrier centered at f_c.

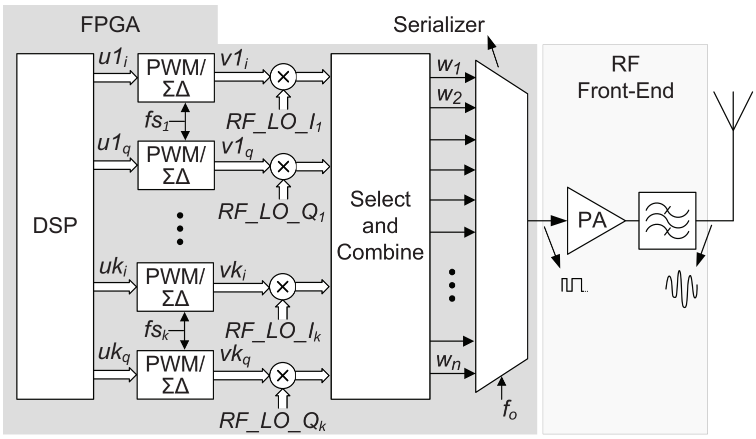

Figure B.3: Block diagram of the multichannel agile transmitter architecture.

In a multichannel transmission scenario, this procedure must be done for each carrier. However, since each channel will have a distinct f_c, applying the above described procedure will result in different output bitrates for each channel. Since this transmitter requires all channels operating at the same rate, the Least Common Multiple (LCM) of all output bitstreams is computed and each preconstructed vector is extended so that its waveform is maintained for the new bitrate given by the LCM. Finally, the multichannel transmission is carried out by time interleaving the vectors of each carrier.

The allowable output frequencies for each carrier are given by: $fc_1 = N_1 \times fs_1$ to $fc_k = N_k \times fs_k$ where N_1 to $N_k \in \mathbb{N}$. Moreover, the sampling frequencies of all PWM/ΣΔ modulators (fs_1 to fs_k) must have an integer relation.

B.5 Experimental Results

The RF transmitter was prototyped in an ML628 development board containing a Virtex6 HX380T FPGA. For the purpose of this proof-of-concept, we implemented the digital datapath shown in Fig. B.3 and connected its digital RF output directly to a Vector Spectrum Analyzer (VSA).

As a first experiment, the RF transmitter architecture was configured to perform the transmission of one carrier centered at 900 MHz and containing a 64-QAM signal. The baseband I and Q signals were stored inside the FPGA's internal memory.

For this implementation example, two ΣΔ modulators using 2-level quantizers were set to operate at a sampling frequency of 225.0 MHz. The *RF_LO* components and the *Select and Combine* block were configured to generate the following 32-bit output word:

$$w_o = [+v_i,\ +v_i,\ +v_q,\ +v_q,\ \text{-}v_i,\ \text{-}v_i,\ +v_q,\ +v_q,\ +v_i,\ +v_i,\ +v_q,\ +v_q,\ \text{-}v_i,\ \text{-}v_i,\ +v_q,\ +v_q,$$
$$+v_i,\ +v_i,\ +v_q,\ +v_q,\ \text{-}v_i,\ \text{-}v_i,\ +v_q,\ +v_q,\ +v_i,\ +v_i,\ +v_q,\ +v_q,\ \text{-}v_i,\ \text{-}v_i,\ +v_q,\ +v_{q,}].$$

Next, the transmitter architecture was reconfigured in order to transmit the same 64-QAM but using ΣΔ modulators with 3-level quantizers. For comparison purposes, the obtained spectrum of both implementations is shown overlapped in Fig. B.4. The obtained results show that using one extra level on the ΣΔ quantizer reduces the quantization noise by about ≈5 dB, which is very close to the ≈6 dB given in the initial simulation.

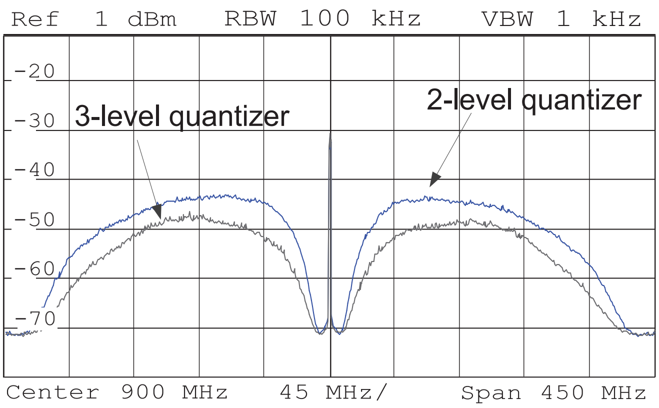

Figure B.4: Overlapped measurement results comparing the use of ΣΔ modulators with 3-level and 2-level quantizers.

Then, for the same input signal and carrier frequency, the FPGA hardware was reconfigured to implement the PWM-based transmitter. For this implementation example, two 5-bit PWM modulators were set to operate at a sampling frequency of 112.5 MHz. Fig. B.5 illustrates the obtained spectrum of the PWM-based transmitter overlapping the results for one implementation with pattern randomization and another without pattern randomization. The obtained results show that using pattern randomization allows reducing the spurious as also it reduces the noise floor, which in turn improves the SNR.

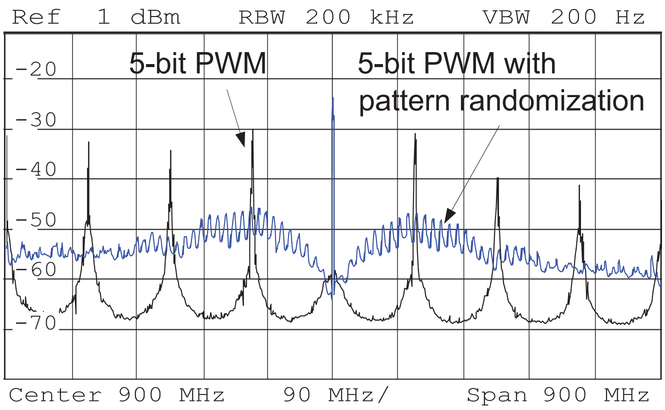

Figure B.5: Overlapped measurement results comparing the PWM-based transmitter with and without pattern randomization.

In Fig. B.6 the spectrum of the ΣΔ-based transmitter using 3-level quantizers and the PWM-based transmitter using pattern randomization are shown overlapped. The obtained results show that the ΣΔ-based transmitter has a higher SNR. However, when comparing Fig. B.4 with Fig. B.5, it can be easily seen that the PWM-based transmitter has less noise closer to the carrier, which alleviates the quality factor requirements of the RF reconstruction filter.

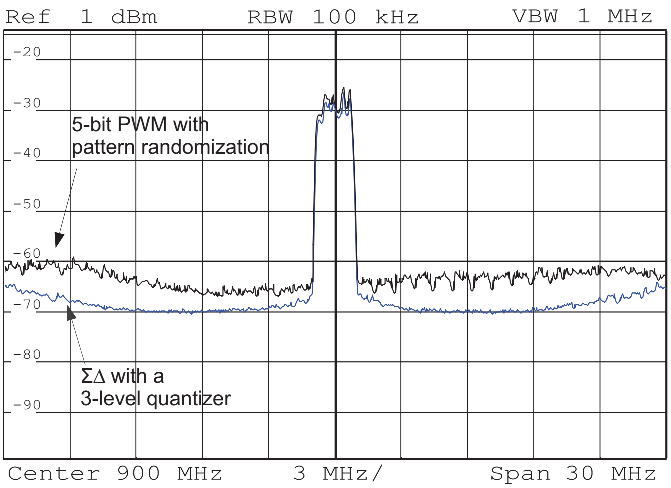

Figure B.6: Overlapped measurement results comparing ΣΔ modulators using 3-level quantizers and PWM with pattern randomization.

Finally, the RF transmitter architecture was reconfigured in order to perform the simultaneous transmission of two different carriers, one centered at 450 MHz, containing a WiMAX signal and the second one centered at 900 MHz, containing a 64-QAM signal. In order to achieve the desired functioning, 4 ΣΔ modulators were set to operate at a sampling rate of 225 MHz. The architecture was configured to generate the following 32-bit output word:

$$w_o = [+v1_i\ +v2_i\ +v1_q\ +v2_i\ \text{-}v1_i\ +v2_q\ \text{-}v1_q\ +v2_q\ +v1_i\ \text{-}v2_i\ +v1_q\ \text{-}v2_i\ \text{-}v1_i\ \text{-}v2_q\ \text{-}v1_q\ \text{-}v2_q$$
$$+v1_i\ +v2_i\ +v1_q\ +v2_i\ \text{-}v1_i\ +v2_q\ \text{-}v1_q\ +v2_q\ +v1_i\ \text{-}v2_i\ +v1_q\ \text{-}v2_i\ \text{-}v1_i\ \text{-}v2_q\ \text{-}v1_q\ \text{-}v2_q].$$

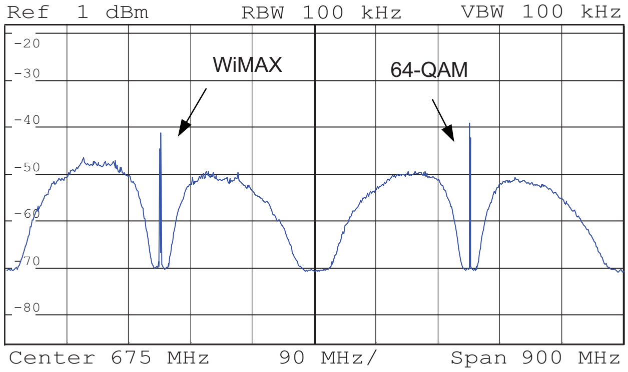

Figure B.7: Measured multichannel spectrum of the ΣΔ-based transmitter.

In Fig. B.7 the spectrum of the multichannel architecture when transmitting a WiMAX signal centered at 450 MHz and a 64-QAM signal centered at 900 MHz is shown.

B.6 Conclusion

A flexible RF multichannel transmitter architecture suitable for using both PWM and ΣΔ modulators was presented in this paper. Due to its high flexibility, it is suitable for multiple applications involving data transmission of current and future wireless standards, and CR. The use of a fast second-order CIFB ΣΔ topology with a 3-level quantizer significantly reduces the quantization noise and provides higher SNR. On the other hand, the PWM-based transmitter using pattern randomization allows a good SNR and reduces the quality factor requirements of the RF reconstruction filter.

Acknowledgment

This work was partially supported by the Portuguese Foundation for Science and Technology (FCT) under project TACCS (ref. PTDC/EEA-TEL/099646/2008) and by the Instituto de Telecomunicações under project DiRecTRadio (ref. LA-LVT-8).

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Paper C

Evaluation of an FPGA-based Reconfigurable SoC for All-Digital Flexible RF Transmitters

Nelson V. Silva, Manuel Ventura, Arnaldo S. R. Oliveira and Nuno Borges Carvalho

in *15th Euromicro Conference on Digital System Design*, Sep. 2012, pp. 890-895.

The format has been revised.

Evaluation of an FPGA-based Reconfigurable SoC for All-Digital Flexible RF Transmitters

Nelson V. Silva, Manuel Ventura, Arnaldo S. R. Oliveira and Nuno Borges Carvalho

Abstract

In this paper an FPGA-based System-on-Chip (SoC) implementation of a flexible digital radio is presented and evaluated. The implemented transmitter is able to perform a direct up-conversion of a baseband signal to RF operating in the gigahertz frequency range as well as it enables the simultaneous transmission of two different carriers, each one having a different modulation, bandwidth, etc. The developed architecture is fully integrated into a single FPGA device and allows software programmability by including an embedded microprocessor for control operations. The high flexibility of this architecture allows to easily change the frequency of the carriers as also the spectral masks, making it interesting in the scope of white spaces exploration and for software radio-based applications.

C.1 Introduction

Over the last years there has been an exponential growth of the communication needs with increasing mobility and autonomy requirements. Moreover, recent changes in the spectrum management policies provide the exploration of white spaces [1] in the RF spectrum (mainly on unused TV bands), thus pushing an additional research effort towards the development of new opportunistic and smart radios [1], capable to adapt to different communication scenarios. In this sense, the well-known Software-Defined Radio (SDR) concept [6] holds the potential for implementing the supreme universal radio, that is, a reconfigurable wireless radio that can change its communication parameters in order to meet the user demands as well as the channel and the network conditions.

However, one of the main challenges for achieving such a new deployment involves the development of a very flexible physical layer in order to support the transmission of multi-band, multi-rate and multi-standard signals, which in practice is very hard to implement using conventional approaches.

On the other hand, the last advances in this field include the development of novel all-digital transmitters where its datapath is digital from the baseband up to the RF stage. Such concept has inherent high flexibility and poses an important step towards the development of SDR transmitters. Moreover, the architecture of this new transmitter can be implemented using Field-Programmable Gate Array (FPGA) devices, which provides additional flexibility as well as field upgradeability and shorter time-to-market.

In fact, current FPGAs have an equivalent logic capacity of millions of logic gates in addition to the large RAM blocks, DSP modules and multigigabit I/O standards. If efficiently explored, these resources can be used to enable the development of agile all-digital transmitters.

Conventional transmitters perform the RF up-conversion stage by multiplying the desired signal by a sinusoidal carrier (e.g. the homodyne transmitter). However, since the FPGA's internal logic typically operates at hundreds of megahertz (e.g. up to 400 or even 500 MHz if good design practices were used), performing the RF up-conversion inside the FPGA using a conventional approach will only allow to generate low RF frequencies (up to dozens or a few hundreds of megahertz), and therefore resulting in a very limited RF transmitter.

On the other hand, all-digital transmitter architectures usually include a first stage where the input information is typically converted into a 2-level representation using either $\Sigma\Delta$ modulation or Pulse Width Modulation (PWM). This data conversion to 1-bit eases the RF up-conversion stage and if conveniently explored allow the use of a single FPGA-embedded multigigabit (MGT) serializer to output the desired RF signal. This way, given the very high speed of current MGT serializers (e.g. up to 28 Gbps in Altera and Xilinx high-end FPGAs), it becomes possible to have a digital RF output signal centered in the GHz frequency range as well as it allows integrating the entire design into a single FPGA.

In this paper we explore the potential allowed by current FPGA technology by presenting and evaluating an FPGA-based SoC all-digital transmitter architecture that is able to simultaneously transmit two independent carriers (i.e. multichannel transmission) and where the RF output operating in the gigahertz frequency range is generated inside a single FPGA device.

The remainder of this paper is organized as follows. Section C.2 presents the related work. Section C.3 introduces the all-digital transmitter architectures. Section C.4 details the architecture of the reconfigurable transmitter. The experimental results are reported in Section C.5 and the conclusion is presented in Section C.6.

C.2 Related Work

In [2] the authors present a digital transmitter where data is shaped using Pulse Width Modulation (PWM) and up-converted to RF using a digital mixer. In [3, 5] the authors present a new transmitter approach using Low-Pass (LP) $\Sigma\Delta$ modulators and digital multiplexers to design an all-digital multimode RF transmitter. In this approach, $\Sigma\Delta$ modulation is used to shape signals centered at baseband, which significantly alleviates the processing speed requirements, and therefore simplifies the design of $\Sigma\Delta$-based transmitters for operation in the gigahertz frequency range. In [4] the authors present a low-pass $\Sigma\Delta$-based transmitter front-end also using external multiplexers for implementing the digital up-conversion to RF.

A SDR transceiver including IF up-conversion, a band-pass $\Sigma\Delta$ modulator and RF up-conversion is presented in [7]. In [8] it is presented an all-digital transmitter with multiple stop-bands in the $\Sigma\Delta$ Noise Transfer Function (NTF) in order to create a concurrent dual-band transmitter.

However, current state-of-the-art digital transmitter architectures are still restrictive for developing a truly SDR-based system as well as for white spaces exploration. In fact, almost all the above presented transmitters require very high-quality filters to remove out-of-band noise, others only generate low RF frequencies [2, 10], many require expensive external multiplexers for implementing the RF up-conversion [3, 5, 4] or have carriers with low Signal-to-Noise Ratio (SNR) [4].

In this paper we addresses some of these limitations and extend previous work [11, 12], by presenting and evaluating an FPGA-based multichannel multistandard all-digital transmitter architecture that reduces the need of using high quality filters and where the RF output carriers operating in the gigahertz frequency range are generated inside a single FPGA device. Moreover, the high flexibility of this reconfigurable transmitter makes possible to easily modify important parameters such as the carriers' frequencies, the usable bandwidth and the dynamic range.

C.3 All-Digital Transmitters Basics

The underlying concepts of all-digital transmitters are presented in this section. As previously stated, the datapath of these transmitters is entirely digital up to the RF stage, which provides high flexibility, specially if implemented using reconfigurable hardware, and poses an important step towards the development of SDR transmitters.

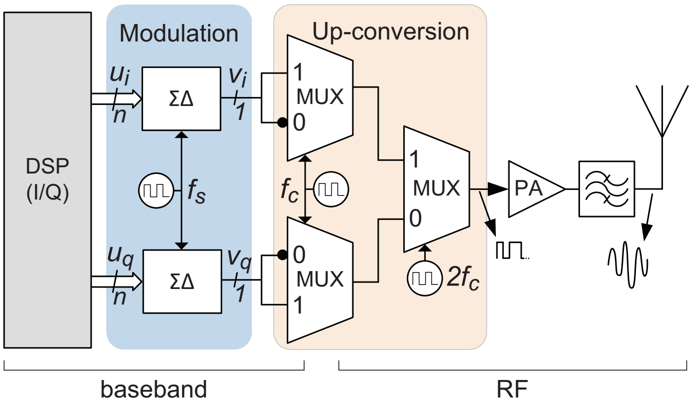

Figure C.1: Architecture of an all-digital transmitter.

The ΣΔ-based transmitter illustrated in Fig. C.1 receives the baseband in-phase (u_i) and quadrature (u_q) components of the desired signal to be transmitted. These components are then shaped using ΣΔ modulation in order to make them suitable for the RF up-conversion process. In the ΣΔ modulation stage the signal information is preserved but out-of-band noise is added as a consequence of converting a n-bit signal representation into a 1-bit output signal, see Fig. C.2.

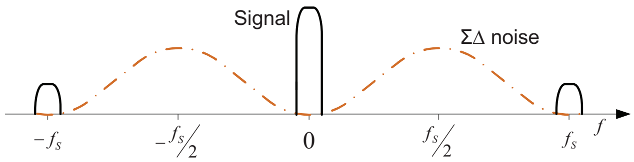

Figure C.2: Frequency response of a low-pass ΣΔ modulator illustrating the signal (solid line) and the ΣΔ noise shaping (dot-dashed).

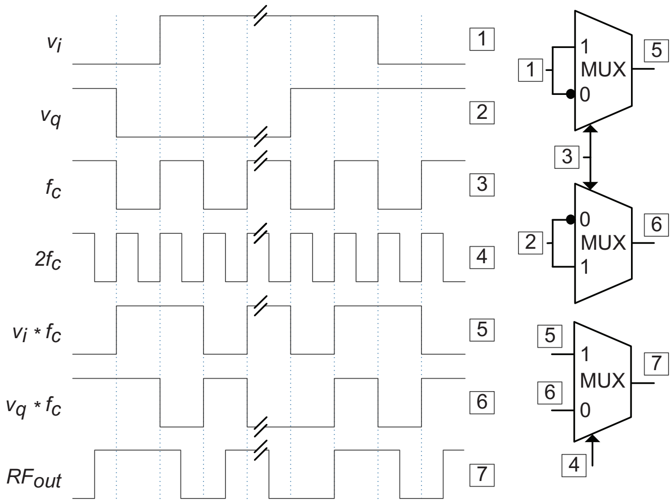

Figure C.3: Timing diagram illustrating the RF up-conversion process.

After the ΣΔ modulation stage, a set of three digital multiplexers are used to modulate the 1-bit baseband signals by a square wave carrier. Similarly to a conventional homodyne transmitter, this approach shifts a baseband signal directly to RF, that is, without passing through an Intermediate Frequency (IF) stage. However, since a square wave is used, odd harmonics of the carrier frequency will also be generated.

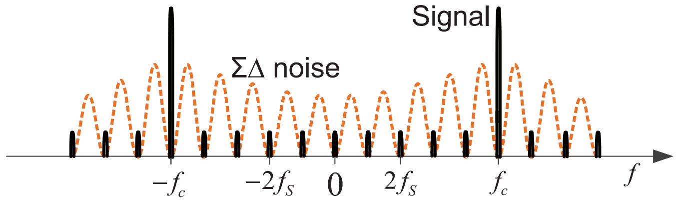

Figure C.4: Signal (solid line) and noise shaping (dashed) of a low-pass ΣΔ modulator after RF up-conversion to f_c.

In this architecture, the leftmost multiplexers shown in Fig. C.1 center the signals at the carrier frequency while the third multiplexer enables the transmission of both components by time interleaving them with a 90 degree phase shift. The timing diagram detailing the RF up-conversion process is illustrated in Fig. C.3 and the RF spectrum of the ΣΔ-based transmitter after the digital up-conversion is shown in Fig. C.4.

C.4 FPGA-embedded RF Transmitter Architecture

In this section, we present an FPGA-based System-on-Chip (SoC) architecture containing a multichannel all-digital transmitter operating in the gigahertz frequency range.

This architecture enables the simultaneous transmission of two different RF carriers, each one having a different standard, frequency, modulation and spectral mask in an FPGA-integrated solution where the digital up-conversion to the gigahertz frequency uses a single MGT transceiver.

C.4.1 ΣΔ Modulator Design

The second-order low-pass ΣΔ-modulator used in this paper is a Cascade-of-Integrator with distributed FeedBack (CIFB) type [11], as illustrated in Fig. C.5 by its general representation in the z-domain. The CIFB structure was chosen due to its good stability when used

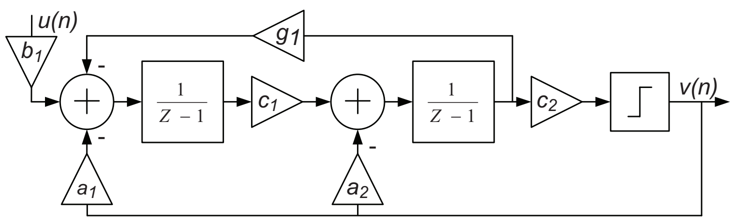

Figure C.5: Structure of the implemented second-order CIFB ΣΔ modulator.

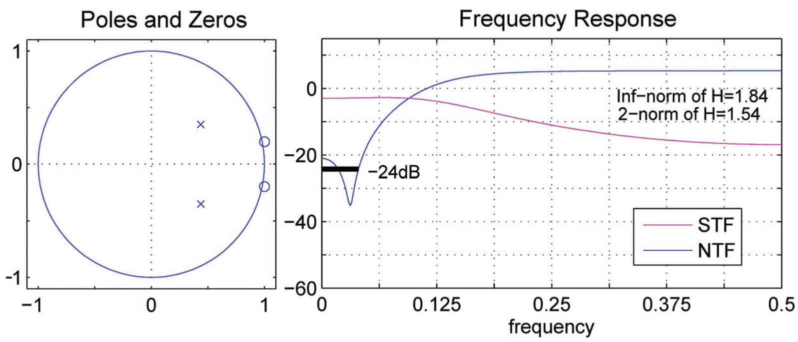

Figure C.6: Zero-pole z-plane and frequency response of the designed second-order CIFB ΣΔ modulator.

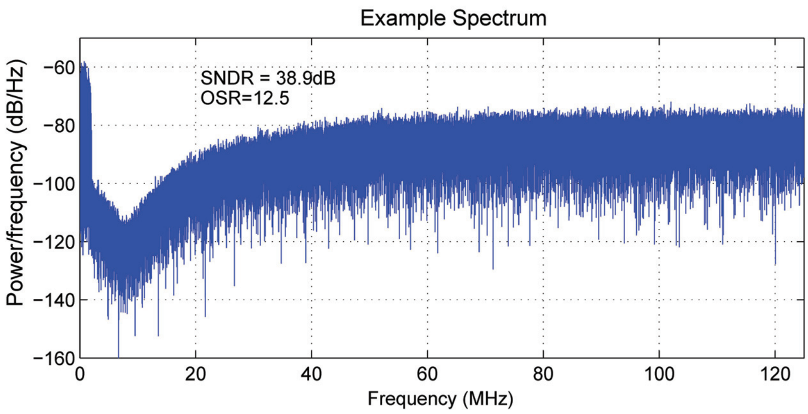

Figure C.7: Example spectrum of a ΣΔ modulator output for a 3.5 MHz baseband input signal.

in a low-pass configuration and because its short critical path allows a higher sampling rate. This is of critical importance since higher sampling rates allow to move away the quantization noise from the desired signal which permits in one hand having wider band signals and in another hand reducing the quality factor of the reconstruction filter.

The ΣΔ coefficients were precomputed using the ΣΔ-toolbox [8], for a sampling rate of $f_s = 250$ MHz and with a bandpass of 20 MHz, resulting in an effective oversampling ratio (OSR) of 12.5. Moreover, in order to guarantee stability, the Lee-criteria was set to $\|\mathrm{NTF}(\omega)\|_\infty < 2$.

These coefficients were then recomputed using a convergence process where all coefficients are rounded to powers of two or if not suitable to a two's-complement binary representation using up to eight bits. This way, the critical path can be further reduced since powers of two coefficients can be implemented using logical shifts.

The resulting type-2 Chebyshev highpass Noise-Transfer Function (NTF) was then calculated to be:

$$\mathrm{NTF}(z) = \frac{z^2 - 2z + 1.039}{z^2 - 0.875z + 0.315}. \tag{C.1}$$

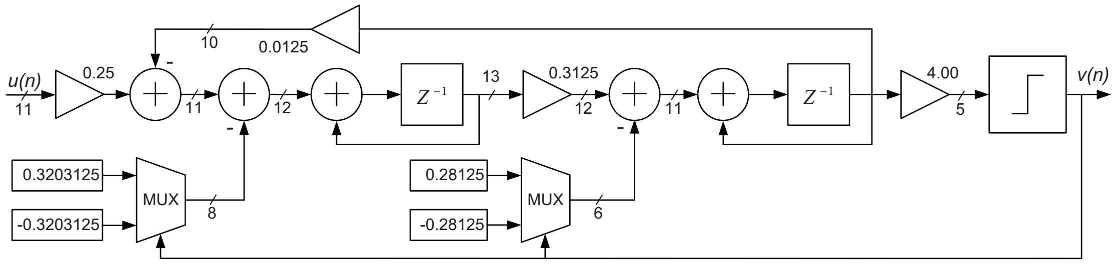

Figure C.8: z-domain representation of the implemented CIFB second-order ΣΔ modulator.

The corresponding zero-pole z-plane and the frequency response of the designed ΣΔ modulator are shown in Fig. C.6. As illustrated in Fig. C.7, the simulated dynamic range is ≈ 40 dBc within the 20 MHz RF bandpass when used with a 3.5 MHz bandlimited signal with 5.4 dB Peak-to-Average Power Ratio (PAPR).

Concerning the ΣΔ datapath implementation, the chosen topology and the optimized coefficients combined with specific design goals and strategies made possible to implement the ΣΔ-modulator at frequencies exceeding the 250 MHz in the current FPGA logic fabric. The implemented ΣΔ modulator illustrating the full datapath and the chosen coefficients is detailed in Fig. C.8.

C.4.2 Digital Up-Conversion

A block diagram of the implemented multichannel transmitter architecture is shown in Fig. C.9. In this architecture, the main blocks for implementing the digital up-conversion stage are the interconnection network and a MGT serializer. The interconnection network block combines the outputs of the ΣΔ modulators (v_i and v_q) with its inverted versions ($\bar{v}_i$ and $\bar{v}_q$), in order to generate the parallel output word (w).

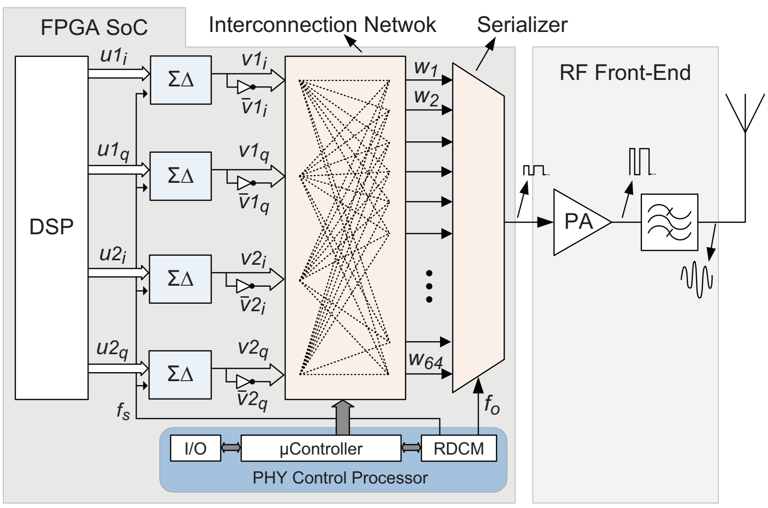

Figure C.9: Block diagram detailing the implemented FPGA SoC transmitter.

The first step to generate w in a single channel scenario consists of constructing a vector containing the four components of the desired signal ($v_i v_q \bar{v}_i \bar{v}_q$), and then replicating it by the digital up-conversion factor N, given by f_c/f_s. The serialization of this vector at a bitrate of $4 \times f_c$ will generate a digital RF carrier centered at f_c.

In a multichannel transmission scenario this procedure must be done for each carrier. Nevertheless, since a distinct f_c is desired for each channel, applying the above described procedure will result in a different output bitrate for each channel. Since the multichannel transmission followed in this approach requires all channels operating at the same rate, the Least Common Multiple (LCM) of all output bitstreams is computed and each pre-constructed vector is extended so that its waveform is maintained for the new bitrate given by the LCM. At last, the multichannel transmission is carried out by time interleaving the vectors of each carrier. The allowable output frequencies for each carrier are given by: $fc_1 = N_1 \times fs$ and $fc_2 = N_2 \times fs$ where N_1 and $N_2 \in \mathbb{N}$. Further details regarding the interconnection network can be found in [11].

Finally, the FPGA-embedded serializer must produce an output bitrate that is eight times the LCM of the desired carrier frequencies in order to ensure the proper functioning. Since the used serializer operates in both clock edges, it should be clocked at a frequency f_o that is half the output bitrate.

After the up-conversion stage, it is enough having an RF front-end containing a switching-mode Power Amplifier (PA) and a reconstruction filter for producing an RF signal that is suitable to be transmitted by the antenna.

C.4.3 PHY Control Processor

The PHY control processor block includes a microcontroller with a Reduced Instruction Set Computer (RISC) architecture for software programmability with low hardware overhead, interconnected to a dynamically Reconfigurable Digital Clock Manager (RDCM) and to Input/Output interfaces for enabling communication with external devices. This way, it is possible through software to change the interconnection network in order to select the desired input signals and up-conversion factors, as well as to configure the RDCM in order to generate the proper clock signals for obtaining the desired RF output.

Regarding the software programming model, the interconnection network and the RDCM have memory mapped registers. This way, by modifying those registers it is possible to alternate between different configurations of the interconnection network as well as to tell the RDCM to synthesize new frequencies for the ΣΔ-modulators and for the MGT serializer.

C.5 Experimental Results

This section firstly presents the experimental results regarding single channel data transmission and then the measured results regarding multichannel data transmission are also shown.

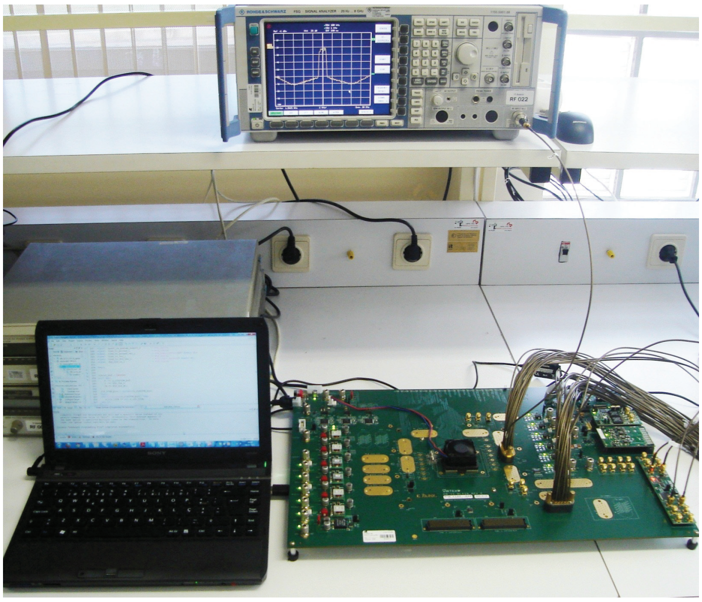

Figure C.10: Setup of the evaluated FPGA-based all-digital transmitter.

The FPGA-SoC depicted in Fig. C.9 was prototyped in an ML628 development board containing a Virtex-6 HX380T FPGA. The measured results were obtained using a Vector Spectrum Analyzer (VSA), model Rohde & Schwarz FSQ8, directly connected to the development board, see Fig. C.10. All baseband signals used for evaluating this transmitter were stored inside the FPGA's internal memory.

C.5.1 Single Channel Data Transmission

In the first implementation experiment the RF transmitter architecture was configured to transmit a 64-QAM signal centered at 3.125 GHz, see Fig. C.11. For this implementation example, the up-conversion factor was set to $N = 16$. This way the $\Sigma\Delta$ modulators were configured to operate at a clock frequency of 195.3125 MHz. The pattern building block was configured to generate the following 64-bit output word:

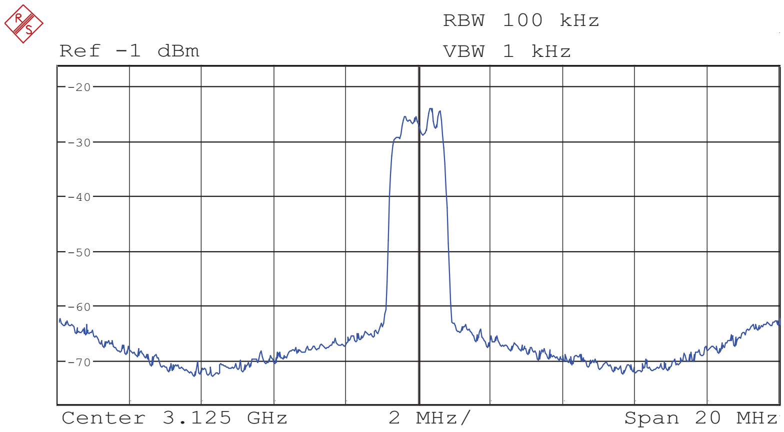

Figure C.11: Output spectrum of the transmitter architecture when sending a 64-QAM signal.

$$w = [v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q\ v1_i\ v1_q\ \bar{v1}_i\ \bar{v1}_q],$$

where $v1_i$ and $v1_q$ are the in-phase and the quadrature components of the 64-QAM baseband signal after the $\Sigma\Delta$ modulation stage and $\bar{v1}_i$ and $\bar{v1}_q$ are its inverted versions.

The serializer was configured in order to produce an output bitstream of 12.5 Gbps. This output signal was then connected to a VSA for spectral and vector analysis. As can be seen in Fig. C.11, the high operating frequency of the $\Sigma\Delta$ modulators allow a Signal-to-Noise and Distortion Ratio (SNDR) of ≈35 dB and a usable bandwidth of ≈15 MHz.

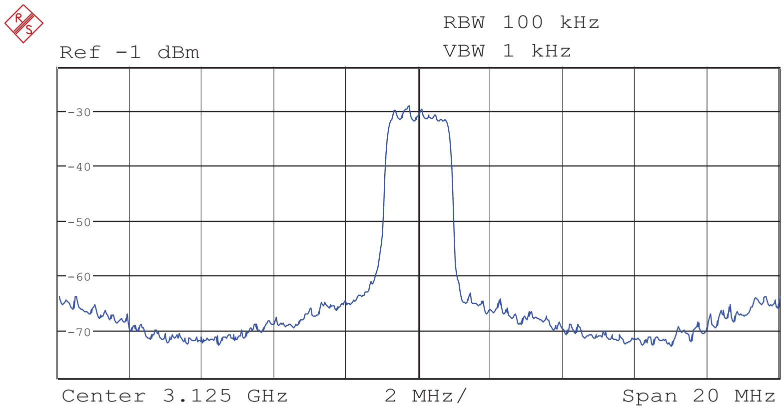

Figure C.12: Output spectrum of the transmitter architecture when sending a WiMAX signal.

Next, the FPGA-SoC transmitter architecture was configured in order to transmit the OFDM modulation of a WiMAX baseband signal centered at the same 3.125 GHz. For this new configuration, it is enough to change the interconnection network for generating the following word:

$$w = [v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q\ v2_i\ v2_q\ \bar{v2}_i\ \bar{v2}_q].$$

The RF spectrum of the FPGA-based transmitter containing a WiMAX signal is illustrated in Fig. C.12. The usable bandwidth of ≈15 MHz is equal to the first implementation since the $\Sigma\Delta$ modulators are operating at the same frequency and have the same coefficients. On the other hand, the used samples containing the WiMAX baseband signal have lower energy than the 64-QAM signal, which explains the lower SNDR of ≈32 dB.

C.5.2 Multichannel Data Transmission

The architecture was now configured to implement the simultaneous transmission of two different carriers, one centered at 1.5625 GHz containing a 64-QAM signal and the second one centered at 781.25 MHz and containing a WiMAX signal. All $\Sigma\Delta$ modulators were configured to operate at 195.3125 MHz. The interconnection network was configured to generate the following 64-bit output word:

$w_o = [v1_i\ v2_i\ v1_q\ v2_i\ \bar{v}1_i\ v2_q\ \bar{v}1_q\ v2_q\ v1_i\ \bar{v}2_i\ v1_q\ \bar{v}2_i\ \bar{v}1_i\ \bar{v}2_q\ \bar{v}1_q\ \bar{v}2_q\ v1_i\ v2_i\ v1_q\ v2_i\ \bar{v}1_i\ v2_q\ \bar{v}1_q$ $v2_q\ v1_i\ \bar{v}2_i\ v1_q\ \bar{v}2_i\ \bar{v}1_i\ \bar{v}2_q\ \bar{v}1_q\ \bar{v}2_q.\ v1_i\ v2_i\ v1_q\ v2_i\ \bar{v}1_i\ v2_q\ \bar{v}1_q\ v2_q\ v1_i\ \bar{v}2_i\ v1_q\ \bar{v}2_i\ \bar{v}1_i\ \bar{v}2_q\ \bar{v}1_q\ \bar{v}2_q$ $v1_i\ v2_i\ v1_q\ v2_i\ \bar{v}1_i\ v2_q\ \bar{v}1_q\ v2_q\ v1_i\ \bar{v}2_i\ v1_q\ \bar{v}2_i\ \bar{v}1_i\ \bar{v}2_q\ \bar{v}1_q\ \bar{v}2_q]$.

Again, the MGT serializer was set to produce an output bitstream of 12.5 Gbps. The obtained spectrum of the multichannel architecture when simultaneously transmitting a WiMAX signal centered at 781.25 MHz and a 64-QAM signal centered at 1.5625 GHz is shown in Fig. C.13. A closer view of the 64-QAM signal can be found in Fig. C.14.

As can be seen, the usable bandwidth of ≈15 MHz is kept in this multichannel transmission scenario.

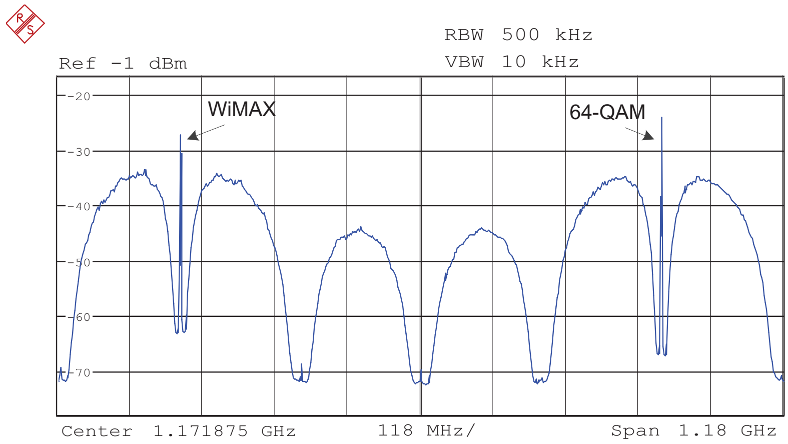

Figure C.13: Measured multichannel spectrum of the proposed transmitter.

The modulation accuracy measurements for a 64-QAM signal centered at 1.5625 GHz when the architecture is configured for a) multichannel data transmission and b) single channel data transmission are shown in Table C.1. The obtained results show a 2.3 dB loss in terms of Modulation Error Ratio (MER) for the multichannel approach. This small degradation is due to the higher in-band noise resulting from overlapping the desired signal within a

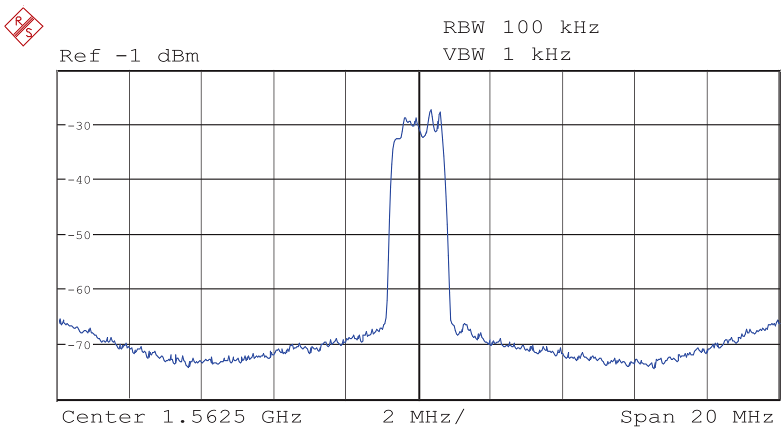

Figure C.14: Measured spectrum of a 64-QAM signal when transmitting in a multichannel configuration.

Table C.1: Modulation accuracy measurements of a 64-QAM signal centered at 1.5625 GHz.

	Result for a multichannel data transmission	Result for a single channel data transmission	Unit
EVM	1,8	1,4	%
Magnitude Error	0,8	0,6	%
Phase Error	1,0	0,7	deg
SNR (MER)	34,7	37,0	dB

low noise region of the other channel. Nevertheless, the Error Vector Module (EVM) is lower than 2% in both cases, which is more than sufficient for enabling a well-defined constellation, as can be seen in Fig. C.15.

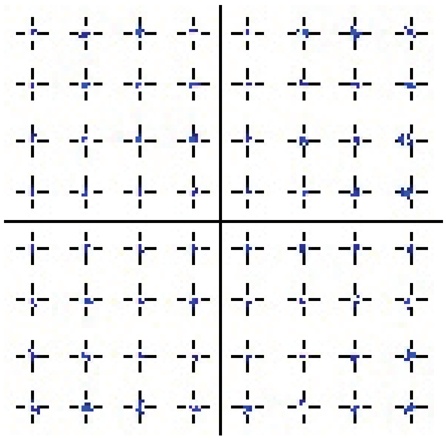

Figure C.15: Constellation of a 64-QAM signal centered 1.5625 GHz.

The maximum operating frequency of this agile RF transmitter is 233.0 MHz for the FPGA internal logic. This frequency is limited by a critical path between the first to the second delay in the $\Sigma\Delta$ modulator datapath shown in Fig. C.8

Regarding the occupied resources, the entire datapath takes only about 1% of the FPGA fabric, see Table C.2, providing a large area available for other system functionalities, as well as a vast grade of integration including, for instance, processing of baseband protocols and higher protocol layers such as the Medium Access Control (MAC).

Table C.2: Main occupied resources of the implemented FPGA-based all-digital transmitter.

Logic resources	Without the PHY control processor	With the PHY control processor	Available
Flip-Flops	291	2516	478080
LUTs	496	3136	239040
RAM36E1	14	15	768
GTHE1_QUADs	1	1	6

C.6 Conclusion

In this paper, an FPGA SoC architecture containing a multichannel RF transmitter is presented and evaluated. The use of a second-order $\Sigma\Delta$ modulator with a CIFB topology permits a high operating frequency which consequently enables a higher usable bandwidth and relaxes the quality factor requirements of the RF output filter.

Moreover, the combined use of reconfigurable hardware with a new radio architecture resulted in a very flexible transmitter, capable of concurrent transmission of multi-band, multi-rate and multi-standard signals, making it interesting in the scope of white spaces exploration and for software radio-based applications.

Acknowledgment

This work was supported in part by the Portuguese Foundation for Science and Technology under PhD scholarship ref. SFRH/BD/76807/2011, under project TACCS ref. PTDC/EEA-TEL/099646/2008 and by the Instituto de Telecomunicações under project DiRecTRadio ref. LA-LVT-8.

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Paper D

Design and Optimization of Flexible and Coding Efficient All-Digital RF Transmitters

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in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 1, pp. 625-632, 2013.

The format has been revised.

Design and Optimization of Flexible and Coding Efficient All-Digital RF Transmitters

Nelson V. Silva, Arnaldo S. R. Oliveira and Nuno Borges Carvalho

Abstract

All-digital transmitters are getting increased attention due to its closer proximity to the ideal Software-Defined Radio (SDR) transmitter. In this paper we propose a new transmitter architecture that addresses two key limitations of current approaches, namely the poor coding efficiency and the high quality factor requirements of the RF output reconstruction filter that significantly limit the practical usability and dissemination of these new flexible RF transmitters.

The proposed architecture combines a maximum coding efficiency of 79.3% and a Signal-to-Noise Ratio (SNR) of 50 dB, while maintaining the high flexibility inherent to the all-digital transmitters and where the RF output carriers operating in the microwave frequency range are generated inside a single Field-Programmable Gate Array (FPGA) device. The obtained results also show the feasibility and potential of using FPGA-based architectures for implementing digital RF transmitters.

D.1 Introduction

The unprecedented attention given to wireless communications over the last years led to the proliferation of dissimilar wireless standards operating at different frequencies, using dissimilar coding and modulation schemes, and targeted for different ends. Such vast proliferation pushes an additional research effort towards the development of new smart radios [1], capable of adapting to different communication scenarios. In this new wireless communication paradigm, the well-known Software-Defined Radio (SDR) concept [6] holds the potential for implementing the supreme universal radio, that is, a fully reconfigurable radio that can adapt its own communication parameters in order to meet the user demands as well as the channel and the network conditions.

However, a key challenge for achieving such a new communications paradigm involves the development of a very flexible physical layer in order to support the transmission of multi-band, multi-rate and multi-standard signals, which in practice is very hard to implement using conventional approaches.

Nevertheless, the last advances in this field include the development of novel all-digital transmitters where its datapath is digital from the baseband up to the RF stage. Such a concept has inherent high flexibility and poses an important step towards the development of SDR transmitters. Moreover, this new approach enables the use of Field-Programmable Gate Array (FPGA) devices for implementing the RF transmitter, which provides additional flexibility as well as field upgradeability.

In fact, current FPGAs have an equivalent logic capacity of millions of logic gates in addition to large RAM blocks, embedded processors, DSP modules and multigigabit I/O standards. If efficiently explored, these valuable resources can be used to enable the development of agile all-digital transmitters.

In [2] the authors present an FPGA-based digital transmitter where data is shaped using Pulse Width Modulation (PWM) and up-converted to 800 MHz using a digital mixer. In [3] and [5] the authors present a new transmitter approach using Low-Pass (LP) $\Sigma\Delta$ modulators and digital multiplexers to design an all-digital multimode RF transmitter. In this approach the $\Sigma\Delta$ modulators shape baseband signals, which significantly alleviates the processing speed requirements, and therefore simplifies the design of $\Sigma\Delta$-based transmitters for operation in the microwave frequency range. In [4] the authors present a low-pass $\Sigma\Delta$-based transmitter front-end also using external multiplexers for implementing the digital up-conversion to RF.

A SDR transceiver including IF up-conversion, a band-pass $\Sigma\Delta$ modulator and RF up-conversion is presented in [7]. In [8] an all-digital transmitter with multiple stop-bands in the $\Sigma\Delta$ Noise Transfer Function (NTF) is presented in order to create a concurrent dual-band transmitter.

However, current state-of-the-art digital transmitter architectures are still very restrictive for developing a truly SDR-based system. In fact, almost all the above presented transmitters require very high-quality filters to remove out-of-band noise, others only generate low RF

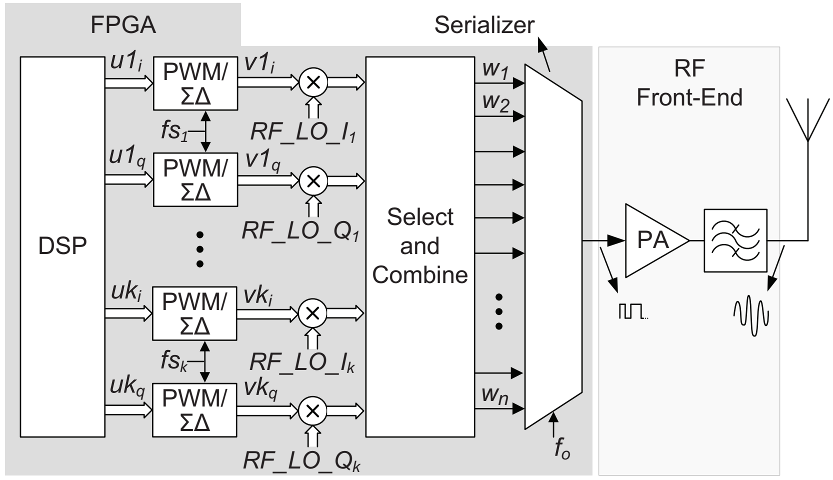

Figure D.1: Block diagram of a multichannel agile transmitter architecture.

frequencies [2], many require expensive external multiplexers for implementing the RF up-conversion [3, 5, 4] or have carriers with low SNR [4] and all have very limited support for multichannel operation.

In [1] a ΣΔ-based all-digital transmitter architecture was presented that is able to simultaneously transmit multiple independent carriers and where the RF output operating in the microwave frequency range is generated inside a single FPGA device. In [10] an agile RF transmitter containing different pulse modulators was prototyped in order to analyze the specific tradeoffs of each modulator, which in turn allowed to improve the carrier dynamic range as well as to reduce the filtering requirements of the RF reconstruction filter; see Fig. D.1.

In this paper we address two key limitations of current approaches, namely the poor coding efficiency and the combined high quality factor and tunability requirements of the RF output filter that significantly limit the practical usability and dissemination of these new flexible RF transmitters. This paper also extends previous work [1, 10] by presenting and evaluating a novel FPGA-embedded agile transmitter based on pulse modulators. This new architecture significantly improves important figures of merit, such as coding efficiency and Error Vector Magnitude (EVM), while maintaining support for multichannel multistandard data transmission and where the RF output carriers operating in the microwave frequency range are still generated inside a single FPGA device. Moreover, the high flexibility of this reconfigurable transmitter makes it possible to easily modify important parameters, such as the carriers' frequencies, usable bandwidth and dynamic range.

The remainder of this paper is organized as follows. The ΣΔ and the PWM design are detailed in Section D.2 and Section D.3, respectively. The proposed RF transmitter architecture integrating several key improvements is presented in Section D.4. The experimental results are reported in Section D.5. At last, Section D.6 presents the conclusion.

D.2 ΣΔ Modulator Design

This Section details the architecture of a second-order low-pass ΣΔ modulator that will be used to build a flexible digital radio transmitter. The ΣΔ modulator used in this paper is a Cascade-of-Integrator with distributed FeedBack (CIFB) type [11] using a 3-level quantizer, as illustrated in Fig. D.2 by its general representation in the z-domain. The CIFB structure was chosen due to its good stability when used in a low-pass configuration and also by its short critical path that allows a higher sampling rate. Regarding the chosen 3-level quantizer, it was shown in [10] that by using one extra level in addition to the conventional bi-level quantizer it is possible to increase the Signal-to-Quantization Noise (SQNR) in approx. 5 dB.

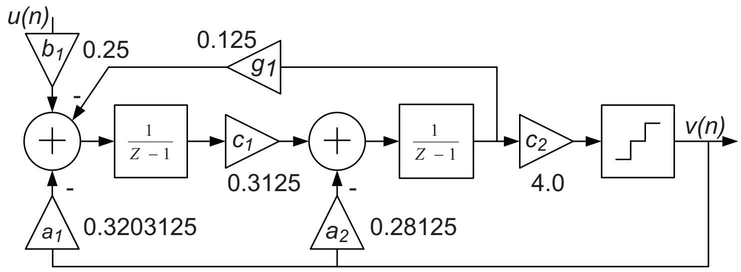

Figure D.2: z-domain representation of the implemented CIFB second-order ΣΔ modulator using a 3-level quantizer.

The ΣΔ coefficients were precomputed using the ΣΔ-toolbox [8], for a sampling rate of $f_s = 250$ MHz and a bandpass of 20 MHz, resulting in an effective oversampling ratio (OSR) of 12.5. These coefficients were then recomputed by a convergence process where all coefficients are rounded to powers of two or if not suitable, to a two's-complement binary representation using up to eight bits. This approach contributes in reducing the critical path since powers of two coefficients can be implemented using logical shifts, hence without occupying additional hardware resources. The resulting type-2 Chebyshev highpass NTF can be given by:

$$\mathrm{NTF}(z) = \frac{z^2 - 2z + 1.039}{z^2 - 0.875z + 0.3145}. \tag{D.1}$$

D.3 Pulse Width Modulator Design

This Section details the design of the PWM-based transmitter. In this architecture, each In-phase (I) and Quadrature (Q) components of the baseband signal are quantized using 8 bits. The 7-bit magnitude data is encoded into a 128-bit PWM word, corresponding to 129 different levels of energy (from 128 bits all zeros up to all ones). This PWM word combined with the signal information will then allow performing the RF up-conversion, see Fig. D.3. However, if a conventional PWM approach is used, such as when using thermometer coding, for each 7-bit input magnitude there is a specific waveform pattern that corresponds to the desired duty cycle. In this scenario, the RF transmitter will generate harmonics spaced at the PWM sampling frequency. On the other hand, if the desired duty cycle is kept but the

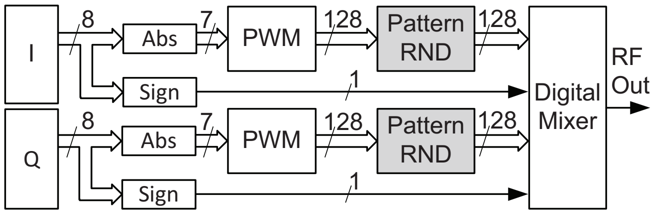

Figure D.3: Block diagram illustrating the architecture of the PWM-based transmitter with pattern randomization.

waveform changes arbitrarily, then it is possible to spread the energy of these harmonics over the RF spectrum, which in turn enables reducing the RF output filtering requirements. This way, the base architecture of the transmitter was extended by adding a pattern randomization block after the PWM waveform generation, see Fig. D.3. This block performs several rotations for each sample of the 128-bit PWM word in a pseudo-random manner; see Fig. D.4.

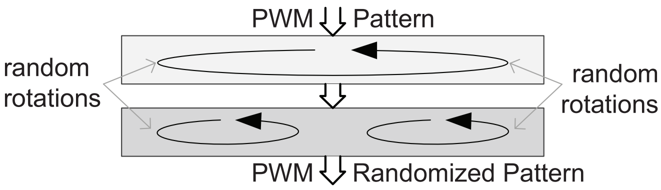

Figure D.4: Block diagram illustrating the PWM pattern randomization process.

Regarding the chosen PWM word length, experimental results show that by increasing from 6 to 8 the number of quantization bits of the baseband signal, that is by using a 128-bit PWM word instead of a 32-bit word, it is possible to increase the dynamic range of the carrier in approximately 3 dB.

D.4 Proposed All-Digital Transmitter

In this section we present a new multichannel transmitter architecture that significantly improves the coding efficiency and also reduces the RF filtering requirements while maintaining the flexibility of conventional all-digital transmitters.

A key idea for improving the coding efficiency of this transmitter without sacrificing the flexibility consisted in reducing the overall noise by using polyphase multipath circuits, such as illustrated in [13] and [14].

The base idea of noise reduction through polyphase circuits relies on having multiple paths where the phase of the desired signal is kept constant but where the unwanted noise

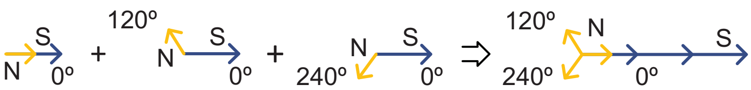

Figure D.5: Illustration of the noise canceling idea when using polyphase noise.

has different canceling phases; see Fig. D.5. This way, when the output signals of the multipath circuits are combined, the energy of the desired signal will grow proportionally to the number of multipath circuits while ideally the noise will cancel, and therefore it will directly improve the overall coding efficiency of the transmitter. The high level block diagram of the proposed polyphase multipath agile transmitter is shown in Fig. D.6 where the multichannel operation and a higher number of phases are omitted for the sake of simplicity.

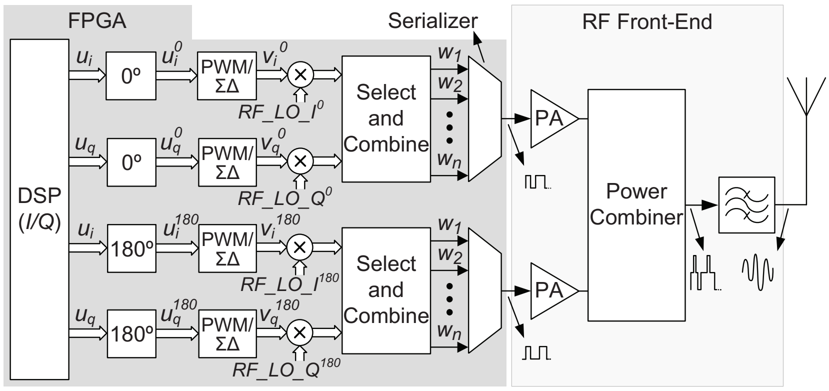

Figure D.6: Single channel illustration of the proposed polyphase multipath agile transmitter architecture.

The proposed transmitter shown in Fig. D.6 is constituted by two independent paths, one containing noise at 0º and another one where the noise was shifted to 180º. Each independent path applies a specific phase shift to the baseband I and Q components (u_i, u_q). These phase shifted signals are then shaped using PWM or ΣΔ modulation in order to make them suitable for the RF up-conversion process. The first step to generate w requires each PWM/ΣΔ modulator to be multiplied by the corresponding *RF_LO* signal. However, each *RF_LO* vector has a specific phase for each independent path. This way, the mixing process also performs a phase shift to the entire signal (both the desired information and the unwanted noise). For the 0º datapath, the $RF\_LO\_I^0$ and $RF\_LO\_Q^0$ vectors should produce a -0º phase shift. In the proposed architecture, these vectors are equal to (+1,0,-1,0,+1,...) and (0,+1,0,-1,0,...), respectively. The *Select and Combine* block will simply add the *RF_I* and the *RF_Q* components, resulting in a vector containing the four components of the desired signal ($+v_i$, $+v_q$, $-v_i$, $-v_q$, ...), with the dimension of w. The serialization of this vector at a bitrate of $4 \times f_c$ will generate a single RF carrier centered at f_c. The allowable output carrier frequency is given by:

$$fc = N \times fs \ , N \in \mathbb{N}. \tag{D.2}$$

For the 180º datapath, the $RF\_LO\_I^{180}$ and $RF\_LO\_Q^{180}$ vectors should produce a -180º phase shift. In the proposed architecture, these vectors are equal to (-1,0,+1,0,-1,...) and (0,-1,0,+1,0,...), respectively. Similarly to the 0º datapath, the serialization of the resulting vector at a bitrate of $4 \times f_c$ will generate a single RF carrier centered at f_c.

After the RF up-conversion stage, the desired signal of all independent paths is now phase aligned while the noise has different canceling phases. This way, it is now possible to combine the energy of all RF paths using a power combiner, and consequently improve the dynamic range of the signal.

D.4.1 ΣΔ-based RF Transmitter

This Subsection details the design stage of the ΣΔ-based agile and coding efficient all-digital transmitter. This transmitter extends the proposed architecture shown in Fig. D.6 by using 90º and 270º phases in addition to the 0º and 180º; see Fig. D.7. This way it is possible to further improve the SNR of the desired signal.

The designed transmitter uses the same baseband information (I and Q) for each specific path. As a good design trade-off between SNR and the ΣΔ operating speed, each baseband component is quantified using 10 bits. This information is then shifted to the proper phase and then shaped to a 3-level representation using ΣΔ modulation. Then, each specific path will perform the Digital Up-Conversion (DUC) using a proper phase so that all paths have the desired signal shifted to the same phase. The LUT block will convert the 3-level two's complement signal into a 2-bit word where the integers *-2*, *0* and *2* are converted into *00*, *01* and *11*, respectively.

The *Select and Split* block will then send to one serializer a vector containing only the Most Significant bit (MSb) while another vector containing only the Least Significant bit (LSb) will be sent to another serializer, as shown in Fig. D.7.

Again, after the serialization process, the desired signal of all independent paths is now phase aligned and centered at fc while the noise has different canceling phases. This way, when all paths are combined, the desired signal will have an improved dynamic range.

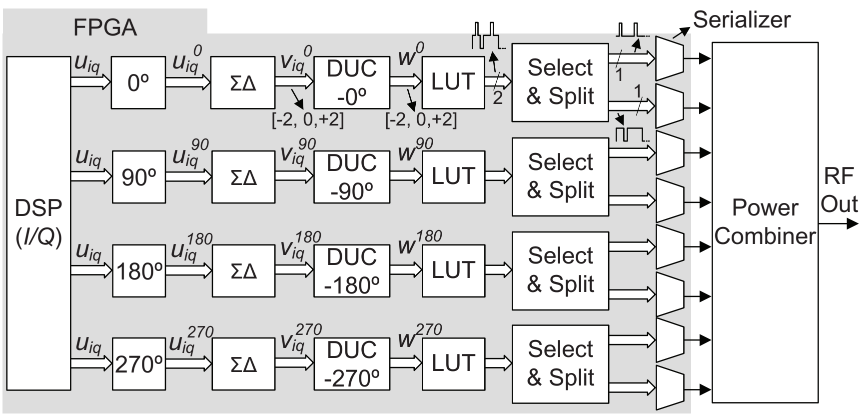

Figure D.7: High level block diagram illustrating the implemented ΣΔ-based polyphase multipath agile transmitter.

D.4.2 PWM-based RF Transmitter

The design stage details regarding the PWM-based transmitter will be given in this Subsection, see Fig. D.8. This transmitter requires a baseband signal where each component is quantified using 8 bits, 1 for the signal and 7 for the magnitude. For each individual path, the 7-bit magnitude information is directly translated into a PWM word accordingly to a specific PWM matrix. For the first two independent paths, the used 128-by-128 PWM matrix can be described as a triangular lower filled with ones, as shown below:

$$PWM_0 = \begin{bmatrix} 1 & & 0 \\ \vdots & \ddots & \\ 1 & \cdots & 1 \end{bmatrix}$$

For the last two independent paths, the used 128-by-128 PWM matrix is a horizontal mirror of the first one, as shown below:

$$PWM_1 = \begin{bmatrix} 0 & & 1 \\ & \iddots & \vdots \\ 1 & \cdots & 1 \end{bmatrix}$$

Since each row of PWM_1 has the same number of ones as in PWM_0, the resulting signal after the PWM modulation will have the same energy, regardless the used PWM matrix. On the other hand, since the ones are placed at different positions for the chosen PWM matrices, the PWM noise will appear with different phases. This way, when combining the outputs, the energy of the desired signal will add in a proportion that is higher than the unwanted noise.

Additionally, when the optional *Pattern Randomization* is used, the PWM noise is spread along the RF spectrum, which can be interesting for reducing the RF filter requirements.

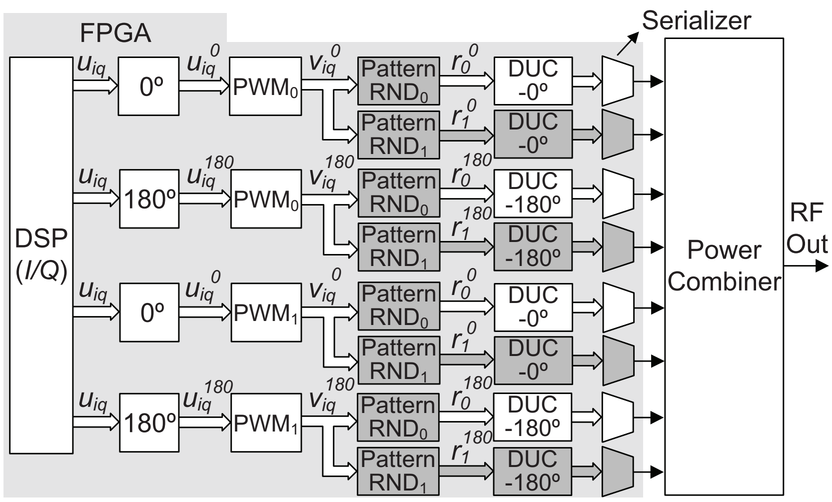

Figure D.8: High level block diagram illustrating the implemented PWM-based polyphase multipath transmitter. The optional blocks are shown in dark gray.

The designed transmitter applies in *Pattern* RND_0 a set of pseudo-random rotations for each PWM word (as previously shown in Fig. D.4). For the used sampling frequency, the same random rotations are applied to several PWM samples, as can be seen in Fig. D.8. On the other hand, since shifting the position of the ones in each PWM word will change the PWM noise phase, we expanded the transmitter to include an additional *Pattern* RND_1. This block will implement a different set of pseudo-random rotations, allowing to duplicate the number of output paths with different phase noise, and therefore improving the dynamic range of the desired signal.

D.5 Experimental Results

This section presents and discusses the main experimental results for three different variants of the proposed agile and coding efficient all-digital transmitter. The first variant will regard $\Sigma\Delta$-based data transmission while the other variants will present PWM-based data transmission with and without pattern randomization.

The proposed RF transmitter was prototyped in an *ML628* development board containing a *Virtex6 HX380T* FPGA. For the purpose of this proof-of-concept, we implemented the base datapath shown in Fig. D.6 and connected its digital RF outputs to a *Mini-Circuits* 8:1 RF power combiner model *ZN8PD1-53+*. Finally, the power combiner was directly connected to a Vector Spectrum Analyzer (VSA), as can be seen in Fig. D.9.

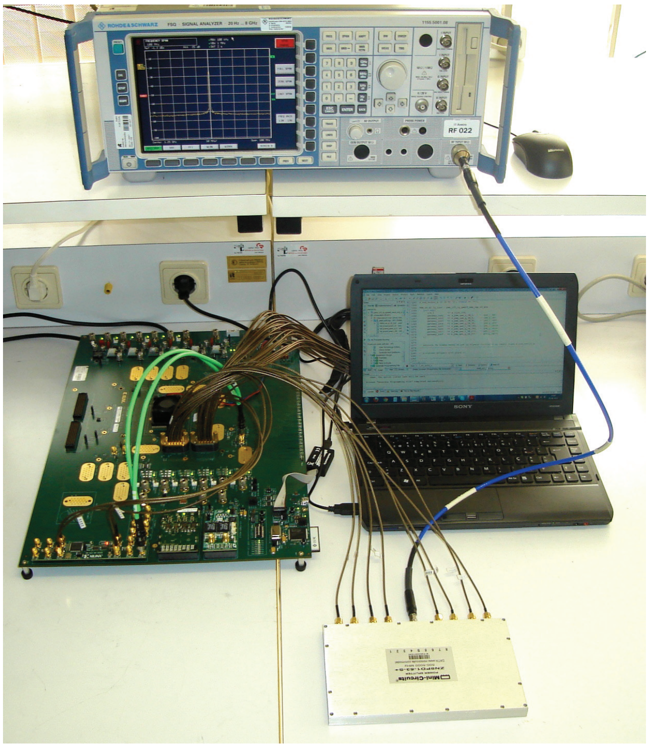

Figure D.9: Setup of the evaluated FPGA-based all-digital transmitter.

The baseband test signals used in this setup are a 64-QAM signal with a symbol rate of 1.25 MSPS and a Peak-to-Average Power Ratio (PAPR) of approx. 7 dB and a WiMAX signal (OFDM based) with a 1.5 MHz bandwidth and a PAPR of 8 dB. Moreover, all baseband signals were stored inside the FPGA's internal memory.

D.5.1 ΣΔ-based Data Transmission

As a first experiment, the implemented RF transmitter architecture illustrated in Fig. D.7 was configured to perform the transmission of one carrier centered at 1.25 GHz and containing a 64-QAM signal. For this implementation example, all ΣΔ modulators were set to operate at a sampling frequency of 156.25 MHz. This sampling frequency, fs is given by:

$$fs = \frac{4 \times fc}{\mathrm{width}(w)}, \tag{D.3}$$

where fc is the chosen carrier frequency, and $\mathrm{width}(w)$ is the width of the word w that will be fed to the serializer.

For the first independent path, the *RF_LO* vectors and the *Select and Combine* block of the *DUC -0º* were configured to generate the following 32-bit output word:

$$w^0 = [\text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,$$
$$\text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_{q,}].$$

For the second path, the *DUC -90º* was configured to generate the following 32-bit output word:

$$w^{90} = [+v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,$$
$$+v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_{i,}].$$

The *DUC -180º* was configured to generate the following 32-bit output word:

$$w^{180} = [+v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,$$
$$+v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_{q,}].$$

For the last independent path, the *DUC -270º* was configured to generate the following 32-bit output word:

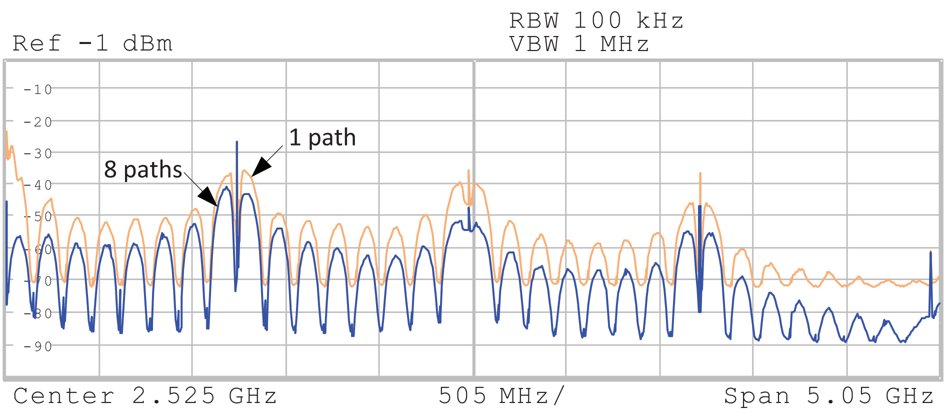

Figure D.10: Overlapped measurement results for the ΣΔ-based agile transmitter when using 8 paths versus a single path approach with a gain normalized to the 8 paths.

$$w^{270} = [\text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i,\ \text{-}v_q,\ +v_i,\ +v_q,\ \text{-}v_i].$$

These output words were then converted into a 2-bit representation and split so that each bit is fed to one multigigabit (MGT) serializer. The serializer must be configured to operate at a line rate that is 4 times the desired carrier frequency. This way, for the 1.25 GHz carrier, the serializer was set to operate at 5 Gbps.

After combining the outputs of the 8 serializers it is possible to obtain the spectrum shown in Fig. D.10. For comparison purposes, the obtained spectrum resulting from combining 8 paths is shown overlapped with a single path and the gain for the single path was normalized to the 8-path implementation results. As can be seen, for the same energy of the desired signal, the 8-path implementation has clearly less out-of-band noise. This way, the proposed transmitter clearly allows to improve the coding efficiency while maintaining the flexibility inherent to the all-digital transmitter concept.

D.5.2 PWM-based Data Transmission

This Subsection presents the experimental results for two different PWM-based approaches followed for realizing an all-digital transmitter. One using a pure PWM-based architecture, while the other combines PWM with a pattern randomizer as illustrated in Fig. D.8.

In both cases the transmitters where configured to implement a 1.25 GHz carrier containing a 64-QAM signal so that it is possible to provide a better comparison with the previously implemented ΣΔ-based transmitter. Accordingly to eq. (D.3), all 7-bit PWM modulators were set to operate at the same sampling frequency of 156.25 MHz. Also, all independent paths perform the DUC in a similar way to the previously implemented ΣΔ-based transmitter.

After combining the outputs of the 4 serializers for the PWM-based transmitter without pattern randomization, it is possible to obtain the spectrum shown in Fig. D.11. For comparison purposes, the obtained spectrum resulting from combining 4 paths is shown overlapped

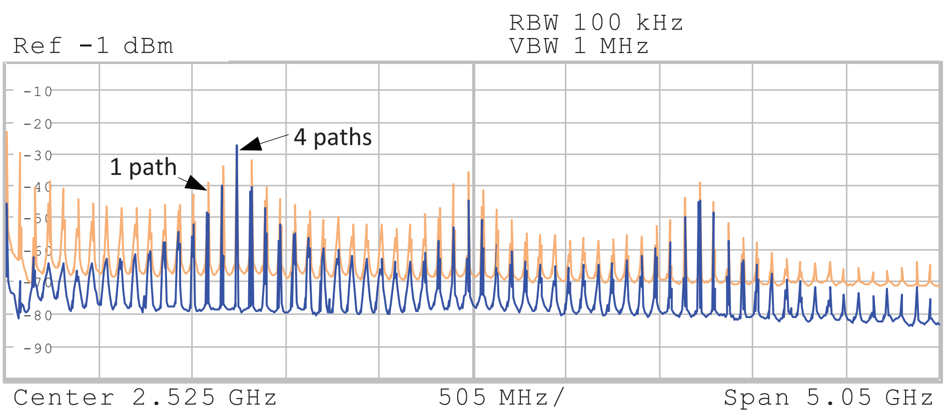

Figure D.11: Overlapped measurement results for the PWM-based transmitter without pattern randomization when configured with 4 paths vs. a single path with normalized gain.

with a single path. Again, the single path spectrum results were normalized to the 4-path implementation results for an easier comparison. As can be seen, for the same energy on the carrier, the single path spectrum shows a considerable higher noise. Moreover, the 8-path implementation has a significant PWM noise reduction for the lower frequency harmonics. This way, it is clear that the proposed PWM-based transmitter allows significant improvements in terms of coding efficiency.

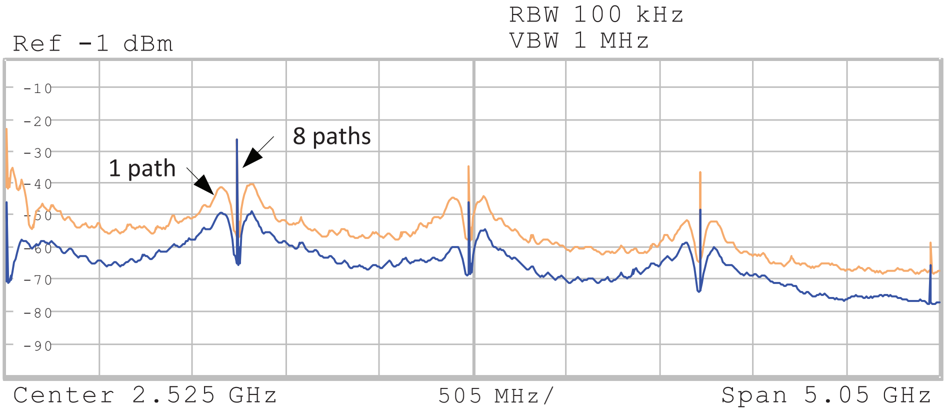

Figure D.12: Overlapped measurement results for the PWM-based transmitter with pattern randomization when configured with 8 paths versus a single path with a gain normalized to the 8 paths.

Then, the FPGA hardware was reconfigured to implement the PWM-based transmitter with pattern randomization. In Fig. D.12 it is illustrated the obtained spectrum of the implemented transmitter overlapping the results for one implementation where 8 paths are combined with a single path approach with gain normalized to the 8-path implementation. Again, the obtained results show clear improvements in terms of coding efficiency. Moreover, it can be seen that using pattern randomization allows reducing the peak spurious which in turn can be interesting for alleviating the quality factor requirements of the RF reconstruction filter.

D.5.3 Multichannel Data Transmission

This Subsection presents the implementation results for a ΣΔ-based architecture when configured for multichannel data transmission. The architecture of the implemented RF transmitter is identical to the previously illustrated in Fig. D.7. However, instead of having 4 independent paths, each one having a different phase noise for the same baseband signal, the multichannel transmitter uses only two different phases (0^o and 180^o) and has two baseband signals, a 64-QAM connected to the first two independent paths and a WiMAX signal connected to the last two independent paths.

The multichannel transmitter was configured to perform the simultaneous transmission of the 64-QAM signal centered at 1.25 GHz and the WiMAX signal centered at 781.25 MHz. For this implementation example, all ΣΔ modulators were set to operate at a sampling frequency of 156.25 MHz. A base requirement of this approach is that the sampling frequencies of all

$\Sigma\Delta$ modulators must have an integer relation. This way, it is possible to overlap the noise transfer function nulls of the multiple $\Sigma\Delta$ modulators, and consequently allowing to insert the desired signals in those nulls.

Accordingly to eq. (D.3), transmitting the 64-QAM signal centered at 1.25 GHz requires the serialization of the parallel word w with a width of 32 bits. On the other hand, transmitting the WiMAX signal centered at 781.25 MHz requires w to have a width of 20 bits.

For the first independent path containing the 64-QAM signal, the *DUC -0º* was configured to generate the following 32-bit output word:

$$w^{0} = [-v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, \\ -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q,}].$$

For the second path, the *DUC -180º* was configured to generate the following 32-bit output word:

$$w^{180} = [+v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, \\ +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q,}].$$

The *DUC -0º* for the third independent path containing the WiMAX signal was configured to generate the following 20-bit output word:

$$w^{0} = [-v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, \\ +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q,}].$$

For the last path, the *DUC -180º* was configured to generate the following 20-bit output word:

$$w^{180} = [+v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, \\ -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q}, +v_{i}, +v_{q}, -v_{i}, -v_{q,}].$$

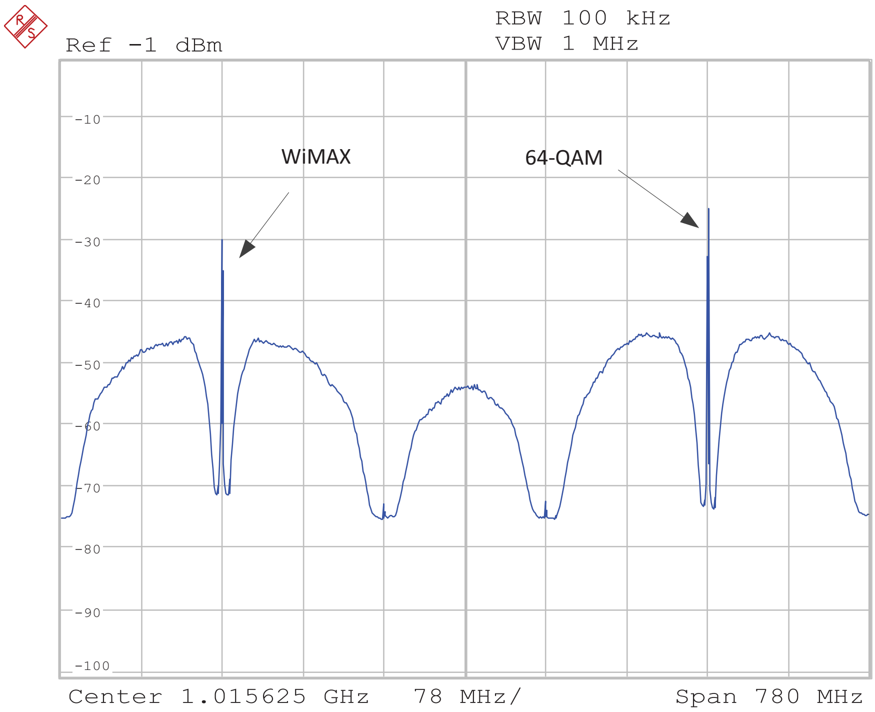

Figure D.13: Measured multichannel spectrum of the $\Sigma\Delta$-based transmitter.

These output words were converted into a 2-bit representation and then split so that each bit is fed to one serializer. At last, since the line rate of each serializer must be 4 times the carrier frequency, the first 4 serializers were set to operate at 5 Gbps while the last 4 serializers were set to operate at 3.125 Gbps. After combining the outputs of the 8 serializers it is possible to obtain the spectrum shown in Fig. D.13.

D.5.4 Comparative Analysis

In Fig. D.14 are shown overlapped the spectrum results for the PWM-based approach with and without pattern randomization and the ΣΔ-based transmitter so that a better comparative analysis between the implemented transmitters is possible.

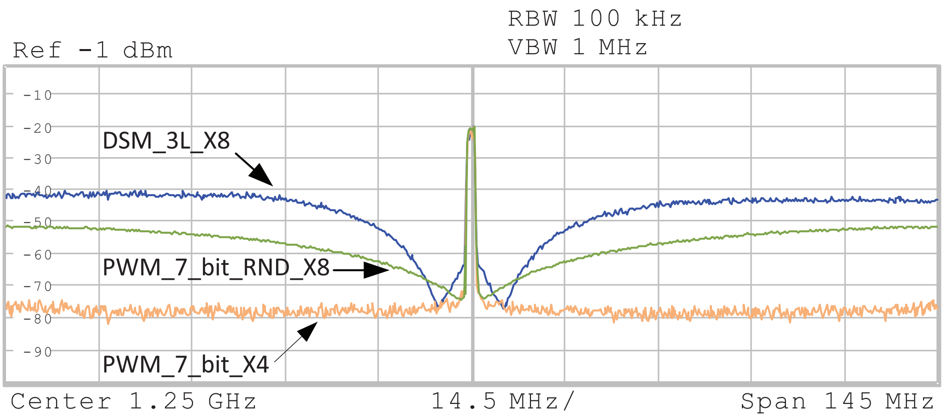

Figure D.14: Overlapped measurement results comparing the PWM-based approach with and without pattern randomization ant the ΣΔ-based transmitter.

As can be seen in Fig. D.14, the worse implementation in terms of coding efficiency is the ΣΔ-based, where the quantization noise is clearly higher than in the other approaches. The implementation with lower out-of-band noise within the 145 MHz span is the 7-bit

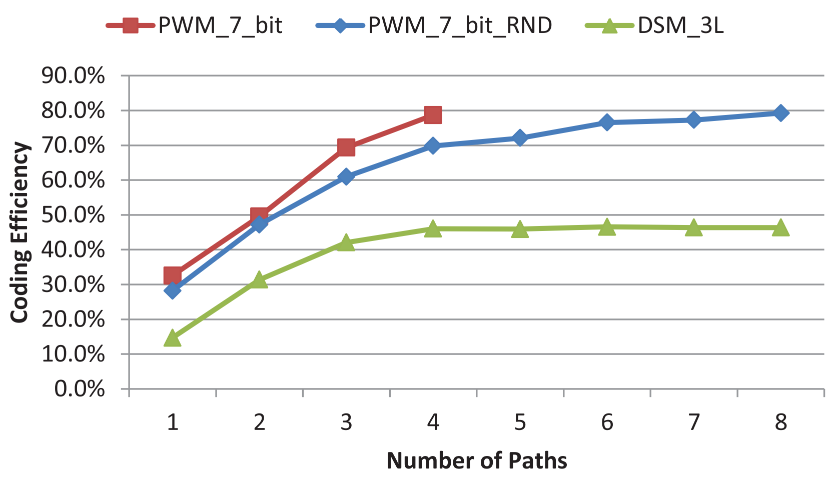

Figure D.15: Coding efficiency evolution accordingly to the number of used transmission paths for the three implemented transmitters.

PWM without pattern randomizer. However, this approach generates PWM harmonics with considerable high levels of energy spaced at the PWM sampling frequency. By spreading the PWM noise over the frequency, the 7-bit PWM implementation with pattern randomization successfully eliminates the undesirable PWM harmonics.

The coding efficiency evolution and the modulation accuracy evolution accordingly to the number of used transmission paths for the three implemented transmitters are shown in Figs. D.15 and D.16, respectively. As anticipated by the previous results shown in Fig. D.14, the ΣΔ-based transmitter approach has the lower coding efficiency and lower Error Vector magnitude (EVM). Moreover, the power combining of multiple independent paths with a different phase noise has also less impact in this approach, especially when combining more than 4 paths. A possible explanation may rely in the fact that in ΣΔ modulation, the variation of the output signal is higher than when using a PWM-based approach. This way, these higher variations at the output of the transmitter combined with non-ideal output waveforms of the serializers and also with small timing mismatches between the independent paths are a possible explanation for this worse performance when combining a higher number of independent paths.

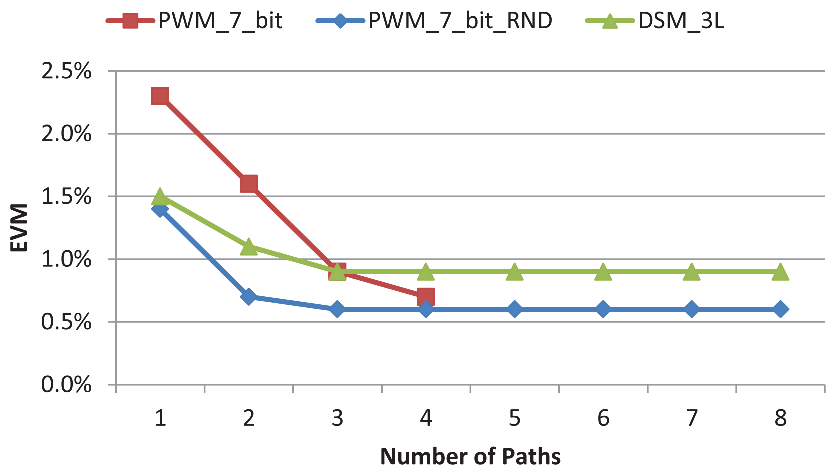

Figure D.16: Error vector magnitude evolution accordingly to the number of used transmission paths for the three implemented transmitters.

The PWM-based approach with pattern randomization combines the best results in terms of modulation accuracy with a high coding efficiency. In fact, discarding the typical 1.5 dB

Table D.1: Comparison with other all-digital transmitter approaches

	Johnson 2006 [15]	Hung 2007 [16]	Ghannouchi 2010 [17]	Schmidt 2011 [18]	PWM_7_bit	PWM_7_bit_RND	DSM_3L
Signal	W-CDMA	CDMA	WiMAX	N/D	64-QAM	64-QAM	64-QAM
Cod. Eff.	3.4%	32.0%	6.6%	35.0%	78.7%	79.3%	46.3%
SNR	74.5dB	43dB	45dB	N/D	50dB	50dB	45dB
Modulation	2-level ΣΔ	3-level ΣΔ	2-level ΣΔ	3-level ΣΔ	7-bit PWM	7-bit PWM	3-level ΣΔ
Validation	Simulation	Simulation	Hardware	Simulation	Hardware	Hardware	Hardware

insertion losses of the power combiner, the total energy resulting from combining the 8 independent paths is only 1.4 dB below when compared with the ideal addition. This means that almost all energy of the desired signal is adding constructively in this proposed all-digital transmitter. At last, the PWM-based transmitter without pattern randomization has also proven to be an interesting approach when combining multiple independent paths, as can be seen by the obtained high coding efficiency and high modulation accuracy.

A comparison between several state-of-the-art all-digital transmitters is shown in Table D.1. As can be seen, all the proposed transmitters provide very high coding efficiency and reasonable high SNR, while maintaining the high flexibility inherent to the all-digital RF transmitters.

Table D.2: Main occupied resources of the implemented FPGA-based all-digital transmitters.

Logic resources	DSM_3L	PWM_7_bit	PWM_7_bit_RND
LUTs	965 (1%)	3513 (1%)	11290 (5%)
Flip-Flops	616 (1%)	2803 (1%)	9540 (2%)
RAM36E1	12 (2%)	28 (2%)	28 (2%)
GTHE1_QUADs	2 (33%)	1 (17%)	2 (33%)

The main occupied FPGA resources for the three implemented transmitters are shown in Table D.2. The 7-bit PWM-based approach with pattern randomization is clearly the larger design, which is due to the additional hardware complexity for implementing the pattern randomization blocks. However, even for the larger design, the entire datapath takes only about 5% of the FPGA fabric, providing a large area available for other system functionalities and a vast grade of integration including, for instance, the processing of baseband protocols.

D.6 Conclusion

In this paper, a new all-digital transmitter architecture using different pulse shaping techniques combined with polyphase multipaths was presented. The proposed transmitter combines multichannel data transmission with high coding efficiency and SNR while maintaining the flexibility.

From the three proposed variants, the 7-bit PWM-based transmitter with pattern randomization has the higher complexity. However it provides the higher coding efficiency and the lower EVM. Moreover, the PWM noise spreading over the spectrum enables relaxing the design constraints for the RF reconstruction filter.

The obtained results also show the feasibility and potential of using FPGA-based polyphase multipath architectures for implementing digital RF transmitters.

Acknowledgment

This work was supported in part by the Portuguese Foundation for Science and Technology under PhD scholarship ref. SFRH/BD/76807/2011, under project TACCS ref. PTDC/EEA-

TEL/099646/2008 and by the Instituto de Telecomunicações under project DiRecTRadio ref. LA-LVT-8.

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Paper E

Novel Fine Tunable Multichannel All-Digital Transmitter

Nelson V. Silva, Arnaldo S. R. Oliveira and Nuno B. Carvalho

in *IEEE MTT-S International Microwave Symposium Digest (MTT)*, June 2013, accepted.

The format has been revised.

Novel Fine Tunable Multichannel All-Digital Transmitter

Nelson V. Silva, Arnaldo S. R. Oliveira and Nuno Borges Carvalho

Abstract

All-digital transmitters are gaining an increased research importance due to the unparalleled proliferation of dissimilar wireless standards and more recently due to the white space technology needs. In this paper, a new fine tunable multichannel transmitter is presented. This new architecture supports concurrent multi-rate, multi-band, multi-standard transmission and significantly minimizes the output frequencies restrictions of current approaches by allowing fine frequency tuning for channel selection.

The obtained results show the feasibility and potential of FPGA-embedded RF transmitters where the use of polyphase datapaths substantially improves the SNR of the desired signals.

E.1 Introduction

The unparalleled proliferation of wireless standards operating at different frequencies, using dissimilar coding and modulation schemes, and targeted for different purposes fosters the development of new flexible radios, capable of adapting to different communication scenarios. However, a key challenge for achieving such a new communications paradigm involves the development of a very flexible physical layer that should support the simultaneous transmission of several multi-rate, multi-band, multi-standard signals, which in practice is very hard to achieve using conventional approaches.

Nonetheless, recent advances in this field include the development of novel all-digital transmitters [2, 3, 4, 5], where its datapath is entirely digital up to the RF stage, see Fig. E.1. The inherent high flexibility of such concept poses an important step towards the development of new radios and shortens the gap towards the ideal Software-Defined Radio (SDR) transmitter [6]. However, current all-digital transmitters still have a few key limitations that prevent its wider dissemination. In fact, almost all the above cited transmitters do not support multichannel operation, others require expensive external multiplexers for the RF up-conversion and most of them require very high-quality filters to remove out-of-band noise.

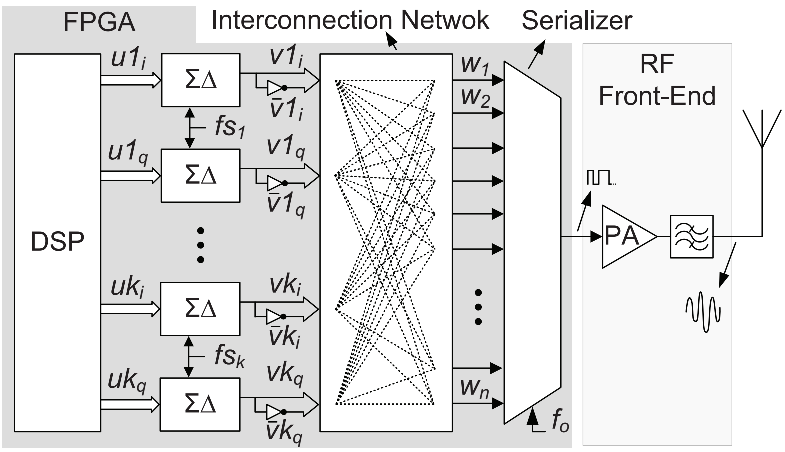

Figure E.1: Block diagram illustrating the architecture of a conventional multichannel agile transmitter, adapted from [1].

In [1] we proposed a new multichannel all-digital transmitter. However, such approach was very limited in terms of allowed output frequencies and provides low SNR, making harder the simultaneous transmission of more than two carriers. In this paper we address those limitations by proposing a new transmitter architecture that allows the fine frequency tuning for each carrier, where the RF output operating in the microwave frequency range is generated inside a single FPGA. Additionally, the proposed RF transmitter explores the use of polyphase datapaths for improving the quality of the transmitting signal in terms of SNR and out-of-band noise.

The remainder of this paper is organized as follows. Section E.2 details the implemented RF transmitter architecture. The experimental results of the proposed fine frequency tuning multichannel transmitter are reported in Section E.3. Finally, Section E.4 presents the conclusion.

E.2 Proposed All-Digital Transmitter

This Section details the design and improvement stages of the proposed fine tunable multichannel transmitter. In this architecture, the fine frequency tuning is achieved by using a two-stage up-conversion approach where IF image rejection is used in order to maximize the usable bandwidth of the RF transmitter. The first up-conversion stage uses a digital Single-SideBand (SSB) signal generation approach based on the Weaver modulator [7], where a set of two multipliers shift the baseband components (b_i and b_q) into an IF signal (u_i) and two other multipliers generate a 90° phase shifted IF signal centered at the same frequency (u_q), as can be seen in Fig. E.2.

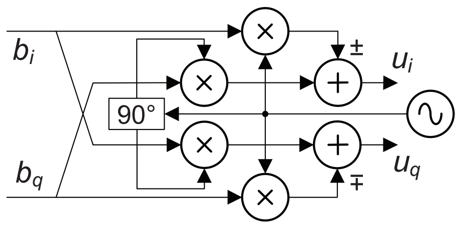

Figure E.2: Block diagram illustrating the implemented quadrature single-sideband up-converter for IF image rejection.

After the first up-conversion stage, the IF signal is converted into a 2-level representation using ΣΔ modulation. The ΣΔ coefficients were precomputed using the ΣΔ-toolbox [8], for a sampling rate of f_s = 150 MHz and a bandpass of 12 MHz, resulting in an effective

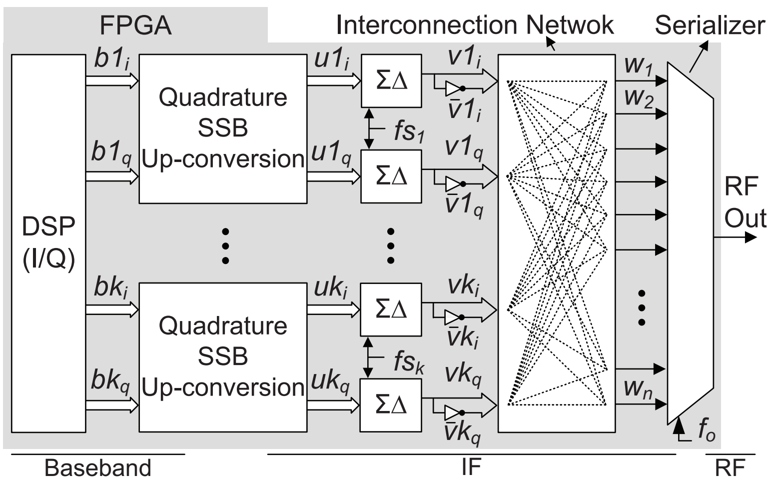

Figure E.3: Proposed agile transmitter detailing the fine frequency tuning of the multichannel carriers by using a two-stage up-conversion approach combined with SSB signal generation.

OverSampling Ratio (OSR) of 12.5. These coefficients were then rounded to powers of two or if not suitable, to a two's-complement binary representation using up to eight bits. This rounding approach contributes in reducing area and most importantly, shortens the critical path. The resulting highpass NTF can be given by:

$$\mathrm{NTF}(z) = \frac{z^2 - 2z + 1.039}{z^2 - 0.875z + 0.3145}. \tag{E.1}$$

A block diagram detailing the architecture of the proposed fine tunable multichannel transmitter is shown in Fig. E.3. In this architecture, each channel uses a $\Sigma\Delta$ pair to process the IF components (u_i and u_q) generated by the first up-conversion stage. The resulting signals of the $\Sigma\Delta$ modulators and its inverted versions are then connected to a multi-gigabit serializer through an interconnection network. This network combines and replicates the $\Sigma\Delta$ output signals to generate a parallel output word (w) that contains for each channel, the four components of the desired signal ($v_i v_q \bar{v}_i \bar{v}_q$).

The serialization of this parallel word will generate a multichannel RF SSB signal where the order given to the four components of the desired signal will determine for each channel, which sideband is generated. For instance, serializing $v_i v_q \bar{v}_i \bar{v}_q$ will generate an RF carrier centered at the Lower SideBand (LSB) and serializing $v_i \bar{v}_q \bar{v}_i v_q$ will result in an RF carrier centered at the Upper SideBand (USB) of the spectrum.

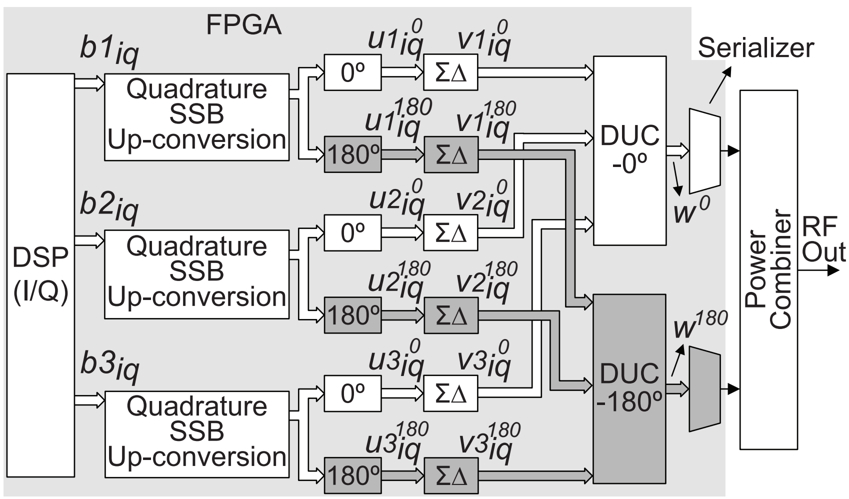

Figure E.4: High-level block diagram illustrating the implemented fine frequency tuning multichannel transmitter combined with a polyphase datapath for improving the quality of the transmitting signal.

The proposed architecture illustrated in Fig. E.3 was further enhanced by using a polyphase datapath approach in order to improve the quality of the transmitting signal in terms of SNR and out-of-band noise emission, see Fig. E.4.

In this approach, the phase of the desired signal is shifted before entering the $\Sigma\Delta$ modulators and shifted back to the original phase in the last up-conversion stage. This way, each serializer will generate an RF output where the desired signal will have the same original phase, while the ΣΔ quantization noise will have a different phase. Therefore, if the RF outputs from each serializer are combined, the in-phase energy of the desired signal will increase more that the unwanted noise.

E.3 Experimental Results

The proposed fine tunable multichannel transmitter was prototyped in an *ML628* development board containing a *Virtex6 HX380T* FPGA. For the purpose of this proof-of-concept, the datapath shown in Fig. E.4 was implemented and its digital RF outputs were connected to a *Mini-Circuits* 2:1 RF power combiner model *ZN2PD2-50-S+*. Finally, the power combiner was directly connected to a Vector Signal Analyzer (VSA). The baseband test signals used in this setup are one WiMAX (OFDM based) and two 64-QAM signals, all stored inside the FPGA's internal memory.

As a first experiment, the implemented RF transmitter was configured to simultaneously transmit three independent carriers, one centered at 745.5 MHz containing a Narrow Band (NB) 64-QAM ($b1_{iq}$), a second one centered at 748.5 MHz containing a Wider Band (WB) 64-QAM ($b2_{iq}$) and a third one centered at 753.0 MHz, containing a WiMAX signal ($b3_{iq}$).

For this implementation example, the first up-conversion stage was configured to shift each one of the three baseband signals to a different IF band. The wider 64-QAM signal was up-converted to a 1.5 MHz IF, while the narrow band 64-QAM was shifted to 4.5 MHz, and the WiMAX to 3 MHz.

Next, all ΣΔ modulators were set to operate at a sampling frequency of 187.5 MHz and each serializer was configured to generate a line rate of 9 Gbps. For the polyphase datapath containing the *DUC-0°* shown in Fig. E.4, the interconnection network was configured to generate the following 48-bit word:

$$w^{0} = [v1_i\ v2_i\ v3_i\ \overline{v}1_q\ \overline{v}2_q\ v3_q\ \overline{v}1_i\ \overline{v}2_i\ \overline{v}3_i\ v1_q\ v2_q\ \overline{v}3_q\ v1_i\ v2_i\ v3_i\ \overline{v}1_q\ \overline{v}2_q\ v3_q\ \overline{v}1_i\ \overline{v}2_i\ \overline{v}3_i\ v1_q\ v2_q\ \overline{v}3_q$$
$$v1_i\ v2_i\ v3_i\ \overline{v}1_q\ \overline{v}2_q\ v3_q\ \overline{v}1_i\ \overline{v}2_i\ \overline{v}3_i\ v1_q\ v2_q\ \overline{v}3_q\ v1_i\ v2_i\ v3_i\ \overline{v}1_q\ \overline{v}2_q\ v3_q\ \overline{v}1_i\ \overline{v}2_i\ \overline{v}3_i\ v1_q\ v2_q\ \overline{v}3_q].$$

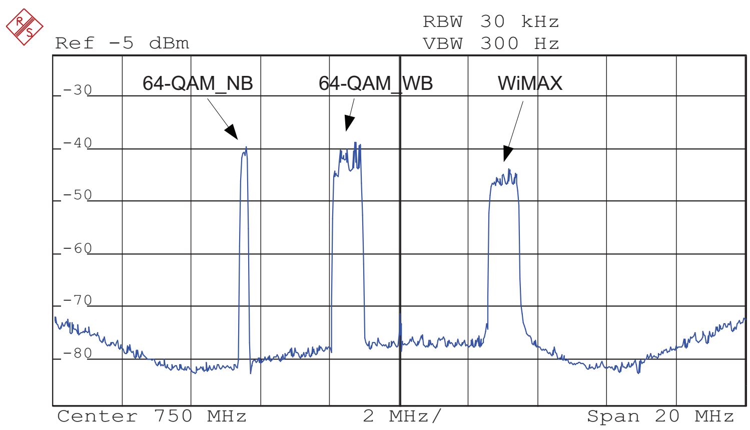

Figure E.5: Measured multichannel spectrum when the fine tunable RF transmitter is configured to simultaneously generate three independent carriers, one centered at 745.5 MHz, a second one centered at 748.5 MHz and a third one centered at 753.0 MHz.

The serialization of w^0 at a rate of 9 Gbps will produce a multichannel RF signal with a 750 MHz central frequency, given by the line rate / (number of channels $\times$ 4). Moreover, the order given in w^0 to the four components $(v_i v_q \bar{v}_i \bar{v}_q)$ of the three channels will impose the two 64-QAM signals appearing at the LSB of the central frequency, while the WiMAX signal will appear at the HSB, as shown in Fig. E.5. For the second path, the *DUC-180°* was configured to generate the following 48-bit output word:

$w^{180} = [\bar{v}1_i\ \bar{v}2_i\ \bar{v}3_i\ v1_q\ v2_q\ \bar{v}3_q\ v1_i\ v2_i\ v3_i\ \bar{v}1_q\ \bar{v}2_q\ v3_q\ \bar{v}1_i\ \bar{v}2_i\ \bar{v}3_i\ v1_q\ v2_q\ \bar{v}3_q\ v1_i\ v2_i\ v3_i\ \bar{v}1_q\ \bar{v}2_q\ v3_q$
$\bar{v}1_i\ \bar{v}2_i\ \bar{v}3_i\ v1_q\ v2_q\ \bar{v}3_q\ v1_i\ v2_i\ v3_i\ \bar{v}1_q\ \bar{v}2_q\ v3_q\ \bar{v}1_i\ \bar{v}2_i\ \bar{v}3_i\ v1_q\ v2_q\ \bar{v}3_q\ v1_i\ v2_i\ v3_i\ \bar{v}1_q\ \bar{v}2_q\ v3_q]$.

This second word is an inverted version of w^0 so that the desired signals are shifted back to their original phases. This way, the RF output of both serializers can be combined and the desired signals will add constructively. In fact, using the VSA to demodulate the wider 64-QAM signal, it was possible to quantify the Modulation Error Ratio (MER) gain when two polyphase datapaths are used. The obtained 35.2 dB for the two polyphase datapaths versus 32.3 dB for the single path approach shows a $\approx$3 dB improvement in the desired signal.

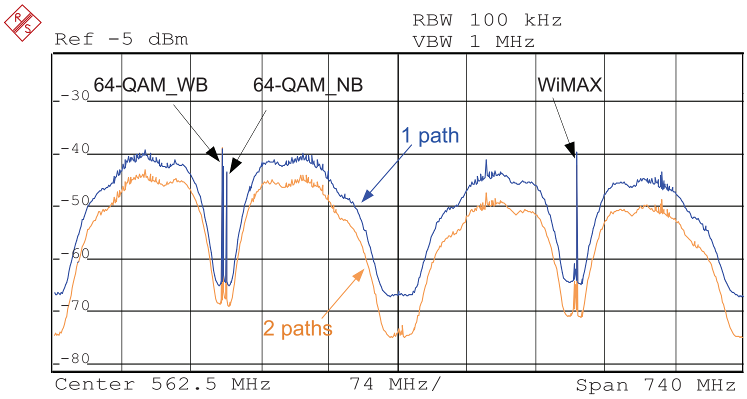

Figure E.6: Measured multichannel spectrum when the proposed agile transmitter is configured to transmit three carriers and where the spectrum obtained by using two independent paths is overlapped with a single path approach with a gain normalized to the 2 paths.

As a second experiment, the implemented RF transmitter was configured to perform the simultaneous transmission of three carriers, one centered at 373.5 MHz, a second one centered at 378.0 MHz and a third one centered at 753.0 MHz.

In this implementation example, all frequencies and data rates are equal to the first experiment, with exception to the narrow band 64-QAM signal that was shifted to a 3 MHz IF in the first up-conversion stage. For the polyphase datapath containing the *DUC-0°*, the interconnection network was configured to generate the following 48-bit output word:

$w^0 = [v1_i\ v2_i\ v3_i\ v1_i\ v2_i\ v3_q\ v1_q\ \bar{v}2_q\ \bar{v}3_i\ v1_q\ \bar{v}2_q\ \bar{v}3_q\ \bar{v}1_i\ \bar{v}2_i\ v3_i\ \bar{v}1_i\ \bar{v}2_i\ v3_q\ \bar{v}1_q\ v2_q\ \bar{v}3_i\ \bar{v}1_q\ v2_q\ \bar{v}3_q$
$v1_i\ v2_i\ v3_i\ v1_i\ v2_i\ v3_q\ v1_q\ \bar{v}2_q\ \bar{v}3_i\ v1_q\ \bar{v}2_q\ \bar{v}3_q\ \bar{v}1_i\ \bar{v}2_i\ v3_i\ \bar{v}1_i\ \bar{v}2_i\ v3_q\ \bar{v}1_q\ v2_q\ \bar{v}3_i\ \bar{v}1_q\ v2_q\ \bar{v}3_q]$.

The serialization of w^0 at a rate of 9 Gbps will generate a multichannel RF signal with a lower central frequency of 375 MHz and a higher central frequency of 750 MHz. Once again, the order given in w^0 to the four components $(v_i v_q \bar{v}_i \bar{v}_q)$ of the three channels will impose the narrow band 64-QAM and the WiMAX signals to appear at the HSB of their central frequencies, while the wider 64-QAM will appear at the LSB. For the second path, the *DUC-180°* was configured to generate the following 48-bit output word:

$w^{180} = [\bar{v}1_i\ \bar{v}2_i\ \bar{v}3_i\ \bar{v}1_i\ \bar{v}2_i\ \bar{v}3_q\ \bar{v}1_q\ v2_q\ v3_i\ \bar{v}1_q\ v2_q\ v3_q\ v1_i\ v2_i\ \bar{v}3_i\ v1_i\ v2_i\ \bar{v}3_q\ v1_q\ \bar{v}2_q\ v3_i\ v1_q\ \bar{v}2_q\ v3_q$
$\bar{v}1_i\ \bar{v}2_i\ \bar{v}3_i\ \bar{v}1_i\ \bar{v}2_i\ \bar{v}3_q\ \bar{v}1_q\ v2_q\ v3_i\ \bar{v}1_q\ v2_q\ v3_q\ v1_i\ v2_i\ \bar{v}3_i\ v1_i\ v2_i\ \bar{v}3_q\ v1_q\ \bar{v}2_q\ v3_i\ v1_q\ \bar{v}2_q\ v3_q].$

As illustrated in Fig. E.6, the use of polyphase datapaths allows to combine the energy of the desired signal in a proportion that is higher than the unwanted noise. This way, it is possible to increase the SNR of the transmitting signal and simultaneously reduce the out-of-band noise.

E.4 Conclusion

A new fine tunable all-digital transmitter architecture was presented in this paper. The proposed RF transmitter supports the concurrent data transmission of multi-rate, multi-band, multi-standard signals and uses polyphase datapaths in order to improve the quality of the transmitting signal.

The obtained results show the feasibility and potential of FPGA-based RF transmitters, where a two-stage up-conversion approach provides the fine frequency tuning for each transmitting channel and where combining two polyphase datapaths significantly improves the SNR of the desired signals.

Acknowledgment

This work was supported in part by the Portuguese Foundation for Science and Technology under PhD scholarship ref. SFRH/BD/76807/2011 and by the Instituto de Telecomunicações under project DiRecTRadio ref. LA-LVT-8.

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