GENERAL MODEL FOR DELAYED FEEDBACK AND ITS APPLICATION TO TRANSIMPEDANCE AMPLIFIER'S BANDWIDTH OPTIMIZATION

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ABSTRACT

Delays in real systems can be of two types: i) intrinsic delays – due to the physical principles of operation of each electronic device; ii) designed delays – due to extra circuits used to add the desired delay. Previous work established the possibility of achieving bandwidth improvements using small delays inside the feedback loop of feedback amplifiers. The modeling approach followed on these contributions used only one designed delay element. The bandwidth reduction effect due to intrinsic delays was not considered on these contributions. This paper extends the concept to the general case of feedback amplifiers that incorporates delays of both types.
An experimental demonstration using a simple 0.35µm BiCMOS transimpedance amplifier further confirms the proposed model.

1. INTRODUCTION

A delayed feedback amplifier is by definition an amplifier configured in a feedback scheme comprising: i) a forward gain amplifier, ii) a delay element, and iii) a β block (feedback factor). This definition obviously includes all real feedback amplifiers, because all electronic devices have small intrinsic delays. In general these small delays produce negligible effects on amplifier's performance. However, there are applications [3] where high-gain, high-bandwidth requirements together with these delays, lead to instability.
Recent developments [1, 2] reported the usage of delayed feedback as a means of achieving significant bandwidth improvements (thus allowing significant gain-bandwidth improvements). Using a small delay inside the feedback loop of a feedback amplifier enables almost 110% bandwidth improvement without losing frequency response performance that is; maintaining flatness and linear phase decay inside the sought bandwidth. A theoretical method to find the necessary condition to achieve maximum flatness operation was developed in [2]. This condition relates all the design variables in a delayed feedback amplifier, namely: the loop-gain, the open-loop poles, and the total delay around the loop. Using this condition it is possible to design stable bandwidth optimized feedback amplifiers. The proposed model assumes that all the delays around the loop can be concentrated in only one pure delay element.
This paper improves this model for the delayed feedback amplifier considering the two types of delays: intrinsic delays – modeled as complex exponentials of the frequency variable; and designed delays – based on first order Pade approximants of the pure delay (suited to active delay modeling [5]). The introduction of the designed delay element further extends the potentialities of the proposed model. An optimized transimpedance amplifier, suited to optical receivers with large area photodiodes (150pF), was designed to evaluate this model.
Section 2 presents the new proposed model and explores its features. Section 3 presents the designed circuit and describes the required optimization steps. Section 4 presents simulation results, and finally on section 5 some conclusions are drawn.

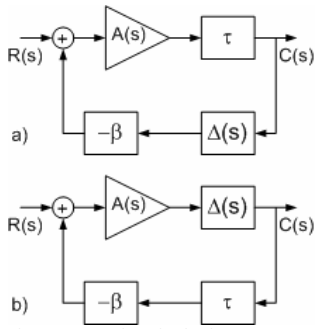

Figure 1 - Circuit design concept

2. MODEL PRESENTATION

Figure 1 represents two delayed feedback amplifiers, comprising both intrinsic and designed delays (τ and $\Delta(s)$ elements, respectively). The difference between the two configurations lies only on the relative position of the delay elements. Designed delays are modeled as Pade approximants of the complex exponential,

$$\Delta(s)=\frac{Z(s)}{Z(-s)}=\frac{1-s\tau_e/2}{1+s\tau_e/2} \quad (1)$$

where τ_e represents the equivalent designed delay. Beginning by the first one (figure 1a), the closed loop transfer function is given by (2),

$$A_f(s)=\frac{A_0 Z(-s)e^{-s\tau_i}}{D(s)Z(-s)+GZ(s)e^{-s\tau_i}} \quad (2)$$

where $A(s)=A_o/D(s)$ is the forward gain transfer function (with $D(0)=1$); $G=\beta A_o$ represents the loop-gain; and τ_i represents the intrinsic delay. The cut-off frequency and the maximum flatness condition require the analysis of the magnitude function associated with (2).

$$\left|A_f(jw)\right|=\frac{A_0\left|Z(-jw)\right|}{\left|D(jw)Z(-jw)+GZ(jw)e^{-jw\tau_i}\right|} \quad (3)$$

One important characteristic of equation (3) rises immediately from the fact that $|Z(jw)|=|Z(-jw)|$. This leads to a set of obvious conclusions. Both systems in figure 1 are magnitude indistinguishable. Furthermore, the relative position of the delay elements inside the loop also leads to magnitude indistinguishable forms, irrespective if they figure either on the forward path, or in the feedback path, as long as they are inside the loop. Another important fact is the invariance of the characteristic equation, as long as the number of elements in the loop is maintained (irrespectively to their positions). These two properties, magnitude and characteristic equation invariance contribute to the equivalence between these systems. In this sense, the models depicted in figure 1 are general and equivalent models.

2.1. Maximum Flatness Condition

In order to achieve maximum flatness operation on the frequency response it is necessary to find the limit condition that still confirms the inequality,

$$\left|A_f(jw)\right|^2 \le \left|A_f(0)\right|^2 \quad ,\forall w \ge 0 \tag{4}$$

This condition can be unfastened if we restrict the possible values of frequency to a well defined interval. It was shown in [2] that the magnitude function has a well defined upper bound function. As a consequence, condition (4) must be met only for values of frequency where the upper bound function exceeds $|A_f(0)|^2$. Using the magnitude definition stated in (3), condition (4) takes the new form,

$$\left|D(jw)Z(-jw)+GZ(jw)e^{-jw\tau_i}\right|^2 \ge (1+G)^2\left|Z(-jw)\right|^2 \tag{5}$$

Assuming the forward transfer function is represented by a simple first order system having only one simple pole, $D(s)=1+s/p_1$. After some simple manipulations, condition (5) takes the form of equation (6) below. The new variables result from several variable transformations, namely: α represents the new frequency variable using the transformation $\alpha=w(\tau_i+\tau_e)$; φ and its complement represent the percentages of intrinsic and designed delays relatively to the total delay around the loop ($\varphi=\tau_i/(\tau_i+\tau_e)$); and δ is the pole-delay product given as, $p_1(\tau_i+\tau_e)$. The maximum flatness condition relates all the design variables, for this case, G, p_1, δ and φ. To achieve this condition we followed the method reported in [2]. This method states that, in order to have some prescribed relation between two continuous and differentiable functions over a given interval, it is necessary and sufficient to: i) verify the relation at the beginning of the interval; and ii) to verify the same relation between the function derivatives on the same interval. Applying this procedure iteratively leads to a succession of inequalities. When a constant derivative is found in one of the terms of the inequality, the test at the beginning of the interval reveals maximum flatness condition given by,

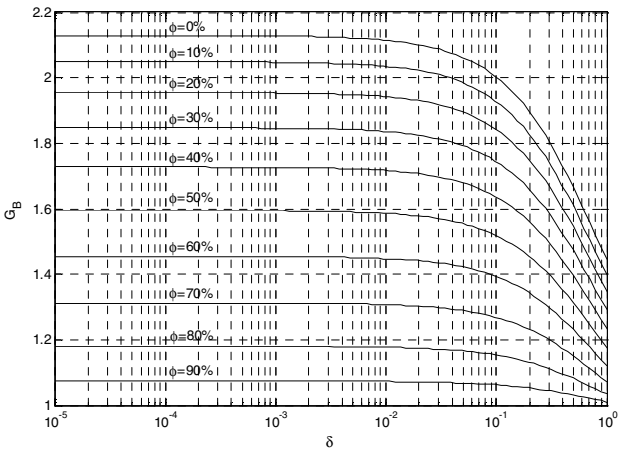

Figure 2 - Bandwidth gain versus pole-delay product

$$G \le 1\Big/\delta\left[2+\delta\left(1+\varphi\bar{\varphi}\right)\right] \tag{7}$$

2.2. Bandwidth Gain

Figure 2 represents the bandwidth gain as a function of the pole-delay product for various values of φ. These gain curves where obtained comparing the bandwidth gains between the system with the total delay (intrinsic and designed) and a system having only the intrinsic delay term (the reference system for each case has no associated delay, thus allowing the definition of bandwidth gain). The reason for this procedure is obvious. Every real amplifier has its internal sources of delay. We used the intrinsic delay term to represent the amplifier's internal delay in order to study its effect on bandwidth gain. On the other hand, the designed delay, represents the added external delay - acting here as an optimizing parameter. Figure 2 shows that for this case: (using a simple one pole forward gain amplifier), the bandwidth gain reaches its maximum value for infinitely small pole-delay products. Furthermore, the maximum bandwidth gain that can be retrieved using a designed delay element depends strongly on the proportion between the intrinsic delay and the total delay (optimized according to (7)). Using the maximum flatness condition, the maximum bandwidth gain reaches 2.1, representing a 110% bandwidth increase.

3. CIRCUIT ARCHITECTURE

The circuit used to validate the proposed model is presented in Figure 3. The designed circuit comprises a total of four stages. It is important that all transistors operate in the active region to avoid transport phenomena, which could increase the intrinsic delay. Using a differential pair as input stage is hence an effective way of guaranteeing a low delay contribution. Transistor Q_3 is used to produce the

$$\frac{\bar{\varphi}}{4\delta^2}\alpha^4+\left(\frac{1}{\delta^2}-\frac{G\bar{\varphi}^2}{2}\right)\alpha^2-2G \ge G\left\{\left[\bar{\varphi}\alpha^2\left(\frac{2}{\delta}+\frac{1}{2}\right)-2\right]\cos(\varphi\alpha)+\alpha\left(\frac{\alpha^2\bar{\varphi}^2}{2\delta}-\frac{2}{\delta}-2\bar{\varphi}\right)\sin(\varphi\alpha)\right\} \quad ,\forall\alpha\in[0,\alpha_H] \tag{6}$$

necessary simulated delay. In accordance with [5], the first order Pade approximant of the complex exponential is implemented using a simple degenerated common emitter stage with enhanced c_μ capacitance. Neglecting the second pole associated with c_π, the transfer function for this stage is given by [5],

$$\frac{V_o(s)}{V_i(s)} = \frac{g_{m1}R_C}{1+g_{m1}R_E} \frac{1-s(C_D+C_\mu)(1+g_{m1}R_E)/g_{m1}}{1+s(C_D+C_\mu)R_C} \quad (8)$$

If the DC gain term is equal to unity, the magnitude of the pole and zero in (8) is the same. Using this condition the resulting delay is determined by,

$$\tau_{2T} = 2R_C(C_D+c_\mu) = \tau_2(C_D)+\tau_2 \quad (9)$$

Where $\tau_2(C_D)$ corresponds to the designed delay, τ_e and τ_2 is part of the contribution of the delay due to the transistor of the second stage to the total intrinsic delay, τ_i. The total intrinsic delay is given by,

$$\tau_i = \tau_1+\tau_2+\tau_3 \quad (10)$$

where τ_k represent the intrinsic delay contribution of each amplifying stage. Transistor Q_4 is necessary to provide the required DC level for the output, in addition, provides high load impedance for the delay stage and small output impedance.

3.1. Delay Optimization

The delay optimization is accomplished using the maximum flatness condition stated in (7). The first step of the optimization procedure begins with the characterization of the open-loop amplifier – it is necessary to measure the loop gain, the open-loop poles and the amplifier's intrinsic delay (using $C_D=0$). The optimum delay is then calculated using equation (7). Figure 4 shows the open-loop small signal equivalent model for the circuit on figure 3. The circuit can be optimized to exhibit one dominant pole due to the input circuitry. For this case, the dominant pole is given by,

$$p_1 = \left[R_i(C_P+C_i)\right]^{-1} \quad (11)$$

where R_i and C_i are the equivalent input resistance and capacitance at the amplifier's input, and C_P may represent the intrinsic capacitance from a photodiode. The loop-gain can be easily computed knowing the voltage gain, A_v of the open-loop amplifier its input resistance, R_i, and the desired feedback resistor, R_F, as in equation (12),

$$G = \frac{R_i}{R_F}(A_v-1) \quad (12)$$

The amplifier's intrinsic delay τ_i, is difficult to calculate. Delays in transistors arise due to transport phenomena in the semiconductor lattices. In general, the simulation models take these effects into account using fitting parameters. For this case we measured the intrinsic delay using transient analysis and sinusoidal input signals with low amplitudes, in order to avoid distortion effects. Finally, the total optimum delay and the percentage of intrinsic delay φ, are calculated using equation (7).

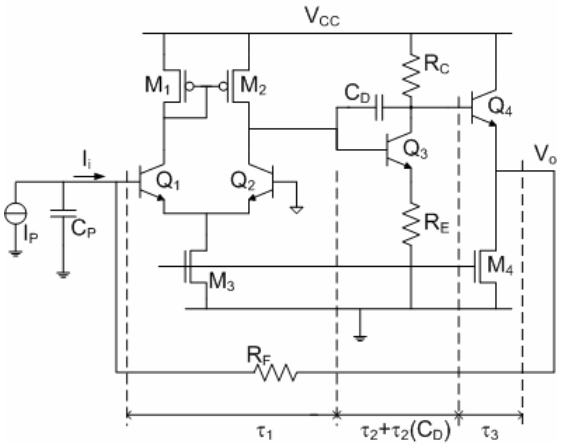

Figure 3 - Circuit conception

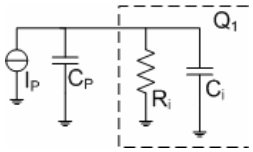

Figure 4 - Input stage equivalent model

Three different case scenarios could arise: i) φ assumes negligible values – this means that the intrinsic delay can be neglected when compared with total delay given by (7). For this case it is possible to explore the maximum bandwidth improvement (110% as stated previously); ii) φ assumes values between 0^+ and 1 – the intrinsic delay represents a substantial fraction of the total delay thus limiting the bandwidth improvement effect; iii) φ assumes values greater than 1 – this means that the desired total delay is less than the intrinsic delay. This is a clear violation of the maximum flatness condition. The best scenario is a frequency response exhibiting peaking behaviors near the cut-off frequency region. However, depending on the amount of the delay, it is also possible to violate the stability restrictions [1]. On the first two scenarios it is possible to optimize bandwidth adding a delay element in the loop. For the third case, compensation may be required. The best solution for compensation is the reduction of the loop-gain, allowing for higher values of the optimum delay. The first two scenarios are more likely to find for operation frequencies below 10GHz, while the third case is of major concern for frequencies above 10GHz even for moderate loop-gain requirements.

4. SIMULATION RESULTS

The circuit of figure 3 was designed using a 0.35μm BiCMOS process from AMS. The circuit was optimized in order to exhibit an open-loop dominant pole behavior, using at its input a photodiode with a (large) equivalent intrinsic capacitance of 150pF. This unusual large value of intrinsic capacitance (even for this scenarios) serves two proposes: i) it establishes that this technique is indeed useful for this kind of applications; ii) and shifts down the dominant pole to a value suitable for this demonstration. The design strategy, sought for high bandwidth operation (using such

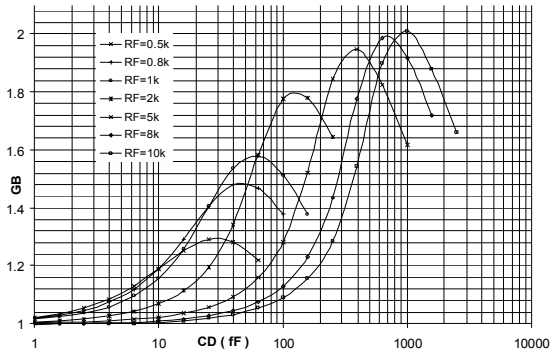

Figure 5 - Bandwidth gain as a function of C_D

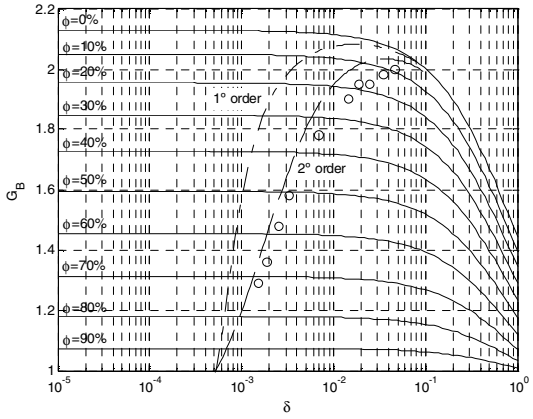

Figure 6 - Bandwidth gain - simulated results comparison

high values of intrinsic capacitance means bandwidths around 50MHz); and high freedom of gain control (imposing stable operation, we achieve a control range from 500Ω to 10kΩ). The gain control feature was used in order to provide a means of simulating equation (7) for different test point examples. The main measured characteristics of the open-loop transimpedance amplifier where: i) intrinsic delay τ_i*=150ps*; ii) first pole p_1*=565 kHz*; iii) second pole p_2*=400MHz*; iv) open-loop transimpedance Z_{OL}*=120dBΩ*. All these characteristics were essentially independent of the loading. Power consumption of the entire circuit was 11mW. The power penalty introduced by the delay stage corresponds only to 3% of the total power consumption of the circuit. The total layout area was 3E-9 m^2, being 25% of this area occupied with the delay stage. However these issues depend strongly on the design considerations.

Figure 5 shows the effect of adding delay to the loop. This was accomplished increasing capacitance C_D for several values of R_F. As can be seen, the bandwidth can be optimized using the proposed scheme. The peaking behavior of these curves suggests that the optimum pole-delay product corresponds to the maximum gain. However, in [2] it was showed that the maximum gain condition implies large overshoot on the frequency response. This was also verified in the present example. Using simulation measurements we select a set of test examples following the maximum flatness criteria. Figure 6 compares the normalized measured results against the proposed model. The dashed line with the '1st order' label, shows what was to be expected from the simple one pole model approximation. It is clear that for this case the simulated results are well far from those predicted. We used a '2nd order' model approximation (including the effect of the second pole). For this case the theoretical predictions were close to the measured data. Both 1st and 2nd order approximations use fixed intrinsic delay. The deviations from figure 2 arise naturally due to the fact that φ varies with δ when the intrinsic delay is fixed. It was also observed that for the 2nd order approximation, the bandwidth gain reduction was more pronounced. This agrees with the bandwidth gain reduction effect observed in second order delayed feedback systems, as reported previously in [1, 2].

5. CONCLUSIONS

A new model suited for delayed feedback analysis has been presented. This model comprised two delay types, intrinsic delays and Pade approximant delays (designed type). Using this approach it is possible to predict and optimize the total delay around the loop, allowing both maximum flatness operation and bandwidth enhancement. Simulation results further validate the results advanced by this model.

The introduction of the pole-zero pair in the system response is explored as an approximation of the ideal delay rather than a classical means of achieving pole-zero compensation schemes. The introduction of positive zero bends the root-locus toward the right half plane, rather than simple cancellation of an existing pole.

Existing deviations from the theoretical predictions are presently a matter of study. We believe that these deviations arise from insufficient detail concerning the open-loop amplifier's characteristics, especially on the intrinsic delay measurement and loading effects.

6. REFERENCES

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