Universidade de Aveiro Departamento de Electrónica, Telecomunicações e Informática
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João Carlos da Silva Carreira

Implementação em hardware de um analisador de espectros baseado em SDR

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Hardware implementation of a spectrum analyzer based in SDR

Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia de Electrónica e Telecomunicações, realizada sob a orientação científica do Professor Doutor Nuno Miguel Gonçalves Borges de Carvalho e do Professor Doutor José Manuel Neto Vieira, Professores do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro

Aos meus pais e ao meu irmão.

o júri / the jury

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Palavras-chave

Analisador de espectros, software defined radio, SDR, arquitecturas de recepção RF

Resumo

A metrologia de rádio-frequência surgiu com as primeiras experiências de sistemas de rádio, pois era importante avaliar as condições em que eram feitas essas experiências assim como avaliar o desempenho dos próprios sistemas. Um dos instrumentos fundamentais na metrologia de rádio-frequência é o analisador de espectros, que tem como principal função apresentar porções do espectro de rádio-frequência, normalmente potência em função da frequência, para posterior análise efectuada pelo utilizador.

Nos últimos tempos temos vindo a assistir a uma revolução ao nível dos sistemas de telecomunicações com o desenvolvimento do conceito de *Software Defined Radio (SDR)*. Com a implementação deste novo conceito pretende-se criar sistemas de rádio reconfiguráveis por software, permitindo-lhes assim uma maior flexibilidade e adaptação às diversas normas de comunicação via rádio-frequência.

Com este documento pretende-se mostrar uma implementação de um analisador de espectros de baixo custo baseado num sistema SDR. Para tal, foi efectuada uma procura por componentes disponíveis no mercado e com base nesta procura decidiu-se implementar este sistema para uma gama de frequências de entrada entre 2.1 GHz e 2.6 GHz e uma frequência intermédia de 100 MHz. Sendo este um sistema de rádio com alguma complexidade, o projecto foi divido em duas partes: software e hardware. Esta dissertação é focada na implementação do hardware.

Keywords Spectrum analyzer, software defined radio, SDR, RF receiver architectures

Abstract

The radio-frequency metrology appeared with the first experiments in radio systems because it was important to assess the conditions under which these experiments were performed as well as to evaluate the performance of the systems themselves. One of the key tools in radio-frequency metrology is the spectrum analyzer, whose main function is to display pieces of the radio spectrum (normally, power as a function of frequency) for further analysis by the user.

In the last years we have been witnessing a revolution in telecommunication systems with the introduction of a new concept: the *Software Defined Radio (SDR)*. With the implementation of this new concept, one intends to create radio systems that are reconfigurable by means of software, giving them a greater flexibility and adaptation to different radio standards.

This document aims to show a possible implementation of a low-cost spectrum analyzer based on an SDR system. To achieve this end, it was performed a search for components that are available in the market and it was decided to implement this system for an input frequency range of 2.1 GHz to 2.6 GHz and an intermediate frequency of 100 MHz. Since this is a radio system with some degree of complexity, the project was divided into two parts: software and hardware. This dissertation is focused on the hardware implementation.

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Acronyms

ADC Analog-to-Digital Converter

ADS Advanced Design System

AGC Automatic Gain Control

ASIC Application-specific Integrated Circuit

BPF Band-pass Filter

CR Cognitive Radio

DAC Digital-to-Analog Converter

DANL Displayed Average Noise Level

DC Direct Current

DFT Discrete Fourier Transform

DR Dynamic Range

DSP Digital Signal Processor

EAGLE Easily Applicable Graphical Layout Editor

FFT Fast Fourier Transform

FPGA Field Programmable Gate Array

FR-4 FR-4 Glass Epoxy PCB substrate

GND Ground

GSPS Giga-Samples Per Second

I/O Input/Output

IC Integrated Circuit

IEEE Institute of Electrical and Electronics Engineers

IF Intermediate Frequency

IMD Intermodulation Distortion

IP3 Third-order Intercept Point

IMR Intermodulation Ratio

ISM Industrial, Scientific and Medical

IT Instituto de Telecomunicações

JTRS Joint Tactical Radio System

LNA Low Noise Amplifier

LO Local Oscillator

LPF Low-pass Filter

MSOP Mini Small Outline Package

NF Noise Figure

P1dB 1 dB Compression Point

PC Personal Computer

PCB Printed Circuit Board

PBAR Policy-Based Adaptive Radio

PLL Phase-locked Loop

RBW Resolution Bandwidth

RF Radio Frequency

RFC RF Choke

RFI Request for Information

RMS Root Mean Square

RSSI Receiver Signal Strength Indication

SCR Software Controlled Radio

SDR Software Defined Radio

SMA SubMiniature version A

SMD Surface Mount Device

SNR Signal-to-Noise Ratio

SOIC Small-Outline Integrated Circuit

SOT Small-Outline Transistor

SR Software Radio

SSOP Shrink Small-Outline Package

TSOP Thin Small-Outline Package

ULP User Language Program

US United States

USB Universal Serial Bus

VCO Voltage-controlled Oscillator

VSA Vector Signal Analyzer

WLAN Wireless Local Area Network

Wi-Fi Wireless Fidelity

Chapter 1

Introduction

1.1 Overview

In the 19th century, James Maxwell predicted the existence of waves of oscillating electrical and magnetic fields, which is now known as electromagnetic radiation. Maxwell published his famous equations, but it was only some years later that his theory was demonstrated experimentally by the physicist Heinrich Hertz. This marks the starting point of radio history. After Maxwell and Hertz, two other individuals, Guglielmo Marconi and Nikola Tesla, stood out in what was called the "wireless telegraphy". The invention of the radio is usually attributed to Marconi, although Tesla had demonstrated the wireless telegraphy before. Despite this claim, Marconi was the first to create a wireless system that was capable of transmitting a signal at long distances. After that, many other people have contributed to bring the radio systems to the level that we know today.

With the development of radio communications, came the need for some instruments that could be used to measure some parameters of the signals transmitted and received by this radio systems, as well as to evaluate the experiments that were taking place in order to develop better radio communications. One of this instruments is the spectrum analyzer which, as the name reveals, is used to analyze the radio spectrum. This instrument became of even great importance with the proliferation of radio communication systems in the late 20th century, where the radio spectrum had become overcrowded with all the different standards and protocols. Today, the spectrum analyzer is one of the fundamental tools in an RF laboratory used to test RF equipment and to develop new prototypes that could improve radio communications. Also, it is of great importance to have a constant monitoring of the radio spectrum for several reasons, including health and fair competition, for example. The agencies that regulate the use of radio spectrum make use of the spectrum analyzer to perform this monitoring, thus reinforcing the importance of this measuring equipment.

As said previously, the radio spectrum is now overcrowded and there is no room for expansion. With the boom of radio communications, many radio standards and protocols were developed and now they have to coexist in the limited radio spectrum. Taking this into account, a new concept of a radio system that is multi-standard, multi-mode and reconfigurable, was introduced by Joseph Mitola in 1991. To this new concept, Mitola gave the

name of Software Defined Radio (SDR). In this technology, the functions of many hardware components are implemented in software, which gives the system a higher degree of freedom to work in multi-standard and multi-mode environments. With SDR technology comes the promise of solving some problems that RF engineers face today. Some of this problems are the overcrowded radio spectrum, the specificity of most RF front-ends that only work with one standard or in a narrow frequency band and the need to implement several RF front-ends in one system in order to provide for communications with more than one standard. However, the concept as Mitola first described is not possible to implement yet, mainly due to restrictions of the current technology of ADCs and DSPs. To solve this problems, approximations to the ideal concept of SDR are being implemented in order to provide current radio systems with new features such as reconfigurability which enable those radio systems to work in a multi-standard environment, for example. Considering all the advantages that SDR promises, this area is receiving much interest from researchers and is regarded as the future of radio communications.

1.2 Objectives

The main goal of this dissertation is to implement a low cost RF front-end that is able to realize spectrum analysis by using a SDR based system. This document is focused on the hardware component, while another dissertation [1] will focus on the software component, as well as the ADC and the USB protocol for connecting the front-end to a PC. Through this dissertation, we intend to study the spectrum analyzer as the tool to perform RF spectrum analysis and to study the concept of SDR and how it can be applied to build a spectrum analyzer. Then, the RF front-end should be developed and implemented in hardware in order to perform tests with that prototype.

1.3 Thesis Outline

This dissertation is organized into seven chapters and two appendices. An insight on this structure will be given in this section.

Chapter 1 presents an introduction to the project, as well as the objectives of this thesis.

In Chapter 2, several architectures of spectrum analyzers will be described. Then, the most widely used architecture is described in more detail, by explaining its theory of operation and its components.

The following chapter, Chapter 3, describes the concept of Software Defined Radio, its advantages and disadvantages, and the possibles architectures. An introduction to the concept of Cognitive Radio is also presented.

In Chapter 4, several receiver architectures will be studied in order to choose the most suitable to implement the RF receiver, that will work as a spectrum analyzer. A more detailed explanation will be provided for the components that are part of the chosen architecture.

Chapter 5 describes the hardware implementation of the receiver, divided into three main sections: RF stage, IF stage and IF filter.

The results achieved with the implemented receiver are presented in Chapter 6.

In Chapter 7, a final conclusion of the work that has been done will be given, as well as some suggestions for a future work.

This thesis will end with two appendices. The first one, Appendix A, contains the detailed explanation as well as the Smith charts used to calculate the matching networks necessary for the mixer. In Appendix B, all the circuit diagrams and the PCB layouts of the implemented hardware are presented.

Chapter 2

The Spectrum Analyzer

2.1 Introduction

The spectrum analyzer is a passive instrument used to display signal information. It is widely used to measure power over frequency, noise and distortion in RF circuits by comparing the input and output signals. In telecommunications, it is frequently used to analyze the RF spectrum to determine the occupied bandwidth of signals, their power and to track interferences [2].

An example of a commercial spectrum analyzer from Agilent[1] can be seen in figure 2.1. These spectrum analyzers are usually very expensive and can cover a large frequency bandwidth, up to 50 GHz.

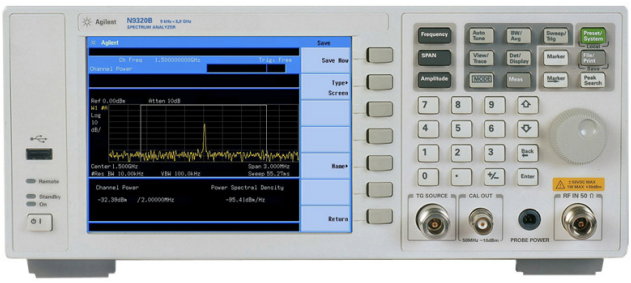


Figure 2.1: Example of a spectrum analyzer from Agilent [3]

2.2 Types of Measurements

The most common measurements that can be made with a spectrum analyzer include power, modulation, distortion and noise.

[1] Agilent Technologies is a spin-off company from Hewlett-Packard which designs and manufactures electronic and bio-analytical measurement instruments and equipment for measurement and evaluation.

Power

The radio spectrum is a limited and shared resource, so it is necessary to regulate and control who can use the spectrum and how it can be used. Here, the power measurement is an important tool used by the agencies that manage and regulate the radio spectrum. While monitoring the spectrum usage, they can measure power over frequency to know if someone is above the maximum limits established in telecommunications standards, for example.

For the manufacturers it is of great importance to measured the transmitted power of their devices, not only to guarantee that it does not exceed the maximum limit allowed by the regulators but also to guarantee a minimum transmitted power so that the signal can reach its destination.

Modulation

The modulation is the process of varying one or more properties of a signal, such as frequency, amplitude and phase, so that it can be physically transmitted. By changing the properties of a signal, it is possible to make it more robust to the adverse conditions of the medium where that signal is being transmitted. Measuring the modulation of a system can be used to check if the information is being properly transmitted.

Common types of modulation measurements are: modulation degree, sideband amplitude, modulation quality and occupied bandwidth.

Distortion

All systems have non-linearities that cause distortion and measuring this distortion is critical for both the receiver and the transmitter. For instance, excessive harmonic distortion in a transmitter can interfere with the signal that carries the information or can interfere with other communication bands. At the receiver, the first stages must be free of intermodulation distortion to prevent crosstalk [2].

Intermodulation, harmonics and spurious emissions are common distortion measurements.

Noise

Noise is present in all active circuits and, in a general way, is unwanted. Measuring noise figure and Signal-to-Noise Ratio (SNR) is important to evaluate the performance of a device and/or its contribution to overall system performance. Actually, noise is often the signal measured in spectrum analysis in order to understand how it can affect a system that is being tested.

2.3 Types of Spectrum Analyzers

There are two main types of spectrum analyzers: the swept-tuned, or superheterodyne spectrum analyzer and the Fast Fourier Transform (FFT) spectrum analyzer [2]. These two architectures will be described in the following sections. There is also another type of modern

spectrum analyzer that combines the advantages of the previous two. It is known as the Vector Signal Analyzer and it will also be described in a later section.

2.3.1 FFT Spectrum Analyzer

The FFT spectrum analyzer, also known as digital spectrum analyzer or simply Fourier analyzer [2], samples the time domain signal and then converts it to the frequency domain using a Discrete Fourier Transform (DFT). After the digitalization of the signal by an Analog-to-Digital Converter (ADC), a Digital Signal Processor (DSP) is used to compute the FFT algorithm. A simplified block diagram of the FFT spectrum analyzer is represented in figure 2.2.

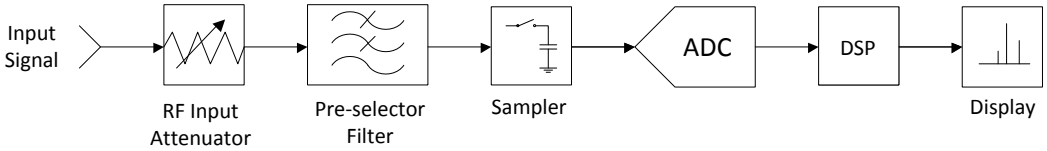


Figure 2.2: Simplified block diagram of a FFT spectrum analyzer

In a Fourier analyzer, the fact that the signal is first digitized and then analyzed enables the signal to be captured in a relatively short time, which can be an advantage. Another advantage of this analyzer regarding the swept-tuned analyzer is the possibility to retrieve the signal's phase.

One of the main disadvantages of this spectrum analyzer is the maximum frequency limit imposed by the ADC. Even today, the ADC's maximum sampling rate isn't sufficient to digitize signals with a high frequency. To convert those signals from analog to digital it is necessary to down-convert them to a lower frequency, which will then impose limits to the bandwidth of the spectrum analyzer. Due to these limitations, the FFT spectrum analyzer is typically used in the analysis of baseband signals.

This architecture requires high performance ADCs which are expensive, so the high cost is another disadvantage of the Fourier analyzer.

2.3.2 Superheterodyne Spectrum Analyzer

The superheterodyne (or swept-tuned) spectrum analyzer is by far the most used type of spectrum analyzer. As the name reveals, this type of spectrum analyzer is based on the superheterodyne principle which enables its operation up to very high frequencies.

Although this type of spectrum analyzer is expensive, the Fourier analyzer is even more expensive for the same performance level, so the superheterodyne spectrum analyzer is often preferred.

The main disadvantages of this type of spectrum analyzer is its inability to measure a signal's phase (it can only measure its amplitude) and the inability to measure transient events effectively because the sweeping of the required bandwidth takes some time.

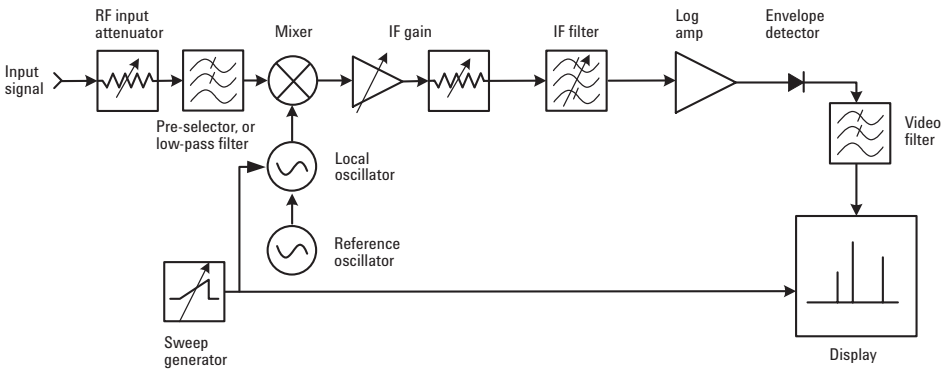


Figure 2.3: Block diagram of a superheterodyne spectrum analyzer, from [2]

A block diagram of the superheterodyne spectrum analyzer is depicted in figure 2.3. This type of spectrum analyzer will be described in detail in section 2.4.

2.3.3 Vector Signal Analyzer

The Vector Signal Analyzer (VSA) is obtained by combining the last two spectrum analyzers technologies. The VSA digitize the time domain signal like the FFT spectrum analyzers, but also uses down-conversion like the superheterodyne spectrum analyzers [4].

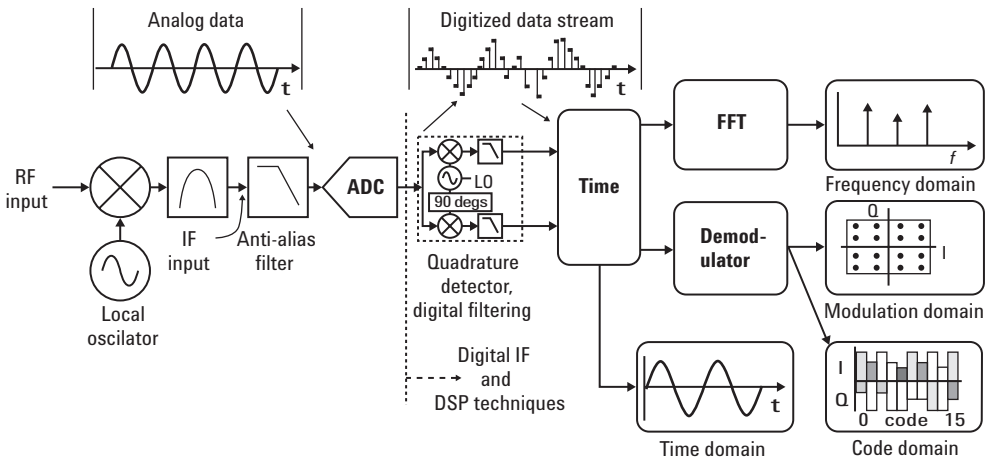


Figure 2.4: Block diagram of a vector signal analyzer, from [4]

The vector signal analyzer is mainly a digital system in contrast to the analog system of the superheterodyne spectrum analyzer. Being essentially a digital system, enables the VSA to perform the same powerful measurements of the Fourier analyzer at very high frequency. The VSA is able to measure phase and to characterize complex signals such as burst, transient or modulated signals [4].

As the signals are becoming more and more complex, this type of analyzer is now a fundamental device in a modern RF laboratory.

A block diagram of the vector signal analyzer is represented in figure 2.4.

2.4 Theory of Operation

This section and the next will focus on the superheterodyne spectrum analyzer, as it is the most used type of spectrum analyzer.

As can be seen in figure 2.3, the major components of the superheterodyne spectrum analyzer are: RF input attenuator, mixer, Intermediate Frequency (IF) amplifier, IF filter, detector, video filter, local oscillator, sweep generator and finally the display.

The input signal passes through the RF input attenuator that will adjust the level of signal incident upon the mixer. This is important to prevent mixer gain compression or distortion due to high-level and/or broadband signals. Between the RF attenuator and the mixer, there is a Low-pass Filter (LPF) used to prevent the higher-frequency signals from reaching the mixer.

In the mixer, the output signal of the LPF is mixed with the signal from the Local Oscillator (LO) to convert it to an Intermediate Frequency (IF), lower than the frequency of the input signal. The mixer is a non-linear device, so its output will include not only the two original signals, but also their harmonics and the sums and differences of the original frequencies and their harmonics. One of the output frequencies (for example, the difference frequency) is the desired signal converted to an IF and the other (sum frequency) is known as *image frequency*.

After the mixer, there is an IF amplifier/attenuator that allows the adjustment of the vertical position of the signal on the display.

Then, to filter the image frequency there is a Band-pass Filter (BPF). This filter has an adjustable bandwidth known as the Resolution Bandwidth (RBW) because it is this filter who will impose the resolution bandwidth of the spectrum analyzer. The selectivity[2] is improved with a narrow RBW, which can also improve the SNR. On the other hand, with a narrower RBW the sweep speed and the trace update rate is degraded.

The signal then passes through the envelope detector to be rectified. This rectified signal is then used to drive the y-axis of the display. Modern spectrum analyzers have digital displays, so the video signal is first digitized with an ADC.

The next element in the block diagram represented in figure 2.3 is the video filter. This filter is a LPF used to smooth the trace seen on the screen.

Finally, the LO is a Voltage-controlled Oscillator (VCO) tuned by the sweep generator. The VCO responds with frequency changes proportionally to the ramp voltage of the sweep generator. It is the sweep generator who creates the frequency domain in the x-axis of the display.

[2]Selectivity is the ability of the receiver to detect the desired signal and reject all the others [5].

2.5 Specifications

When working with a spectrum analyzer it is important to know its specifications. The specifications are a set of requirements that a device should satisfy. For example, if a spectrum analyzer is being used to measure the power of a RF signal, the signal's frequency must be within the frequency range of the spectrum analyzer, otherwise it is referred as being *out of specification*.

The manufacturers usually write in datasheets, user's guide or product brochures the specifications of the spectrum analyzers. That way, the user know if the spectrum analyzer is indicated for the tests and measurement the user pretend to do. Table 2.1 represents various spectrum analyzer's specifications, and is quoted from a Rohde & Schwarz's[3] product brochure [6].

	R&S®FSU3	R&S®FSU8	R&S®FSU26	R&S®FSU 43	R&S®FSU46	R&S®FSU 50
Frequency range	20 Hz to 3.6 GHz	20 Hz to 8 GHz	20 Hz to 26.5 GHz	20 Hz to 43 GHz	20 Hz to 46 GHz	20 Hz to 50 GHz
Reference frequency	aging: 1×10^{-7}/year; with R&S®FSU-B4 option: 3×10^{-8}/year					
Spectral purity						
Phase noise	typ. –133 dBc (1 Hz) at 640 MHz from carrier					
Residual FM	1 Hz					
Sweep time						
Span ≥10 Hz	2.5 ms to 16000 s					
Span 0 Hz (zero span)	1 µs to 16000 s					
Resolution bandwidth	10 Hz to 50 MHz (R&S®FSU43: 10 Hz to 10 MHz), FFT filter: 1 Hz to 30 kHz, channel filter, EMI bandwidth					
Video bandwidth	1 Hz to 10 MHz					
Display range	displayed average noise level to +30 dBm					
Displayed average noise level (10 Hz RBW)						
1 GHz	typ. –148 dBm	typ. –148 dBm	typ. –146 dBm	typ. –146 dBm	typ. –146 dBm	typ. –146 dBm
7 GHz	–	typ. –144 dBm	typ. –146 dBm	typ. –143 dBm	typ. –143 dBm	typ. –143 dBm
13 GHz	–	–	typ. –143 dBm	typ. –143 dBm	typ. –143 dBm	typ. –143 dBm
26 GHz	–	–	–	typ. –138 dBm	typ. –138 dBm	typ. –138 dBm
40 GHz	–	–	–	typ. –133 dBm	typ. –133 dBm	typ. –126 dBm
50 GHz	–	–	–	–	–	typ. –121 dBm
Displayed average noise level with pre-amplifier ON (R&S®FSU-B25), 1 GHz, 10 Hz RBW	<–152 dBm	<–152 dBm	<–152 dBm	<–152 dBm	<–152 dBm	<–152 dBm
Displayed average noise level with pre-amplifier ON (R&S®FSU-B23), 26 GHz, 10 Hz RBW	–	–	<–140 dBm, typ. –150 dBm	–	–	–
Trace detectors	max peak, min peak, auto peak, sample, RMS, average, quasi-peak, CSIPR-AV, CSIPR-RMS					
Total measurement error, f < 3.6 GHz	0.3 dB					
Display linearity	0.1 dB (0 dB to –70 dB)					

Table 2.1: Typical table of specifications from a manufacturer, from [6]

The most important specifications of a spectrum analyzer are: frequency range, frequency and amplitude accuracy, frequency resolution, sensitivity, distortion and dynamic range [7, 8]. These will be explained in the following sections.

2.5.1 Frequency Range

When choosing a spectrum analyzer to perform some measurements, the first specification to know is the frequency range. The spectrum analyzer should cover not only the fundamental

[3]Rohde & Schwarz is a well known German company that manufacture electronic test equipment.

frequency of the signal but also the harmonics. The baseband and IF frequencies are also important, so the spectrum analyzer should be able to measure high frequency signals (RF and harmonics) and at the same time low frequency signals (baseband and IF).

2.5.2 Accuracy

There are two types of accuracy specification: absolute accuracy and relative accuracy. While the absolute measurement is made with a single marker, the relative measurement is made with a delta marker which make this more accurate than the absolute measurement [8]. In spectrum analysis, both frequency and amplitude accuracy are important.

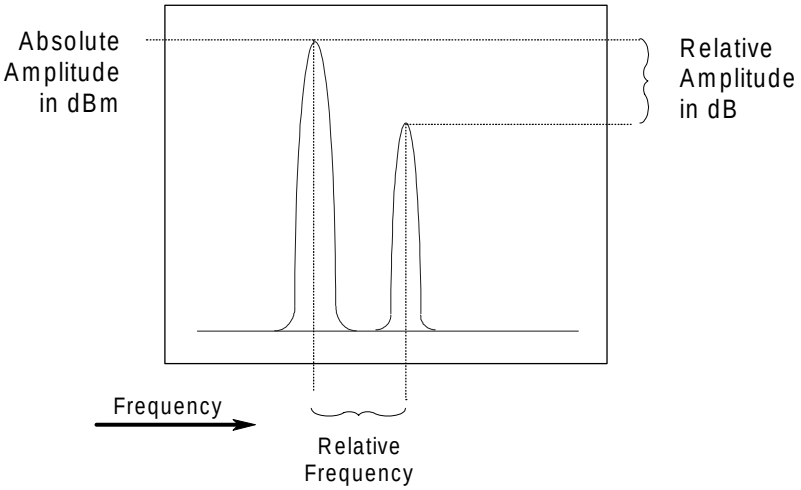


Figure 2.5: Frequency and amplitude accuracy, from [8]

Frequency Accuracy

The frequency accuracy of a spectrum analyzer depends upon several terms, such as the frequency readout, frequency reference accuracy, frequency span, RBW and the residual error. To provide the frequency reference for the spectrum analyzer there is usually a crystal oscillator that has a small variation of frequency with the temperature. This is why modern spectrum analyzers include an oven to control the temperature of the crystal oscillator in order to provide the best frequency accuracy possible.

Amplitude Accuracy

The frequency response and the display fidelity will directly affect the amplitude accuracy of the measurement. There are other items that will also affect the amplitude accuracy, but only if they are changed in the course of the measurement. Some of these item include:

- Variations in the RF input attenuator. Ideally, this element should respond equally to the entire frequency range of the spectrum analyzer, but in practice this does not

occurs. For instance, the IF gain block has a minor contribution to the amplitude accuracy because it operates only at one frequency;

- Variations in the RBW. These variations result from the different insertion losses of the filters used in the spectrum analyzer.
- Calibrator accuracy. The spectrum analyzer must be calibrated, so the calibrator accuracy is relevant to know how the measurement of a signal's amplitude is accurate.

2.5.3 Frequency Resolution

This is a specification of great importance to the spectrum analyzer's user. It tells what is the frequency separation of the two closest signals that the spectrum analyzer can distinguish. If two signals are separated with less than the frequency resolution, the spectrum analyzer can't resolve the two signals, and they will appear in the display as only one signal.

2.5.4 Sensitivity

The sensitivity of a receiver defines the weakest signal level that the receiver can detect to produce a desired SNR [5]. It depends on the temperature, bandwidth of the signal, noise figure of the receiver and the SNR desired. The sensitivity S_i can be defined as:

$$S_i = k \cdot T \cdot B \cdot NF \cdot SNR \ \ [\mathrm{W}] \tag{2.1}$$

where $k = 1.38 \times 10^{-23} JK^{-1}$ is the Boltzmann's constant, T is the equivalent noise temperature in Kelvin, B is the bandwidth of the signal, NF is the noise figure of the receiver and SNR is the signal to noise ratio.

At room temperature ($T = 290$K), kT is equal to -174 dBm/Hz, so equation (2.1) can be re-written as:

$$S_i = -174 \text{ dBm/Hz} + 10\log(B) + NF \text{ dB} + SNR \text{ dB} \ \ [\text{dBm}] \tag{2.2}$$

Another specification of a spectrum analyzer that is related to the sensitivity is the Displayed Average Noise Level (DANL). This is the term for the noise floor of the spectrum analyzer, in a particular bandwidth and represents the best-case sensitivity of the spectrum analyzer in that bandwidth. This best-case sensitivity is achieved when there is minimum RF input attenuation and the RBW is the narrowest possible.

2.5.5 Distortion

The spectrum analyzer is often used to measure signal distortion, but its components also add some distortion. For instance, the mixers are non-linear devices that will generate internal distortion and in the worst case scenario, this internal distortion can cover up the signal's distortion we want to measure. Therefore, this specification is very important and is specified by the manufacturer.

This specification, particularly the Intermodulation Distortion (IMD), will be discussed later in section 4.5.2, where the IP3 figure of merit will be presented.

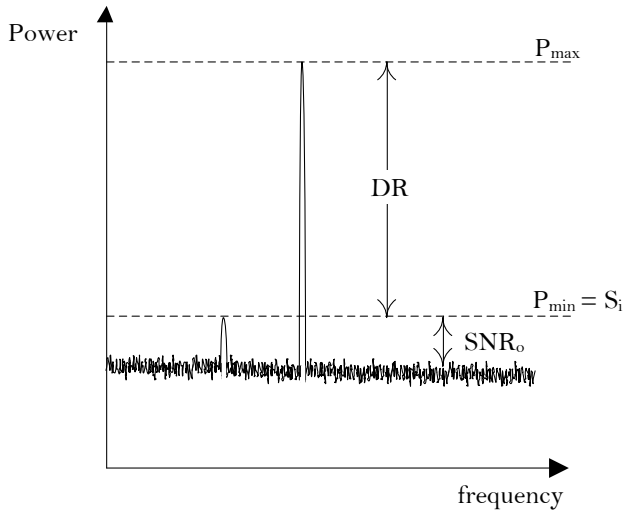


Figure 2.6: Sensitivity and dynamic range

2.5.6 Dynamic Range

Dynamic range is, by definition, the maximum ratio of two signal levels simultaneously present at the input of the spectrum analyzer that allows the signals to be measured to a given degree of uncertainty [2]. Graphically, it is determined in a spectrum analyzer's display like the one depicted in figure 2.6, where the dynamic range is represented as *DR*, the difference between the maximum signal and the minimum signal at the input.This specification is expressed in dB by the manufacturers since it is a ratio between two signal powers.

Chapter 3

Software Defined Radio

3.1 Introduction

In the early 1990s, Joseph Mitola introduced the concept of Software Defined Radio (SDR). He described SDR as:

> *"A software radio is a radio whose channel modulation waveforms are defined in software. That is, waveforms are generated as sampled digital signals, converted from digital to analog via a wideband Digital-to-Analog Converter (DAC) and then possibly upconverted from IF to RF. The receiver, similarly, employs a wideband ADC that captures all of the channels of the software radio node. The receiver then extracts, downconverts and demodulates the channel waveform using software on a general purpose processor."* [9]

In other words, the concept of SDR proposes that the digital-to-analog conversion (in the transmitter) and the analog-to-digital conversion (in the receiver) is performed as close as possible to the antenna.

The ideal SDR transceiver is depicted in figure 3.1. The filters, mixers, modulators or demodulators and others, are implemented in software using a DSP. This provides the system with flexibility because it only requires switching the software in order to adapt the system to another standard.

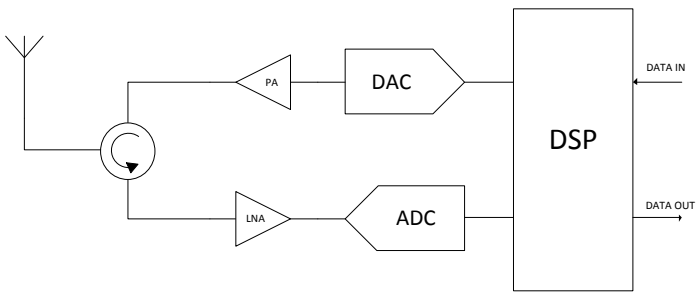


Figure 3.1: Ideal SDR concept

Although Joseph Mitola coined the term Software Defined Radio in 1991, the concept of a reconfigurable, multi-mode and multi-band system was introduced several years before, in the 1970s, by the US military with a project called Speakeasy [10]. The purpose of Speakeasy was to emulate several military radios into one unique radio by using programmable processing. This project was a success in creating a software-defined radio capable of emulating more than 10 different military radios that operated from 2 MHz to 2 GHz. Although the Speakeasy was portable, it was not a handheld radio.

With the conclusion of the Speakeasy project, a new project named Joint Tactical Radio System (JTRS) was born [11, 12]. This radio system is planned to be the next-generation radio used by the US military and can be seen as an improvement of Speakeasy project. It provides the capability to communicate with systems that use similar or diverse waveforms, which gives the military flexibility to communicate with different standards while maintaining the interoperability between new and old radio systems. Also, the JTRS is planned to help reducing costs in the fields of operation, training and maintenance.

Nowadays, there is an even greater need for a unique multi-standard and multi-mode hardware platform that is re-programmable and reconfigurable by software. This need comes from the excess of mobile system standards enhanced by the rapid growth occurred in the telecommunications world since the massive use of cellphones. One porpuse of SDR is to solve this problem, but unfortunately the ideal concept is very difficult to implement at this time or even in the nearest future, due to the restrictions imposed by the state-of-art hardware, such as the antenna, the ADC/DAC or the DSP [13].

An SDR system should have one or more of the following characteristics [14]:

- a transceiver architecture that can be controlled and programmed by software;
- radio functions mainly implemented in DSP;
- re-programmability via air interface;
- support for multi-standards and multi-mode.

3.2 Front-End Receiver Architectures

As the ideal SDR represented in figure 3.1 is not possible to implement at the present time, other architectures have to be considered to implement SDR. These architectures differ in the place where the digitalization occurs, so three types of configurations will be considered: baseband digitalization, IF digitalization and RF digitalization. These configurations will be presented over the next subsections.

3.2.1 Baseband Digitalization

In the baseband digitalization, the ADC is placed in the baseband stage and the signal suffers two down-conversions before reaching the baseband frequency, as depicted in figure 3.2.

Although this architecture is widely used in radio receivers, it is not suitable for SDR. Because it is an architecture that is designed for narrowband porpuse, it goes against one of

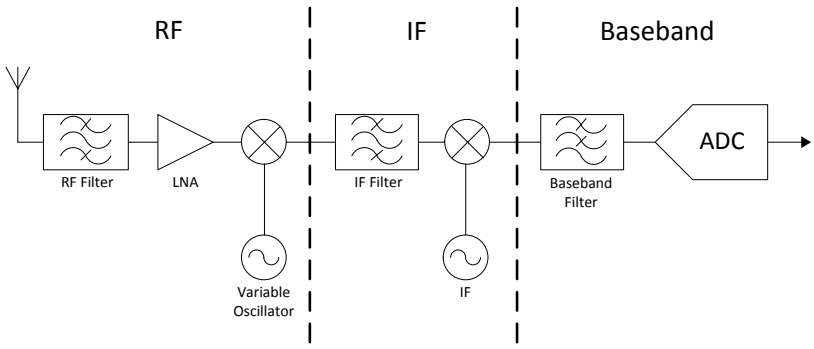


Figure 3.2: Baseband digitalization architecture

the objectives of an SDR system, which is to be broadband. Another problem is the number of components required by this architecture, which make the integration of the system in a single Integrated Circuit (IC) difficult to implement.

3.2.2 IF Digitalization

In this approach, the ADC is now placed in the IF stage. This allows for a wider bandwidth when compared to the previous architecture, thus making this implementation closer to the ideal SDR. Now, the received band can be wider, and since the digitalization is done at IF, digital filters and further processing can be used for channel selection. This architecture allows for more standards to be implemented and it is suitable of being realized with the components currently available. That is the reason why this architecture is the most feasible and preferred to implement a SDR system these days.

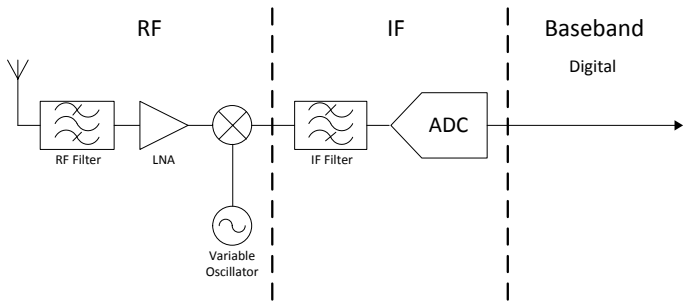


Figure 3.3: IF digitalization architecture

3.2.3 RF Digitalization

By moving the ADC closer to the antenna once more, the digitalization is now performed at RF. This is the final architecture of the evolution of SDR and is the one proposed by Joseph Mitola as the ideal SDR architecture, but unfortunately is still utopical. The ADC must have both high dynamic range and high sampling ratio, preferably with a large number

of resolution bits. Nowadays, there are high-speed ADCs that can achieve high sampling rate with a fair number of resolution bits, but they are too expensive. For instance, one of the best ADCs in the market is manufactured by National Semiconductor[1] and has a sampling rate of 3.6 GSPS with 12 resolution bits [15], costing over $3,000, which is too expensive for commercial applications.

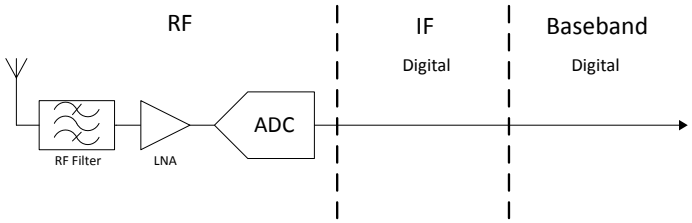


Figure 3.4: RF digitalization architecture

A lot of research is yet to be done in the field of ADCs and DSPs in order to implement the RF digitalization. For now, the most feasible implementation for a SDR system is the IF digitalization which is still somewhat expensive for high IFs.

3.3 SDR Concerns

One of the key components in SDR is the ADC. The most important parameters of an ADC are the sampling rate, the number of bits (resolution) and the dynamic range. Advances in this area allowed the ADC to move from baseband to IF, sampling the signal at higher frequencies. As stated before, there are now in the market high speed ADCs with sampling rates of GSPS but they are too expensive and are not feasible for implementation in commercial applications where the end user normally want low cost systems. Another drawback is the power consumption because the higher the speed of the ADC, the higher the power consumption will be. This limits the application of these ADCs because one important characteristic of a radio system is its portability, which would be limited through battery life. That is why the current research on ADCs focus in increasing sampling rate and reducing power consumption.

The processing unit is also of great importance in an SDR system. This unit has to keep up with the speed of ADC to be able to process all the digital signal. An ASIC can perform this processing with good performance and high speed; however, it is limited to the functionalities for which it was design. In an SDR system this is not very useful because it does not provide the system with the desired reconfigurability. Currently, this processing is mainly done with DSPs, which have lower performance than ASICs but can provide the system with more flexibility.

[1]National Semiconductor is a company founded in 1959 that designs and produces integrated circuits, such as amplifiers, data converters, etc. It has more than 10,000 products and a number of patents that exceeds 3,000. It has reported $1.42 billion in sales for fiscal 2010.

Both ASICs and DSPs have pros and cons and in an attempt to conjugate the pros of both components, the FPGA arises. An FPGA is an IC that is designed to be reconfigurable and reprogrammable and is able to perform complex operations such as the ones performed by an ASIC. For its characteristics, the FPGA is a desired component for an SDR system, but this comes with a price. The FPGAs are usually very expensive compared to ASICs or DSPs.

3.4 Cognitive Radio

With the concept of SDR, Joseph Mitola came up with a new idea, the Cognitive Radio (CR) [16]. This new concept can be viewed as an upgrade of SDR, because it is an intelligent radio that is aware of the environment in which it is inserted, that is, location and utilization of the RF spectrum. Therefore, the CR can make decisions based on the knowledge acquired by itself in order to give the best communications experience to end-users. While doing this, the CR must be fair with other users and obey to the basics rules of RF spectrum sharing.

The CR should be able to operate in a wide range of frequencies, have support for multi-standard and multi-mode and be re-programmable, just like an SDR. The advantage of CR over SDR is the capability of making decisions for itself.

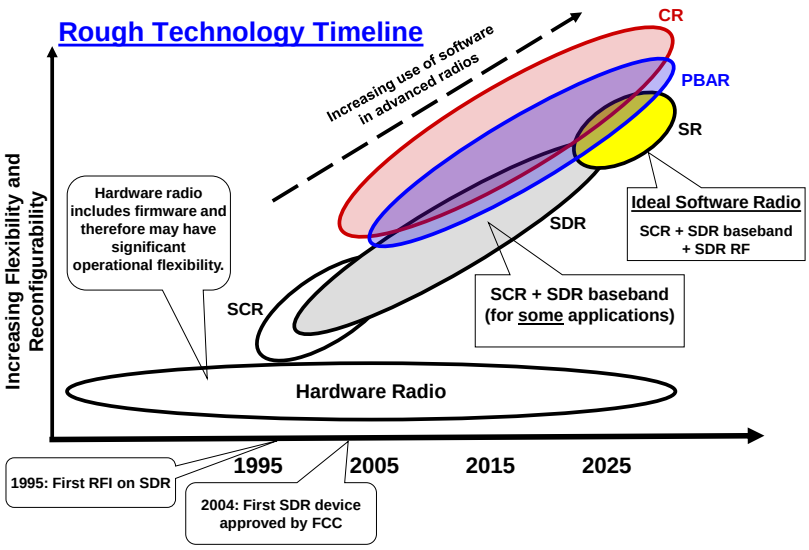


Figure 3.5: Radio technology time evolution, from [17]

For a better understanding of this concept, let's take an example of a CR that is using Wi-Fi. While monitoring the RF spectrum, the CR detects that the channel used is too crowded with other users, so in order to avoid interference and to improve the quality of the communication the CR automatically changes to another frequency channel that is less occupied. The user is unaware of that change because this process is totally transparent to the end-user.

At the beginning, the CRs and SDRs may be expensive due to the high performance components required, but with the advance of technology and mass production the cost of this type of radios would become less expensive to the end-user, allowing for better communications. In figure 3.5 it is represented the expected evolution of the radio technology, predicted by Hoffmeyer [17]. With this in mind, it can be said that the future of radio communications will pass through SDRs and CRs!

Chapter 4

Receiver Architecture

4.1 Introduction

Due to the analog nature of the air interface where the radio waves propagate, a Software Defined Radio will always have an analog front-end to receive the radio signals called the RF receiver. This is an electronic circuit whose purpose is to receive a RF signal and to perform some operations with that signal, such as amplification, filtering and frequency mixing. The objectives of the receiver RF front-end are [5]:

- capture the desired signal while rejecting unwanted signals;
- convert the signal's center frequency to a range that is compatible with the ADC. This should be performed with minimal distortion;
- amplify the signal to match the level required by the ADC;
- minimize the noise added while performing amplification and frequency mixing.

This chapter is intended to describe some receiver's architectures and to compare the advantages and disadvantages of these architectures in order to find the best suitable architecture for SDR receiver.

4.2 Direct Conversion Architecture

In a direct conversion receiver, the received signal is down-converted directly to the baseband using a mixer and a local oscillator. Because the frequency of the local oscillator is set to the same frequency of the desired input signal, this type of receiver is also called a homodyne receiver [18]. A block diagram of this type of receiver is presented in figure 4.1.

In this receiver, the input signal is filtered in order to attenuate undesired signals and is amplified in a LNA. Then, a mixer and a LO are used to down-convert the signal directly to baseband. Two signals will then appear at the output of the mixer: one is the baseband signal and the other is a signal whose frequency is twice the frequency of the input signal.

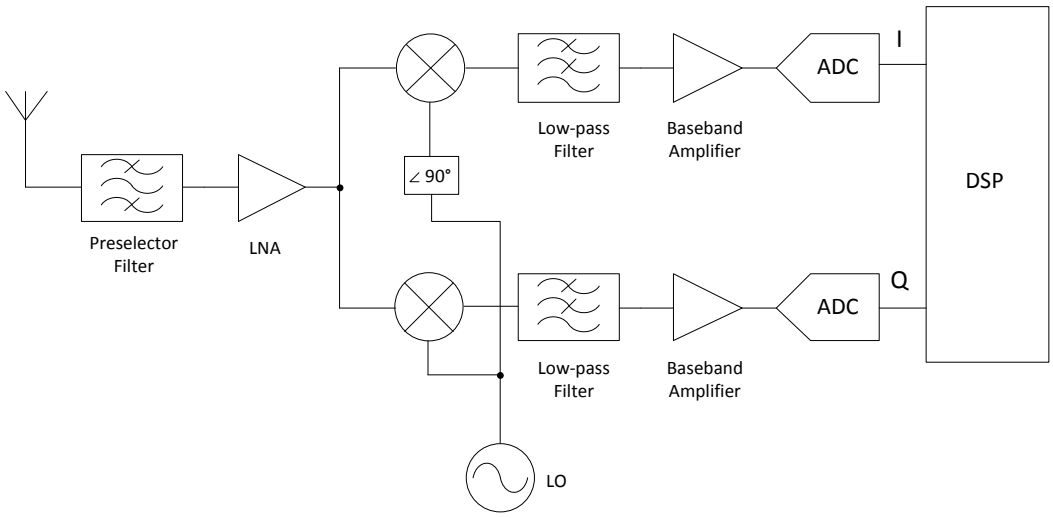


Figure 4.1: Block diagram of a direct conversion receiver

This last signal is also known as the *image frequency* signal and to remove it a low-pass filter is used. Later, the wanted signal is amplified in order to fit in the ADC's dynamic range.

The advantages of this receiver, when compared to a multiple conversion receiver, are [18, 19, 20]:

- low complexity;
- simple filtering requirements;
- easier image frequency suppression.

As this receiver doesn't have an IF, it is simpler and less costly than a multiple conversion receiver. The low-pass filter in the baseband stage is also easier to implement than a narrow band-pass filter required at the IF stage of a multiple conversion receiver.

Despite this advantages, there are some disadvantages that makes the direct conversion receiver difficult to implement, such as [18, 19, 20]:

- LO drift;
- DC offset;
- LO-to-RF and RF-to-LO leakage;
- ADC sampling rate.

The LO must be of high precision and stability so that the desired RF signal is correctly down-converted to the baseband. The Direct Current (DC) offset is another major problem in a homodyne receiver. This can occur if the LO signal leaks to the input of the LNA because the LO and the RF frequencies are equal. The RF signal usually has a very low power when

compared to the LO signal and if this leakage occurs, the LO signal is mixed with itself to produce a DC voltage that will be present at the input of the baseband amplifier.

In the past, one of the biggest obstacles to implement this type of receiver was the low sampling rate and resolution of the ADCs. As stated in subsection 3.2.3, in the present time there are high-speed ADCs that can achieve high sampling rate with a fair number of resolution bits, but they are too expensive.

The homodyne architecture enables wideband signals to be received [13], which is an important feature of an SDR receiver, but the limitations described above makes this type of receiver to be difficult to implement with low cost components, because it requires expensive components (such as a very stable LO).

4.3 Multiple Conversion Architecture

In the multiple conversion receiver, the desired signal is firstly down-converted to an intermediary frequency before it is down-converted to baseband. This type of receiver is known as a superheterodyne receiver, and in the figure 4.2 it is represented a superheterodyne with two down-conversions.

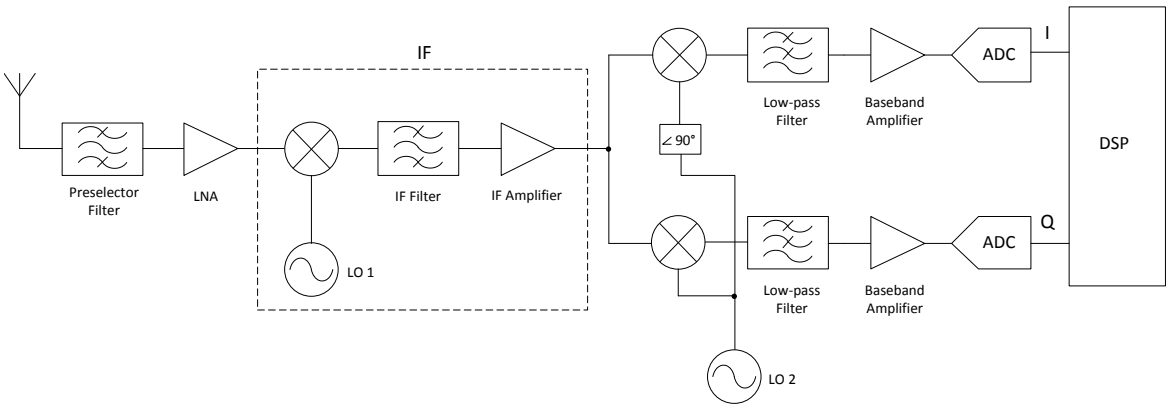


Figure 4.2: Block diagram of double conversion receiver

Despite having its own disadvantages, this type of receiver can overcome the main problems of the homodyne architecture. This is one of the reasons why nowadays the superheterodyne receiver is used in the majority of the communications systems, such as cellular telephone systems, data communication systems and radar systems [18].

As can be seen in the figure 4.2, the first stage is similar to the direct conversion receiver. The main difference is that in the multiple conversion receiver there is an intermediary stage between the RF and the baseband stages. One problem that arises with this architecture is the presence of an *image frequency* at the output of the first mixer. In order to prevent this signal from reaching the second mixer, the IF band-pass filter should have a narrow bandwidth. This type of filter is more difficult to implement than the low-pass filter required in the direct conversion receiver, so this is a disadvantage of this architecture.

A superheterodyne receiver has a better performance than a homodyne receiver because it does not suffer from the problems caused by DC offsets and self-mixing at the input of the mixers. However, the incapability of dealing with wideband signals [13] dictates that this architecture is not suitable to use in a SDR system.

4.4 Low IF Architecture

To overcome the problems in the two architectures presented before, it was developed another architecture [21, 20] that combine the best features of the two presented above. The conversion from analog to digital is done at IF instead of being done at baseband, so there is no problem with DC-offset because the wanted signal is not located around DC. Also, the LO frequency is not equal to the RF carrier signal, so the LO-to-RF and RF-to-LO isolation is not as important as the one needed in the homodyne receiver.

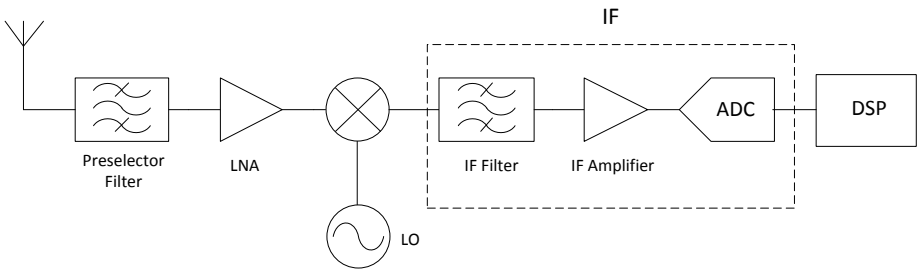


Figure 4.3: Block diagram of low IF receiver

As can be seen in figure 4.3, the ADC is placed in the IF stage closer to the antenna than in the other two architectures. This architecture is suitable to be used in a SDR communication system and it is a close approach to the ideal SDR receiver (figure 3.1). For this reason, the low IF architecture was the one chosen to implement the front-end of the spectrum analyzer.

4.5 Figures of Merit

To better understand the operation of the RF receiver, some important figures of merit that characterize the elements used in the receiver will be explained in the following subsections. These figures of merit are: Noise Figure (NF), Third-order Intercept Point (IP3) and 1 dB Compression Point (P1dB).

4.5.1 Noise Figure

The Noise Figure (NF) is an important figure of merit, specially for the LNA. It is defined as [22]:

$$NF = \frac{SNR_i}{SNR_o} \tag{4.1}$$

where SNR_i is the signal-to-noise ratio of the input and SNR_o is the signal-to-noise ratio at the output.

The NF is a measure of the degradation in SNR between the input and output ports of the device. A RF receiver is composed by several devices, so in order to calculate the overall noise figure of the receiver, the following equation is used:

$$NF_T = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 \cdot G_2} + \frac{NF_4 - 1}{G_1 \cdot G_2 \cdot G_3} + ... \tag{4.2}$$

where NF_n is the noise factor of each stage and G_n is the numerical gain of each stage (not in dB).

This expression and its deduction can be found in [23], and in many other books about RF. Equation 4.2 shows that the first stage is the one who has a larger contribution to the total NF of the system, and this is the reason why the first amplifier of the receiver must have a low noise figure.

4.5.2 Third-order Intercept Point

Another important figure of merit is the Third-order Intercept Point (IP3). This parameter is related with the linearity and is used to calculate the Intermodulation Distortion (IMD).

Intermodulation products are a source of distortion in non-linear devices. Even devices that are assumed to be linear, can have non-linearities in certain conditions of operation. For example, when two RF signals with the same amplitude are applied to the input of the mixer,

$$v(t) = A \cos 2\pi f_1 t + A \cos 2\pi f_2 t \tag{4.3}$$

the output voltage can be represented as the power series:

$$v_o(t) = a_1 v(t) + a_2 v^2(t) + a_3 v^3(t) \tag{4.4}$$

This output signal will contain several frequency components, where the most important are presented in table 4.1 and are shown graphically in figure 4.4. Placing two sinusoidal signals at the input of a device while reading the response at the output is a common test that is done to characterize and understand how the device works; this is known as the *two tone test*.

In figure 4.4, we can see that the IMD products will appear inside the bandwidth. Because of this, the removal of these frequency components is very difficult to do with a simple filter. Another problem of IMD is that the two can mask the desired signal if their power is sufficiently high.

As an example, when measuring the output power of the third-order intermodulation product $P_{2f_1-f_2}$ versus the input power P_{f_1}, we obtain the graphic shown in figure 4.5. The slope of the fundamental output power is 1 dB/dB and the slope of the IMD products output power is 3 dB/dB. This occurs because the power of the third-order IMD is proportional to the cube of the input signal (equation 4.4). By definition, the third-order intercept point is the point where the extrapolated lines P_{f_1} and $P_{2f_1-f_2}$ intersect each other. This is a conceptual point that does not exist in reality because at very large signal levels, both curves

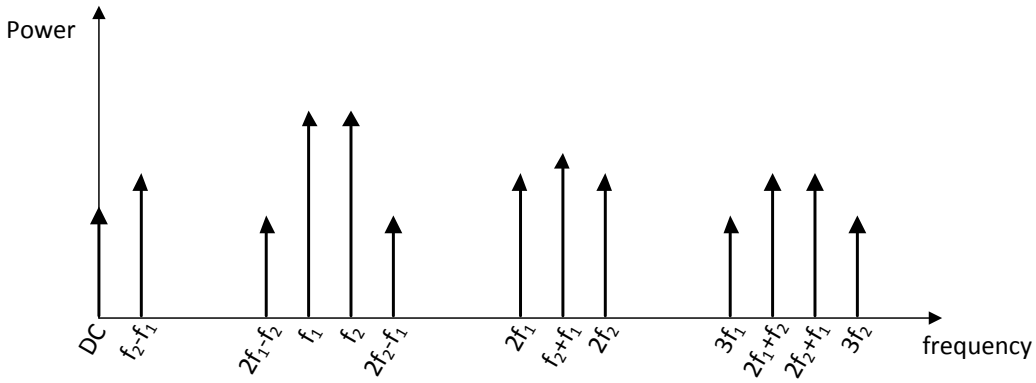


Figure 4.4: Input and output of a two tone test

Description	Frequency component
Component resulting from $f_1 - f_1$ and $f_2 - f_2$	DC
f_1 fundamental frequency	f_1
f_2 fundamental frequency	f_2
f_1 second harmonic	$2f_1$
f_2 second harmonic	$2f_2$
f_1 third harmonic	$3f_1$
f_2 third harmonic	$3f_2$
Second-order intermodulation products	$f_2 \pm f_1$
Third-order intermodulation products	$2f_1 \pm f_2$
Third-order intermodulation products	$2f_2 \pm f_1$

Table 4.1: Output frequency components from a two tone test

tend to compress towards a constant value of output power due to the contribution of higher order terms [24].

Another important figure of merit directly related with intermodulation distortion is the Intermodulation Ratio (IMR), which is defined as the ratio between the fundamental output power and the IMD output power:

$$\text{IMR} = \frac{P_{f_1,o}}{P_{2f_1-f_2,o}} = \frac{P_{f_2,o}}{P_{2f_2-f_1,o}} \tag{4.5}$$

or in dB units:

$$\text{IMR}_{dB} = P_{f_1,o}\ (\text{dBm}) - P_{2f_1-f_2,o}\ (\text{dBm}) = P_{f_2,o}\ (\text{dBm}) - P_{2f_2-f_1,o}\ (\text{dBm}) \tag{4.6}$$

In figure 4.6 is represented a typical spectrum analyzer's display when a two tone test is

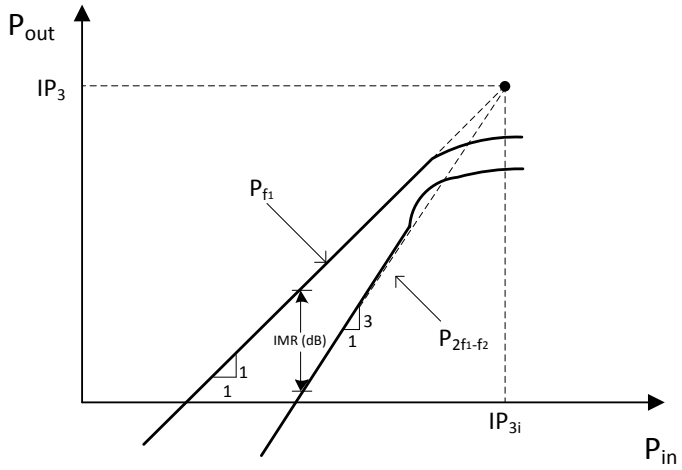


Figure 4.5: Third-order intercept point

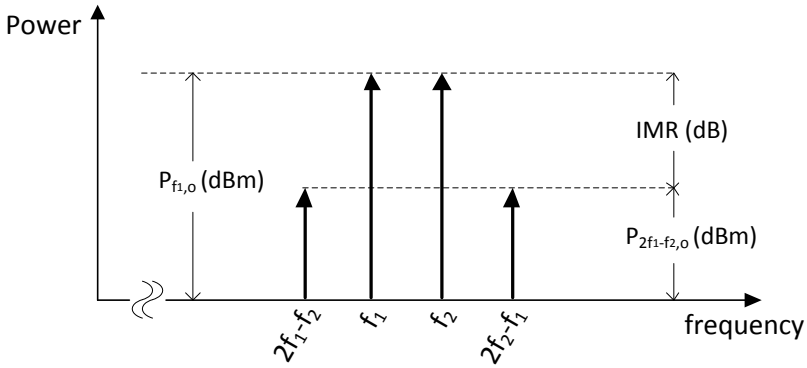


Figure 4.6: Two tone test: measuring IP3 with a spectrum analyzer

being performed in a RF device. Using this display of the spectrum analyzer, the IP3 can be calculated as:

$$\text{IP3 (dBm)} = P_{f_1,o} \text{ (dBm)} + \frac{\text{IMR}_{dB}}{2} \tag{4.7}$$

From (4.7) it can be observed that, for the same $P_{f_1,o}$ value, the higher the IP3 is, the higher, and therefore better, the IMR will be.

4.5.3 1 dB Compression Point

As seen before, in the linear zone of an amplifier the output power raises 1 dB for each dB raised in the input power, for the fundamental frequency. However, the amplifier cannot maintain this ratio indefinitely and there is a certain point where the amplifier saturates and starts to compress the signal. This point is typically specified as the 1 dB Compression Point (P1dB) by the manufacturers and is defined as the value of output power at which the

output signal is compressed in 1 dB compared to the extrapolated line of the small-signal characteristic of the linear system [24].

This is an important figure of merit for amplifiers because they have to be kept working far from this point, otherwise the amplifier could enter in the non-linear zone adding more distortion to the system where the amplifier is inserted. Figure 4.7 represents an example of a P1dB measurement.

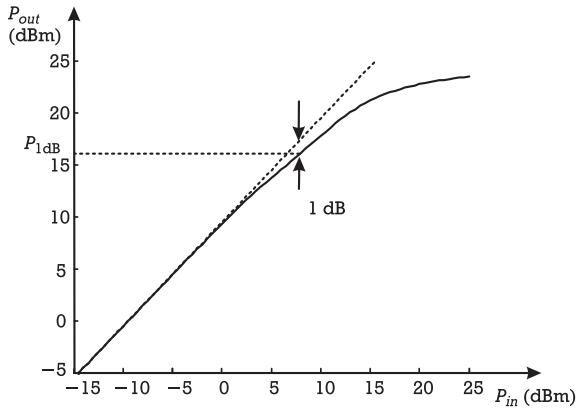


Figure 4.7: Example of a P1dB measurement, adapted from [24]

Chapter 5

Implementation

5.1 Introduction

In this chapter, the implementation of the receiver's hardware will be explained. The components chosen will be presented, as well as the reasons why they were chosen. Also, the electric diagrams and the Printed Circuit Board (PCB) layouts will be presented.

While studying the best approach to implement the receiver, it quickly became clear that if the hardware was divided in various boards, instead of being only one, the implementation and testing of the hardware would become easier. For that reason, it was decided to divided the receiver in four stages, as represented in figure 5.1:

- The antenna and the pre-selector filter;
- The RF stage, with the LNA, the mixer and the frequency synthesizer;
- The IF filter;
- The IF stage, with the IF amplifier and the power detector.

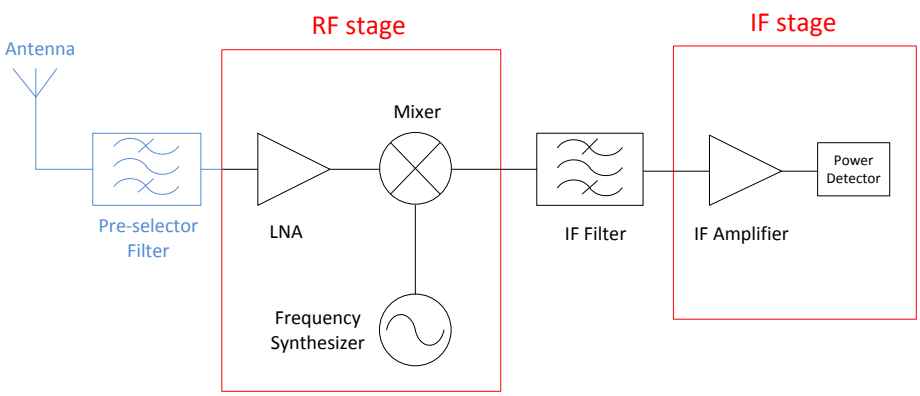


Figure 5.1: Block diagram of the receiver

This thesis work has focused on the RF stage, the IF stage and the IF filter, so this chapter will explain the implementation of these stages. The antenna and the pre-selector filter weren't implemented, so they will not be referred in this chapter.

5.2 RF stage

The RF stage is composed by one LNA, one mixer and one frequency synthesizer. This stage will receive an input frequency of 2.1 GHz to 2.6 GHz (RF frequency) and will have an output frequency of 100 MHz (IF frequency).

These components work at RF and IF frequencies and they will need impedance matching circuits for the inputs/outputs as well as bias circuits to provide the supply power needed. Therefore, a diagram of the implementation of this stage is presented in figure 5.2.

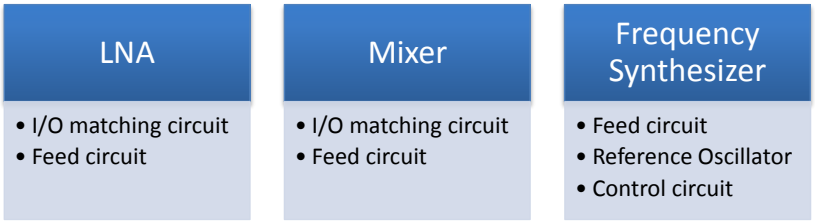


Figure 5.2: Implementation diagram of the RF stage

5.2.1 Frequency Synthesizer

The frequency synthesizer will be the first one explained here because it was the choice of this component that limited the frequency range of the RF signals.

The frequency synthesizer consists of two main components: a Phase-locked Loop (PLL) and a VCO. Attending to this information, the frequency synthesizer could be bought as one monolithic IC or it could be realized with a PLL and a VCO. To implement a simple and low cost receiver, is was decided to buy the frequency synthesizer as one monolithic IC.

From the beginning it was intended that the frequency synthesizer could generate a wide range of frequencies around the ISM band of 2.4 GHz to 2.5 GHz, because this is the frequency range used by many communication standards, such as IEEE 802.11 (Wi-Fi, WLAN), IEEE 802.15.4 (ZigBee) and Bluetooth. The characteristics wanted in the frequency synthesizer are:

- **low supply voltage**, preferably 3V, 3.3V or 5V because these are common supply voltages found in many circuits;
- **low supply current**, for low power consumption;
- frequency range that includes frequencies from **2.4 GHz to 2.5 GHz**;

- **SOT, TSOP, SOIC** or similar SMD package. Because the assembly of the components in the PCB will be made at Instituto de Telecomunicações (IT), the choice of SMDs are limited to the packages that can be assembled there.

While conducting a search for a frequency synthesizer that complies with the desired characteristics, the **Si4136** frequency synthesizer from Silicon Labs was found. This frequency synthesizer features [25]:

- 2.7V to 3.6V supply;
- 25.7 mA typical supply current;
- Dual-band RF synthesizers:
  - RF1: 2300 MHz to 2500 MHz;
  - RF2: 2025 MHz to 2300 MHz;
- IF synthesizer (62.5 MHz to 1000 MHz);
- `RFOUT` = -3.5 dBm;
- Integrated VCOs, loop filters, varactors and ressonators;
- Minimal external components required;
- 24-pin TSSOP package.

Assuming an IF of 100 MHz, with this frequency synthesizer it is possible to have RF input signals from 2125 MHz to 2600 MHz. This will be the frequency range of the RF signals and this will limit the choice of the LNA and the mixer.

The functional block diagram is represented in figure 5.3. At pin `XIN`, an oscillator should be connected to provide the frequency reference for the PLLs. Pins $\overline{\texttt{PWDN}}$, `SDATA`, `SCLK` and $\overline{\texttt{SEN}}$ are used for control and programming of the synthesizer while pin `AUXOUT` is used for synthesizer testing. `RFOUT` and `IFOUT` pins provide the generated RF and IF frequencies, respectively. Pins `IFLA` and `IFLB` are part of the IF synthesizer, so they are not relevant for this work.

The frequency synthesizer is programmable through a three-wire serial interface, but the programing of this device is beyond the scope of this dissertation, which is only focused on the receiver's front-end, from the LNA to the power detector. The ADC and the software implementation is presented in [1].

Reference Oscillator

As indicated in the datasheet [25], the frequency synthesizer Si4136 requires an external reference oscillator connected to pin `XIN`. The minimum input frequency in the `XIN` pin is 2 MHz and the maximum is 50 MHz.

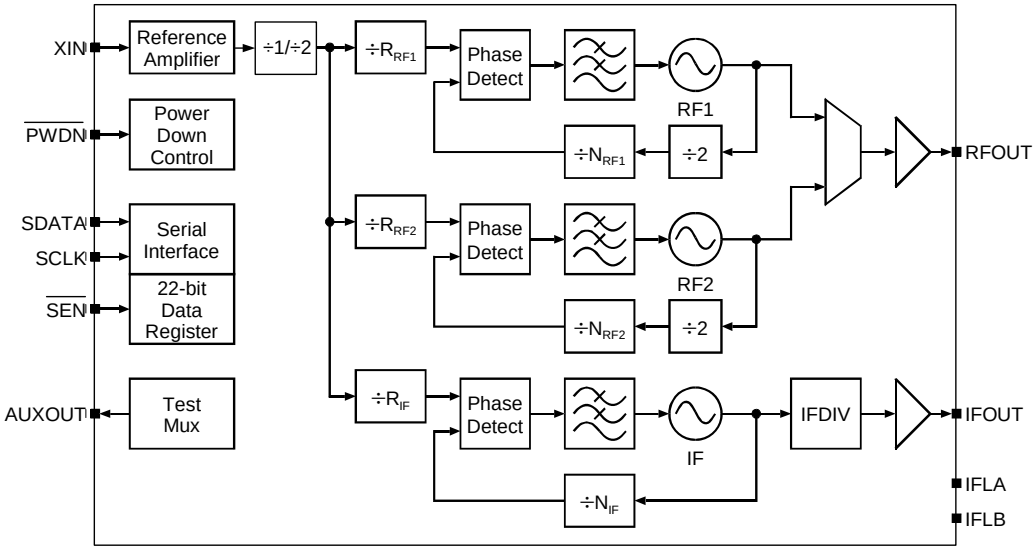


Figure 5.3: Synthesizer functional block diagram, from [25]

A search for a reference oscillator was perform in Farnell's[1] website [26] and the oscillator selected was the **LTC1799** from Linear Technology. The oscillator features are [27]:

- One external resistor sets the frequency;
- 1 kHz to 33 MHz frequency range;
- 2.7V to 5.5V supply;
- 1 mA typical supply current;
- Frequency Error $\leq$ 2% 5 kHz to 20 MHz;
- 50% $\pm$ 5% duty cycle 2 MHz to 20 MHz;
- CMOS output driver;
- SOT-23 package.

This oscillator was chosen mainly for its simplicity because the frequency can be selected with only one resistor, calculated by the following equation:

$$f_{OSC} = 10\text{MHz} \cdot \frac{10\text{k}}{N \cdot R_{SET}}, N = \begin{cases} 100, & \texttt{DIV} \text{ Pin} = \text{V}^+ \\ 10, & \texttt{DIV} \text{ Pin} = \text{Open} \\ 1, & \texttt{DIV} \text{ Pin} = \text{GND} \end{cases} \tag{5.1}$$

[1]Farnell is a world leading distributor of electronic and electrical products, with over 480.000 stocked products from several manufacturers.

The frequency of the oscillator ranges from 1 kHz to 33 MHz, so the resistor R_{SET} can take values from 3 kΩ to 1 MΩ. To calculate the value of R_{SET}, an oscillator frequency had to be chosen so it was decided that $f_{OSC} = 10$ MHz and $N = 1$, that is, the `DIV` pin is connected to Ground (GND). Replacing this values in equation 5.1 we obtain $R_{SET} = 10$ kΩ.

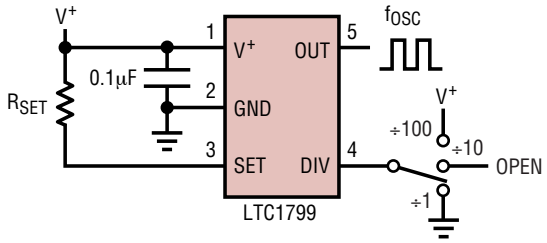


Figure 5.4: LTC1799 basic connections, adapted from [27]

A basic connection diagram for the LTC1799 oscillator is represented in figure 5.4. As can be seen, this oscillator requires only two external elements, R_{SET} and a 0.1 μF capacitor.

Electrical diagram

The frequency synthesizer implemented is composed by the Si4136 RF synthesizer and the LTC1799 oscillator presented before. The electrical diagram of the synthesizer is represented in figure 5.5.

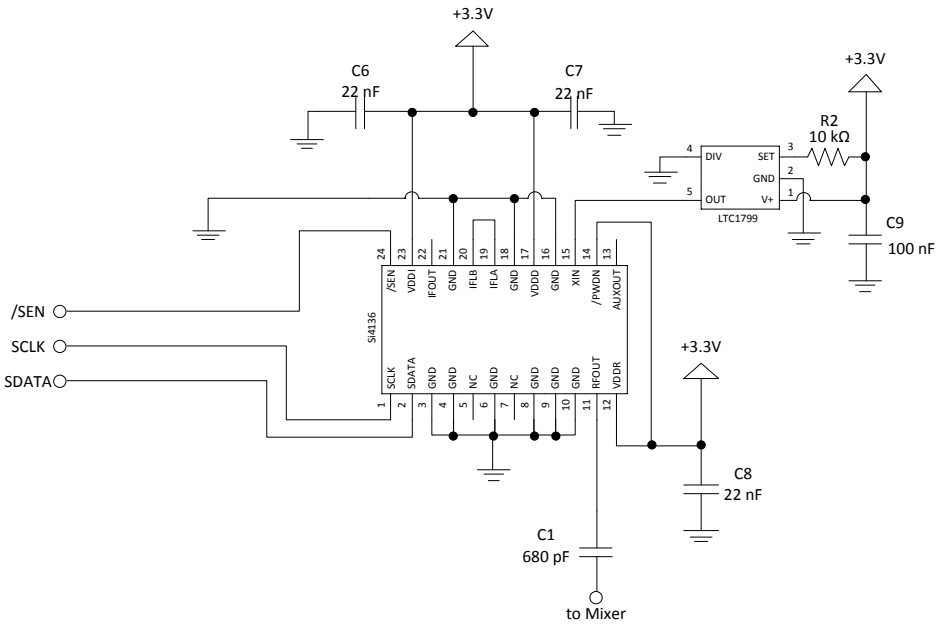


Figure 5.5: Electrical diagram of the frequency synthesizer

To filter noise in the DC bias lines were used capacitors `C6`, `C7` and `C8` with the value of 22nF, as indicated in the datasheet [25]. Capacitor `C1` is used to prevent DC from entering the synthesizer. The resistor `R2` in figure 5.5 is the R_{SET} resistor seen in figure 5.4 and capacitor `C9` is used to filter noise at the DC input of the oscillator.

5.2.2 LNA

The LNA is one of the first elements in the receiver chain. Its purpose is to amplify the input RF signals.

In the market there are many LNAs with different characteristics so, in order to limit the choice, some specifications that the LNA should achieve were defined:

- **Low supply voltage**, preferably 3V, 3.3V or 5V;
- **Low supply current**, because in the future it might be useful to use batteries in order to make the receiver portable. With low power consumption, the batteries last longer;
- **Low noise figure**, typically less than 1 dB. Because the LNA is the first element of the receiver, its contribution to the overall noise figure will be greater than the contribution of the other components, according to equation (4.2);
- **2.1 GHz to 2.6 GHz of frequency range**. Considering the chosen frequency synthesizer, this is the frequency range of the signals at the input of the LNA;
- **High IP3**. See section 4.5.2 for an explanation about this figure of merit;
- **High gain**. If two LNAs have similar characteristics, the one chosen should be the one with a higher gain;
- **SOT, TSOP, SOIC** or similar SMD package;
- availability of **S-parameters** from the manufacturer, in order to simulate the circuit.

Taking into account these specifications, it was performed a search in Farnell's website [26] and a couple of LNAs were compared.

The LNA chosen was the **MGA-62563**, Current-Adjustable Low Noise Amplifier from Avago Technologies.

According to the datasheet [28], this LNA features:

- Single +3V supply;
- 62 mA typical device current;
- NF = 1.2 dB @ 2.0 GHz;
- Gain = 15.5 dB @ 2.0 GHz;
- IP3 = 32.3 dBm @ 2.0 GHz;

- P1dB = 17.7 dBm @ 2.0 GHz;
- SOT-363 package.

A simplified schematic is represented in figure 5.6. The values for V_d, I_d and R_{bias} have to be chosen and to simplify the maths the manufacturer includes in the datasheet [28] several possibilities for this values. It was chosen $V_d = 3$V and $I_d = 30$ mA because the manufacturer provides S-parameters of the LNA for these values. Therefore, and once again consulting the datasheet, the value of R_{bias} is 1 kΩ.

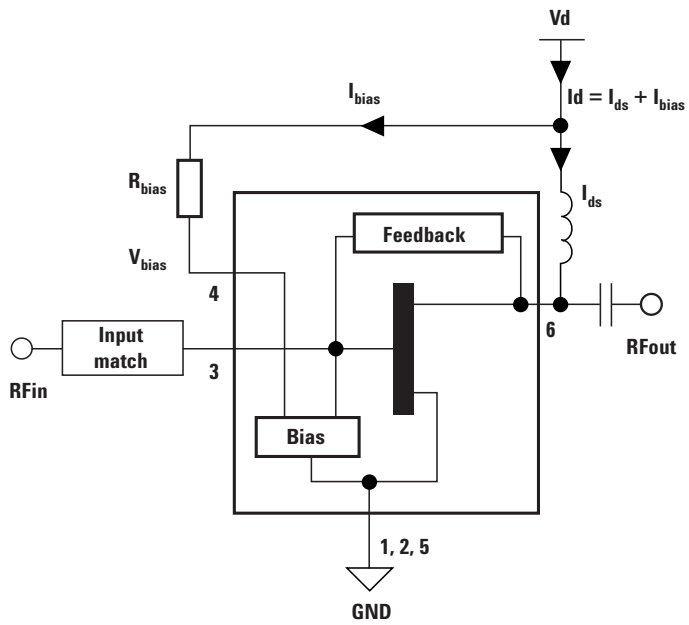


Figure 5.6: MGA-62563 LNA simplified schematic, from [28]

As indicated in the datasheet, the input of the amplifier needs to be matched. Therefore, a impedance matching circuit was simulated and optimized in ADS software. Also, an impedance matching circuit for the output and a biasing circuit were simulated in the same software. These three circuits are described below.

I/O Matching Networks & Bias Circuit

When working with radio frequencies it is important to have the impedance of the components adapted to each other, in order to improve the SNR of the system, to deliver the maximum power to a load and to minimize power losses [18].

Impedance matching networks are usually made with transformers, lumped elements (resistors, inductors, capacitors) or transmission lines. In this dissertation, impedance matching networks were projected using lumped elements and transmission lines, depending on the working frequency. At higher frequencies, the lumped elements may not be realizable or their parasitic elements are not negligible. With low frequencies, the size of the transmission lines

becomes very large for its implementation to be feasible. Therefore, lumped elements are usually used at low frequencies and transmission lines are preferred at higher frequencies.

For the reasons discussed previously, the three circuits were made with microstrip lines, which are a common type of electrical transmission lines used in PCBs.

The simulated circuit can be seen in figure 5.7. A more detailed diagram of the simulation and optimization performed in ADS is presented in figure B.1 from appendix B.

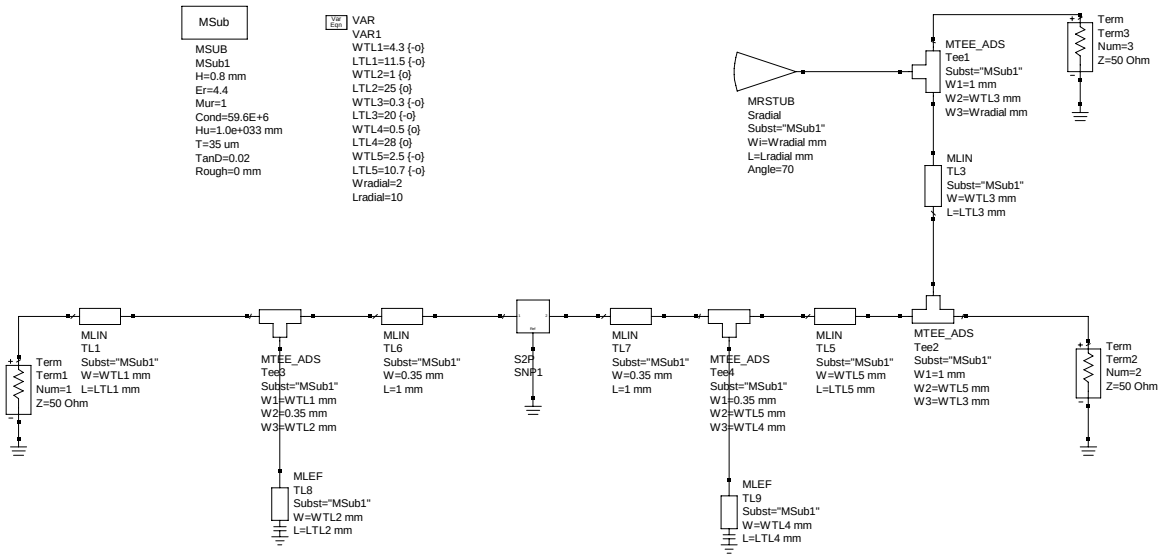


Figure 5.7: LNA related circuits, simulated in ADS software

The input impedance matching network of the LNA is composed by the microstrip lines identified in figure 5.7 as `TL1`, `Tee3`, `TL8` and `TL6`. These microstrip lines are placed according to the single-stub tuning technique presented in [18]. This technique can be realized using a single short-circuited or open-circuited stub connected either in parallel or in series with the transmission bias line. In microstrip technology it is easier to implement parallel open-circuited stubs, so this was the one implemented in this circuit. A description of the microstrip lines for the input matching network is as follows:

- `TL1`: transmission bias line;
- `TL8`: microstrip open-circuited parallel stub, with open-end effect to simulate parasitic capacitances at the open-end of the stub;
- `Tee3`: connection needed by ADS software to place the microstrip lines in the correct position;
- `TL6`: microstrip line that can be viewed as an extension of the footprint pad of the LNA. If the transmission bias line (`TL1`) was connected directly to the input pin of the LNA,

that transmission line would connect also the other pins due to the pin spacing of the LNA package. For this reason, a small microstrip line (`TL6`) was added to avoid this problem.

As indicated in the figure 5.6, the output is connected with the power supply through a RF Choke (RFC). The purpose of the RFC is to prevent RF from going to the power supply and at the same time allow DC to pass to the output pin. The RFC is simply an inductor that has a very high reactance to high frequencies and very low reactance to low frequencies. The reactance X_L of an inductor is calculated as:

$$X_L = 2\pi f L \tag{5.2}$$

where f is the frequency in [Hz] and L is the inductance in [H].

The LNA should work from 2.1 GHz to 2.6 GHz, so this poses a problem to the use of a lumped inductor in two ways. First, there is the problem of lumped elements working at high frequencies and second, the inductor should work equally in a relative wide bandwidth (500 MHz) to prevent the RF signals from going to the supply power.

To overcome this problem, a radial stub was used. The radial stub provides low-impedance for a broadband DC bias at the point where is inserted [29, 30] and for that reason it is widely used in bias circuits for RF elements.

Another element that is used with the radial stub for DC bias circuits is the *quarter-wave transformer*. Considering a lossless transmission line terminated with a load Z_L, the impedance seen at the input is given by [18]:

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l} \tag{5.3}$$

where l is the length of the transmission line, Z_0 is the characteristic impedance and β is the phase constant. This phase constant can be expressed as:

$$\beta = \frac{2\pi}{\lambda} \tag{5.4}$$

where λ is the wavelength, defined by:

$$\lambda = \frac{c}{f} \tag{5.5}$$

where $c \approx 3 \times 10^8$ m/s is the speed of light and f is the frequency.

As the name indicates, the length of a quarter-wave transformer is $\frac{\lambda}{4}$. Replacing $l = \frac{\lambda}{4}$ in equation 5.3 we obtain:

$$Z_{in} = \frac{Z_0^2}{Z_L} \tag{5.6}$$

Equation 5.6 represents the input impedance of the quarter-wave transformer. It is easy to see that when the load is a short-circuit ($Z_L = 0$), the input of the transformer will be an open-circuit ($Z_{in} = \infty$) and when the load is an open-circuit ($Z_L = \infty$) the input impedance will be a short-circuit ($Z_{in} = 0$).

At a chosen frequency, the radial stub creates a low-impedance where it is inserted. Therefore, if we place the radial stub at one end of the quarter-wave transformer, then at the other end it will be a high-impedance at the same frequency.

Regarding figure 5.7, the DC bias circuit is composed of:

- `Tee1`, used as connection for the radial stub and the quarter-wave transformer;
- `Sradial`, the radial stub;
- `TL3`, the quarter-wave transformer[2];
- `Tee2`, used to connect the microstrip line `TL5`, the quarter-wave transformer and the mixer's input.

Finally, the microstrip lines that compose the output matching network are:

- `TL7`, microstrip line with the same function of `TL6`, explained before;
- `Tee4`, provides connection for `TL6`, `TL9` and `TL5`;
- `TL9`, microstrip open-circuited parallel stub, with open-end effect to simulate parasitic capacitances at the open-end of the stub;
- `TL5`, transmission bias line.

Before the simulation and optimization of this circuit can be done, a substrate for the PCB was chosen. It is intended that the spectrum analyzer is low cost, so the substrate chosen was FR-4, because it is a common, low cost substrate and widely used. The relevant substrate parameters that were used in ADS for the simulation are presented in table 5.1. The other ADS parameters were left default.

Substrate parameter	ADS parameter	Value
Thickness	H	0.8 [mm]
Relative dielectric constant	Er	4.4
Conductor conductivity	Cond	59.6×10^6 [S/m]
Conductor thickness	T	0.35 [µm]

Table 5.1: FR-4 substrate parameters

[2]As it will be explained later, the length of this microstrip line is not $\frac{\lambda}{4}$. The function of TL3 is the same of a quarter-wave transformer, so this microstrip line will continue to be referred as the quarter-wave transformer.

Circuit Simulation & Optimization

The approach used to calculate the length (L) and width (W) of the microstrip lines is described below.

In the first place, maximum and minimum limits were defined as:

- 3 mm $\leq L \leq$ 25 mm. This limits were chosen so that the microstrip lines would not become neither too small nor too large;
- 0.25 mm $\leq W \leq$ 6 mm. The lower limit is the minimum that can be realized at IT, where the board was made, and the maximum limit was chosen arbitrarily so that the microstrip line would not become too large.

The radial stub was defined with the following parameters:

- $\alpha = 70^{o}$. This value was fixed, so the only parameter calculated by the simulator was the length of the radial stub;
- 3 mm $\leq L \leq$ 15 mm. This limits were chosen for the same reason as the ones mentioned previously for the length of the microstrip lines;
- 0.25 mm $\leq W \leq$ 6 mm. The reason for this limits is the same as the one presented for the widths of the other microstrip lines.

The lengths and widths of `TL6` and `TL7` were defined as:

- $L = 1$ mm;
- $W = 0.35$ mm.

To set up the simulation, the S-parameters file was imported into ADS and three "port impedance termination for S-parameters", represented in figure 5.7 as `Term1`, `Term2` and `Term3`, were added to the circuit. To perform the optimization, six goals were defined, two for each termination.

At `Term1` and `Term2`, both module and phase of the reflection coefficient (S11) should be zero, which means that these terminals are adapted to 50 Ω. At `Term3`, a short circuit is wanted at RF so the module and phase of the reflection coefficient were set to 1 and 180°, respectively. These goals were defined to a frequency of 2.4 GHz.

The circuit was then simulated and optimized. Soon after the first steps of the optimization algorithm the parameters of `Sradial` were set to fixed values, so we can ensure that the radial stub has a size that is realizable. This is the reason why the `TL3` microstrip line doesn't have a length equal to $\frac{\lambda}{4}$, because in the bias circuit the only parameters the simulator could optimize were the parameters of `TL3` line.

After setting the values for `Sradial`, the optimization was executed again and when the parameters of the microstrip values stabilized, the optimization was stopped. Then, the values

were rounded to one decimal place and a simulation was performed to verify if the graphics of the reflection coefficients Γ_r were as expected. These values are represented in figure 5.8 and the lengths and widths of the microstrip lines are presented in table 5.2.

As can be seen in figures 5.8(a) and 5.8(b), the reflection coefficients are near the center of the Smith chart, which means that both the input and the output of the LNA is matched to an impedance of 50 Ω in the desired frequency range. The reflection coefficient in figure 5.8(c) is near the point of zero impedance, which means that it will be a short-circuit as expected.

	Microstrip Line	Length [mm]	Width [mm]
Input matching network	TL1	11.5	4.3
	TL8	25.0	1.0
Output matching network	TL5	10.7	2.5
	TL9	28.0	0.5
Bias circuit	TL3	20.0	0.3
	Sradial (α=70º)	10.0	2.0

Table 5.2: LNA's microstrip line values for the matching networks and bias circuit

Electrical diagram

The circuit diagram related to the LNA is represented in figure 5.9. The purpose of capacitor `C10` and inductor `RFC` is to filter the noise and to prevent RF signals from going to the power supply.

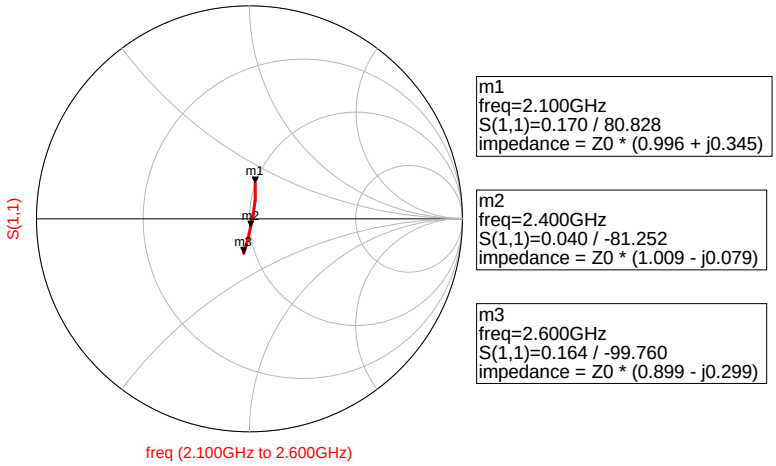
5.2.3 Mixer

After choosing the frequency synthesizer and the LNA, the last component to be chosen in the RF stage is the mixer.

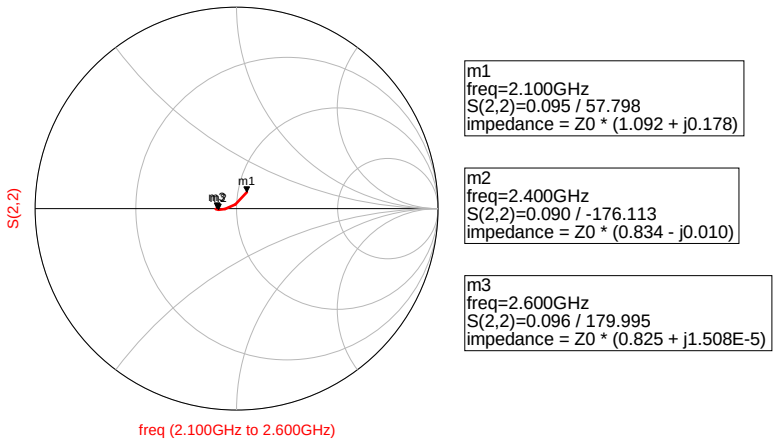
To choose this component, a search in Farnell's website [26] was performed and several mixers were compared until the choice fell on the **IAM-91563** mixer from Avago Technologies. This mixer has the following characteristics [31]:

- 0 dBm Input IP3 at 1.9 GHz;
- Single +3V supply;
- 9.0 dB conversion gain at 1.9 GHz;
- 8.5 dB SSB noise figure at 1.9 GHz;
- SOT-363 package.

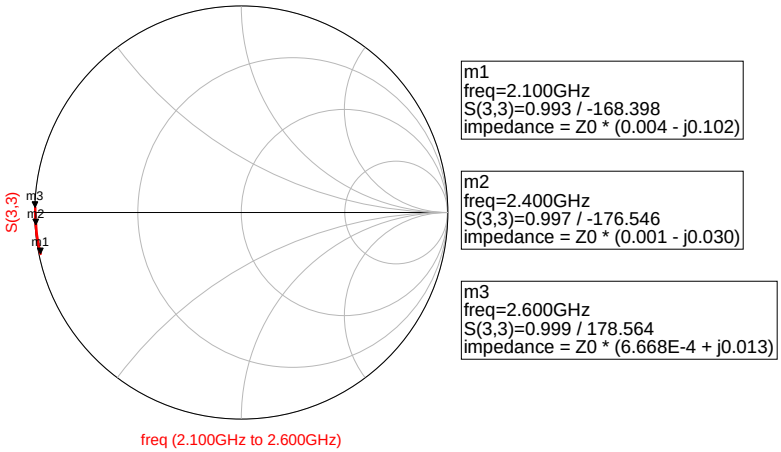
This mixer has a RF frequency coverage from 800 MHz to 6 GHz and an IF coverage from 50 MHz to 700 MHz which means it can be used in this receiver. Furthermore, instead



(a) Γ_r at the input of the LNA



(b) Γ_r at the output of the LNA



(c) Γ_r at radial stub insertion point

Figure 5.8: Simulated reflection coefficients of the LNA with matching networks

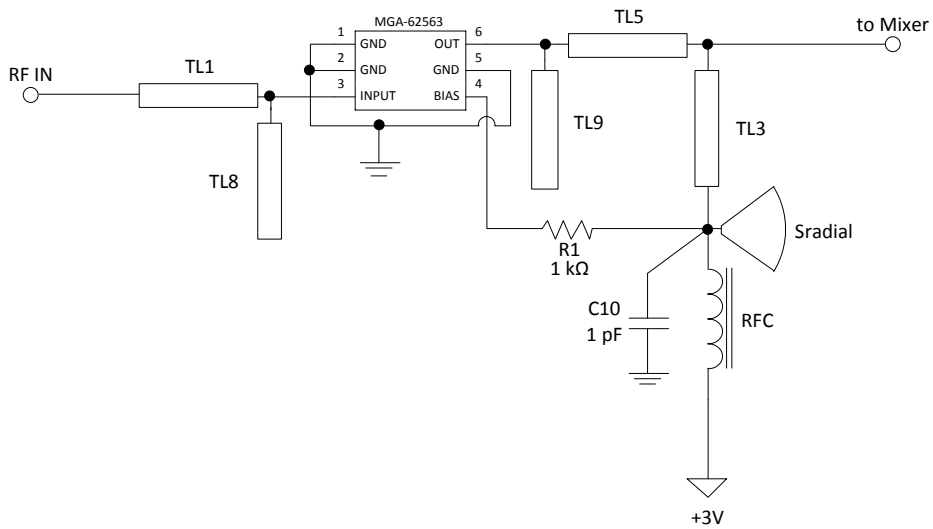


Figure 5.9: Circuit diagram related to the LNA

of having conversion losses it has a conversion gain of 9 dB at 1.9 GHz, making this mixer a useful gain block to amplify the RF signal together with the LNA.

Matching Networks

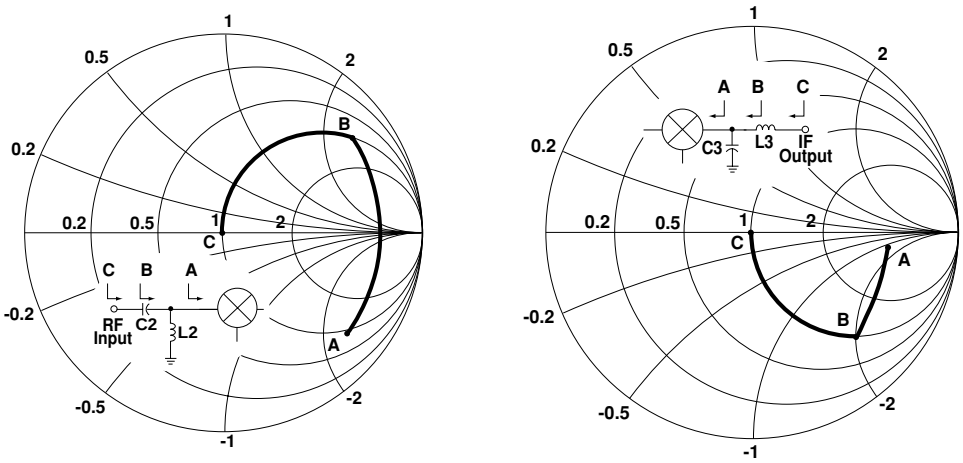
As stated on the datasheet, the RF and IF ports need impedance matching. This will be done with a 2-element matching network for each port.

Using the reflection coefficients present in table 5.3 and the Smith chart it is relatively easy to project a 2-element matching network.

Frequency (MHz)	RF (Mag)	RF (Ang)	LO (Mag)	LO (Ang)	IF (Mag)	IF (Ang)
100	-	-	-	-	0.64	-8
2000	-	-	0.39	-29	-	-
2100	0.81	-40	0.38	-31	-	-
2200	0.81	-41	0.38	-31	-	-
2300	0.81	-42	0.37	-32	-	-
2400	0.81	-44	0.37	-33	-	-
2500	0.80	-45	0.36	-34	-	-
2600	0.80	-45	-	-	-	-

Table 5.3: Typical reflection coefficients, $Z_0 = 50\Omega$, $V_d = 3$V, from [31]

The procedure to calculate the values of the two matching networks is described in detail in Appendix A. Therefore, only the values of the lumped elements will be presented in this section. Regarding the two matching networks represented in figure 5.10, the values of the



(a) RF input impedance match

(b) IF output impedance match

Figure 5.10: Mixer's impedance matching, adapted from [31]

lumped elements obtained by following the procedure explained in Appendix A are:

$$\texttt{C3} = 10 \text{ pF} \qquad \texttt{C2} = 0.5 \text{ pF}$$
$$\texttt{L3} = 150 \text{ nH} \qquad \texttt{L2} = 4.7 \text{ nH}$$

Electrical diagram

The electrical diagram of the mixer can be seen in figure 5.11. Inductor `L1` is a small series inductor to improve the LO match, as indicated in the mixer's datasheet [31]. `C4` and `C5` are both bypass capacitors and `L4` is used to isolate the IF from the DC supply. `L3` and `C3` are the matching network for IF while `L2` and `C2` are the matching network for the RF input. The purpose of the capacitor `C11` is to act as a DC block.

5.2.4 Overall circuit and PCB layout

The whole circuit diagram for the RF stage can be seen in figure B.2 at Appendix B.

For a better presentation, the PCB layouts were also placed in Appendix B (figures B.3 and B.4).

The PCB layouts were design in EAGLE Light Edition software, which is freeware. In EAGLE's website [32] there are many User Language Programs (ULPs) free to use and one that was useful to design the radial stub can be found in the downloads section under the name `microstrip-radial-stub.zip`.

To provide I/O connections for RF IN and IF OUT, RF connectors of the SMA type were used. This type of connector has an impedance of 50 Ω and offers excellent performance from DC to 18 GHz.

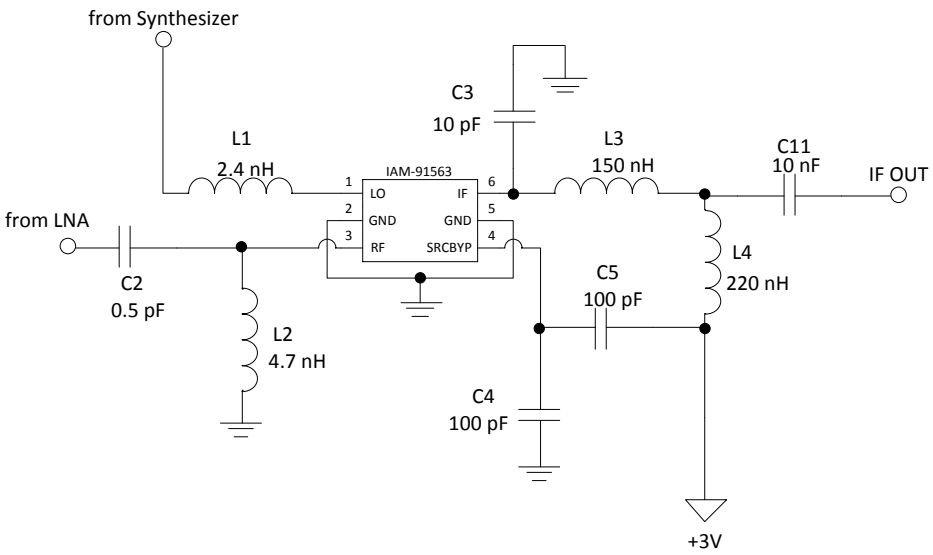


Figure 5.11: Circuit diagram related to the mixer

5.3 IF stage

The IF stage porpuse is to receive an IF signal, amplify it and detect its power. Referring to figure 5.1, the IF stage is composed by a gain block and a power detector. These two elements will be described below.

5.3.1 IF Gain

Before reaching the IF stage, the signal is amplified two times, one in the LNA and the other in the mixer. Despite this gain added to the signal, the RF input signal can be of very low power, say -100 dBm, and will be attenuated in the receiver chain due to losses in the microstrip lines and in the filters used. Therefore, this gain block should add high gain in order to match the signal's power to the dynamic range of the power detector.

The amplifier chosen for this gain block was the **MAR-1+** from Mini-Circuits. The choice fell on this amplifier because of its characteristics [33]:

- Wideband, DC to 1 GHz;
- Gain = 17.8 dB @ 100 MHz;
- NF = 3.3 dB @ 500 MHz;
- Output IP3 = +14 dBm @ 500 MHz;
- Output P1dB = +2.5 dBm @ 500 MHz;
- Low current, 17 mA;
- Single supply voltage, from +7V to +15V.

One feature mentioned in the datasheet was that this amplifier is cascadable and unconditionally stable, so it was decided to use two amplifiers to provide a gain of 35.6 dBm at 100 MHz.

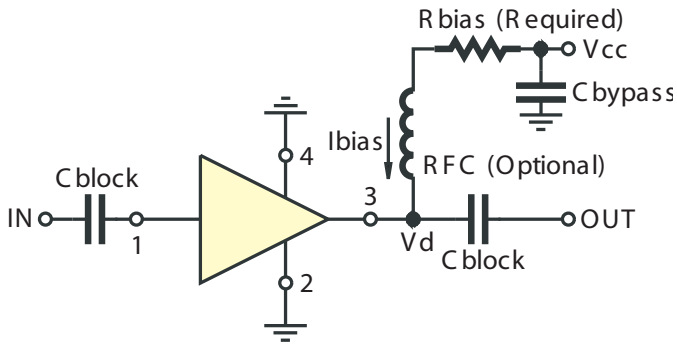


Figure 5.12: Recommended application circuit for MAR-1+, from [33]

The recommended application circuit in figure 5.12 was used as a base to the design of MAR-1+ circuit presented in figure 5.13. This amplifier has an operating voltage `Vd` = +5V, but is fed with a `Vcc` voltage ranging from +7V to +15V. To maintain 17 mA of supply current, different values of `Rbias` have to be chosen according to the value of `Vcc`.

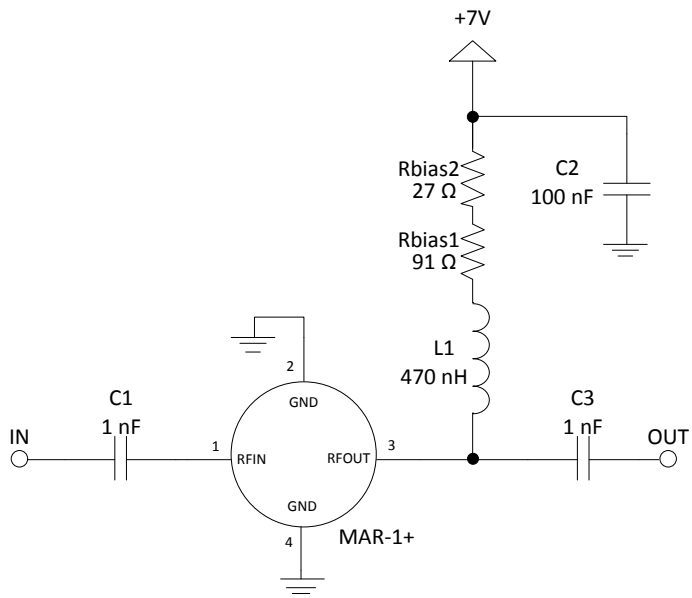


Figure 5.13: MAR-1+ circuit diagram

The lower supply voltage was chosen, `Vcc` = +7V, and the corresponding value of `Rbias` is 118 Ω, as indicated in the datasheet [33]. As the value of 118 Ω does not exist in the E24 series resistors, two resistors in series, $91\Omega + 27\Omega$, were used to achieve the desired value for

`Rbias`.

The porpuse of inductor `L1` is to act as a RFC, and its reactance is calculated by equation (5.2). At a frequency of 100 MHz, the reactance of the 470 nH inductor is 295Ω, which is about six times the characteristic impedance of the system (50 Ω). `C2` is a bypass capacitor to filter noise from the power supply and `C1` and `C3` are DC block capacitors.

5.3.2 Power Detector

The power detector is an important element used in wireless systems. In the transmitter, it is used to measure the transmitted output power and on the receiver side it is used to measure the Receiver Signal Strength Indication (RSSI). It is important to measure the output power in a transmitter because there are certain maximum values that cannot be exceed according to regulations. In the receiver, the RSSI is used to control the gain of the received signal by using an Automatic Gain Control (AGC) circuit. This signal is also used to indicate the "quality" of reception in cellphones, for example.

There are two types of power detectors: the RMS and the logarithmic detector. The RMS detector outputs a DC voltage that is proportional to the RMS value of the signal, while the logarithmic detector converts the input power into a DC voltage proportional to the logarithm of the input [34].

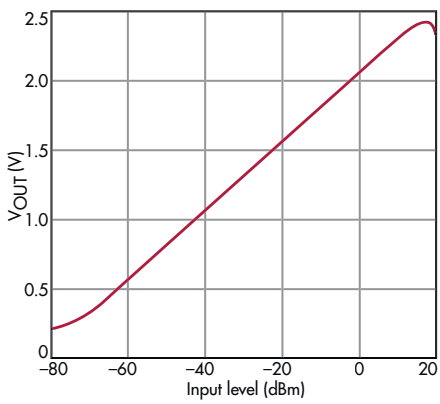


Figure 5.14: Typical output curve for a logarithmic power detector, from [34]

For this project it was selected the logarithmic type because its output is directly related to decibels. This means that when we read a voltage at the output it is easy to know the power at the input, in dBm. Figure 5.14 represents a typical output curve for a logarithmic power detector.

Once again, Farnell's website [26] was used to perform a search for a logarithmic power detector, where the **AD8310** Logarithmic Amplifier from Analog Devices was selected. The main features of this power detector are [35]:

- Single supply voltage, from +2.7V to 5.5V;
- 8 mA typical supply current;

- Frequency range from DC to 440 MHz;
- 95 dB dynamic range: -78 dBm to +17 dBm;
- Slope of +24 mV/dB, intercept of -95 dBm;
- 8-lead MSOP package.

The functional block diagram is presented in figure 5.15. Although this component uses the name logarithmic amplifier, its purpose is not to amplify (despite the internal amplification needed) but to compress a signal to its decibel equivalent. Therefore, this can be seen as a measurement device. The theory of operation of this power detector is beyond the objectives of this dissertation and it will not be explained here, but more information about its internal operation can be found in [35].

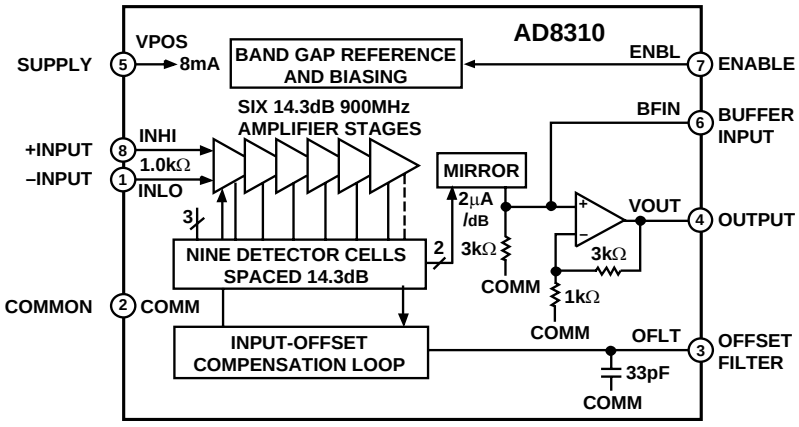


Figure 5.15: AD8310 functional block diagram, from [35]

Based on the information found in the datasheet [35], a circuit for the power detector was design and is represented in figure 5.16.

The signal at the input of the AD8310 is single-ended, so the input `INLO` is tied to the ground through capacitor `C7` while the input signal is coupled to `INHI` through `C6`. Capacitor `C8` is used to decoupled the supply voltage applied to `VPOS`. Pins `BFIN` and `OFLT` aren't needed in this application and for that reason they have been left without connection.

5.3.3 Overall circuit and PCB layout

As stated before in this document, for a better reading the overall circuit diagram of the IF stage and the corresponding PCB layout are presented in figures B.5, B.6 and B.7 from Appendix B.

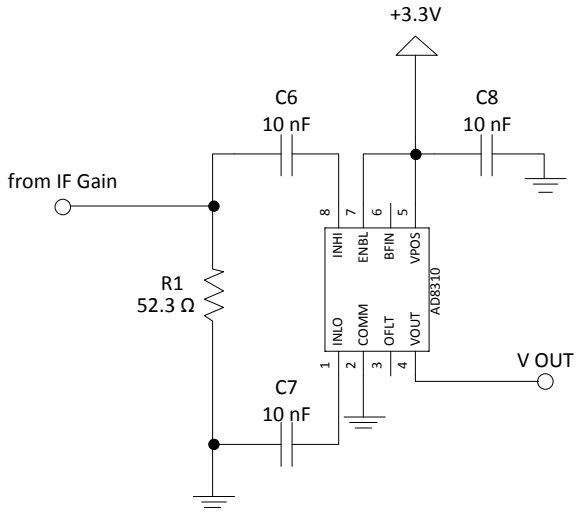


Figure 5.16: AD8310 circuit diagram

5.4 IF Filter

As stated in [18], there are two main design methods for microwave filter design: the *image parameter method* and the *insertion loss method*. The last method is a more modern procedure and uses network synthesis techniques to design the filters with a specified frequency response. To design a BPF with this method it is first necessary to design a LPF prototype and then apply transformations to convert this prototype to the desired frequency range and impedance level. To design the IF filter it was used the *insertion loss method* that will be described below.

5.4.1 Filter design using the *insertion loss method*

Before going straight to the calculations of the filter elements, it is necessary to know what is the desired filter response. The most common are the *maximally flat*, the *equal ripple*, the *elliptic function* and the *linear phase*. The last two are more complicated to implement and require complex calculations, while the first two are easier to implement, so the choice fell upon this two filter responses.

Both the *maximally flat* (also known as *Butterworth*) and the *equal ripple* (also known as *Chebyshev*) bandpass filters are designed as follows:

- Define the filter specifications;
- Design the low-pass prototype (normalized in frequency and impedance);
- Convert to the desired frequency and impedance;
- Implement.

The bandpass filter specifications that need to be defined are the order of the filter and the bandpass frequency. For the *equal ripple* type it is also necessary to specify the ripple in the passband.

An N-order LPF prototype have N lumped elements, and when converting to a BPF it will have $2N$ elements that will be symmetrical, that is, the input and the output can be interchanged. For this reason, it was decided to design an odd-order BPF and for simplicity and lower cost, were only studied filters of 3rd- and 5th-order with different bandwidth and ripple.

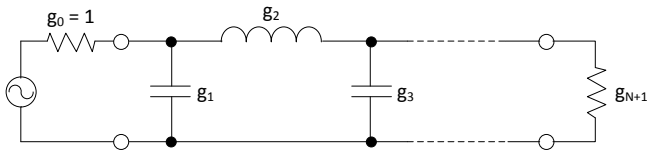


Figure 5.17: Low-pass prototype filter

The obtained values for the lumped elements were then rounded to the nearest available value and the filters with the rounded values were simulated in ADS software. The filters with poor performance or filters with element values not available in the market were excluded until one candidate was remaining. The procedure to calculate the selected BPF will be presented next.

In figure 5.17 is represented the generic low-pass prototype with N reactive elements. The values for this elements differ with the filter's response and the ripple. The values for the implemented filter are presented in table 5.4 and were taken from [36].

Equal Ripple Low-pass Prototype – 3rd Order – Ripple 0.1 dB			
g_0	g_1	g_2	g_3
1	1.0315	1.1474	1.0315

Table 5.4: 3rd order *equal ripple* prototype, ripple 0.1 dB

The next step is to transform the low-pass prototype into the bandpass filter. A shunt capacitor is transformed into a shunt LC circuit and a series inductor into a series LC circuit. The circuit in figure 5.17 will then be transformed into the bandpass filter circuit seen in figure 5.18.

To calculate the values of the capacitors and the inductors of the bandpass filter, some parameters must be known in advance:

$$\omega_0 = \sqrt{\omega_1 \omega_2} \tag{5.7}$$

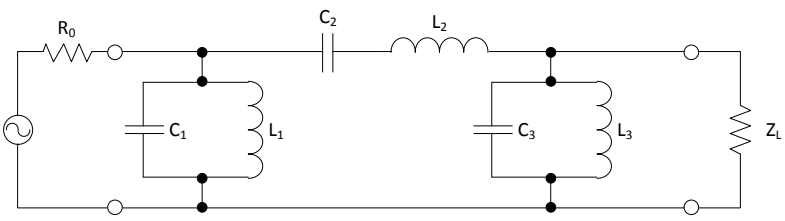


Figure 5.18: Bandpass filter circuit diagram

and

$$\Delta = \frac{\omega_2 - \omega_1}{\omega_0} \tag{5.8}$$

where $\omega_1 = 2\pi f_1$ and f_1 is the lower cutoff frequency. $\omega_2 = 2\pi f_2$ and f_2 is the upper cutoff frequency.

The IF filter was project for a bandwidth of 12 MHz and a center frequency of 100 MHz. Therefore, $f_1 = 94$ MHz and $f_2 = 106$ MHz.

The values of the bandpass filter are calculated using the following equations:

$$C_1 = \frac{g_1}{R_0\,\Delta\,\omega_0} = 273.6\,\text{pF} \quad ; \quad L_1 = \frac{R_0\,\Delta}{\omega_0\,g_1} = 9.3\,\text{nH} \tag{5.9}$$

$$C_2 = \frac{\Delta}{R_0\,\omega_0\,g_2} = 3.3\,\text{pF} \quad ; \quad L_2 = \frac{R_0\,g_2}{\Delta\,\omega_0} = 760.9\,\text{nH} \tag{5.10}$$

$$C_3 = \frac{g_3}{R_0\,\Delta\,\omega_0} = 273.6\,\text{pF} \quad ; \quad L_3 = \frac{R_0\,\Delta}{\omega_0\,g_3} = 9.3\,\text{nH} \tag{5.11}$$

These values were rounded to the nearest available value, becoming $C_1 = C_3 = 270$ pF, $C_2 = 3.3$ pF, $L_1 = L_3 = 9.1$ nH, and $L_2 = 750$ nH.

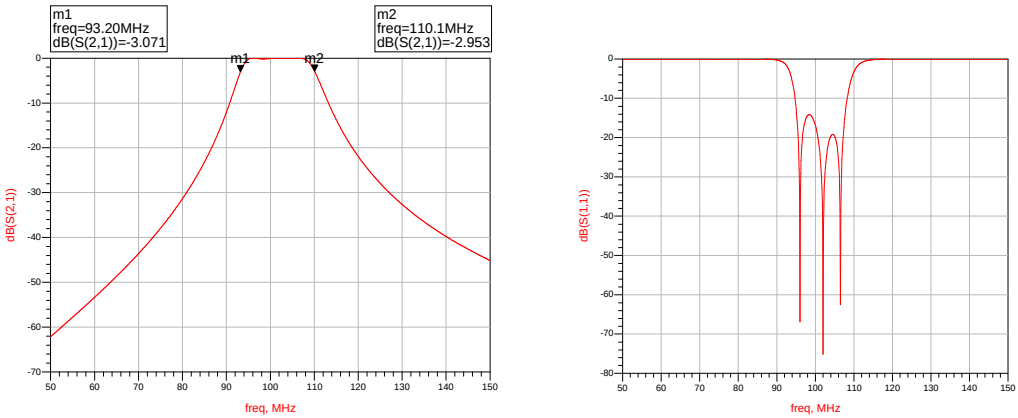
5.4.2 Simulation

The IF filter was simulated in ADS and the results obtained can be seen in figure 5.19. The values of the lumped elements were rounded, so it was expected that the bandwidth and the center frequency were not exactly the ones that were projected.

Looking into figure 5.19(a), the 3 dB cutoff frequencies are approximately $f_1 = 93.2$ MHz and $f_2 = 110.1$ MHz, which gives a bandwidth of 16.9 MHz and a center frequency of 101.65 MHz.

The return loss in the passband is below -14 dB, as can be seen in figure 5.19(b).

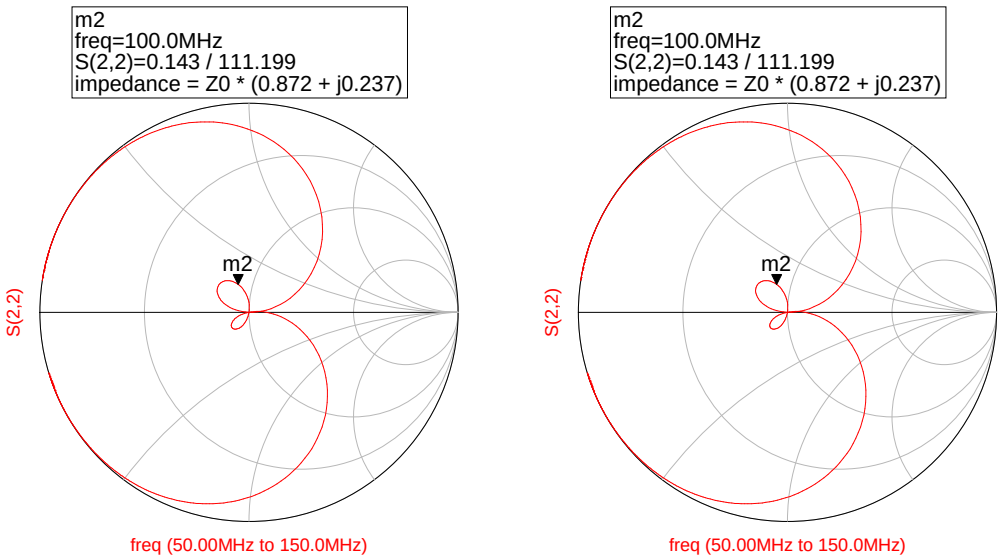
In figure 5.20 is possible to see that the filter is not perfectly matched to 50 Ω at 100 MHz and a perfect match occurs to a frequency of about 102 MHz. Another characteristic that can be seen is that the input and the output graphics of figure 5.20 are equal, as expected, because the input port is equal to the output.



(a) IF filter response

(b) IF filter return loss

Figure 5.19: Simulation of the IF filter



(a) Input impedance

(b) Output impedance

Figure 5.20: Adaptation of the IF filter to 50Ω [50 MHz to 150 MHz]

5.4.3 Circuit diagram & PCB layout

The IF filter circuit diagram and PCB layout are presented in Appendix B, section B.3.

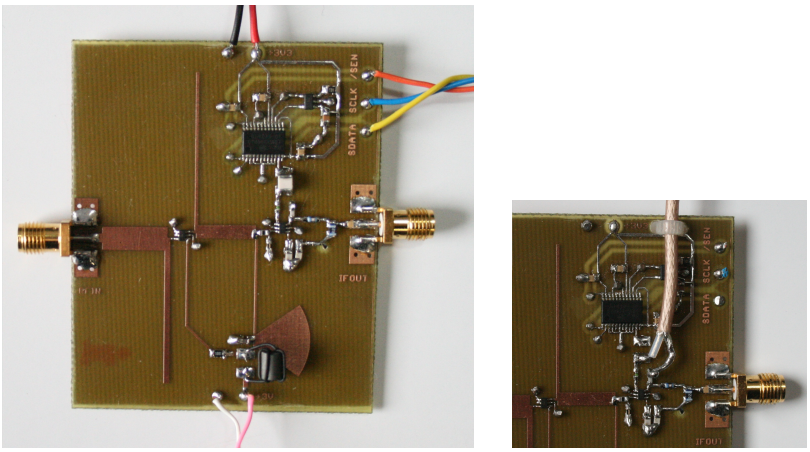
Chapter 6

Tests & Results

In this chapter the tests and results obtained with the hardware implemented will be presented. To perform the tests and measurements, the following lab equipment was used:

- HP 8753D Network Analyzer;
- R&S SMU200A Vector Signal Generator;
- FLUKE-111 Digital Multimeter;
- R&S FSP Spectrum Analyzer;
- Wiltron 6769B Synthesized Swept Signal Generator;
- various power supplies.

6.1 RF Stage



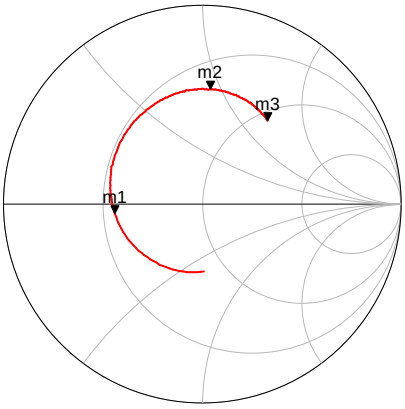
(a) Photo of the RF stage PCB (b) Modification detail

Figure 6.1: Photos of RF stage's PCB

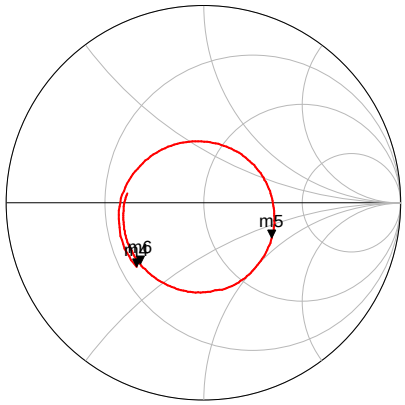
In figure 6.1(a) is depicted a photo of the PCB of RF stage as it was projected. Unfortunately, after some tests with the board and before any data could be obtained, the synthesizer stopped working when it was being programmed. The synthesizer is presented in the datasheet as a black box so the cause of this problem is unknown. In order to perform some tests with the board, the capacitor `C1` (see figure B.2) was removed thus opening the circuit between the synthesizer and the mixer. Then, a piece of coaxial cable was connected to the `LO` port of the mixer, replacing the signal that would come from the synthesizer. A detail on this modification can be seen in figure 6.1(b).

The board was connected to the power supply with +3V and it was verified that the current consumption was 38 mA, which is close to the expected value, since the mixer's device current is typically 9 mA and the LNA is fed with 30 mA.

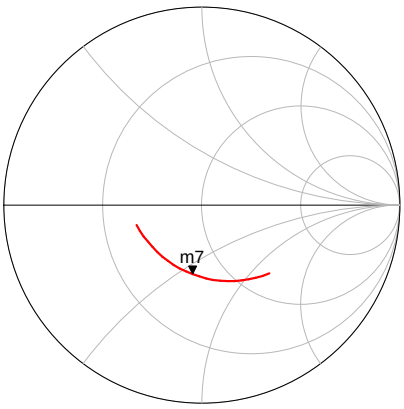
To measure the reflection coefficients of the RF and oscillator inputs and the IF output, the HP 8753D Network Analyzer was calibrated with the HP 85033D 3.5mm Calibration Kit and the S11 parameters of these ports were measured. The results obtained are represented in figure 6.2.



(a) S11 parameter at the RF input



(b) S11 parameter at the oscillator input



(c) S11 parameter at the IF output

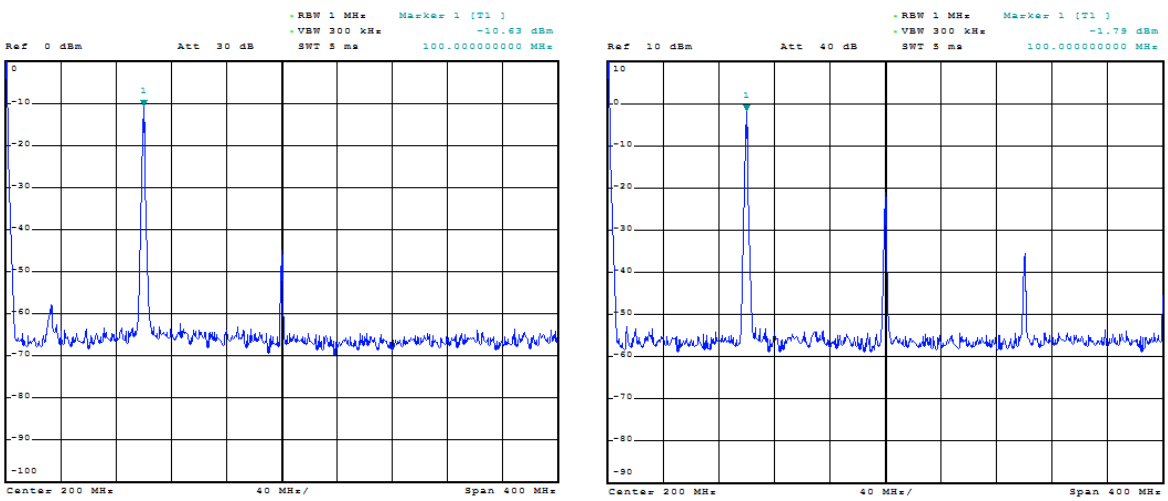
m1 = 2.1 GHz
m2 = 2.4 GHz
m3 = 2.6 GHz
m4 = 2.0 GHz
m5 = 2.3 GHz
m6 = 2.5 GHz
m7 = 100 MHz

Figure 6.2: S11 parameters measured in the RF stage

The S11 parameters in figures 6.2(a) and 6.2(b) were measured from 2.0 GHz to 2.6 GHz and the S11 parameter represented in figure 6.2(c) were measured from 90 MHz to 110 MHz. Also, in this measurements, the test power from the network analyzer was set to -20 dBm and the unused ports of the RF stage were terminated with a 50 Ω load.

Regarding the whole figure 6.2, we can see that there isn't a perfect match to 50 Ω at the desired frequencies. An explanation for this could be the use of FR-4 as substrate, since it is not a recommended substrate for this type of RF circuits, but on the other side it is almost inexpensive compared to other substrates for RF. This substrate has a high value of loss tangent and the dielectric constant itself varies significantly with the frequency, so this could be an explanation for these results. Also, a modification was made in the board to allow for an oscillator signal to be injected into the `LO` pin of the mixer, and this modification may have contributed negatively to the results obtained.

Next, the Wiltron 6769B Synthesized Swept Signal Generator was connected to the oscillator input with a constant power of -5 dBm, because this is the LO power recommended in the mixer's datasheet [31], and in the RF input was connected the R&S SMU200A Vector Signal Generator. The frequencies of both signal generators were changed in the desired frequency range[1], always maintaining a difference of 100 MHz between the two signals, so we have an IF of 100 MHz. The power of the RF signal was changed from -30 dBm[2] until the system started to compress the signal, i.e., when it was observed that the output power decreased despite the increase of input power.



(a) RF Power: -30 dBm

(b) RF Power: -13 dBm

Figure 6.3: Mixer's IF output: LO = -5 dBm @ 2.0 GHz and RF = 2.1 GHz

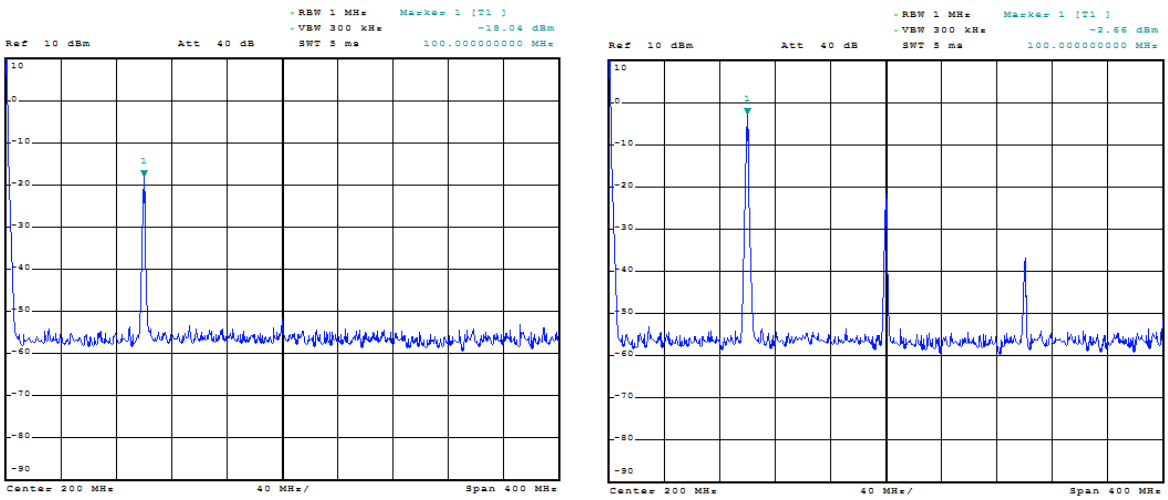
In figure 6.3 it is represented the signal obtained at the IF output with the R&S FSP Spectrum Analyzer for a LO frequency of 2.0 GHz and RF frequency of 2.1 GHz. With an input

[1]The frequency range of the oscillator is 2.0 GHz to 2.5 GHz and the frequency range of the RF input is 2.1 GHz to 2.6 GHz.

[2]The minimum power generated by the R&S SMU200A Vector Signal Generator is -30 dBm.

power of -30 dBm, the output power at 100 MHz is approximately -10 dBm (figure 6.3(a)), which corresponds a gain of 20 dB (LNA and mixer). At these frequencies, the maximum IF output power is approximately -1.8 dBm with an input RF power of -13 dBm (figure 6.3(b)), thus decreasing the total gain to 11.2 dB.

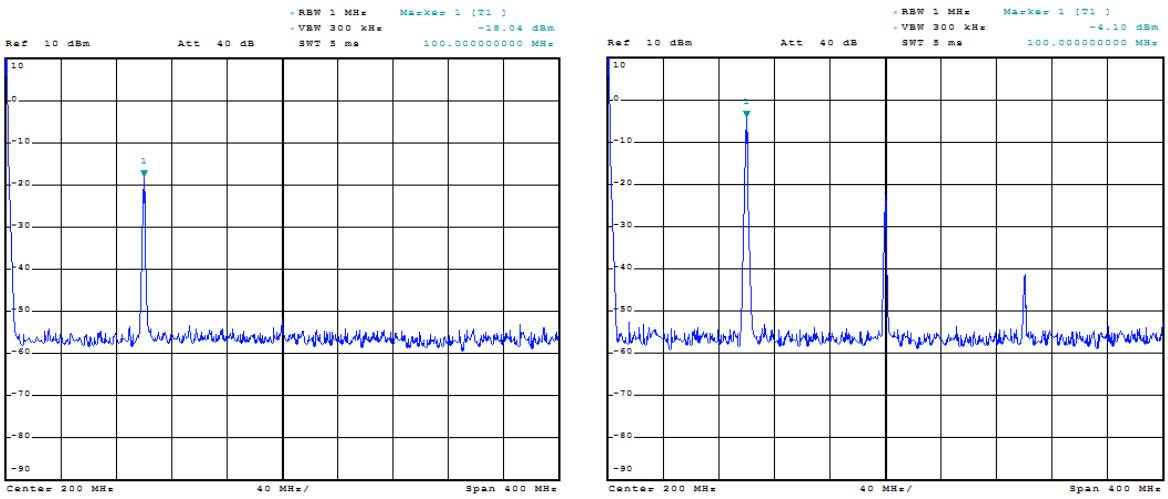
In this graphics it is possible to see the presence of signals appearing at intervals of 100 MHz from the IF signal (at 200 MHz, 300 MHz and 400 MHz in figure 6.3(b)). These signals are probably caused by distortion, because they are spaced at 100 MHz from each other, and they can be removed with a filter after this stage.



(a) RF Power: -30 dBm

(b) RF Power: -9 dBm

Figure 6.4: Mixer's IF output: LO = -5 dBm @ 2.3 GHz and RF = 2.4 GHz



(a) RF Power: -30 dBm

(b) RF Power: -5 dBm

Figure 6.5: Mixer's IF output: LO = -5 dBm @ 2.5 GHz and RF = 2.6 GHz

In figure 6.4 it is presented the IF output of the mixer with a RF signal of 2.4 GHz and an oscillator frequency of 2.3 GHz. In figure 6.4(a), the IF power is -18 dBm which corresponds a total gain (LNA and mixer) of 12 dB. The maximum IF output power for these input frequencies, figure 6.4(b), is -2.6 dBm and is achieved with a RF input power of -9 dBm. The corresponding gain is 6.4 dB.

There is an evident loss of gain that can be explained with the worse adaptation to 50 Ω of the RF input at 2.4 GHz, as seen in figure 6.2(a). Also, the products caused by distortion can be seen in the last two figures, especially for the higher input power.

The same behavior that we saw for the last two cases can be observed in figure 6.5, now for an oscillator frequency of 2.5 GHz and a RF input of 2.6 GHz. The power at IF is approximately -21.4 dBm for a RF power of -30 dBm which results in a gain of 8.6 dB. The gain decreases to 0.9 dB for a RF power of 5 dBm, thus giving us a power of -4.1 dBm at IF.

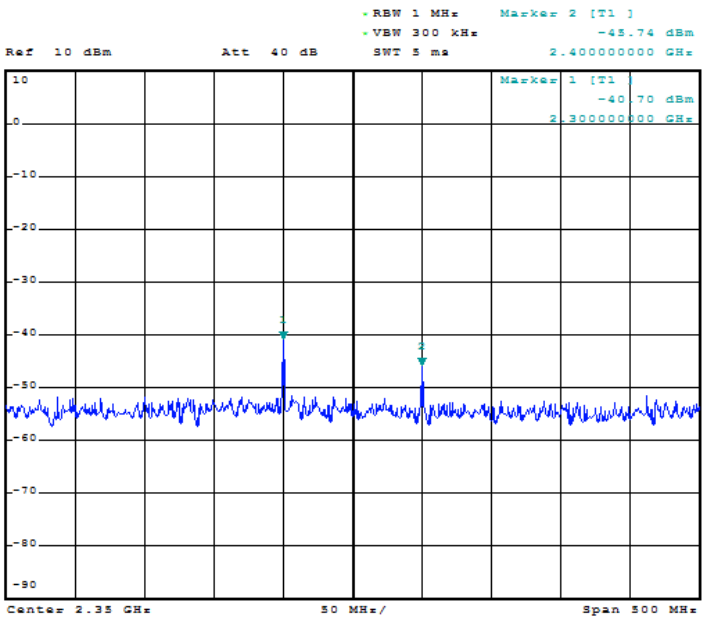


Figure 6.6: Mixer's IF output with LO = -5 dBm @ 2.3 GHz and RF = -20 dBm @ 2.4 GHz

To have an idea of the mixer's isolation between RF-IF and LO-IF, the window of the spectrum analyzer was focused in the range of frequencies of the input signals. A measurement was made with a RF power of -20 dBm at 2.4 GHz and a LO signal of -5 dBm at 2.3 GHz. The result is depicted in figure 6.6 where the power of the LO signal that passes directly to the IF output is approximately -41 dBm and the power of the RF signal in the IF output is about -46 dBm. These two signals are far away from the wanted signal, which is at a frequency of 100 MHz, and they are usually removed with the IF filter. This result is not as important as the ones presented before, but it is presented here to show that the mixer's isolation between RF-IF and LO-IF is good because the input signals that pass directly to the output are being greatly attenuated.

6.2 IF Stage

The PCB of the IF stage is depicted in figure 6.7. In this figure, the PCB has only one MAR-1+ amplifier; the reason for this will be presented below. With the SMA connector, the dimensions are 66 mm length by 40 mm width.

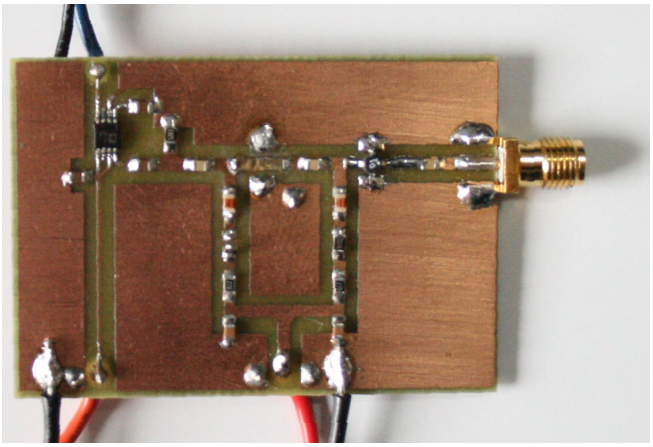
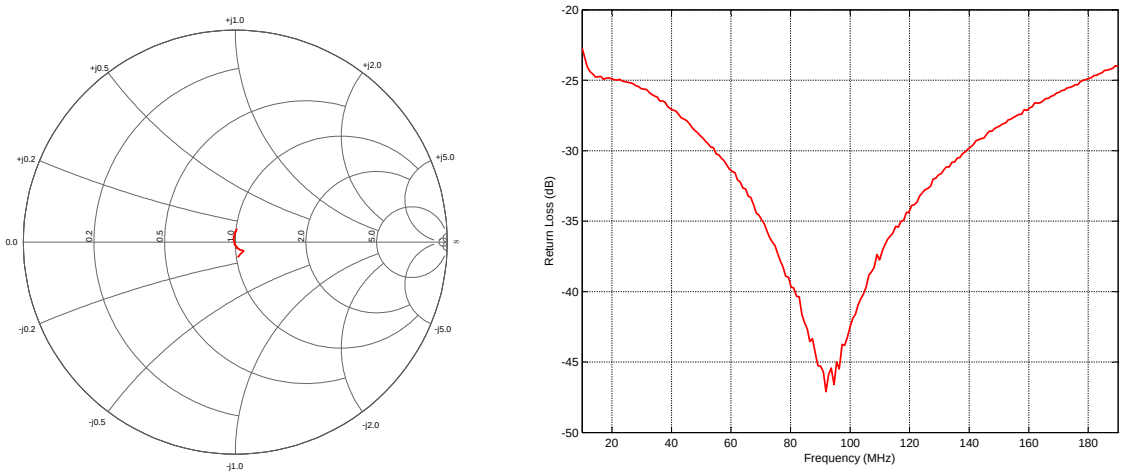


Figure 6.7: Photo of the IF stage PCB

In the first test of the board, after all the connections to the power supplies were made, a multimeter was used to check if the amplifiers were properly biased. As stated in the section 5.3.1, the voltage drop in the resistors of the bias circuit (see figure 5.13) must be approximately 2V to guarantee the amplifier is properly biased. With the multimeter, it was found that the two MAR-1+ amplifiers were not correctly biased since the voltage drop in the two resistors was higher than 2V (about 3V in one amplifier and 4.5V in the other). Because both amplifiers were sharing the same point where the supply power is connected to the PCB, it was decided to deactivate one amplifier by opening its feeding circuit. Once this was done, a 2V voltage drop across the resistors of the active amplifier was measured. The same procedure was made with the other amplifier and the same result was obtained, revealing that the problem was not with one of the amplifiers because it only occurred when the two amplifiers were active. For this reason, it was decided to remove one amplifier (the second counting from the input signal connector) as can be seen in figure 6.7. The amplifier was replaced with a brass strip to establish connection between the first amplifier and the power detector.

With this modification, the first measurement made in the IF stage was to see the adaptation of the input port. To perform this measurement, the HP 8753D Network Analyzer was used, properly calibrated with the HP 85033D 3.5mm Calibration Kit. The obtained results are represented in figure 6.8.

These measurements were taken in a frequency range from 10 MHz to 190 MHz with -20 dBm input test power. A special attention is needed when choosing the value of the input test power so that the signal that reaches the power detector does not reach its maximum input power of 18 dBm [35]. Since the gain expected in the amplifier is 17.8 dB, approximately,



(a) Reflection coefficient

(b) Return loss vs frequency

Figure 6.8: Results obtained at the input of the IF stage

with a input test power of -20 dBm the signal at the input of the power detector won't reach the maximum limit.

In the graphic of figure 6.8(b) we can see that the return loss is below -40 dB at 100 MHz. From the Smith chart represented in figure 6.8(a) it can be observed that the input of the IF stage is correctly matched to 50 Ω.

In order to see if the whole system is working properly, the R&S SMU200A Vector Signal Generator was connected to the input of the IF stage and a digital multimeter was connected at the output. The signal generator will feed the input with a 100 MHz sinusoidal signal and the power of that signal will be controlled in the signal generator. By varying the power of the input signal, it is expected the output voltage read at the multimeter to vary. While this measurement was being made, it was observed that the current feeding the MAR-1+ amplifier was 18 mA and the one feeding the detector was 8 mA. These values are consistent with the information present in the datasheet of both components [33, 35].

Input Power (dBm)	**Output Voltage** (V)	**Input Power** (dBm)	**Output Voltage** (V)	**Input Power** (dBm)	**Output Voltage** (V)
-100	0,592	-65	1,142	-30	1,976
-95	0,598	-60	1,255	-25	2,097
-90	0,620	-55	1,376	-20	2,219
-85	0,675	-50	1,501	-15	2,325
-80	0,778	-45	1,617	-10	2,425
-75	0,898	-40	1,737	-5	2,506
-70	1,016	-35	1,862	0	2,567

Table 6.1: Output voltage of the power detector for different values of input power

The values of output voltage for the corresponding input power are presented in table 6.1. With this values, the graphic of the output voltage as a function of the input power was made and is presented in figure 6.9. In this figure, we can observe that between -80 dBm and -10 dBm of input power the graphic is approximately linear, with a slope of +23.8 mV/dB, very close to the +24 mV/dB slope announced by the manufacturer.

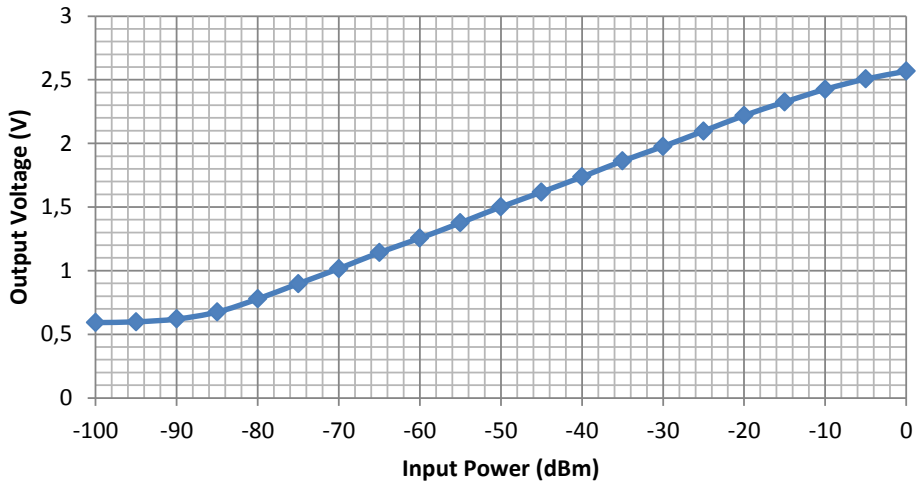


Figure 6.9: Output voltage vs input power of the IF stage

It is important to note that between the input signal and the detector there is an amplifier with an unknown gain so far. The only information on this gain is the one announced by the manufacturer, which states that this amplifier has a typical gain of +17.8 dB at 100 MHz. To get an estimate, we can use the graphic of the typical RSSI output vs input power present in the AD8310 datasheet [35], represented in figure 6.10. This was obtained with a 100 MHz sine input at temperatures of -40°C and +25°C.

By observing the graphic of figure 6.10, an estimate on the values of the typical output voltage from the power detector was made and these values are presented in table 6.2. This values only represent the linear part of the graphic presented in figure 6.10. Also, the linear part of the graphic obtain with the measured results, represented in figure 6.9, was chosen and represented alongside with the estimated output voltage in figure 6.11. A linear regression was made with the two set of values in order to obtain two equations, one for each set of values. Comparing the two equations, we can see that the slope in the measured values is 23.8 mV/dB and the slope in the estimated values is 24.1 mV/dB. This values are close to each other and close to the 24 mV/dB slope announced by the manufacturer.

To calculate the approximate gain of the IF amplifier, we can calculate the difference between the measured and the estimated values of the output voltage. The arithmetic mean of the difference values is 399 mV, which means that the measured output voltage is, in average, 399 mV above the estimated value for the same input power. When replacing $y = 399$ mV in both equations we obtain:

$$x_m = \frac{0.399 - 2.6852}{0.0238} = -96.06 \text{ dBm} \tag{6.1}$$

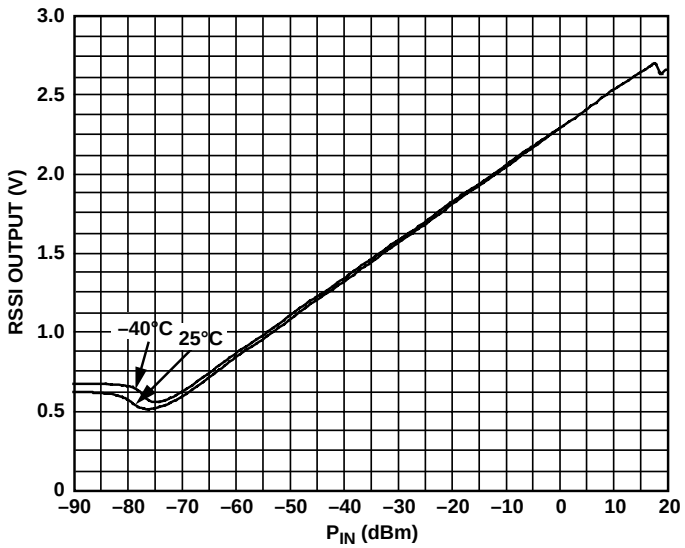


Figure 6.10: Typical values of output voltage vs input power, adapted from [35]

Input Power (dBm)	**Estimated Output Voltage** (V)	**Input Power** (dBm)	**Estimated Output Voltage** (V)	**Input Power** (dBm)	**Estimated Output Voltage** (V)
-70	0.62	-45	1.19	-20	1.81
-65	0.74	-40	1.31	-15	1.94
-60	0.87	-35	1.45	-10	2.06
-55	0.97	-30	1.61	-5	2.19
-50	1.10	-25	1.69	0	2.31

Table 6.2: Estimation on the output voltage of the power detector

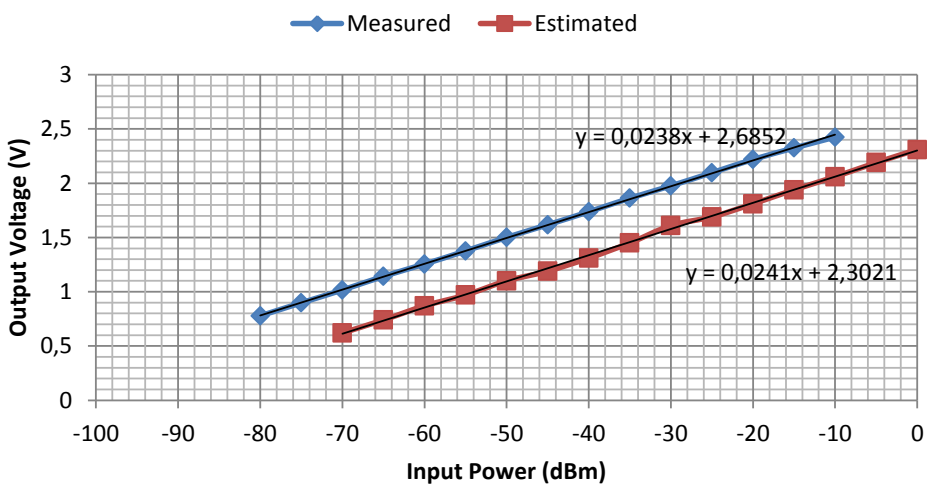


Figure 6.11: Comparison between estimated and measured values of output voltage

$$x_e = \frac{0.399 - 2.3021}{0.0241} = -78.97 \text{ dBm} \tag{6.2}$$

Then, the gain of the IF amplifier can be estimated as:

$$G_{IF} = x_e - x_m = 17.09 \text{ dB} \tag{6.3}$$

This estimate is consistent with the value announced by the manufacturer, which is 17.8 dB at 100 MHz.

Given the results obtained, we conclude that the IF board is working properly, despite having a smaller gain then the one initially expected because one of the amplifiers had to be removed for the reasons previously explained.

6.3 IF Filter

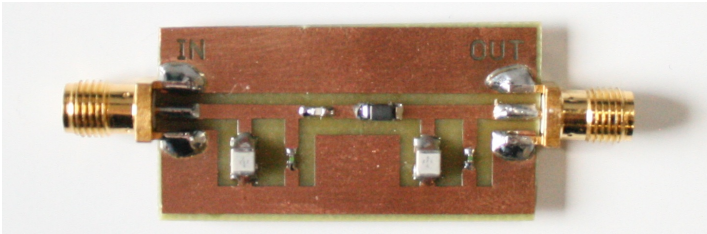


Figure 6.12: Photo of the IF filter PCB

The final look of the IF filter is depicted in figure 6.12. With connectors, the dimensions are 60 mm length by 20 mm width.

The S-parameters of the IF filter were measured with the HP 8753D Network Analyzer. Before measuring the S-parameters, the network analyzer was calibrated with the HP 85033D 3.5mm Calibration Kit in order to have accurate measurements.

The return loss of the implemented IF filter is represented in figure 6.13, where the simulated return loss is also represented for comparison. It can be observed that the return loss obtained is very different from the one expected. The minimum return loss is -16.6 dB obtained at 78 MHz.

It can be seen in figure 6.14 that the insertion loss measured is different from the one simulated. The filter is centered around 80 MHz but has a large attenuation, and the maximum value of insertion loss is -8.1 dB at 89 MHz.

A simulation was performed in ADS, varying the value of the elements to the maximum of their tolerance indicated by the manufacturer. Given the result obtained in this simulation, presented in figure 6.15, we can concluded that the lumped elements have to be very precise, otherwise the response of the filter can be very different from the expected result, which was this case.

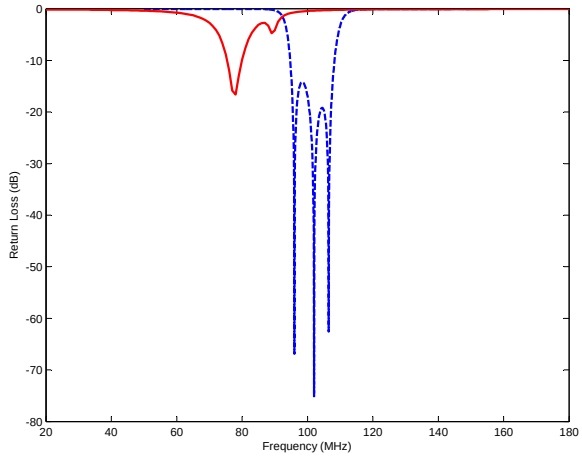


Figure 6.13: Simulated (dashed blue) and measured (solid red) return loss of IF filter

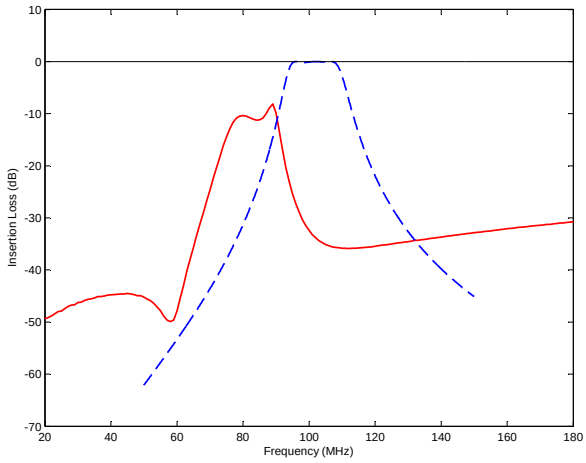


Figure 6.14: Simulated (dashed blue) and measured (solid red) insertion loss of IF filter

In the PCB layout, the width of the line between the components is 1.5 mm and this value was calculated[3] for a characteristic impedance of 50 Ω, at 100 MHz, in the FR-4 substrate. Despite this calculation, no simulation of the microstrip lines and the position of the components was carried out. This may have also influence on the result obtained.

Since the performance of the IF filter obtained is very poor, it won't be used in the implementation of the system.

[3]To calculate the line width was used the LineCalc tool from ADS software.

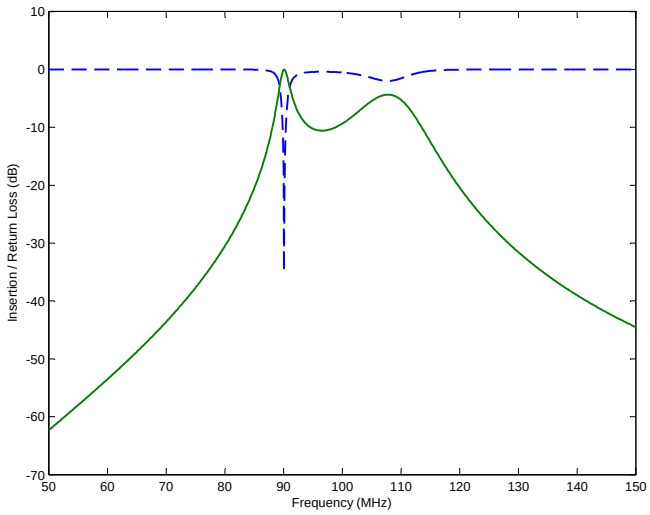


Figure 6.15: Insertion loss (solid green) and return loss (dashed blue) simulation with maximum tolerance values

Chapter 7

Conclusions

7.1 Final Conclusion

The main goal of this dissertation was to implement the hardware for a spectrum analyzer based in SDR. Before starting the hardware implementation, it was necessary to understand what is a spectrum analyzer and how it works, as well as understand the concept of SDR and the theory subjacent to this concept.

The main architectures of a spectrum analyzer were studied, as well as the most common specifications indicated by the manufacturers of spectrum analyzers. The architecture used in most spectrum analyzers is the superheterodyne, so the theory of operation of this type of spectrum analyzer was presented.

The concept of SDR was introduced and the possible SDR architectures were exposed along with the main concerns about the necessary technology to implement a SDR system. Also, the concept of cognitive radio was introduced. The cognitive radio is viewed as an evolution of SDR since it takes the same principles but adds new features to the system.

After this, the most common RF receiver architectures were presented, compared and the one that best approaches the concept of SDR was chosen. A few figures of merit were also explained, as they would become important to characterize the components chosen to implement the receiver's front-end.

Because the receiver has a certain degree of complexity, it was decided to divide the implementation into several parts: antenna + preselector filter, RF stage, IF filter and IF stage. From these blocks, only the antenna and the preselector filter were not attempted to implement.

The RF stage had a problem with the first tests and could not be test in the way it was intended, since the synthesizer stopped working and it was not possible to replace it due to timing issues. However, from the tests conducted with a modification on the board, it could be conclude that the substrate was not indicated for this type of operation at the chosen frequencies and the results were very different from the ones obtained with simulation. Also, more simulations should have been made at different frequencies and with different dielectric constants of the substrate, since the FR-4 used had not a specific dielectric constant for the range of frequencies used.

The IF stage was implemented successfully but not in the way it was initially projected. With two amplifiers this stage wasn't working and after a few tests it was found that removing one amplifier the results in the power detector were similar to the ones expected.

Given the results obtained with the IF filter and the ones expected, we can affirm that the implementation of this filter had failed. One of the reason presented in the previous chapter was the influence of the tolerance of the lumped elements, but other details could have contributed to the failed implementation of the filter. The choice of the filter's order and configuration was limited by the available lumped elements, so other filters with different orders and configurations could not be implemented. In the simulation of the IF filter the lines connecting the lumped elements were not taking into account because the frequency of operation was relatively low, but maybe this should have been considered in the simulation. Also, the position of the lumped elements was not considered, and it was chosen an arrangement similar to the one represented in the schematic. All these details were not taken into account, which may have contributed to the unsuccessfully implementation of the IF filter. Due to timing limits, it was not possible to experiment other methods to project the filter.

7.2 Future Work

A first suggestion for future work is to implement correctly an IF filter, maybe with other methods for projecting the filter. An extensive study could be done, comparing the various filter responses and simulating them, taking into account the arrangement of the elements in the board.

The synthesizer should be replaced in order to connect this system with a controller that could program the synthesizer and retrieve values from the power detector automatically, as this was the first idea for this project. If successfully implemented, the power detector could be replace directly with an ADC thus allowing for vector signal analysis or other function that could be programmed in a DSP or FPGA. If this were implemented, we could be in the presence of a true SDR system.

It would be interesting to study an implementation of a wideband filter to be placed between the antenna and the LNA. With this filter and an antenna would allow this system to receive real signals and not only the ones produced by the signal generators from the laboratory.

The theory and some practical results present in this dissertation could be useful to an implementation with a better substrate, since FR-4 is not indicated for this range of frequencies.

This project is just in the beginning and there are many things yet to be done!

Appendix A

Mixer's Matching Networks

The procedure used to calculate the values of the lumped elements used in the two matching networks of the mixer will be described in this appendix.

A.1 RF input

To match the RF input of the mixer to a 50 Ω load, a L-network will be used since it is the simplest type of matching network. The mixer will receive signals with a frequency range from 2.1 GHz to 2.6 GHz. The impedance match will be calculated to one frequency only, 2.4 GHz, because it is near the center frequency and the manufacturer provides the value of the reflection coefficient at this frequency, which is $\Gamma = 0.81 \angle -44^{o}$. The impedance that corresponds to this reflection coefficient was plotted in the Smith chart depicted in figure A.2 and is represented as point A.

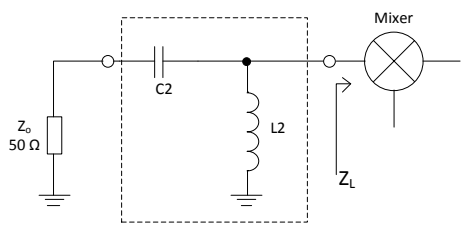


Figure A.1: Mixer RF input matching network

This point corresponds to the Z_L impedance seen into the RF input of the mixer, as represented in figure A.1. This figure also represents the configuration of the L-network used (shunt L and series C) which is the one suggested by the manufacturer [31].

Starting from point A, a shunt inductor (L2) will be added. Adding a shunt element is easier to be done with admittances, so we transform impedance point A into admittance point A'. The shunt inductor L2 was added, and its value is given by:

$$\mathtt{L2} = \frac{Z_o}{2\pi f \cdot (\mathrm{Im}(\mathsf{A'}) - \mathrm{Im}(\mathsf{B'}))} = \frac{50}{2\pi \cdot 2.4 \times 10^9 \cdot (0.4 - (-0.32))} \approx 4.61 \text{ nH} \tag{A.1}$$

The next element to add is the series capacitor C2, and since it is a series element, the admitance point B' was transformed into impedance point B. Starting from this point, we follow the $1 + jx$ circle until we reach the center of the Smith chart (point C). The value of the C2 capacitor is calculated by:

$$\mathtt{C2} = \frac{1}{2\pi f \cdot (\mathrm{Im}(\mathsf{B}) - \mathrm{Im}(\mathsf{C})) \cdot Z_o} = \frac{1}{2\pi \cdot 2.4 \times 10^9 \cdot (2.7 - 0) \cdot 50} \approx 0.49 \text{ pF} \tag{A.2}$$

Both values of the lumped elements from the matching network were approximated to the nearest value in the E24 series. Therefore, the values used were:

$$\mathtt{C2} = 0.5 \text{ pF} \qquad \text{and} \qquad \mathtt{L2} = 4.7 \text{ nH}$$

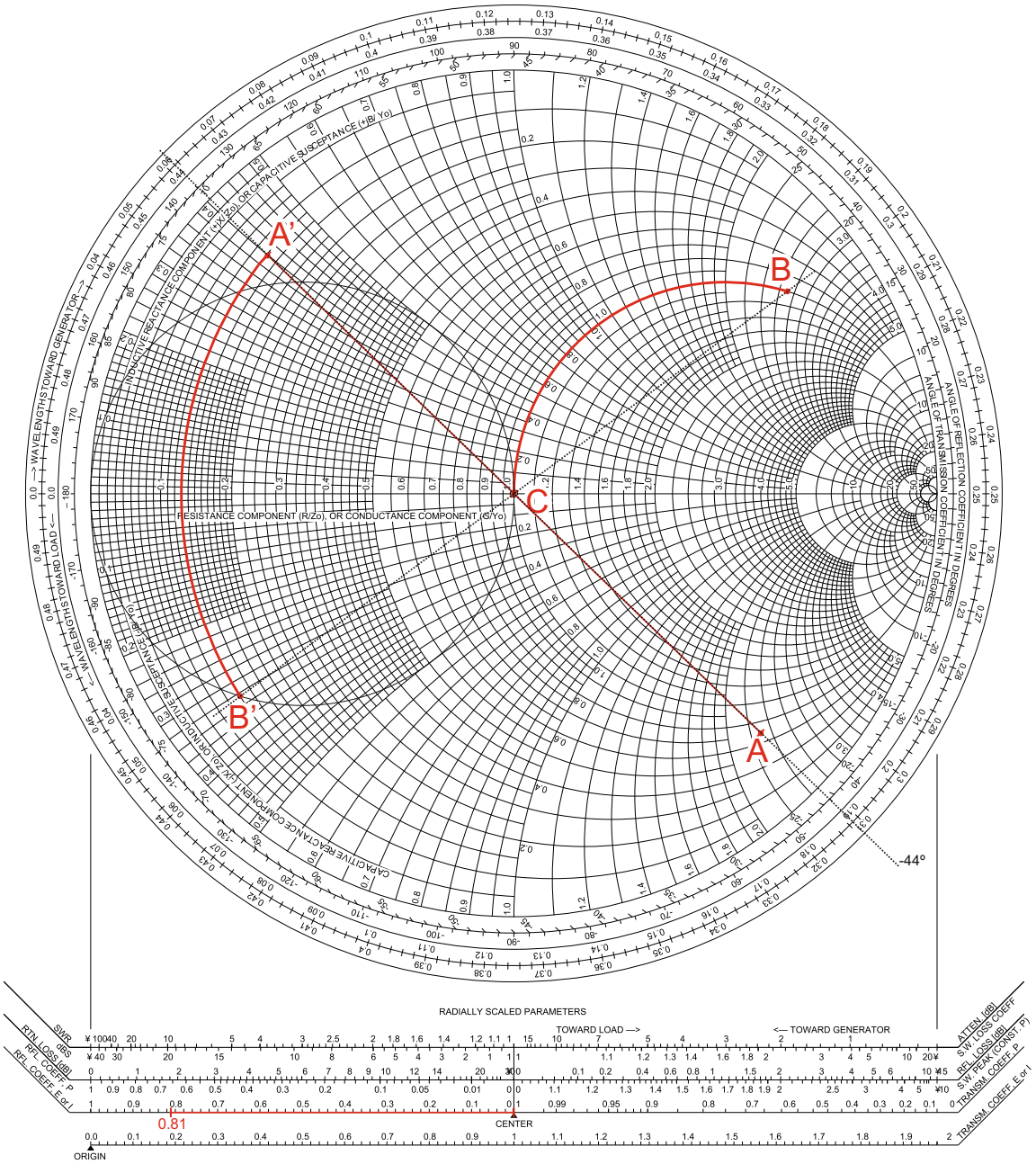


Figure A.2: Mixer RF input matching network

A.2 IF output

A process similar to the one used for the RF input was used to calculate the IF output matching network of the mixer and the corresponding Smith chart is depicted in figure A.4.

The L-network used in this impedance matching is depicted in figure A.3 and is the one suggested by the manufacturer.

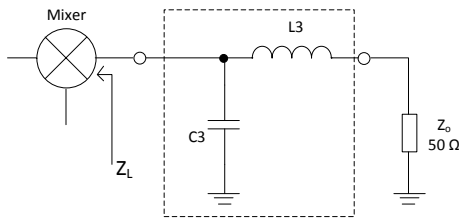


Figure A.3: Mixer IF output matching network

The reflection coefficient for the IF output of the mixer at 100 MHz is $\Gamma = 0.64\angle -8^{o}$ [31]. This is represented as point D in the Smith chart, figure A.4, and corresponds to the impedance Z_L seen into the IF port of the mixer (figure A.3). Next, the capacitor C3 will be added and, since it is a shunt element, the impedance point D will be converted into admittance point D'. Starting from this point, we will move in the circle of constant resistance until we reach the circle of constant conductance, $y = 1+jb$. This point is marked in the Smith chart as point E', and the value of the shunt capacitor is given by:

$$\texttt{C3} = \frac{\text{Im}(\texttt{E'}) - \text{Im}(\texttt{D'})}{2\pi f \cdot Z_o} = \frac{0.42 - 0.07}{2\pi \cdot 100 \times 10^6 \cdot 50} \approx 11.1 \text{ pF} \tag{A.3}$$

To add the series inductor L3, the admitance point E' will be converted into the impedance point E. Then, we move in the constant resistance circle of $z = 1 + jx$ to the center of the Smith chart, point F. The value of the inductor is calculated by:

$$\texttt{L3} = \frac{\text{Im}(\texttt{E}) - \text{Im}(\texttt{F})}{2\pi f} \cdot Z_o = \frac{1.8 - 0}{2\pi \cdot 100 \times 10^6} \cdot 50 \approx 143.2 \text{ nH} \tag{A.4}$$

Once more, the values of the lumped element were approximated to the nearest value in the E24 series. So, the values used were:

$$\texttt{C3} = 10 \text{ pF} \qquad \text{and} \qquad \texttt{L3} = 150 \text{ nH}$$

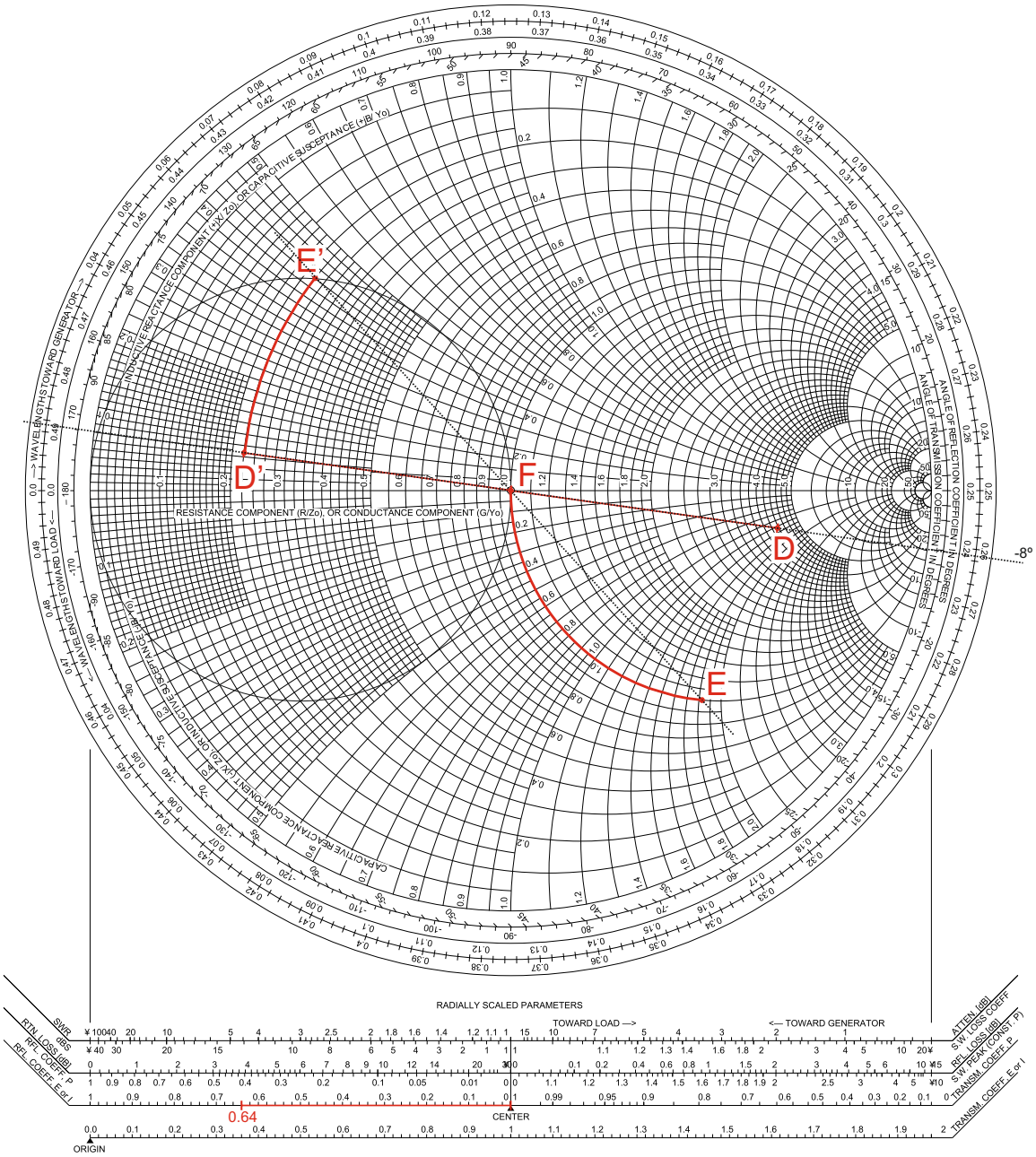


Figure A.4: Mixer IF output matching network

Appendix B

Circuit diagrams & PCB Layouts

For a better presentation of this document, the circuit diagrams and the PCB layouts are presented in this appendix instead of being in the middle of the text in the previous chapters.

The PCB layouts were made in EAGLE software and the simulations and optimizations circuits were performed in ADS software.

NOTE: The PCB layouts represented in this appendix are not at scale. For reference, the PCB dimensions are (width $\times$ height):

- RF stage: 55 $\times$ 67 (mm)
- IF stage: 55 $\times$ 38 (mm)
- IF filter: 40 $\times$ 20 (mm)

B.1 RF Stage

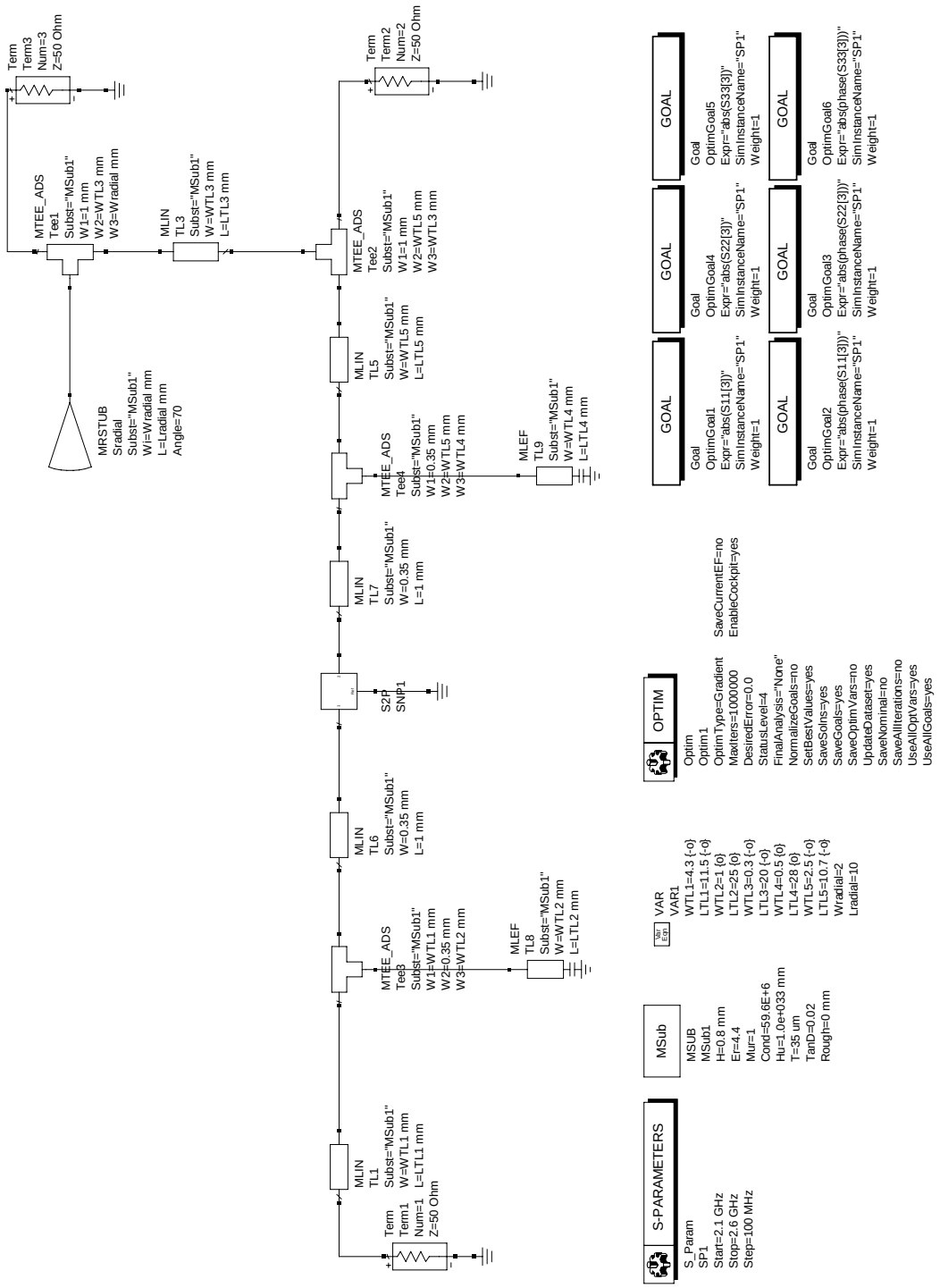


Figure B.1: Simulation of the I/O matching networks and bias circuit of the LNA

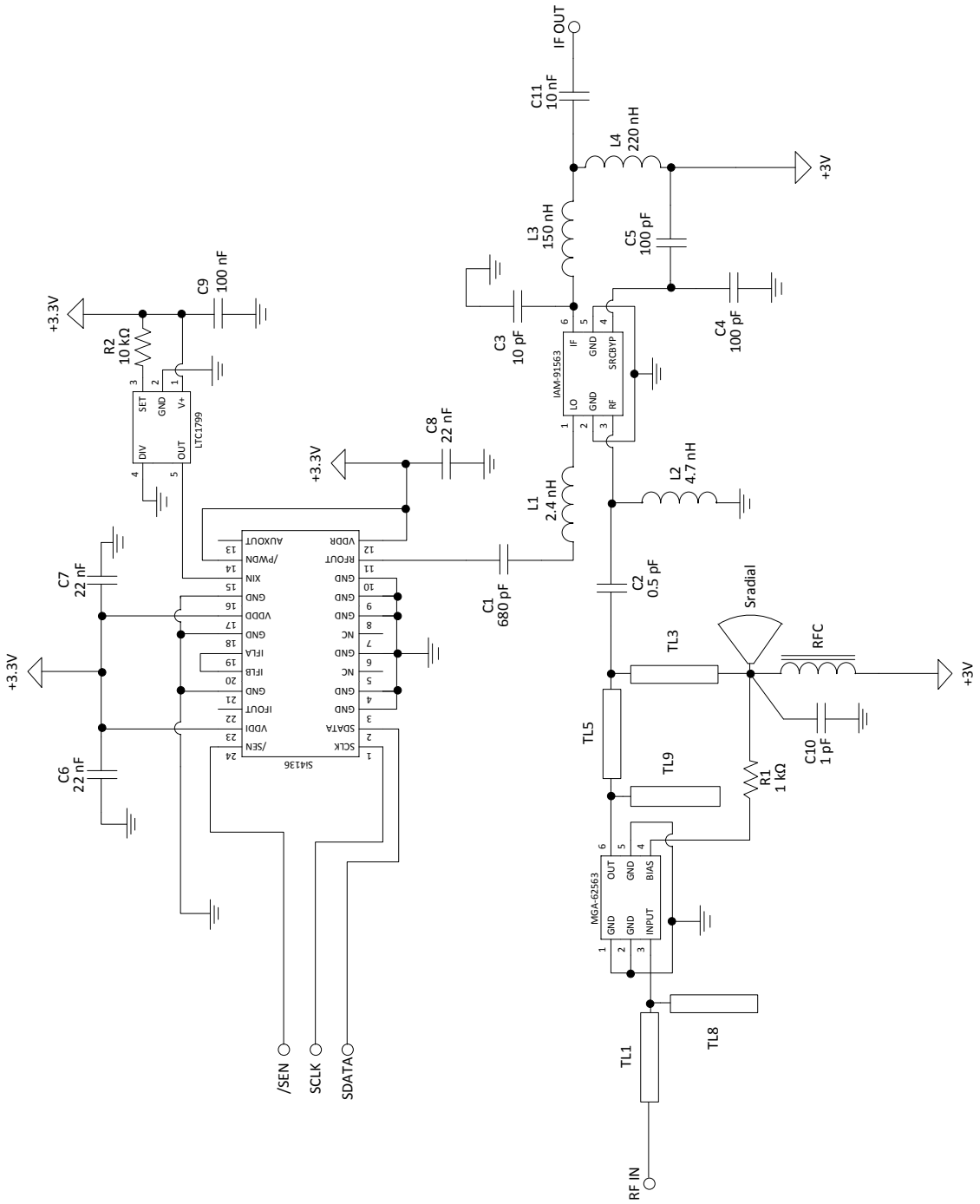


Figure B.2: Circuit diagram of the RF stage

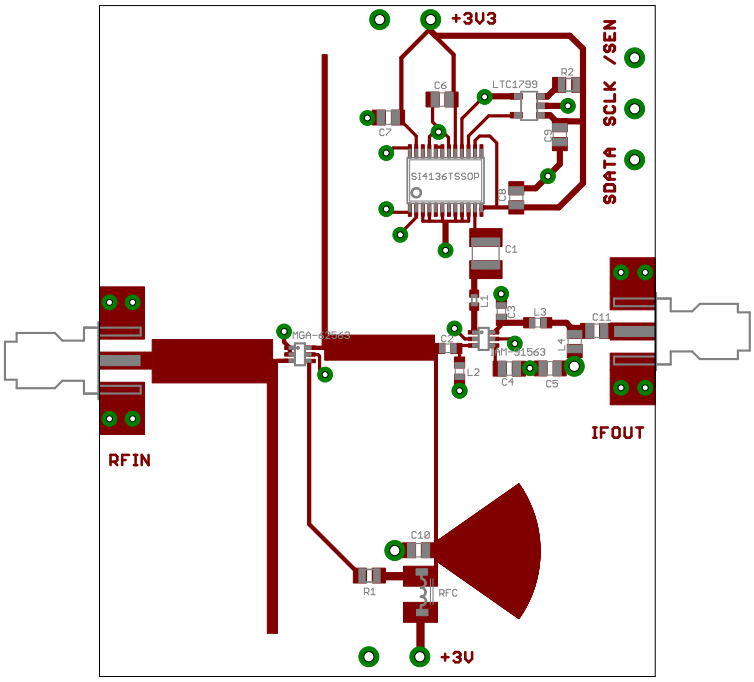


Figure B.3: RF stage PCB layout (top view)

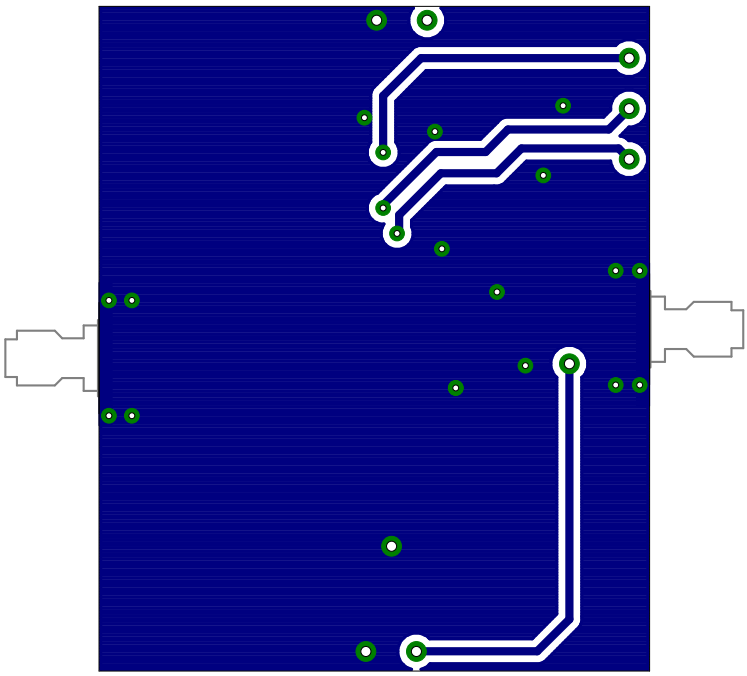


Figure B.4: RF stage PCB layout (bottom view)

B.2 IF Stage

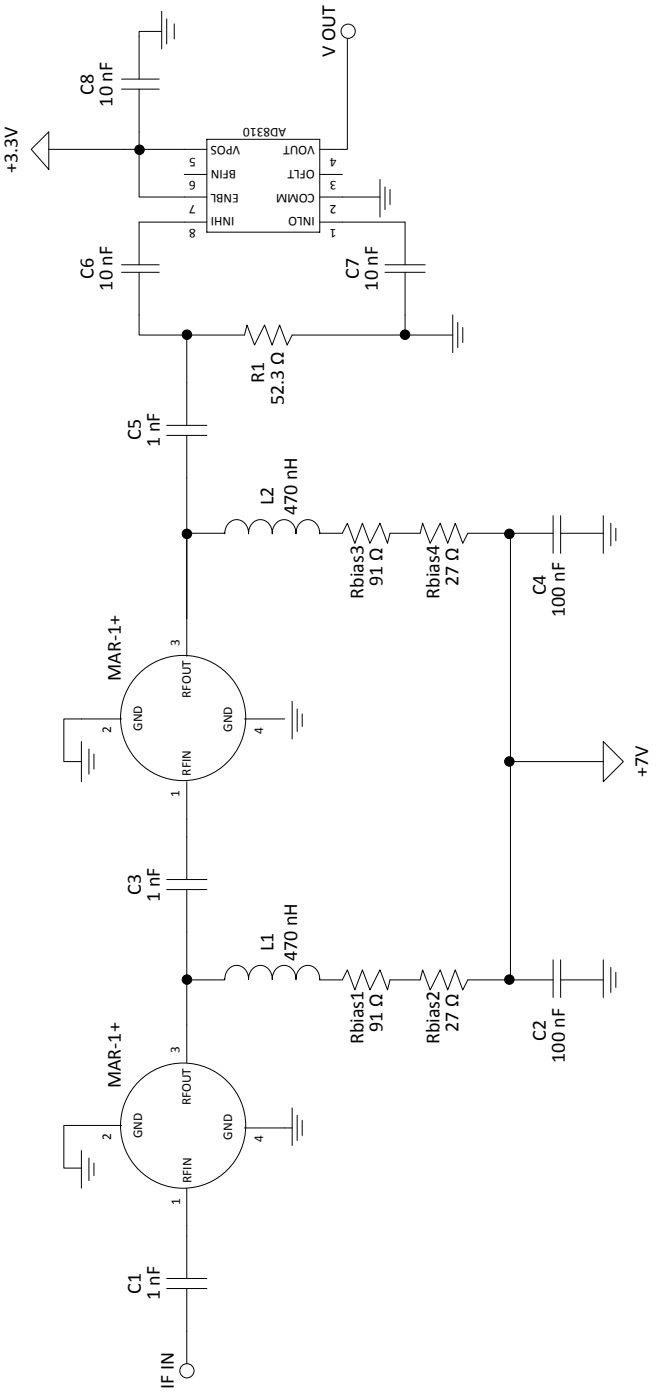


Figure B.5: Circuit diagram of the IF stage

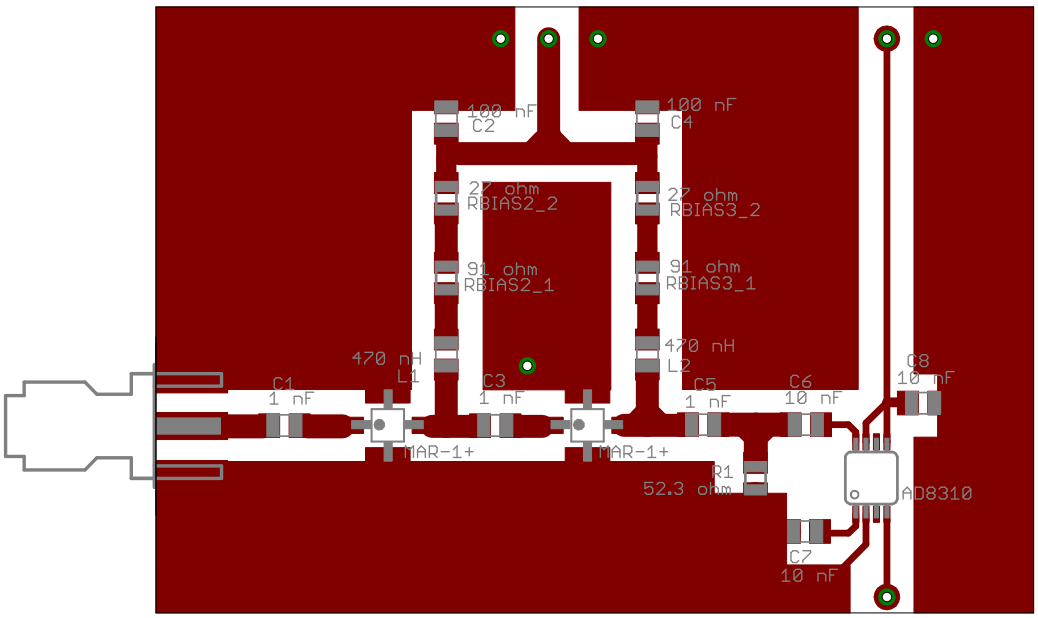


Figure B.6: IF stage PCB layout (top view)

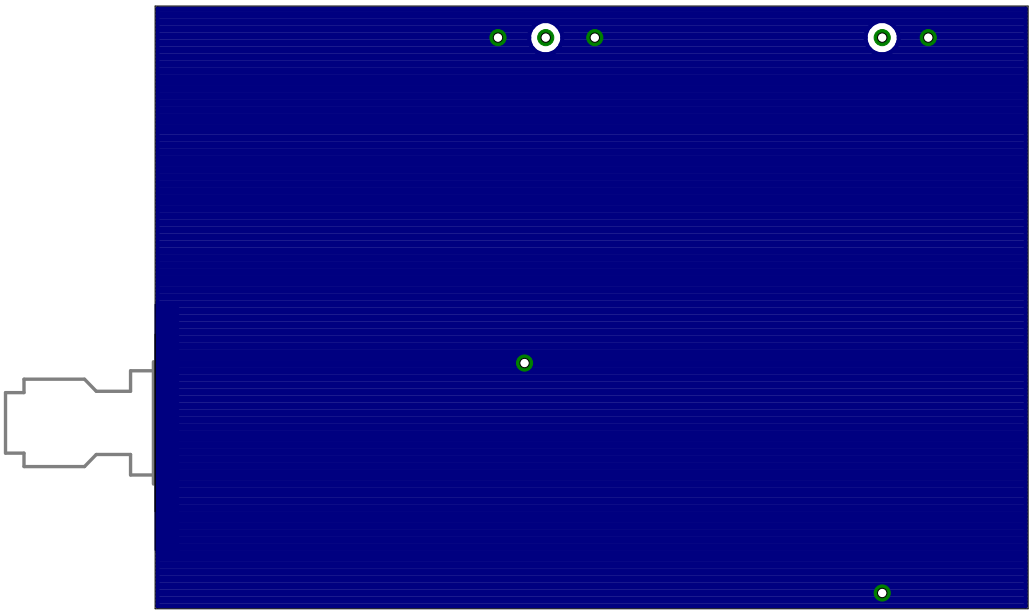


Figure B.7: IF stage PCB layout (bottom view)

B.3 IF Filter

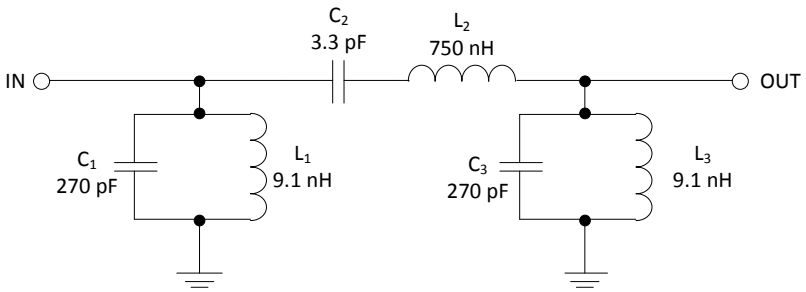


Figure B.8: IF filter circuit diagram

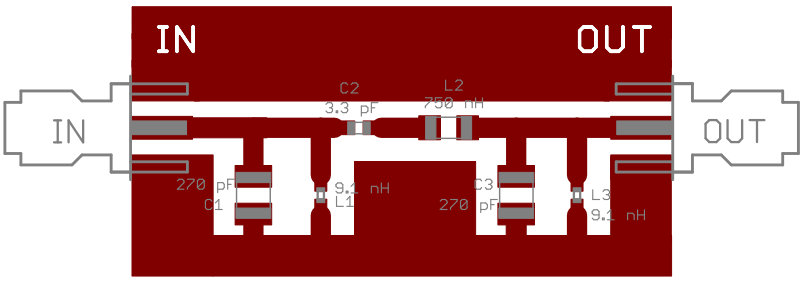


Figure B.9: IF filter PCB layout (top)

Bibliography

[1] Teófilo Monteiro. Projecto de um analisador de espectros baseado em SDR. Master's thesis, Universidade de Aveiro, 2010.

[2] Agilent Technologies. *Spectrum Analysis Basics*, 2004. Application Note 150.

[3] Agilent Technologies website. `http://www.agilent.com/` [cited 26-10-2010].

[4] Agilent Technologies. *Vector Signal Analysis Basics*, 2004. Application Note 150-15.

[5] Jeffrey H. Reed. *Software Radio: A Modern Approach to Radio Engineering.* Prentice Hall, 1st edition, 2002.

[6] Rohde & Schwarz website. Available from: `http://www.rohde-schwarz.com` [cited 1-11-2010].

[7] Jeff Thomas and Terri Hightower. RF Spectrum Analysis Basics. *eSeminar: Back to Basics*, 2003. Agilent Technologies.

[8] Christie Brown. Spectrum Analysis Basics. *Back to Basics Seminar*, 1998. Hewlett Packard.

[9] J. Mitola. The software radio architecture. *Communications Magazine, IEEE*, 33(5):26 –38, May 1995.

[10] R.I. Lackey and D.W. Upmal. Speakeasy: the military software radio. *Communications Magazine, IEEE*, 33(5):56 –61, May 1995.

[11] J. Melby. JTRS and the evolution toward software-defined radio. In *MILCOM 2002. Proceedings*, volume 2, pages 1286 – 1290 vol.2, October 2002.

[12] E. Koski and C. Linn. The JTRS program: software-defined radios as a software product line. In *Software Product Line Conference, 2006 10th International*, pages 10 pp. –191, 2006.

[13] Daniel Albuquerque. "Front-Ends for SDR - State-of-Art". *Department of Electronics, Telecommunications and Informatics*, 2009. University of Aveiro.

[14] R. Schiphorst, F.W. Hoeksema, and C.H. Slump. The front end of software-defined radio: Possibilities and challenges. In *7th annual CTIT Workshop. Mobile Communications in Perspective, Enschede, The Netherlands*, pages 97–100. CTIT, 2001.

[15] National Semiconductor website. Available from: `http://www.national.com/` [cited 25-10-2010].

[16] III Mitola, J. and Jr. Maguire, G.Q. Cognitive radio: making software radios more personal. *Personal Communications, IEEE*, 6(4):13 –18, August 1999.

[17] Jim Hoffmeyer. Next generation radio and spectrum management. In *IEEE 1900 Committee*, 2006.

[18] David M. Pozar. *Microwave Engineering.* Wiley, 3rd edition, 2004.

[19] Jack Smith. *Modern Communication Circuits.* McGraw-Hill, 2nd edition, 1997.

[20] Walter Tuttlebee, editor. *Software Defined Radio: Enabling Technologies.* Wiley, 1st edition, 2002.

[21] J. Crols and M.S.J. Steyaert. Low-if topologies for high-performance analog front ends of fully integrated receivers. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 45(3):269 –282, mar. 1998.

[22] Chris Bowick. *RF Circuit Design.* Newnes, 1997.

[23] Guillermo Gonzalez. *Microwave Transistor Amplifiers: Analysis and Design.* Prentice Hall, 2nd edition, 1996.

[24] José Carlos Pedro and Nuno Borges Carvalho. *Intermodulation Distortion in Microwave and Wireless Circuits.* Artech House, 1st edition, 2003.

[25] Silicon Labs. *Si4136/Si4126 - ISM RF Synthesizer With Integrated VCOs For Wireless Communications*, 2010. Rev. 1.41.

[26] Farnell website. Available from: `http://www.farnell.com/` [cited 5-11-2010].

[27] Linear Technology. *LTC1799 - 1kHz to 33MHz Resistor Set SOT-23 Oscillator*, 2001. 1799fbs.

[28] Avago Technologies. *MGA-62563 Current-Adjustable, Low Noise Amplifier*, August 2008. AV02-1237EN.

[29] B.A. Syrett. A broad-band element for microstrip bias or tuning circuits (short papers). *Microwave Theory and Techniques, IEEE Transactions on*, 28(8):925 – 927, August 1980.

[30] R. Sorrentino and L. Roselli. A new simple and accurate formula for microstrip radial stub. *Microwave and Guided Wave Letters, IEEE*, 2(12):480 –482, December 1992.

[31] Avago Technologies. *IAM-91563 0.8-6GHz 3V Downconverter*, May 2006. 5989-4218EN.

[32] CadSoft EAGLE website. Available from: `http://www.cadsoft.de/` [cited 5-11-2010].

[33] Mini-Circuits. *MAR-1+ Monolithic Amplifier from DC to 1GHz.* Rev. B.

[34] Louis E. Frenzel. *Design FAQs - RF Detectors For Wireless Devices.* Analog Devices.

[35] Analog Devices. *AD8310: Fast, Voltage-Out DC-440MHz, 95dB Logarithmic Amplifier*, June 2005. Rev. E.

[36] George L. Matthaei, Leo Young, and E. M. T. Jones. *Microwave Filters, Impedance-Matching Networks, and Coupling Structures.* Artech House, 1980.