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Telecomunicações e Informática

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Amplificador Doherty e Antena Combinadora

Doherty Amplifier and Antenna Combiner

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações, realizada sob a orientação científica de Doutor Telmo Reis Cunha, Professor Auxiliar do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro.

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O júri / The jury

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Palavras Chave

Amplificador de Potência, Amplificador Doherty, Rádio-frequência, transístores GaN, modulação dinâmica de carga.

Resumo

A arquitetura Doherty convencional é tipicamente utilizada em transmissores sem fios pela sua capacidade de aumentar a eficiência média de um tradicional amplificador em classe B. O amplificador Doherty consiste em dois amplificadores em paralelo (chamados de amplificadores *carrier* e *peaking*) que são ligados, na saída, através de um combinador de $\lambda/4$. Este combinador de saída geralmente tem um impacto significativo na largura de banda do amplificador, pois é tipicamente construído a partir de uma estrutura de linhas de transmissão com dimensões ajustadas para uma frequência. Outras estruturas de combinadores não convencionais podem ser projetadas, visando uma largura de banda maior, contribuindo para um aumento geral da largura de banda do amplificador Doherty. Sendo este um tópico de investigação de elevada relevância para o desenvolvimento de amplificadores de alta eficiência e largura de banda, seria interessante ter um *setup* de laboratório que implemente um amplificador de potência Doherty para o qual estruturas combinadoras distintas possam ser ligadas à saída do amplificador e testadas. Nesse sentido, o projeto de dois amplificadores (*carrier* e *peaking*) foi realizado num simulador de circuitos (ADS, da Keysight) junto com o divisor de potência de entrada que compõe a arquitetura Doherty. A placa principal do amplificador Doherty foi projetada para incorporar os amplificadores *carrier* e *peaking*, e também o divisor de potência na entrada, e foi preparada de modo que pudesse ser ligada a qualquer combinador desejado a ser testado. Um combinador de potência Doherty tradicional foi projetado e ambas as placas (amplificador Doherty e o combinador) foram produzidas, soldadas e testadas no laboratório de RF. O amplificador medido apresentou as características típicas de um amplificador Doherty com aproximadamente 75% de eficiência de dreno na potência máxima e aproximadamente 50% no ponto de *output back-off*. Além disso, foi projetado um segundo combinador com dois objetivos. O primeiro foi demonstrar o funcionamento do amplificador Doherty projetado com um combinador de saída distinto, mostrando que, como pretendido neste trabalho, o amplificador desenhado é adequado para testar múltiplas estruturas combinadoras. O segundo objetivo foi servir como teste preliminar para avaliar a possibilidade de fundir o combinador de saída com a antena. Aproveitando o acoplamento eletromagnético entre antenas, esta segunda estrutura combinadora utiliza duas antenas que foram projetadas para se comportarem simultaneamente como combinador de saída do amplificador Doherty e como elemento radiante.

Keywords

Power Amplifiers, Doherty Amplifier, Radio Frequency, GaN transistors, dynamic load modulation.

Abstract

The conventional Doherty architecture is commonly used in wireless transmitters for its ability to boost the average efficiency of a traditional single-ended class B amplifier. It consists of two parallel single-ended amplifying branches (named carrier and peaking amplifiers) which are linked, at the output, through a $\lambda/4$ combiner. This output combiner commonly has a significant impact on the overall bandwidth, as it is usually built from a transmission line structure with tuned dimensions. Other non-conventional combining structures could be designed, targeting a wider bandwidth, contributing to an overall increase of the Doherty amplifier's bandwidth. Being this an high relevance research topic for the development of high efficient and broadband amplifiers, it is highly desirable to have a laboratory setup that implements a Doherty power amplifier to which distinct output combiner structures can be connected and tested. In that sense, the design of two single-ended amplifiers (the carrier and the peaking) was performed in a circuit simulator (ADS, from Keysight) together with the input power divider that compose the Doherty architecture. The Doherty amplifier main board was designed to incorporate the carrier and peaking amplifiers, and also the power splitter at the input, and it was prepared so that it could be connected to any desired combiner to be tested. A traditional Doherty power combiner was designed and both boards (Doherty amplifier and the combiner) were produced, connected and tested in the RF laboratory. The measured amplifier presented the typical caractheristics of a Doherty amplifier with nearly 75% of drain efficiency at full-power, and nearly 50% at the output back-off level. In addition, a second combiner unit was designed with two purposes. The first was to demonstrate the operation of the designed Doherty amplifier with a distinct output combiner, showing that, as intended in this work, it is suited to test multiple combiner structures. The second objective was to serve as preliminary test to evaluate the possibility of merging the output combiner with the antenna element. Taking advantage of the electromagnetic coupling between antennas, this second combiner structure uses two antenna elements that were tuned to simultaneously behave as output combiner of the Doherty amplifier and a radiating element.

Contents

List of Figures

List of Tables

List of Acronyms

ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
AM	Amplitude Modulation
AM/AM	Amplitude to Amplitude conversion
AM/PM	Amplitude to Phase conversion
CST	Computer Simulation Technology
CW	Continuous Wave
DC	Direct Current
DhPA	Doherty Power Amplifier
DPD	Digital Predistorter
EER	Envelope Elimination and Restoration
EM	Electromagnetic
ET	Envelope Tracking
GaN	Gallium Nitride
GMP	Generalized Memory Polynomial
GSM	Global System for Mobile communications
HEMT	High Electron Mobility Transistor
IMN	Input Matching Network
OBO	Output Back-Off
OFDM	Orthogonal Frequency-Division Multiplexing
OMN	Output Matching Network
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCB	Printed-Circuit Board
PDF	Power Spectral Density
PM	Phase Modulation
RF	Radio Frequency
SCS	Signal Component Separator

SMD	Surface Mount Device
SMA	SubMiniature version A
VNA	Vector Network Analyzer
VSA	Vector Signal Analyzer
VSG	Vector Signal Generator
W-CDMA	Wideband Code Division Multiple Access

CHAPTER 1

Introduction

1.1 Motivation and Context

In wireless communications, with a particular scope on cellular communication networks, a significant effort has been made for improving the efficiency of both mobile devices and base-stations (the transmitters - known for their high energy waste). Since the Radio Frequency (RF) Power Amplifier (PA) is the last element in a transmitter chain, it is also the one that handles the highest power levels. Hence, it is of high importance to increase the efficiency of the PA.

The traditional current mode classes, particularly the class B PA, provide efficient operation and reasonable output power for large signals. However, the efficiency severely decreases when the input signal decreases.

The modulation techniques used in modern comunication systems present high Peak-to-Average Power Ratio (PAPR) (defined in equation (1.1)).

$$PAPR_{dB} = 10log_{10}\left(\frac{P_{peak}}{P_{avg}}\right). \tag{1.1}$$

Therefore, the average power handled by these amplifiers cannot be set to their peak value, but kept several dB below it. As a consequence, their average efficiency is far from desirable levels. To illustrate this, Figure 1.1 depicts the Power Spectral Density (PDF) of the amplitude of two modulated signals (a 2-carrier Wideband Code Division Multiple Access (W-CDMA) and a 6 carrier Global System for Mobile communications (GSM)), superimposed to the efficiency characteristics of ideal class A and class B amplifiers. As can be seen, the signal amplitude region with higher PDF occurs for very low efficiency levels, resulting in an average efficiency that is much below the theoretical maxima.

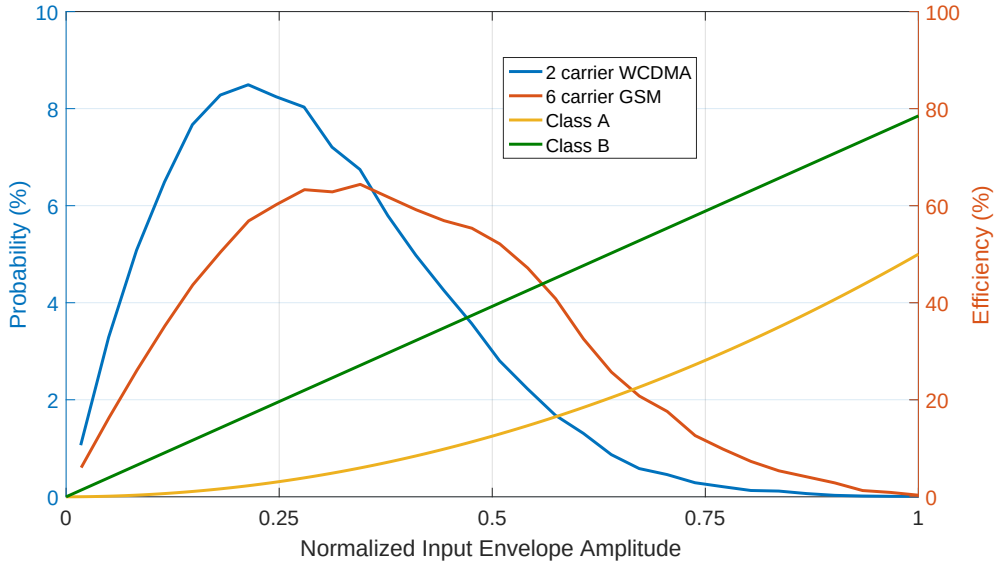


Figure 1.1: Illustration of the low average efficiency achieved in power amplifiers as a consequence of the amplitude PDF of the transmitted signals.

Compensation techniques are commonly used to boost the amplifier efficiency for the region corresponding to the average signal power. Among many, the Doherty architecture has been adopted for several applications, such as cellular base-station transmitters, due to its performance characteristics. The Doherty Power Amplifier (DhPA) consists of a main amplifying branch - usually called the carrier amplifier - which operates in class B or AB, targeted to present maximum efficiency at some output power level (the Output Back-Off (OBO) level) below its peak power, saturating in voltage at that point. A second amplifying branch - the peaking amplifier - is set in parallel with the carrier, biased in class C operation and starting to conduct when the carrier enters saturation. At the output, the carrier and the peaking are connected through a $\lambda/4$ combiner, imposing a varying load impedance to the carrier as the peaking enters further into conduction - the carrier load impedance decreases with the increase of signal amplitude, allowing the carrier to deliver higher current while keeping the same (saturated) voltage and, at the limit, delivering its maximum output power (that also corresponds to its maximum efficiency operation).

One known drawback of the Doherty configuration is its narrow bandwidth, mainly due to the output combiner, traditionally composed of transmission lines with tuned dimensions. However, other non-conventional combiners could also be used in the Doherty setup, which could be able to provide wider bandwidth to the overall amplifier, being this a research topic of high relevance for the development of high efficiency and wide bandwidth amplifiers, especially in the vicinity of the next generation of cellular communications - the 5G - for which bandwidth is required to be very wide and, naturally, efficient energy usage will still be an optimization target.

In this context, it is highly desirable to have a laboratory setup that implements a Doherty power amplifier to which distinct output combiner structures can be connected and tested. This setup would allow testing the behavior of the same Doherty amplifier hardware but with distinct output combiners, permitting a fair comparative analysis (since it would be guaranteed that differences in the measured behavior are exclusively due to the selected output combiners, and not to distinct instantiations of the amplifying branches). The purpose of this work was, therefore, to design, implement and test this Doherty amplifier setup. To provide results that are compatible with foreseen applications for 5G base-stations, in the low GHz region, the center frequency of this Doherty setup was targeted for 4.5 GHz - this frequency is still sufficiently low to permit the use of most of the measurement equipment available in the RF laboratory.

A conventional microstrip output combiner was considered in this work for testing the Doherty amplifier. In addition, as an aside, it was intended to conceive a second combiner that followed a distinct strategy - to incorporate in the same structure the antenna and combiner, taking profit from the electromagnetic coupling between radiating sections to impose the adequate signal combination between carrier and peaking outputs. Besides permitting the test of the Doherty amplifier with a distinct combiner, the idea behind this integrated antenna-combiner was, as a test-of-concept, to give the initial steps towards a circuit that, using the coupling between wide bandwidth radiating elements, could lead to improve the bandwidth of the amplifier. Furthermore, it would contribute to a reduction of the overall size of the transmitter. As will be shown latter, the design of this structure has proved to be quite difficult to achieve, contrary to initial expectations, due to the interdependence of the S-parameters seen by its two ports (one for the carrier output, and another for the peaking output). As this was an aside to the main objective of this work, and considering the lack of an adequate measurement setup in the laboratory (as it would be required to measure the radiated power from the antenna, in several directions, to adequately characterize the overall amplifier characteristics), the design and test of this antenna-combiner structure considered only its implementation in a simulation environment.

1.2 Objectives

As mentioned in the previous section, the main objective of this work was to design, implement and test a Doherty power amplifier that can be connected to distinct output power combiners, permitting, in the future, the study and test of different strategies that may allow improving overall characteristics of this amplifier, such as its bandwidth (a critical feature of this type of amplifiers). This goal implies, naturally,

the accomplishment of secondary objectives. The first one was to acquire knowledge on the operation and design of Doherty amplifiers, which demanded for a thorough study of literature, circuit level simulations, and many discussions with researchers and experts on RF power amplifier design. The second objective was to gain expertise on the (complex) details of the appropriate design techniques of RF power amplifier circuits, and to define and establish the guidelines that pave the way from the amplifier design goals to the implemented circuit. A further secondary objective was to learn and to gain experience on establishing test setups in the RF laboratory and to adequately deal with the available RF instrumentation (including the different steps for calibrating the equipment and the setup measurements), leading to accurate and time efficient amplifier characterization measurements. Finally, it was also a goal to gain specific knowledge on circuit and electromagnetic simulation techniques and state-of-the-art tools.

1.3 Outline

In the first chapter, Chapter 1, the motivation, context and objectives are explained. This first chapter provides an overview of the work developed further on, and the outline of this report is presented.

In Chapter 2, an introduction and brief analysis of some power amplifier topologies are made. The aim of this chapter is to explain and explore the advantages and disadvantages of the described PAs. A special analysis of the working principles and different architectures of the Doherty power amplifier are presented, as this topology is the main focus of this work.

The next chapter, Chapter 3, is dedicated to the Doherty power amplifier development. The design of each element of a DhPA is described. This chapter also includes the simulation results of the amplifier with an ideal and the designed power combiners.

The measurement results of the developed circuits are presented in Chapter 4 as well as the modifications of the original board.

In the final chapter, Chapter 5, conclusions and some final remarks are made. Moreover, to evaluate the implemented solutions, a brief discussion on the developed work is given. This chapter also includes some suggestions for future work.

CHAPTER 2

Power Amplifiers: Performance Enhancement Techniques

2.1 Overview

A power amplifier can be seen as an electronic transducer since it converts Direct Current (DC) power into RF power. Unfortunately, this power conversion is not 100% efficient - part of the power delivered to the PA is dissipated.

Power efficiency must be taken into account during the design of an amplifier, resulting in a more appropriate use of the available supplied power. Likewise, spectrum is one of the most expensive resources because all wireless channels share the same transmission medium (the air interface), so linearity must be preserved.

However, power efficiency and spectral efficiency are conflicting requirements: spectral efficiency demands amplitude modulation linearity and for higher power efficiency, maximized signal excursion is required, leading to nonlinearity [1].

To obtain a good performance in the RF transmitter, the choice of the PA's architecture is crucial. Thus, the characteristics of the architecture must meet the requirements of the type of the signal in terms of linearity, modulation scheme used, PAPR, and so on.

In order to improve efficiency, the conduction angle of the transistor is usually reduced (although it may compromise the linearity). A different approach is to dynamically reduce the DC voltage at the output when its maximum is not required.

2.2 Current and Switching Mode Amplifiers

The current mode operation is based on waveform shaping of the output current of the active device to achieve different compromises between efficiency, linearity and maximum output power. This is the traditional architecture for celullar base-station applications, not only for its simplicity, but also for its ability to amplify constant envelope signals, such as single carrier GSM signals in a second generation system.

The ideal generic structure of a current mode PA is presented in Figure 2.1.

Since the harmonic content in the output current is quite high for some biasing points, a resonant circuit at the output is required to obtain linear amplification. This resonant circuit is tuned to the fundamental frequency - the PA output will have R_L as the load impedance - and short-circuits all the harmonic frequencies.

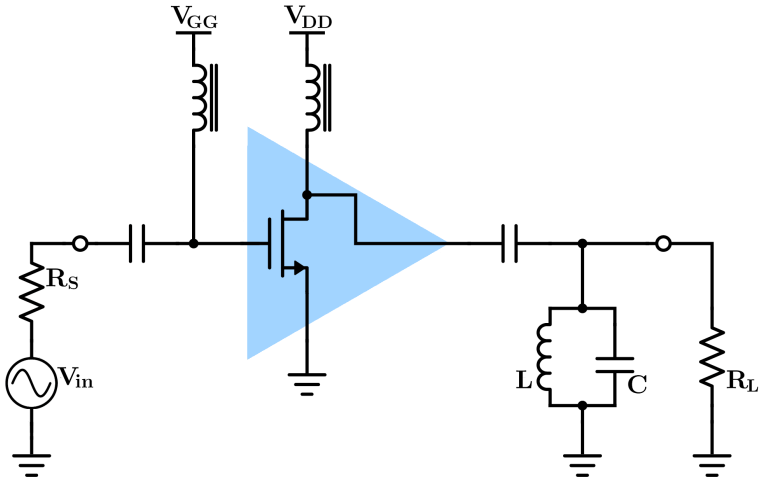


Figure 2.1: Current mode amplifier schematic.

Changing the bias point of the transistor will lead to different current mode classes with specific characteristics in terms of linearity, efficiency and maximum output power.

Class A is the most linear one - the harmonic content is very low [2]. However, it is the least efficient class - it is consuming power even when no signal is being amplified since the transistor is biased in conduction. This class is only used when very high linearity amplification is required.

In class B, the bias point is at the threshold voltage of the device - the transistor is in the cut-off region if there is no input signal and starts conducting when there is a positive signal variation. This will produce an higher efficiency than class A amplification, yet with lower small-signal gain [2].

Biasing the transistor between class A and class B leads to class AB, which is a compromise between the former two - it has an higher efficiency and lower small-signal gain than class A and higher small-signal gain and lower efficiency than class B.

The bias point in class C is below the threshold voltage of the device. Although it is the most efficient of the previous classes, it is also the most nonlinear one making it unsuitable for amplitude modulation applications.

Figure 2.2 shows the relation between output current and input voltage for current mode classes (assuming an idealized transistor behavior), and Table 2.1 the conduction angle range and maximum theoretical efficiency for each class.

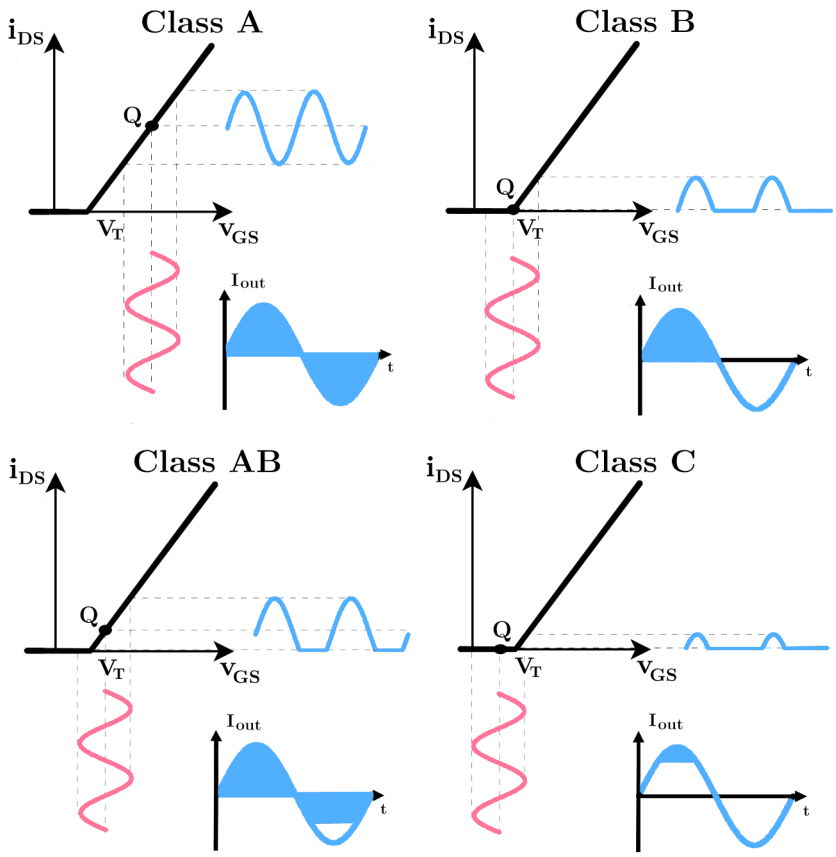


Figure 2.2: Transistor output current versus input voltage for classes A, B, AB and C.

Class	Conduction Angle (2θ)	Maximum Efficiency
A	360^o	50%
AB	$360^o > 2\theta > 180^o$	$50\% < \eta_{Max} < 78.5\%$
B	180^o	78.5 %
C	$180^o > 2\theta > 0^o$	$78.5\% < \eta_{Max} < 100\%$

Table 2.1: Conduction angle and maximum theoretical efficiency for classes A, AB, B and C.

In order to produce a linear yet efficient amplifier, class B amplification can be selected for its simplicity as it can be proved to be linear [3] and it has an ideal maximum efficiency of 78.5%.

Some amplifier architectures use the transistor as a switch to take profit of its maximum efficiency. As a switch, when the transistor is on, the drain-to-source voltage is almost zero and high current is flowing through the device - the device acts as a low resistance. When the transistor is off, the current is zero and the voltage across the device is high - the transistor acts as an open circuit [4].

The class D amplifier, proposed in 1959 [5], operates with two active devices and a square signal at its input. At the output, the signal is filtered with an harmonically tuned filter. A simplified schematic of this amplifier in a complementary voltage-switching configuration can be seen in Figure 2.3a. The input transformers create a phase difference of 180^o between the two switches. This amplifier can operate at low RF frequencies [6], offering high power and efficiency. However, for higher frequencies the parasitic effects and drive requirements limit its viability [7].

The class E PA was initially introduced in 1975 [8]. It consists of a single switch, a DC feed and a filter. Figure 2.3b shows a simplified schematic of this amplifier. When the switch is on, the inductor is charged and the output voltage remains zero. When the switch is off, a pulse of the current previously stored in the inductor is applied to the output filter. The output filter is designed to ensure two conditions [8]:

- Zero Voltage Switching - the voltage across the switch should reach zero just before the switch closes, i.e., just before current starts to flow through the transistor. This allows the output capacitor to have no stored energy, avoiding dissipation in the transistor.
- Zero Slope Voltage Switching - when the transistor switches from the off state to the on state, the derivative of the voltage must be zero, allowing a phase shift without compromising the efficiency.

In the class E amplifier, the effects of the transistor parasitics are taken into account in the output filter design, solving the problem of the class D amplifier. However, high non-linearity and the complexity of the output filter are the main issues of the class E PA [2].

The class F amplifier (1958 [9]) relies on harmonic control to obtain a square voltage wave at the output. The output network is designed to present to the drain of the transistor:

- the optimum load (for efficiency and/or delivered power) at the fundamental frequency;
- a short circuit at all even harmonics;
- an open circuit at all odd harmonics.

Figure 2.3c shows a simplified schematic of a class F amplifier.

Due its high efficiency capability, the class F amplifier has received considerable attention in the literature over the past few years [10]–[12] .

Likewise, its dual, the inverse class F, is a very considered approach [13]–[15]. In the F^{-1} PA, the output network generates a square wave of current by presenting a short circuit at all odd harmonics and an open circuit at all even harmonics.

In a practical class F PA, it is impossible to indefinitely increase the number of filters. Additionally, at higher harmonic frequencies, the behaviour of the system is degraded - the output waveforms diverge from the ideal squared ones resulting in an increase of the dissipated power, and so, a decrease of efficiency.

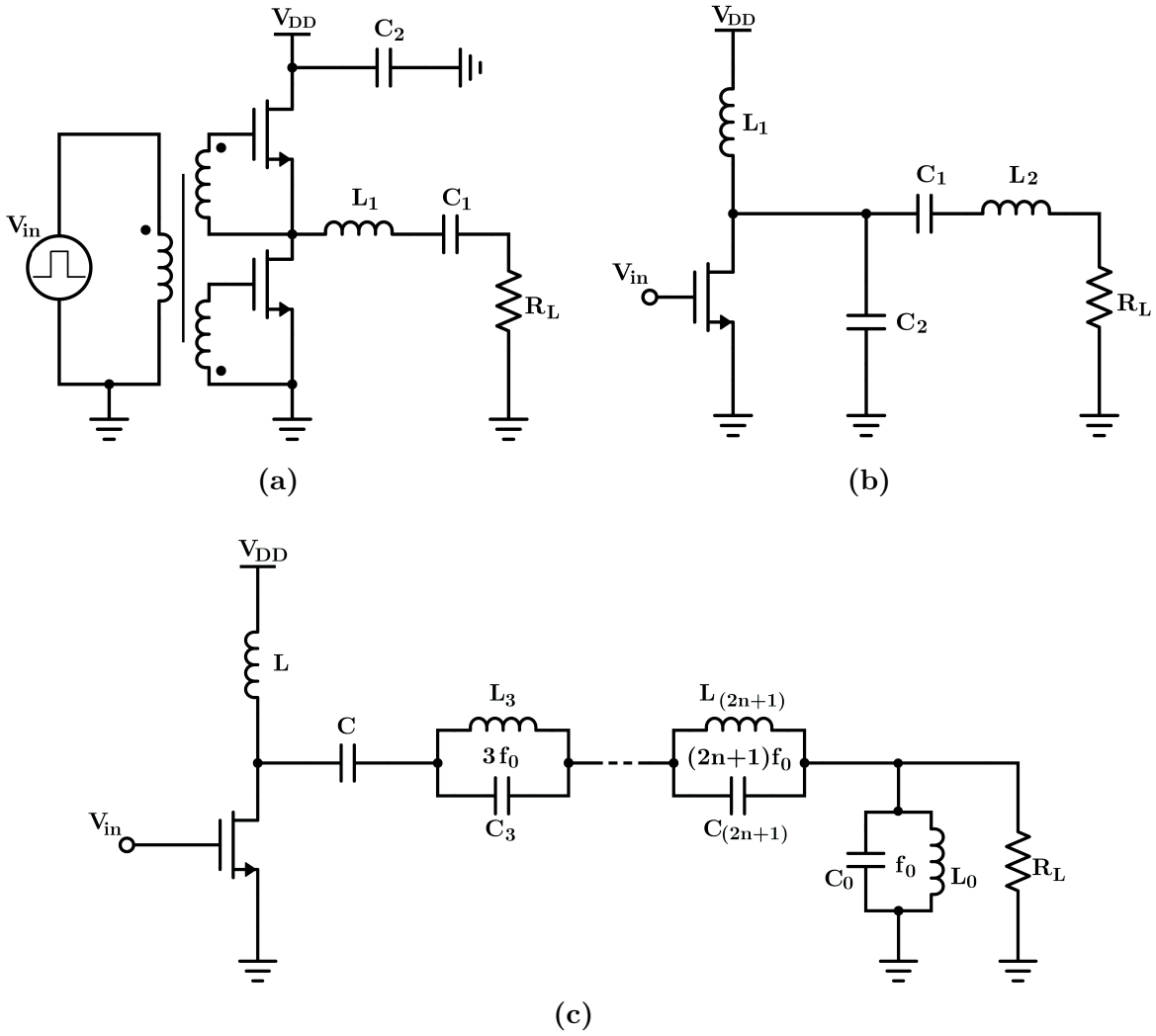


Figure 2.3: Amplifiers in different classes of operation: (a) class D; (b) class E; (c) class F.

Compared to current mode PAs, switching mode amplifiers can reach higher efficiencies (ideally 100%). However, their design becomes more demanding, especially for higher frequencies.

2.3 Efficient Architectures

The classic class B amplifier offers efficient operation when the envelope of the signal is close to the peak power. However, when the PAPR increases the amplifier becomes less efficient, for example for a W-CDMA signal the average efficiency is typically in the range of 15-25% [3].

There are some techniques to boost the efficiency in which the architecture of the amplifier may use more than a single transistor.

The efficiency enhancement techniques in power amplifiers can be divided in two groups: DC supply modulation and load modulation. The DC supply modulation is composed of two techniques: Envelope Tracking (ET) and Envelope Elimination and Restoration (EER).

In this section, a brief introduction of these techniques is presented.

2.3.1 Envelope Tracking

In the Envelope Tracking architecture, the power supply of the amplifier is modulated. Following the signal envelope, by reducing the supply voltage from its maximum value, ensures that the device stays in an efficient operating region (near saturation), decreasing the dissipated energy. Figure 2.4 shows the block diagram of this architecture.

Although the amplifier is operating in a linear mode - class B, for example - the overall efficiency is higher when compared to the constant supply case [16].

A comparison between conventional and ET amplification can be found in Figure 2.5 and the bias modulation principle is displayed in Figure 2.6.

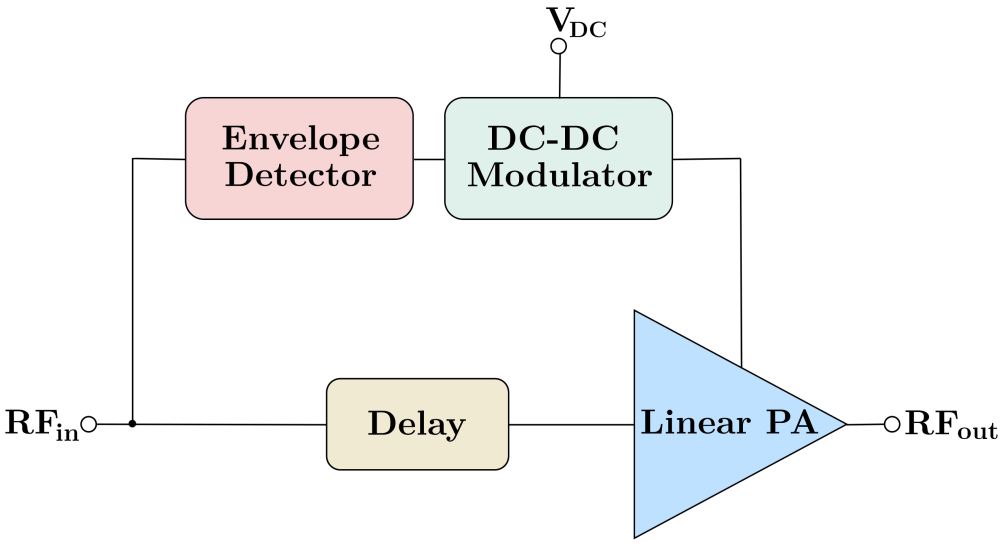


Figure 2.4: Envelope Tracking block diagram.

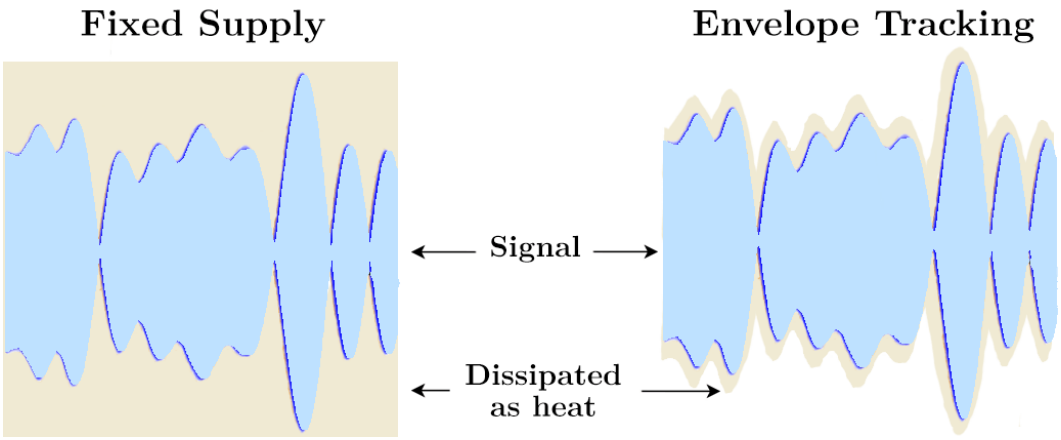


Figure 2.5: Comparison between conventional and ET amplification.

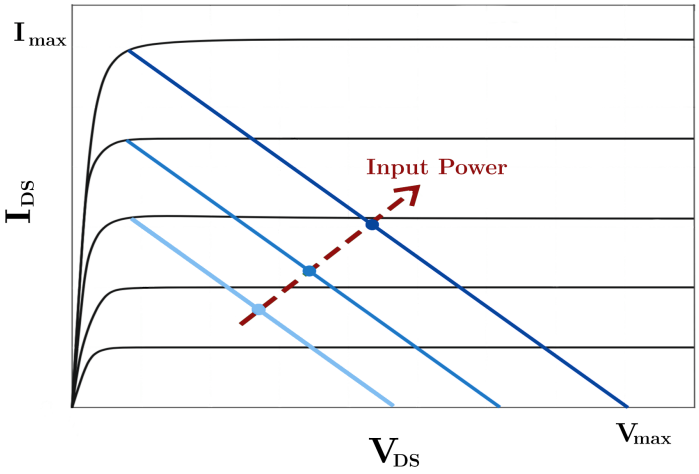


Figure 2.6: Power supply modulation principle: the load line is shifted according to the input signal, maintaining a constant slope.

2.3.2 Envelope Elimination and Restoration

Kahn's technique or Envelope Elimination and Restoration was introduced in 1952 [17] and its working principle is identical to that of ET but, instead of a linear amplifier, it operates with a switching mode amplifier - the main amplifier receives a signal that is only modulated in phase.

The efficiency of the EER technique lies on the switching mode PA used and its highly efficient power supply. Power losses on the transistor are lower in switching PAs, when compared to current mode PAs, and, using the EER technique, the efficiency of the system does not depend heavily on the level of the input signal. Figure 2.7 shows the EER block diagram.

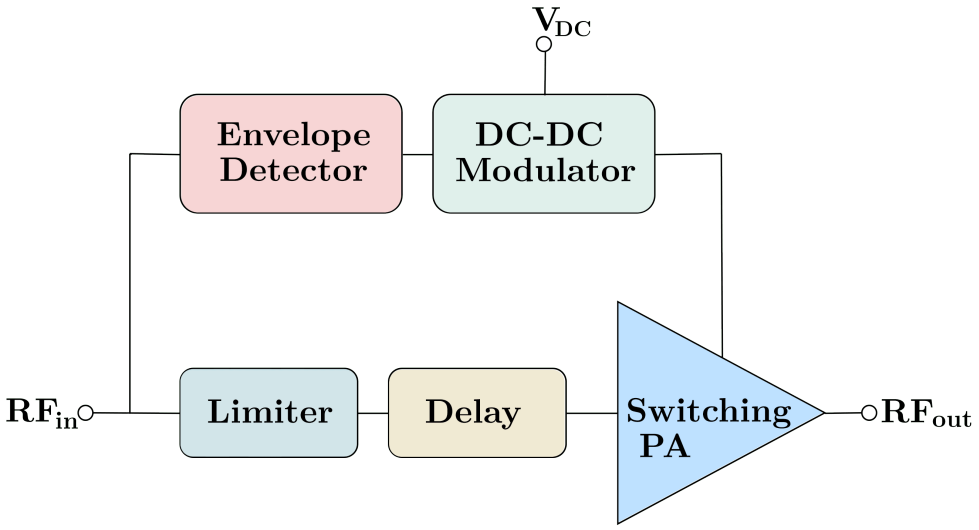


Figure 2.7: Envelope Elimination and Restoration block diagram.

2.3.3 Load Modulation

Load modulation is a technique that aims to improve the drain efficiency by changing the effective load impedance seen by the transistor, as illustrated in Figure 2.8.

The most popular load modulation applications in power amplifiers are the Doherty Power Amplifier [18], whose operating principle will be explained in the next section, and the Chireix outphasing amplifier [19].

In the original concept of the outphasing amplifier, Figure 2.9, the Signal Component Separator (SCS) network transforms the AM signal into two constant envelope PM signals with opposite phase. The signals are amplified and combined resulting in an AM signal. The PAs can operate in a switching mode, since the signals have a constant envelope, resulting in high efficiency.

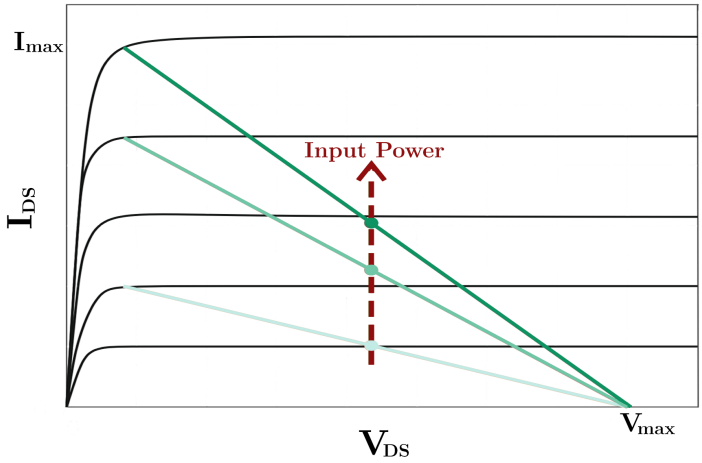


Figure 2.8: Load modulation principle: the slope of the load line is changed according to the input signal.

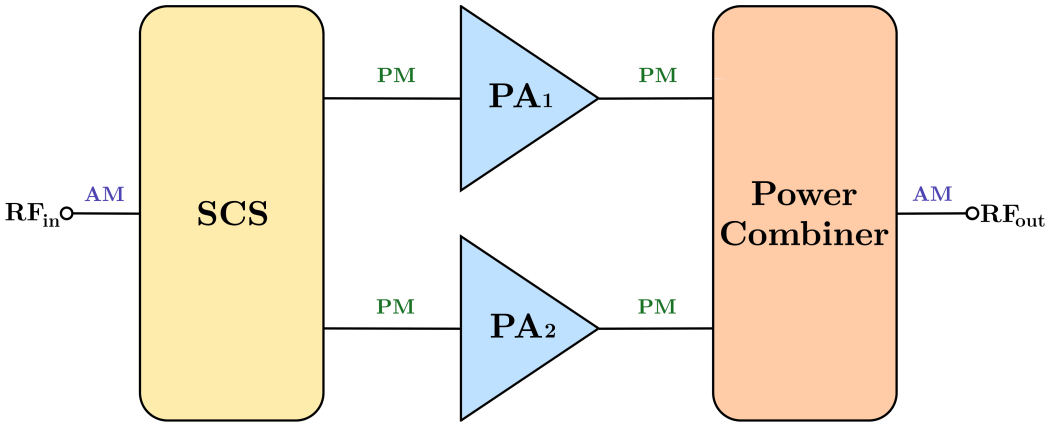


Figure 2.9: Outphasing PA block diagram.

2.4 The Doherty Power Amplifier

The Doherty power amplifier was proposed in 1936 by William. H. Doherty [18], as a way to improve the average efficiency in power tubes. It consists of two amplifiers connected by an impedance inverter network, Figure 2.10. This topology was almost forgotten for decades but, recently, it was rediscovered.

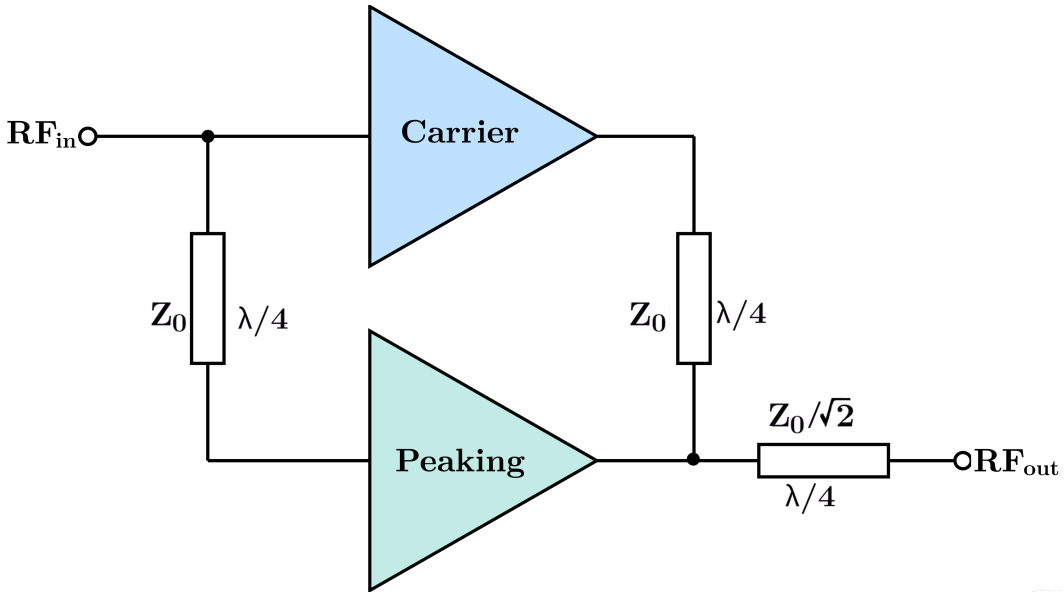
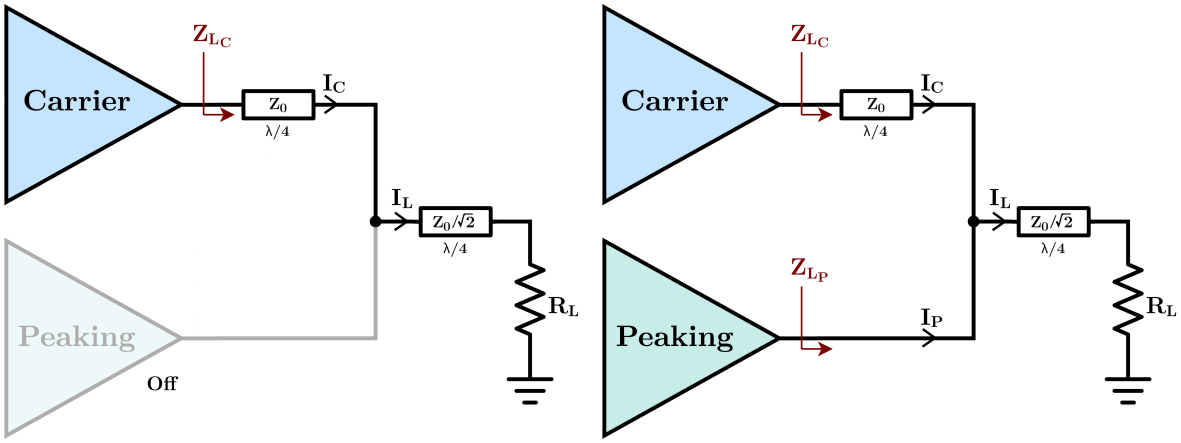


Figure 2.10: Structure of the traditional DhPA.

When the transistors were created, the power tubes were replaced by the solid state devices in several applications. However, the latter were much far from the ideal current sources and the DhPA no longer worked satisfactorily (especially from the overall linearity view point). Nevertheless, nowadays, this architecture is widely adopted in mobile telecommunication transmitters. Digital signal processing started to be used

and it became possible to correct some imperfections introduced by the transistors in the DhPA, with the inclusion of digital predistortion.

The underlying concept of this architecture is to increase the signal excursion, for lower input signals, at the output of a traditional class B PA - which is called the Carrier PA - Figure 2.11a. When the amplitude of the envelope is higher and the carrier PA starts to compress, an extra power is added from an auxiliary PA - called the Peaking PA (since it only operates at the peaks) - Figure 2.11b. As this auxiliary PA is connected to the main one, it is seen as an active load performing the Doherty dynamic load modulation of the carrier PA - it modulates the carrier load according to the input envelope.



(a) Low power region. **(b)** Doherty region.

Figure 2.11: Illustrative diagram of the two operation stages of the DhPA.

The carrier PA is biased in class B and is typically designed to have a higher load impedance than a conventional single-ended PA. The peaking PA is biased in class C - only operates for higher input power levels - and its biasing point is tuned so it enters into conduction when the main amplifier starts to saturate. The current injected into the load by the peaking PA, I_P, and the inverting network (represented in the Figures 2.10 and 2.11 as a quarter-wavelength line, $\lambda/4$) cause the impedance seen by the carrier PA, Z_{LC}, to decrease. Therefore, the slope of the load line of the main PA increases, keeping it near saturation for higher input power levels and, this way, increasing its efficiency for a larger range of output power.

Due to the quarter-wavelength line, a phase delay of 90^o is introduced at the output of the carrier PA. In order to have the currents of the carrier and peaking PAs in phase at the load, a phase lag of 90^o is also added at the input of the peaking amplifier. After the input power splitter that divides the power equally (or unevenly) by the two amplifiers, the line length for the peaking amplifier is $\lambda/4$ longer than that of the carrier amplifier.

To further analyze the load modulation principle in the DhPA, an equivalent schematic of the output part of this amplifier can be seen in Figure 2.12a.

The carrier amplifier is represented by an ideal current source, where $I_C(t) = \frac{1}{2}G_m V_i(t)$, and the peaking amplifier is represented by an ideal current source, whose current is dependent on I_C: $I_P(t) = -j\alpha I_C(t)$ and α is a factor that depends on V_i and varies from 0 to 1. In fact, the dependence of α on the input voltage $V_i(t)$ can be easily determined by assuming that both carrier and peaking PAs deliver the same maximum current, I_{max}, and, as mentioned before, the peaking enters into conduction only from $V_{i_{max}}/2$ (assuming the typical 6 dB backing off, as will be described below). Thus, as these ideal I_C and I_P current sources produce currents that are linear with V_i, these follow the trends shown in Figure 2.13.

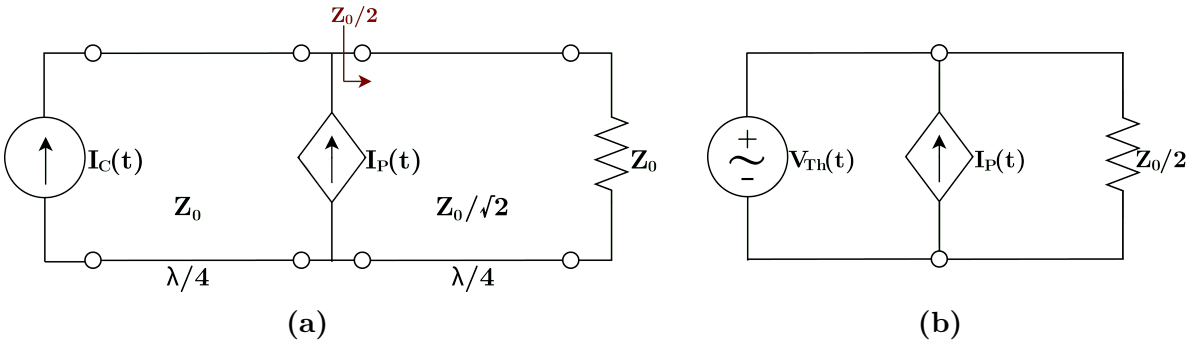


Figure 2.12: Equivalent schematic of a DhPA (a), and the Thévenin equivalent of the carrier PA (b).

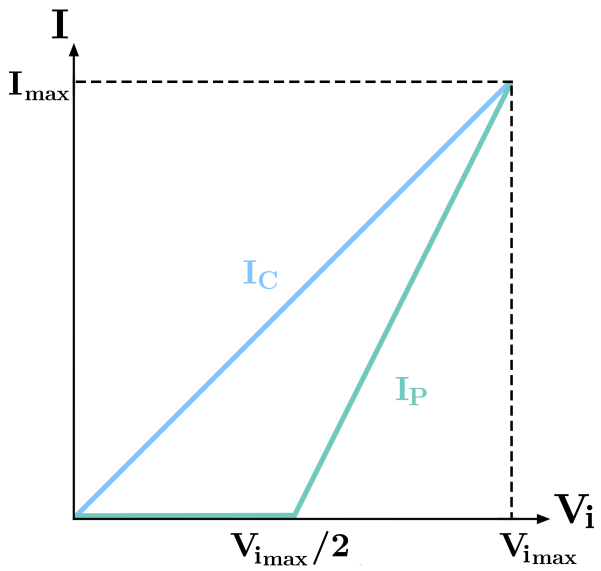


Figure 2.13: Current of carrier and paking PAs.

Using the line equations of Figure 2.13, the evolution of α with V_i is:

$$\alpha \equiv \frac{|I_P|}{|I_C|} = \begin{cases} 0, & 0 \leq V_i < \dfrac{V_{i_{max}}}{2} \\ \dfrac{2V_i - V_{i_{max}}}{V_i}, & \dfrac{V_{i_{max}}}{2} \leq V_i \leq V_{i_{max}}. \end{cases} \tag{2.1}$$

In the quarter-wavelength transformer between the carrier and peaking PAs, in Figure 2.12a, the currents and voltages (both incident and reflected) are [20]:

$$\begin{aligned} V(x) &= V_i(x) + V_r(r) = V_1 e^{-j\beta x} + V_2 e^{+j\beta x}, \\ I(x) &= I_i(x) - I_r(r) = \frac{V_1}{Z_0} e^{-j\beta x} - \frac{V_2}{Z_0} e^{+j\beta x}, \end{aligned} \tag{2.2}$$

where $\beta = \frac{2\pi}{\lambda}$.

The Thévenin equivalent of the main amplifier and the quarter-wavelength line, Figure 2.12b, can be calculated from:

$$\begin{aligned} I(0) &= \frac{V_1}{Z_0} - \frac{V_2}{Z_0} = I_C \rightarrow V_2 = V_1 - Z_0 I_C \\ I(l) &= \frac{V_1}{Z_0} e^{-j\frac{\pi}{2}} - \frac{V_2}{Z_0} e^{+j\frac{\pi}{2}} = 0 \rightarrow V_2 = -V_1 \end{aligned} \quad \rightarrow \quad V_1 = -V_2 = Z_0 \frac{I_c}{2}, \tag{2.3}$$

$$V(l) = V_1 e^{-j\frac{\pi}{2}} + V_2 e^{+j\frac{\pi}{2}} = -2jV_1 = V_{Th}, \tag{2.4}$$

$$\begin{aligned} V_{Th} &= -jZ_0 I_C, \\ Z_{Th} &= 0. \end{aligned} \tag{2.5}$$

Also, the load impedance when seen from the junction point can be obtained from:

$$Z_{L_J} = \frac{Z_T^2}{Z_L} = \frac{(\frac{Z_0}{\sqrt{2}})^2}{Z_0} = \frac{Z_0}{2}. \tag{2.6}$$

The dynamic load impedance seen by the peaking PA, Z_{L_P}, is:

$$Z_{L_P} = \frac{V_{Th}}{I_P} = \frac{-jZ_0 I_C}{-j\alpha I_C} = \frac{Z_0}{\alpha}. \tag{2.7}$$

Since the current at the load is given by $I_L = \frac{V_{Th}}{Z_L} = 2\frac{V_{Th}}{Z0} = -j2I_C$, the dynamic load impedance seen by the carrier amplifier, Z_{L_C}, is that seen by Thévenin source and transformed by the quarter-wavelenght line:

$$Z_{L_C} = \frac{Z_0^2}{V_{Th}/(I_L - I_P)} = \frac{Z_0^2}{-jZ_0 I_C/(-j(2-\alpha)I_C)} = (2-\alpha)Z_0 \tag{2.8}$$

As the α varies from 0 to 1 with the increase of the input power, the dynamic load impedance of the carrier PA changes from $2Z_0$ to Z_0, while the the dynamic load impedance of the peaking PA varies from ∞ to Z_0.

The output power of each amplifier can also be calculated:

$$\begin{aligned} P_{out_C} &= \frac{1}{2} R_{L_C} |I_C|^2 = \frac{1}{8}(2-\alpha) R_0 G_m^2 V_i^2, \\ P_{out_P} &= \frac{1}{2} R_{L_P} |I_P|^2 = \frac{1}{8} \alpha R_0 G_m^2 V_i^2, \end{aligned} \tag{2.9}$$

where R_{L_C}, R_{L_P} and R_0 are the real part of Z_{L_C}, Z_{L_P} and Z_0, respectively.

The total output power, at the load, is the sum of the former two:

$$P_{out_L} = P_{out_C} + P_{out_P} = \frac{1}{4} R_0 G_m^2 V_i^2. \tag{2.10}$$

Despite both carrier and peaking PAs are nonlinear with the input power (V_i^2) in the Doherty region (as P_{out_C} and P_{out_P} depend on α, which in turn is a function of V_i), the overall conceptual Doherty amplifier is linear with V_i^2. The contribution of the P_{out_P} is exactly the one required so that $P_{out_C} + P_{out_P}$ is proportional to the input power. Naturally, beyond P_{max}, both amplifiers saturate, Figure 2.14.

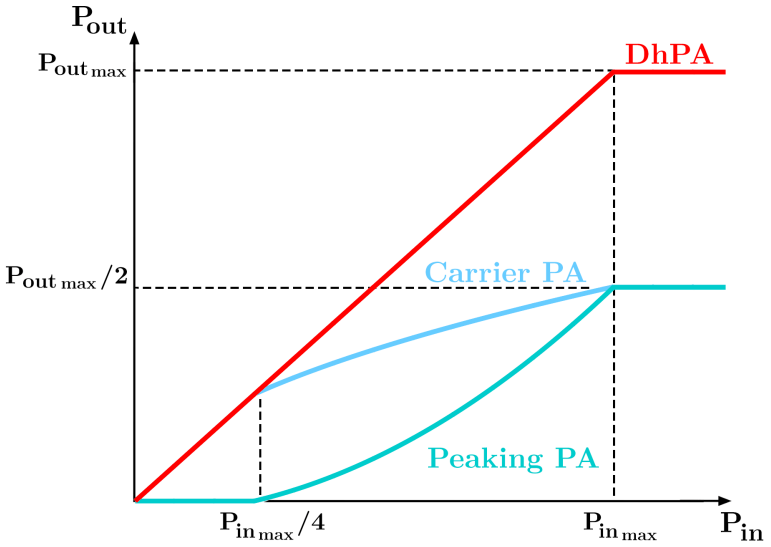


Figure 2.14: Output power as a function of the input power for the carrier, peaking and overall DhPA.

Lastly, to calculate the efficiency of the DhPA, the DC power of each amplifier needs to be determined, which, knowing that the average current of a half-sinusoidal waveform (assuming pure class B operation) is equal to its peak valued times $2/\pi$, are given by:

$$\begin{aligned} P_{DC_C} &= V_{DC_C} \frac{G_m V_i}{\pi}, \\ P_{DC_P} &= V_{DC_P} \alpha \frac{G_m V_i}{\pi}. \end{aligned} \tag{2.11}$$

If $V_{DC_C} = V_{DC_P} = V_{DC}$:

$$P_{DC_T} = P_{DC_C} + P_{DC_P} = (1+\alpha) V_{DC} \frac{G_m V_i}{\pi} = V_{DC} \frac{G_m}{\pi} (3V_i - V_{i_{max}}), \tag{2.12}$$

Considering $V_{DC} = \frac{V_{max}+V_K}{2}$ and $R_0 = \frac{V_{max}-V_K}{I_{max}}$ (where V_K is the knee voltage of the transistor), the efficiency of the DhPA is:

$$\eta_T = \frac{P_{out_L}}{P_{DC_T}} = \frac{\pi}{4}\frac{1}{1+\alpha}\frac{R_0}{V_{DC}}G_m V_i = \frac{\pi}{4}\frac{V_{max}-V_K}{V_{max}+V_K}\frac{2V_i^2}{V_{i_{max}}(3V_i - V_{i_{max}})}. \tag{2.13}$$

The latter expression has two maxima and one minimum, Figure 2.15:

$$\begin{cases} \eta_{max} = \dfrac{\pi}{4}\dfrac{V_{max}-V_K}{V_{max}+V_K}, & \text{when } V_i = \dfrac{V_{i_{max}}}{2} \text{ and } V_i = V_{i_{max}}, \\ \eta_{min} = \dfrac{\pi}{4}\dfrac{V_{max}-V_K}{V_{max}+V_K}\dfrac{8}{9}, & \text{when } V_i = \dfrac{2}{3}V_{i_{max}}. \end{cases} \tag{2.14}$$

Figure 2.16 shows a comparison between the efficiency as a function of the normalized input envelope amplitude for class A, class B, ET, EER and DhPA.

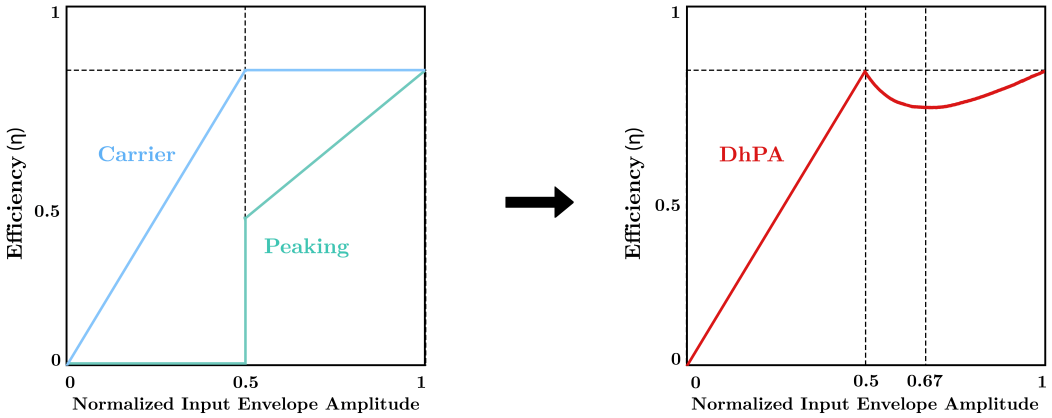


Figure 2.15: Efficiency curves of a DhPA.

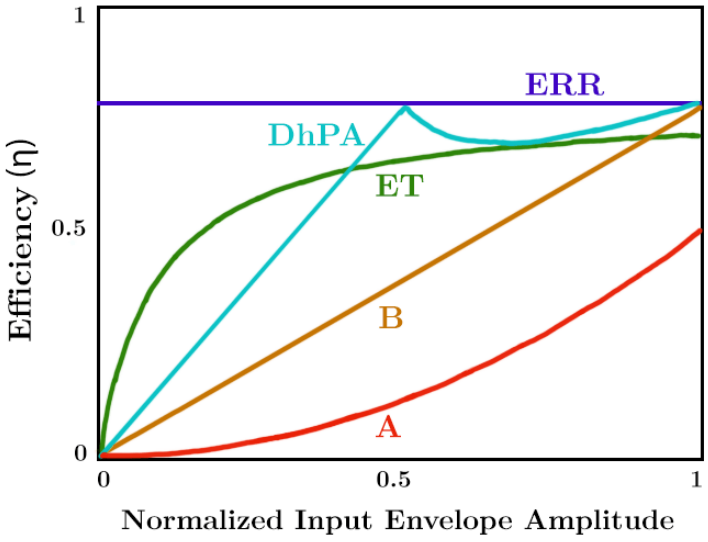


Figure 2.16: Efficiency comparison between class A, class B, ET, EER and DhPA.

2.4.1 Different Architectures

The previous analysis was conducted for the simpler case - a 2-way DhPA with even power splitting. This topology leads to an efficiency curve with the two maxima located at the maximum output power, P_{max}, and at (P_{max} − 6 dB), i.e. at the OBO of 6 dB. The OBO can be defined as:

$$OBO_{dB} = 10log_{10}\left(\frac{P_{max}}{P_b}\right) \equiv 20log_{10}\left(\frac{V_{max}}{V_b}\right), \tag{2.15}$$

where P_b and V_b are the power and voltage levels, respectively, from which the peaking amplifier enters into conduction. Moreover, it can be defined N as:

$$N = \frac{V_{max}}{V_b}. \tag{2.16}$$

N determines the backed-off output power level for the first maximum efficiency point, and it can also determine the number of amplifiers in the DhPA - one carrier PA and (N-1) peaking PAs compose the N-way DhPA, Figure 2.17.

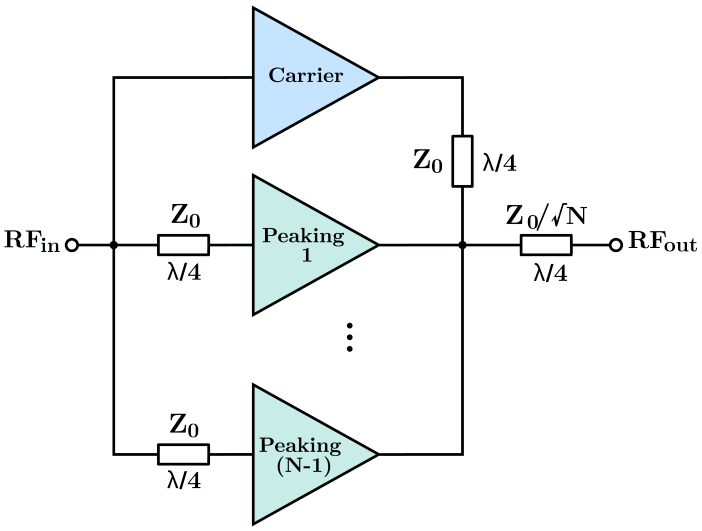


Figure 2.17: N-way DhPA diagram.

As demonstrated previously, load modulation is carried out by the fundamental current ratio between the carrier and peaking PAs - the dynamic load impedance of the carrier amplifier is varied by the current delivered by the peaking amplifier.

The current and impedance variation of the 2-way and 3-way DhPAs are shown in Figure 2.18. In the 3-way case, the carrier amplifier has a load impedance of 3 Z_0 while the peaking amplifiers are off. The peaking amplifiers start to operate with lower input voltage ($V_{i_{max}}/3$) leading to a first maximum efficiency point at an higher OBO - at 9.54 dB (20 $log_{10}(N)$ [dB]) [21], Figure 2.19.

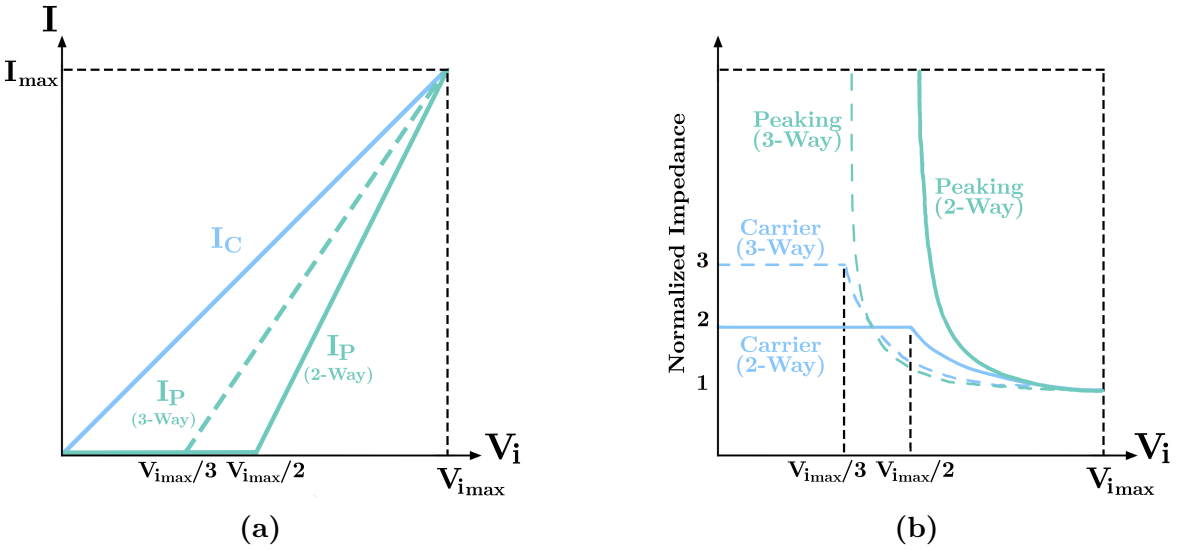


Figure 2.18: Current (a) and impedances (b) comparison between 2-way and 3-way DhPAs.

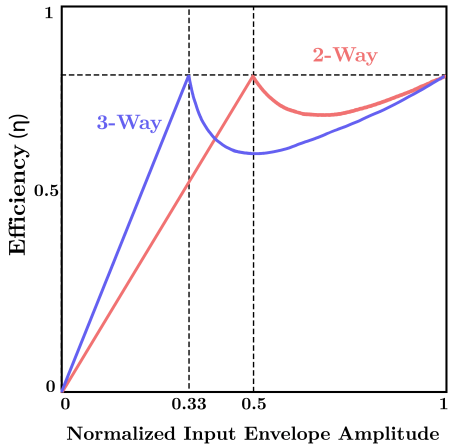


Figure 2.19: Efficiency curves of the 2-way and 3-way DhPAs.

Notice, however, that the inclusion of additional peaking branches, in parallel, does not lead to an overall increase of the DhPA output power. The total current produced by the peaking PAs needs to be set in accordance with the maximum current of the carrier, to lead the carrier impedance to swing from the N $\times$ Z_0 to Z_0. The inclusion of additional peaking branches is used, instead, to adjust the carrier/peaking transconductance ratio, which allows, for instance, to have a DhPA completely implemented with equal devices, but presenting distinct carrier/peaking transconductances, as shown in the desired characteristics of Figure 2.18a. This could be difficult to achieve with non-equal devices since, for example, it may be hard to find two transistors where the transconductance of one is twice of that of the other.

Uneven power splitting at the input of the DhPA can be made to improve the current ratio. It adjusts the relative gain in each PA branch. However, the gain of the overall DhPA is lower, since the gain of the main amplifier decreases.

The 2-way DhPA provides a significant efficiency improvement over the class B case but, when using signals with higher PAPR, it is required to further increase the OBO of the first efficiency maximum. Increasing the number of peaking PAs does so, however, the degradation of the efficiency in the Doherty region increases when the OBO is higher, as represented in Figure 2.19. A different approach is the N-stage DhPA [22], which is a direct extension of 2-way DhPA, as shows Figure 2.20.

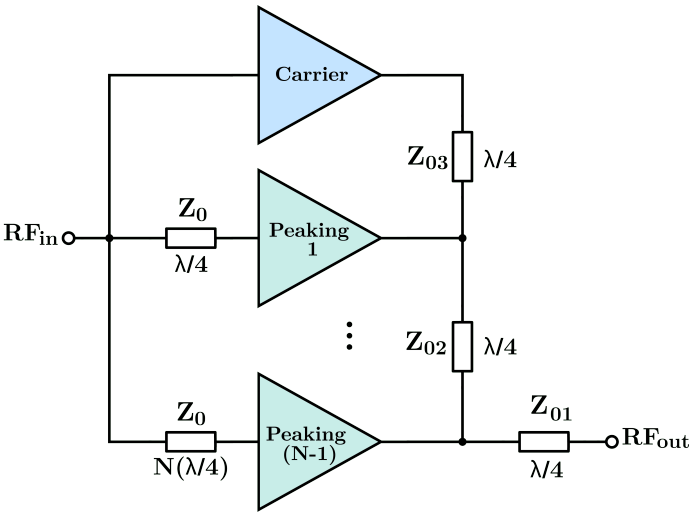


Figure 2.20: N-stage DhPA diagram.

In this architecture, the number of peaking PAs is also (N-1). However, they enter into conduction with different power levels to ensure that the load is continuously modulated - increasing the efficiency in a larger range of OBO [23]. A comparison between the efficiency curve of the 2-way, 3-way and 3-stage DhPA is presented in Figure 2.21. In the 3-stage DhPA, the efficiency maxima are located at 0, 6 and 12 dB OBO.

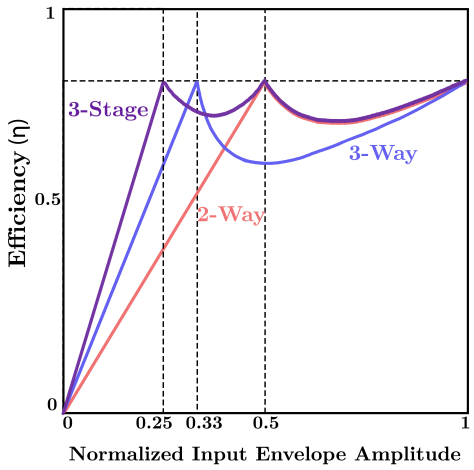


Figure 2.21: Comparison between the efficiency curve of the 2-way, 3-way and 3-stage DhPA.

Up to the second peak of efficiency (6 dB of OBO), the 3-stage DhPA behaves as a 2-way Doherty and, from the second peak to full power, the carrier and peaking 1 behave as a main PA whose load is being modulated by the second peaking amplifier.

Enhanced uneven power splitting, optimal biasing of the carrier and peaking PAs and other techniques have been proposed to improve the overall linearity of the DhPA [24]. Intermodulation cancellation is created for accurate load modulation and to increase linearity.

2.4.2 Bandwidth Limitations

The increasing number of frequency bands used for wireless communications also requires that the RF systems work at multi-bands. Hence, the power amplifiers have to support both high PAPR and wideband signal requirements. The Doherty architecture is a way to address the high PAPR signal requirements but, unfortunately, this amplifier is affected by considerable bandwidth limiting factors.

The impedance inverter network of the output combiner commonly has a significant impact on the overall amplifier bandwidth, as it is usually built from a transmission line structure that is tuned for a specific frequency – as the frequency of the signals deviates from this nominal frequency, the combiner characteristics also deviate from the most adequate ones, leading to a loss of performance as the signal bandwidth increases.

Additionally, in practical implementations, the bandwidth of the DhPA is also reduced due to the device parasitics. An analyzed possibility was to take into account the output capacitance of the transistors in the combiner network design [25].

Also, by modifying and enhancing the peaking output network, the bandwidth can be increased - a resonant LC network added at the peaking output can improve linearity, and harmonic tuning efficiency [26]. Furthermore, by including a two section impedance transformer to the peaking PA, the back-off efficiency bandwidth increases [27]–[30].

CHAPTER 3

Designing a Doherty Power Amplifier

In this chapter, the steps followed to design a Doherty power amplifier are described, starting by introducing the design guidelines and the selected architecture for the amplifier. All the simulations were performed in Advanced Design System (ADS) 2016 and Momentum, both from Keysight Technologies.

3.1 Design Guidelines

The design of the DhPA was conducted in a modular way, starting with the main amplifier, followed by the auxiliary amplifier, and then the input power divider and output power combiner. The PA was designed to operate on RF signals centered at the 4.5 GHz carrier frequency, which already presents relevant constraints to both the design and the realization of the PA board. The selected architecture for this amplifier is shown in Figure 3.1.

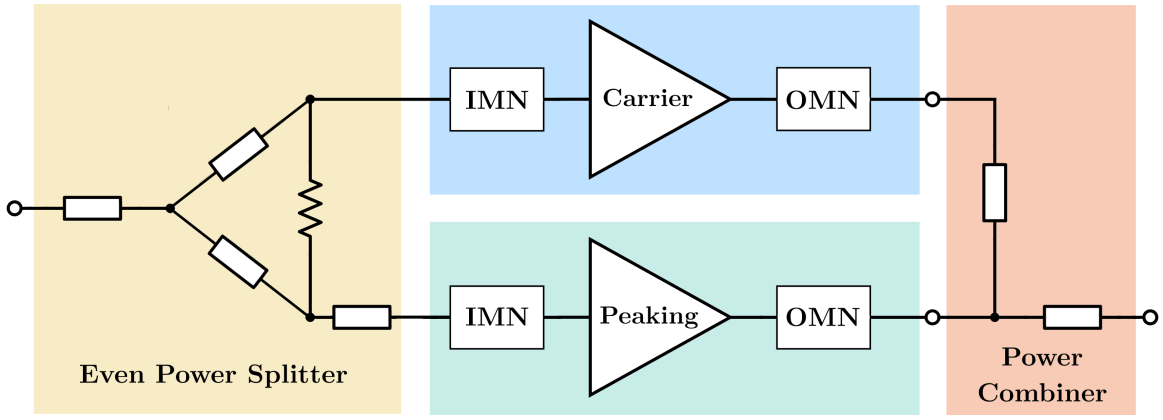


Figure 3.1: Selected structure for the DhPA.

To implement a simpler PA, the ratio of the transconductance between carrier and peaking amplifiers was selected to be equal to 1. Hence, the auxiliary PA used a single transistor, identical to that of the main PA. Also, the power splitter was chosen to present an equal power division between the carrier and peaking branches, the conventional DhPA [31]. It is known that an uneven power splitting would compensate the fact that both carrier and peaking transistors have the same transconductance (as they use equal transistors). However, this would lead to the carrier to receive less power (when compare to the equal power splitting case), leading also to a gain reduction of the overall PA.

In order to test different power combiners, the developed DhPA consists of two boards - one containing the input power splitter and the two amplifiers, and the other containing the output power combiner.

3.2 Active Device

The first step in a power amplifier design is the selection of the active device. As the objective was to design a Doherty amplifier for 4.5 GHz, and aiming for an output power on the order of a few tens of Watt, the selected transistor was the CGH40010F, an unmatched device from CREE, Figure 3.2, whose ADS model was already available.

This transistor can operate up to 6 GHz, has a typical output power of 10 W and uses the state of the art Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) technology. The latter offers several advantages over the traditional Silicon in terms of saturation velocity, electron mobility, breakdown field, heat conductivity and other characteristics [32].

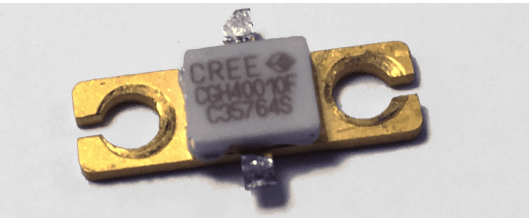


Figure 3.2: CGH40010F transistor.

3.3 Carrier Amplifier

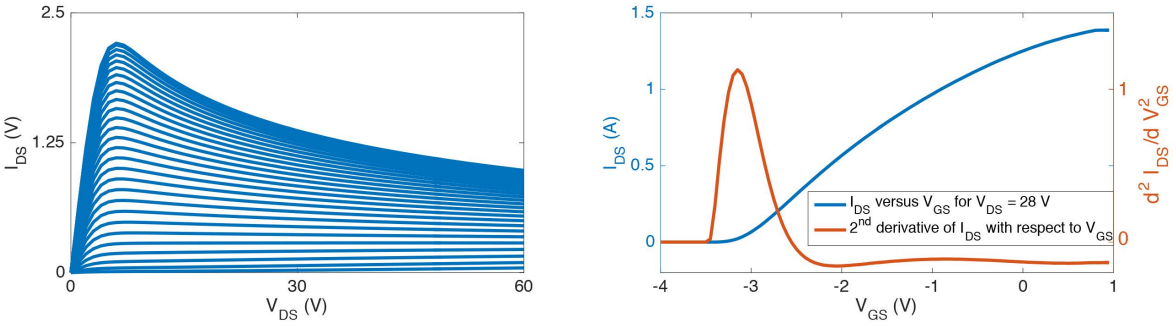
The development of the carrier amplifier followed the steps of a conventional single-ended PA design. However, its output network was made so this amplifier could operate in the Doherty mode when connected to the auxiliary PA, as described in the following sub-sections.

3.3.1 Bias Point

The design of the carrier amplifier started by studying the biasing of the transistor in ADS, using the provided model from CREE.

To achieve class B amplification, the gate bias voltage should be at the threshold voltage of the transistor. Since the transition from the cut-off to the active region is not abrupt in real transistors (nor in the corresponding ADS model of the considered transistor), the second derivative of the I_{DS} current with respect to V_{GS} (the second order transconductance, gm_2) was calculated, as its maximum corresponds to the class B operation point [33].

From the I-V characteristic curves of Fig. 3.3, the bias point chosen was: V_{DS} = 28 V (as suggested in [34]); V_{GS} = -3.15 V; I_{DS} = 22 mA.



(a) **(b)**

Figure 3.3: I-V characteristic curves: (a) I_{DS} versus V_{DS} for different V_{GS} values, and (b) I_{DS} versus V_{GS} for V_{DS} = 28 V and 2^{nd} derivative of I_{DS} with respect to V_{GS}.

3.3.2 Bias Networks

The typical biasing circuit in a PA is a bias-tee composed of a RF choke (also called DC feed) and a DC block, Figure 3.4. Each RF choke connects the drain and the gate of the transistor to the respective power supply and imposes a very high impedance at the design frequency to block the RF signals from leaking through the bias network while, at DC, it behaves as a short circuit. The DC block, placed between the input and the gate, and between the drain and the output, is the opposite - behaves as a short to RF signals while blocking the DC component.

In this work, for implementing the function corresponding to the RF choke, one radial stub and three capacitors were used to ensure a short-circuit close to the power supply terminal, at both fundamental and second harmonic frequencies, and a transmission line transforms such low impedance point into a very high impedance at the gate/drain of the transistor (while conducting the DC bias voltages and currents); and for the DC block, a 10 pF capacitor was used, suitable for operation at the considered frequencies.

A few capacitors of different values were placed in parallel with the DC power supply to reinforce the short circuit at different frequencies.

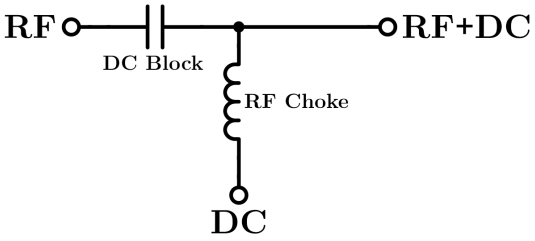


Figure 3.4: Bias-tee circuit.

3.3.3 Matching Networks

A PA usually operates in large-signal conditions, showing a strong nonlinear behavior. Therefore, traditional methods based on the linear theory and small-signal S-parameters, adopted to design small-signal amplifiers, cannot be used when designing a power amplifier for RF. A popular procedure is to obtain curves of equal output power and efficiency, using the load-pull (and source-pull) procedure. Using large electric signals, the load-pull technique consists in varying the impedance presented to a device under test, typically a transistor, to obtain its performance, displayed over a Smith Chart as the referred curves of equal output power and efficiency.

The first step to design the output and input matching networks was to perform a set of load-pull (and source-pull) simulations where the load (source) impedances at the fundamental, second harmonic and third harmonic frequencies were varied. Figure 3.5 shows the Power Added Efficiency (PAE) and delivered power contours obtained from the load-pull simulation at the fundamental frequency for an input power of 27 dBm.

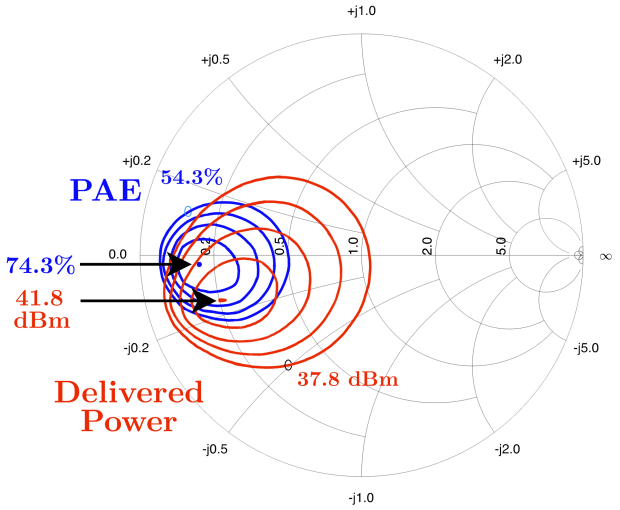


Figure 3.5: Load-pull results for the fundamental frequency.

The results of these simulations revealed that the adjustment of the second harmonic contributes to a significant increase in efficiency, since class B biasing results in significant signals at the even harmonics in the drain current [35]. Also, the third harmonic termination did not contribute to the overall efficiency. This can be justified by the fact that the transistor only operates up to 6 GHz and the third harmonic is well beyond that, and the transistor model may well consider such limitation.

The Output Matching Network (OMN) of the main amplifier of a DhPA should present to the drain of the transistor (at the fundamental frequency) the following conditions, Figure 3.6:

- the impedance leading to the highest efficiency ($Z_{L_{eff}}$), when the OMN is terminated by a 100 Ω load;
- the impedance leading to the highest delivered power ($Z_{L_{pwr}}$), when the OMN is terminated by a 50 Ω load.

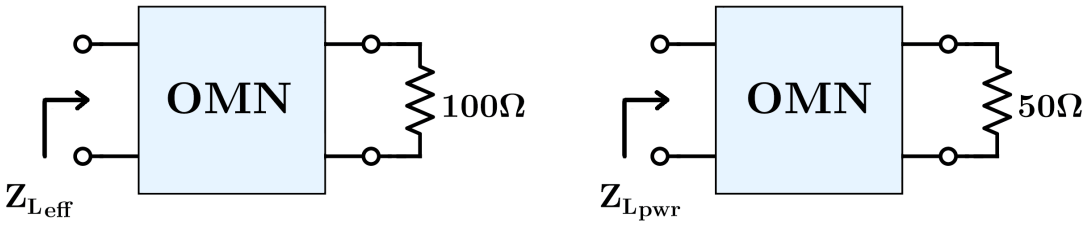


Figure 3.6: OMN conditions for the fundamental frequency - carrier amplifier.

The DhPA is designed for presenting a peak of efficiency at the maximum delivered output power, and another peak of efficiency at the OBO point (thus leading to an overall high efficiency when operating with signals with a PAPR similar to the considered OBO). In this work, an OBO of 6 dB was assumed (a common value in DhPA design for telecommunication signals). Therefore, assuming that the transistors are able to deliver their specified peak output power of 10 W (40 dBm), the overall ideal peak output power of the DhPA would be 20 W (43 dBm). Hence, the DhPA output power at 6 dB of OBO should be 37 dBm. This is the point where the peaking amplifier should enter into conduction (starting to modulate the carrier's output load). Therefore, at the OBO point only the carrier amplifier should be delivering power to the load (i.e., delivering 37 dBm). Thus, the design conditions for the carrier's OMN should consider the maximum efficiency when delivering 37 dBm to a 100 Ohm load, and the maximum output power (the 40 dBm) when loaded with 50 Ohm.

To generate the Input Matching Network (IMN), the source impedances Z_S for the fundamental and second harmonic were obtained through source-pull, for an output power of 40 dBm, seeking a compromise between maximum transducer power gain and efficiency.

Table 3.1 shows the selected impedances for the carrier amplifier, for the fundamental frequency and second hamonic, and Figure 3.7 presents the obtained impedances for the carrier amplifier for the fundamental frequency (from 4.25 to 4.75 GHz).

Frequency (GHz)	$Z_S(\Omega)$	$Z_{L_{eff}}(\Omega)$	$Z_{L_{pwr}}(\Omega)$
4.5	2.3 - j 21.5	5.9 + j 0.0	7.9 - j 4.6
9	430 + j 0	0.0 + j 0.0	0.0 + j 0.0

Table 3.1: Selected impedances for the carrier amplifier.

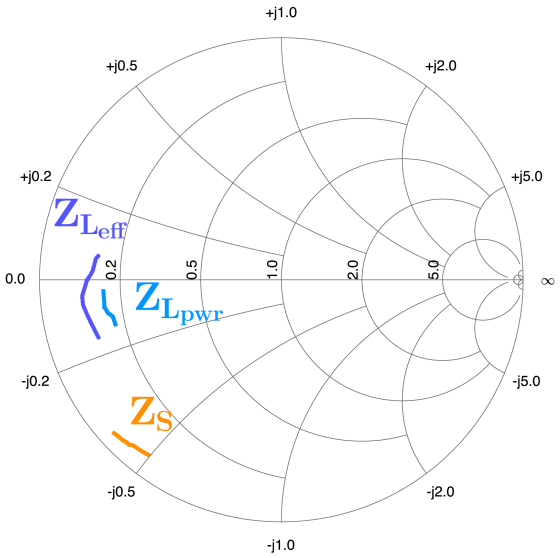


Figure 3.7: Obtained impedances for the IMN and OMN of the carrier amplifier for the fundamental frequency (from 4.25 to 4.75 GHz).

The next step was to create a basic structure for the matching networks, Figure 3.8. The traditional stub was replaced by a radial stub, to improve the bandwidth, and the matching networks were optimized to obtain the desired impedances (for 4.4, 4.5, 4.6 and 9 GHz) at the gate and drain terminals of the transistor. Moreover, for a PA designed to operate at 4.5 GHz, another concern to consider was the transition between lines of different width - tappers were included to soften the transitions.

From the available substrates for implementation, it was selected the Isola Astra [36] for its low loss tangent and its adequate dielectric constant. The relevant parameters of the substrate for simulation can be found in Table 3.2.

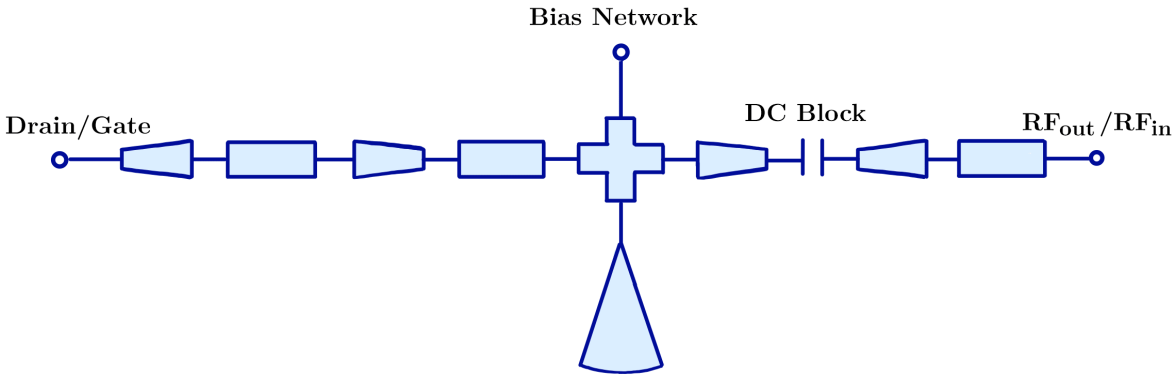


Figure 3.8: Schematic used to generate both the input and output matching networks.

Substrate Height, H	0.762 mm
Conductor Thickness, t	35 μm
Dielectric Constant, ε_r	3.00
Dissipation Factor, TanD	0.0017

Table 3.2: Parameters used in the simulation model of the substrate Isola Astra.

3.3.4 Stability of the Amplifier

After the design of the input and output matching networks, stability was analyzed from 20 MHz to 6 GHz using an ADS template.

In this template, the circuit was separated in two blocks: one containing the transistor, the output bias network and the output matching network; and the other containing the input bias network and input matching network. With the transistor biased at the selected biasing point, S-parameter simulation was performed and the stability circles were calculated for the first block (containing the transistor). Then, in a Smith Chart, the calculated stability circles and impedance presented by the input matching network were displayed. In order to have a stable system, the impedance of the input matching network could not cross the unstable region.

At the fundamental frequency, the amplifier was stable. However, for lower frequencies (around 600 MHz and 1.8 GHz) the simulated amplifier was unstable.

To ensure stability, several procedures were tested (such as adding a resistor to the gate bias network and a capacitor in parallel with a resistor in the input RF path). Introducing a resistor in the gate bias network, between the set of capacitors used for creating a short at the fundamental frequency, and those for creating a low impedance for baseband frequencies, produced the desired results since it ensured stability without compromising the gain at the fundamental frequency.

However, this procedure proved (at a later stage) to be insufficient as the actually implemented circuit was unstable when it was initially tested in the laboratory. Further simulations were performed a posteriori to solve the issue of instability as will be discussed and described in the next chapter.

3.3.5 Layout

After optimizing the matching networks, the following step was to generate the layout of the circuit and to perform Electromagnetic (EM) simulation. At this point, the size of the discrete components and the position of the heat sink and its screw holes had to be taken into account. Also, it was added a ground line surrounding the circuit to better shield it.

Figure 3.9 shows the obtained layout for the main amplifier, where the light blue rectangle represents the Surface Mount Device (SMD) connector for the DC power supply connection and the dark blue rectangles represent the discrete components (capacitors, resistor and transistor). The values and models of the passive components used in simulation can be seen in Table 3.3.

Figure 3.10 shows the obtained impedances after EM simulation for the fundamental frequency (from 4.25 to 4.75 GHz) and the respective second harmonic. Tables 3.4 and 3.5 present the comparison between the desired and obtained impedances both in the schematics and the layout (after EM simulation).

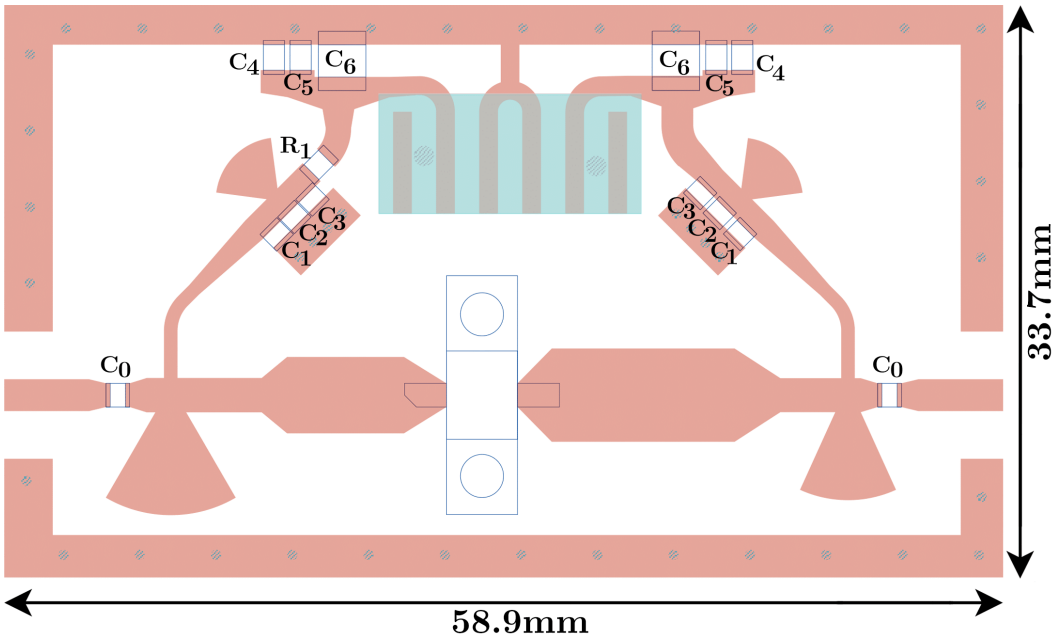
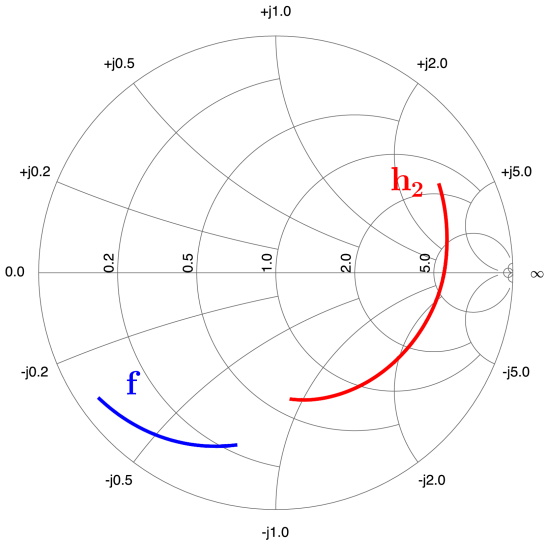


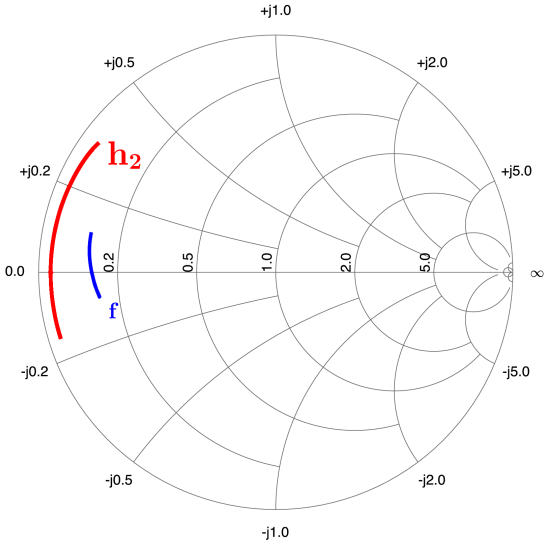
Figure 3.9: Obtained layout for the carrier PA.

Component	Value	Model
C_0	10 pF	ATC - 800A100 [37]
C_1	8.2 pF	ATC - 800A8R2BT [37]
C_2	22 pF	ATC - 800A220JT [37]
C_3	47 pF	ATC - 800A470 [37]
C_4	470 pF	-
C_5	33 nF	-
C_6	4.7 μF	-
R_1	24 Ω	-

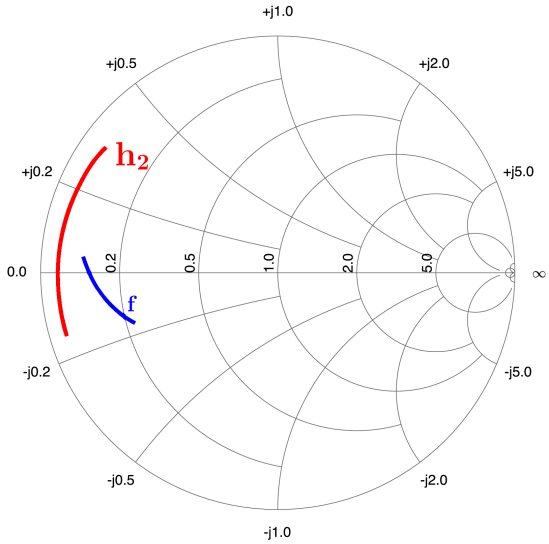
Table 3.3: Components used in the carrier amplifier.



(a) IMN.



(b) OMN - $Z_{L_{eff}}$ condition (100 Ω load).



(c) OMN - $Z_{L_{pwr}}$ condition (50 Ω load).

Figure 3.10: Obtained impedances (in layout) for the carrier amplifier for the fundamental frequency, f (from 4.25 to 4.75 GHz) and the respective 2^{nd} harmonic, h_2.

Frequency (GHz)	$Z_S(\Omega)$	$Z_{S_{Schm}}(\Omega)$	$Z_{S_{Layout}}(\Omega)$
4.5	2.3 - j 21.5	2.8 - j 25.3	4.9 - j 25.3
9	430.0 + j 0.0	430.1 + j 3.4	160.0 - j 102.5

Table 3.4: Comparison between selected and obtained impedances for the carrier PA - IMN.

Frequency (GHz)	$Z_L(\Omega)$	$Z_{L_{Schm}}(\Omega)$	$Z_{L_{Layout}}(\Omega)$
4.5	5.9 + j 0.0	6.3 - j 0.1	6.1 + j 1.2
9	0.0 + j 0.0	0.4 - j 0.3	1.3 + j 4.3

(a) OMN - $Z_{L_{eff}}$ condition (100 Ω load).

Frequency (GHz)	$Z_L(\Omega)$	$Z_{L_{Schm}}(\Omega)$	$Z_{L_{Layout}}(\Omega)$
4.5	7.9 - j 4.6	7.9 - j 4.7	7.3 - j 3.0
9	0.0 + j 0.0	0.7 - j 0.2	1.9 + j 4.3

(b) OMN - $Z_{L_{pwr}}$ condition (50 Ω load).

Table 3.5: Comparison between selected and obtained impedances for the carrier PA - OMN.

3.4 Peaking Amplifier

The design of the peaking amplifier started with the matching networks, as the bias point would only be selected later on. For the matching networks it was also essential to obtain the optima impedances.

The OMN of a peaking PA should be designed so that, Figure 3.11:

- when the peaking amplifier is off, the OMN should present, at the drain, the complex conjugate of the output impedance of the transistor (impedance seen from the drain), $Z^*_{L_{off}}$, and transform it into an open circuit;
- when the peaking is on and receiving its maximum input power, the OMN (terminated with a 50 Ohm impedance) should produce, at the drain of the transistor, the impedance for the highest delivered power ($Z_{L_{pwr}}$).

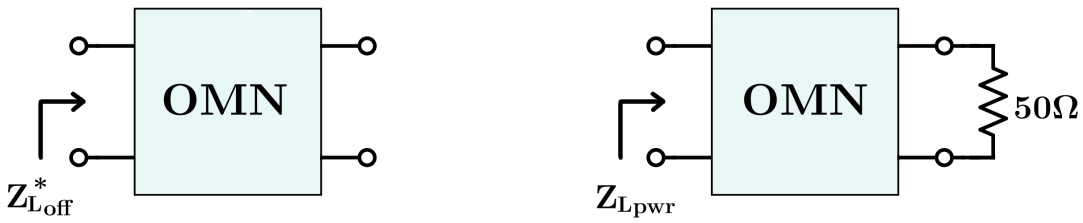


Figure 3.11: OMN conditions for the fundamental frequency - peaking amplifier.

Load pull simulations were performed to obtain the impedances for the highest delivered power, resulting in impedances very similar to those of the carrier amplifier.

The variation of the bias point did not impact heavily on the impedance values. Hence, for simplicity, it was selected the same Z_S and $Z_{L_{pwr}}$ for carrier and peaking PAs. $Z_{L_{off}}$ was obtained from S-Parameters simulation. Table 3.6 shows the selected impedances for the peaking amplifier and Figure 3.12 the $Z^*_{L_{off}}$ impedance for the fundamental frequency (from 4.25 to 4.75 GHz).

Frequency (GHz)	$\boldsymbol{Z_S(\Omega)}$	$\boldsymbol{Z^*_{L_{off}}(\Omega)}$	$\boldsymbol{Z_{L_{pwr}}(\Omega)}$
4.5	2.3 - j 21.5	0.7 + j 7.2	7.9 - j 4.6
9	430 + j 0	0.0 + j 0.0	0.0 + j 0.0

Table 3.6: Selected impedances for the peaking amplifier.

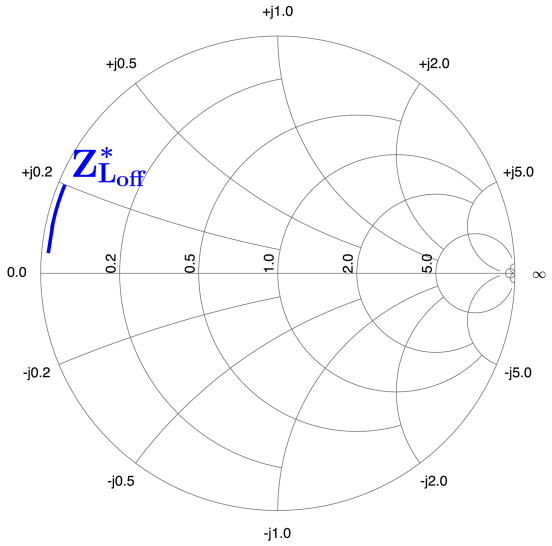


Figure 3.12: Obtained $Z^*_{L_{off}}$ impedance for the fundamental frequency (from 4.25 to 4.75 GHz).

The layout of the carrier amplifier was used as a starting point to generate the layout for the peaking amplifier, since some conditions were the same. The OMN was reshaped to produce the selected impedances at the drain terminal.

The layout of the peaking PA is represented in Figure 3.13 (the components used are identical to that of the carrier PA - Table 3.3).

Figure 3.14 shows the obtained layout impedances of the peaking amplifier OMN for the fundamental frequency (from 4.25 to 4.75 GHz) and the respective 2^{nd} harmonic. Table 3.7 shows a comparison between the selected and obtained impedances in schematics and layout. The obtained impedances of the IMN are not represented here since the peaking IMN is identical to that of the carrier PA.

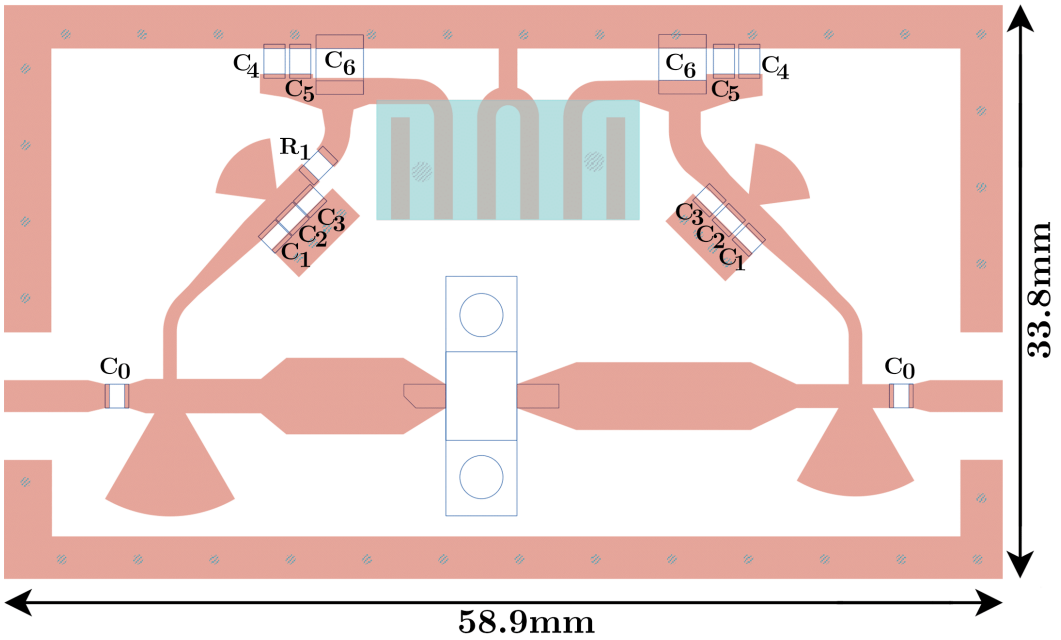
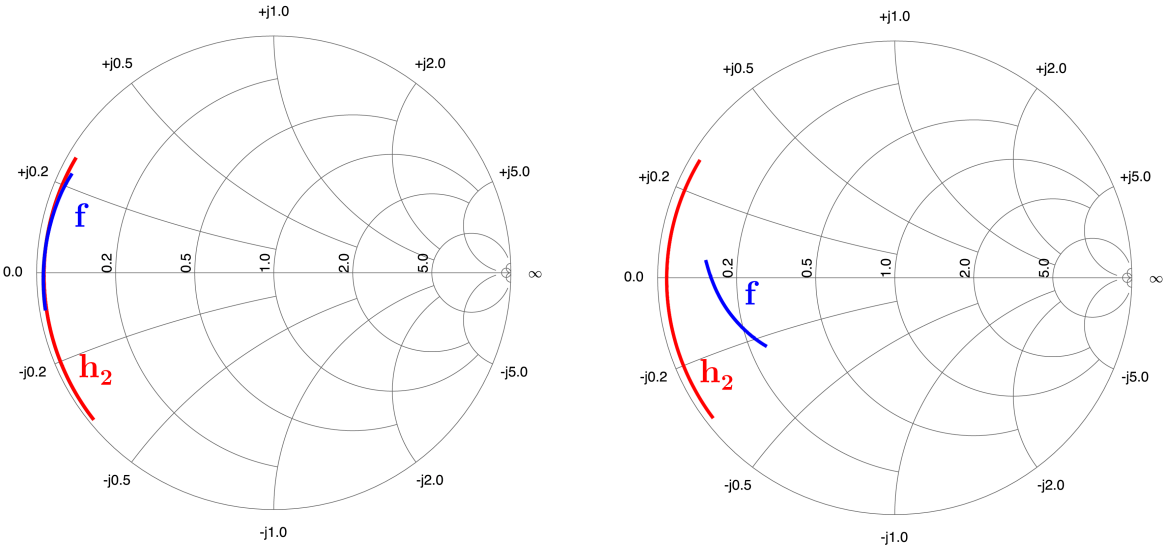


Figure 3.13: Obtained layout for the peaking PA.



(a) OMN - $Z_{L^*_{off}}$, condition.

(b) OMN - $Z_{L_{pwr}}$ condition (50 Ω load).

Figure 3.14: Obtained impedances (in layout) for the peaking amplifier for the fundamental frequency, f (from 4.25 to 4.75 GHz) and the respective 2^{nd} harmonic, h_2.

Frequency (GHz)	$Z_L(\Omega)$	$Z_{L_{Schm}}(\Omega)$	$Z_{L_{Layout}}(\Omega)$
4.5	0.7 + j 7.2	0.3 + j 5.5	1.0 + j 6.1
9	0.0 + j 0.0	0.1 +j 0.1	0.9 + j 0.3

(a) OMN - $Z^*_{L_{off}}$ condition.

Frequency (GHz)	$Z_L(\Omega)$	$Z_{L_{Schm}}(\Omega)$	$Z_{L_{Layout}}(\Omega)$
4.5	7.9 - j 4.6	8.1 + j 4.6	6.0 - j 6.8
9	0.0 + j 0.0	0.4 + j 0.1	1.2 + j 0.5

(b) OMN - $Z_{L_{pwr}}$ condition (50 Ω load).

Table 3.7: Comparison between selected and obtained impedances for the peaking PA - OMN.

3.5 Input Power Splitter

In order to divide the input power by the carrier and peaking PAs, a 2-way equal-split Wilkinson power divider [38] was analyzed and designed. The equivalent schematics is represented in Figure 3.15.

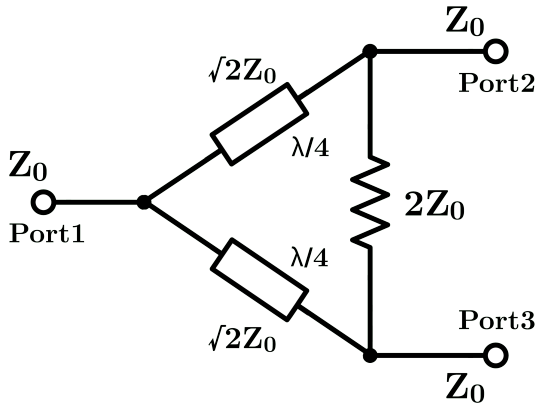


Figure 3.15: A 2-way Wilkinson power divider schematics.

To guarantee matching to the system impedance, two quarter-wavelength transformers and a resistor are used. The resistor allows all three ports to be matched and isolates port 2 from port 3 at the design frequency. Ideally, this resistor adds no resistive loss to the system.

The ideal characteristic impedance of the quarter-wavelength lines and the resistor can be calculated using even-odd mode analysis [2] leading to the values represented in Figure 3.15.

As mentioned in the previous chapter, a phase lag of 90^o needs to be included at the input of the peaking PA. Hence, at the third port of the power splitter, a quarter-wavelength line was added.

From the ideal characteristic impedances and electrical lengths, the physical width and length of microstrip lines were calculated using the LineCalc tool from ADS. This calculation takes into account the operating frequency and the parameters of the substrate mentioned in Table 3.2. Table 3.8 presents the results of the mentioned calculations, where W is the line width and L the line length.

$Z_0 = 50\ \Omega$	$\sqrt{2}Z_0 = 70.7\ \Omega$	$\lambda/4$ @ Z $= 70.7\ \Omega$
W = 1.874 mm	W = 1.021 mm	L = 10.974 mm

Table 3.8: Physical parameters of the lines of the initial input power splitter.

The first structure of the Wilkinson power divider with microstrip lines was shaped to guarantee a certain distance between ports 2 and 3 and optimized to present the desired impedances (50 Ω in the three ports). This structure was designed to adequately interface the following circuit of the carrier and peaking amplifiers, as is shown in the next section.

The layout of the designed Wilkinson power divider can be found in Figure 3.16. The resistor used, and represented by R_0 in the Figure 3.16, was the FC0603E1000BTBST1 from Vishay [39]. Extra lines were included to have an adjustable electrical length - the main transmission line could be cut and copper tape used to form a longer or shorter transmission line.

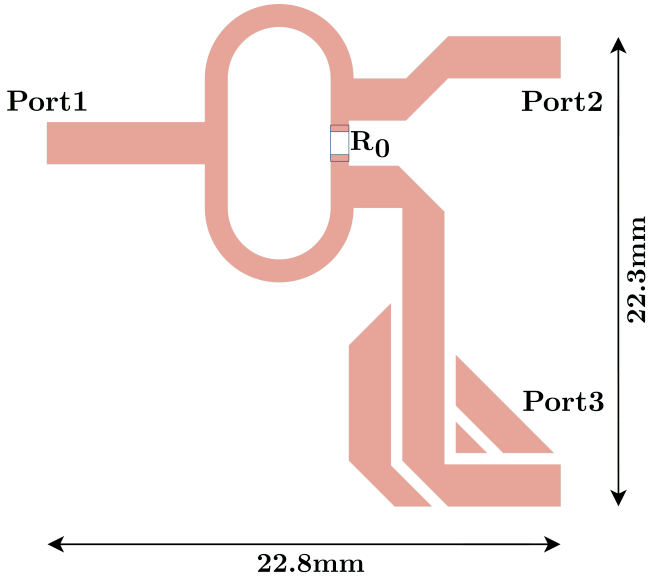


Figure 3.16: Input power splitter layout with trimmable phase shifter.

Figure 3.17 shows the simulated impedances seen from the three ports (in layout) and Figure 3.18 the magnitude of S_{12} and S_{13} and the phase difference between the former two, both in schematics and layout, from 4 to 5 GHz.

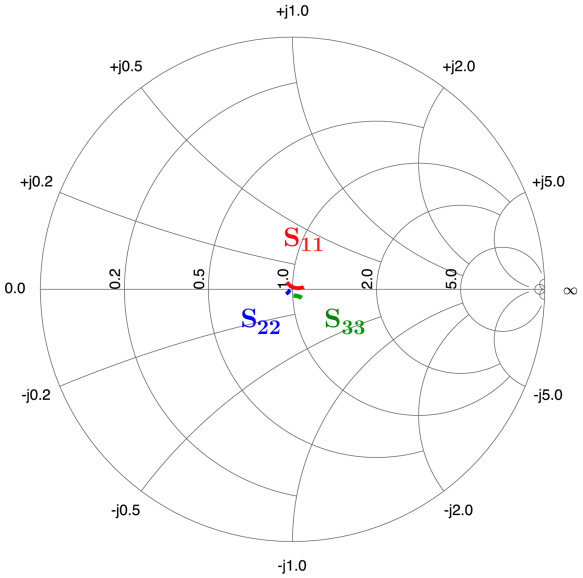


Figure 3.17: Impedances seen from the three ports in the power splitter after EM simulation.

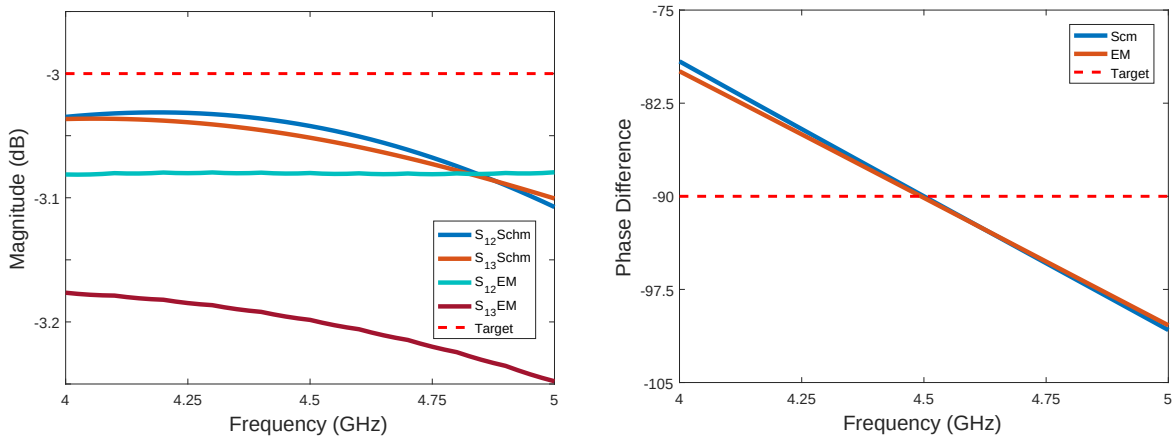


Figure 3.18: Magnitude of S_{13} and S_{12} (a) and phase difference between S_{13} and S_{12} (b) (both in schematics and layout).

3.6 Doherty Power Amplifier Main Board

In order to connect the amplifiers through the input power splitter, the peaking PA was mirrored and the beginning of each input matching network connected to the input power splitter. To better shield the circuit, ground lines were placed between the amplifiers an surrounding them. Several screw holes were placed to attach the Printed-Circuit Board (PCB) to the heat sink.

As previously mentioned, the output power combiner should be on a separate board to allow multiple combiners to be tested. Hence, an output power combiner was not

included at this stage. The main board (containing the input power splitter and the carrier and peaking amplifiers) is presented in Figure 3.19.

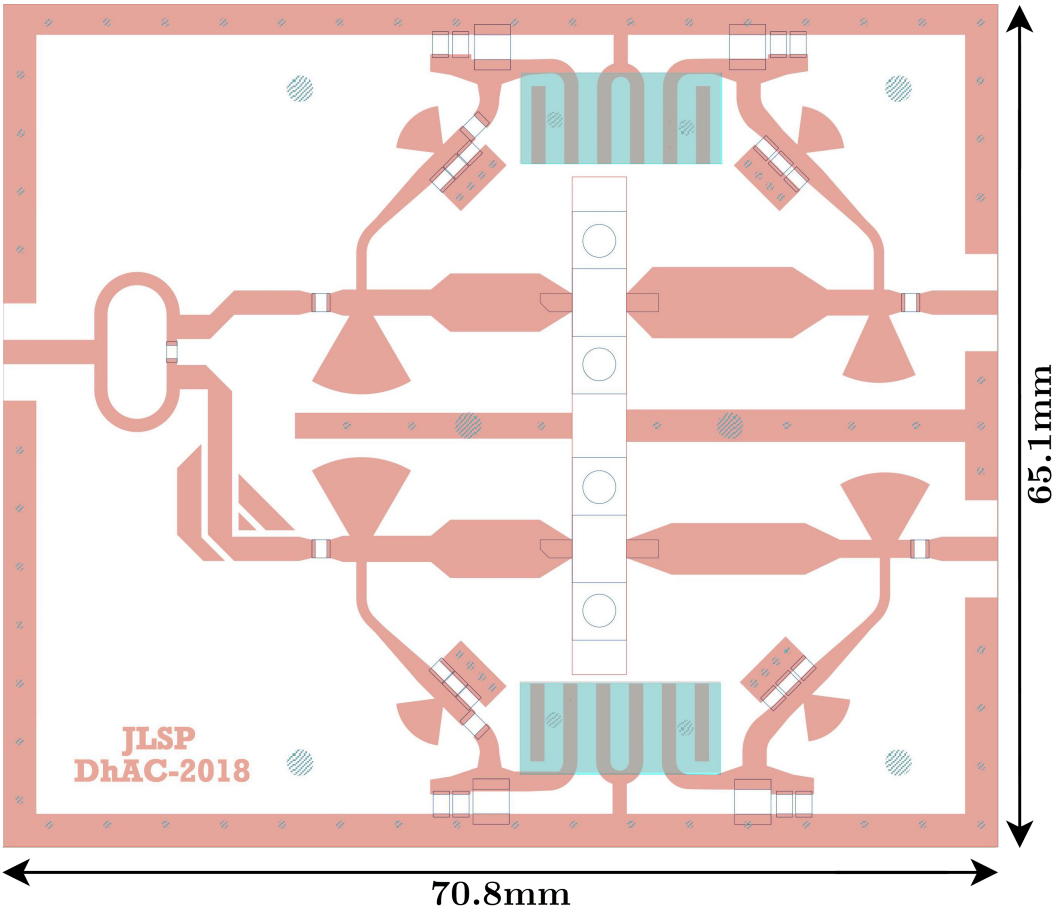


Figure 3.19: Layout of the DhPA.

3.7 Traditional Output Combiner

The output combiner of a Doherty amplifier not only merges the output power of the carrier and peaking PAs but is also used to transform the load impedances of the two, since the ports are not isolated.

In the Doherty region, when both amplifiers are conducting, the impedance seen by the two amplifiers in each port should be Z_0. Hence, the characteristic impedance of the quarter-wavelength transformer between them should also be Z_0 (since the impedance seen from a quarter-wavelength transformer is $Z_{in} = Z_T^2/Z_L \Rightarrow Z_T = \sqrt{Z_{in}Z_L} = Z_0$, where Z_T is the characteristic impedance of the transformer line).

In the low power region, the load impedance of the carrier amplifier should be $2Z_0$. Thus, the impedance seen from the other port of the transformer is: $Z_{out} = Z_0^2/2Z_0 = Z_0/2$. In order to connect a Z_0 load at the output of the Doherty amplifier,

it is required to transform the $Z_0/2$ impedance into Z_0. This is achieved through another quarter-wavelength transformer whose characteristic impedance should be $Z_T = \sqrt{Z_0 Z_0/2} = Z_0/\sqrt{2}$.

The schematics of the Doherty ideal output combiner is shown in Figure 3.20.

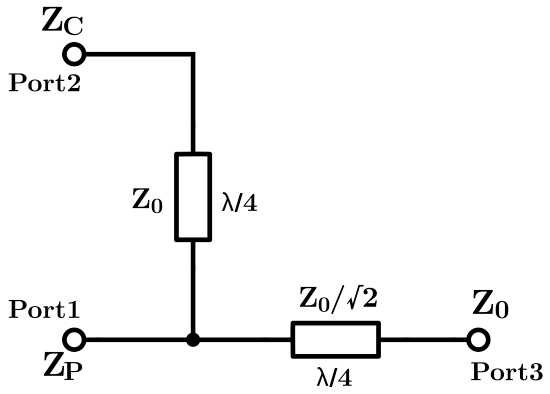


Figure 3.20: Schematics of the DhPA ideal output combiner.

The ideal output combiner was implemented in ADS and the S-parameters of the three-port network were calculated. The relation between the input ports, assuming a Z_0 termination, is:

$$\begin{cases} S_{11} = 0.5\angle \quad 0^o; \\ S_{12} = S_{21} = 0.5\angle -90^o; \\ S_{22} = 0.5\angle -180^o. \end{cases} \tag{3.1}$$

The resulting impedances of the three-port network are: $Z_1 = 150\ \Omega$, $Z_2 = 16.67\ \Omega$ and $Z_3 = 50\ \Omega$.

From the ideal characteristic impedances and electrical lengths, the physical width and length of microstrip lines were also calculated using the LineCalc tool from ADS. Table 3.9 shows the physical parameters of the initial output combiner.

$\boldsymbol{Z_0 = 50\ \Omega}$	$\boldsymbol{\lambda/4}$ **@ Z = 50** $\boldsymbol{\Omega}$	$\boldsymbol{Z_0/\sqrt{2} = 35.36\ \Omega}$	$\boldsymbol{\lambda/4}$ **@ Z = 35.36** $\boldsymbol{\Omega}$
W = 1.874 mm	L = 10.711 mm	W = 3.136 mm	L = 10.479 mm

Table 3.9: Physical parameters of the initial output power combiner.

As shown in Figure 3.19, the physical distance between the carrier and peaking amplifiers' output ports was already defined (and was confined by the possible placement of the circuits of the two amplifiers). This distance of 19 mm is longer that $\lambda/4 = 10.7$ mm, which does not allow the structure of Figure 3.20 to be directly implemented as is. Therefore, additional offset lines were considered in the ports 1 and 2 of the coupler,

and their length and width (and also that of the other features of the coupler) were optimized so that the S-parameters presented by this three-port network were those desired for the coupler operation (i.e., those of equation (3.1)).

Figure 3.21 shows the layout of the designed power combiner, Figure 3.22 and Table 3.10 the S-parameter simulation results (both in schematics and layout): the impedances (in ports 1 and 2) and the phase difference between the input ports.

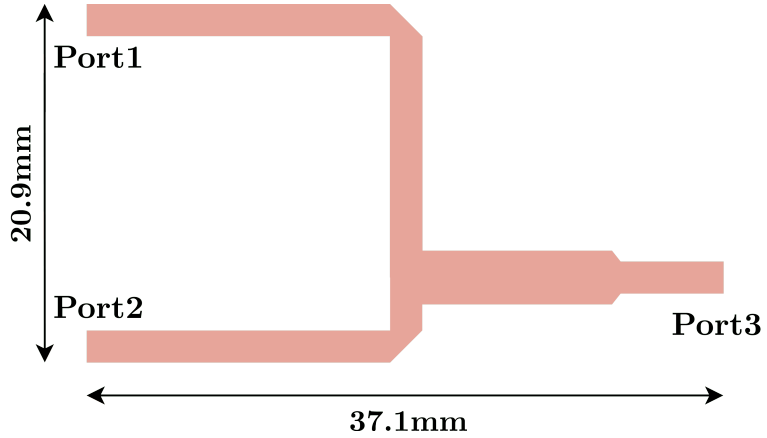


Figure 3.21: Traditional power combiner layout.

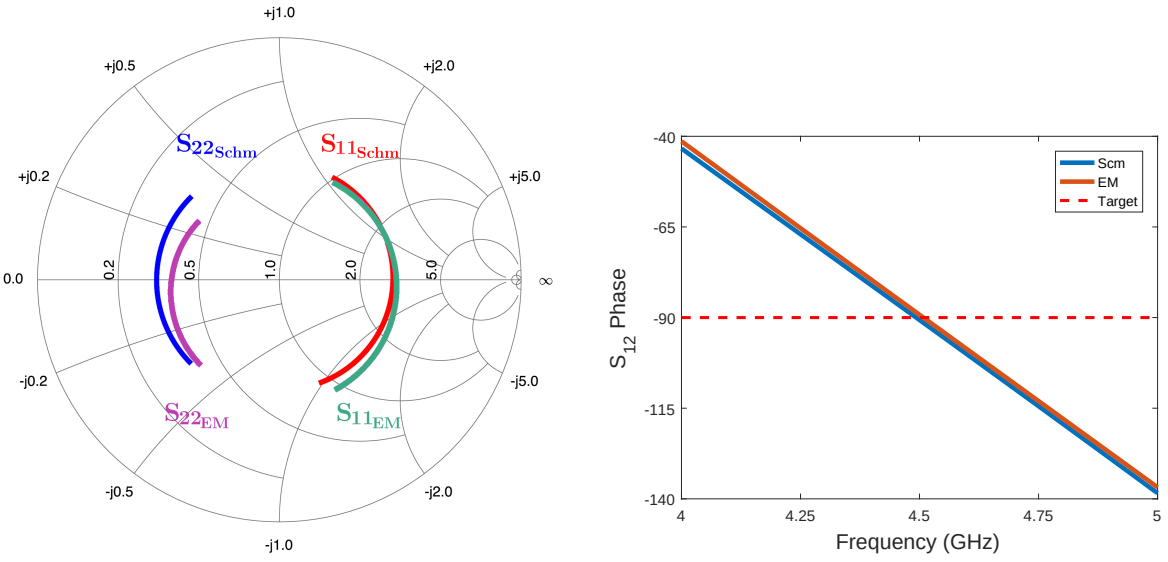


Figure 3.22: S_{11} and S_{22} (a) and phase of S_{12} (b) (both in schematics and layout).

	Z_1 (Ω)	Z_2 (Ω)	Phase (S_{12}) (^{o})
Schematics	139.27 - j 8.50	16.39 - j 0.01	-90.06
Layout	144.81 - j 11.96	18.00 - j 2.37	-89.29

Table 3.10: Simulated impedances and phase difference between the ports 1 and 2 at the central frequency - 4.5 GHz.

To further analyze the performance of the power combiner, the simulation schematics of Figure 3.23 was set. It consists of two ideal current sources, the power combiner and a 50 Ω load. The current sources represent the ideal behavior of the carrier and peaking amplifiers (where the phase of I_C and I_P are 0 and -90^o, respectively) and their normalized current expressions are:

$$I_C = 1;$$
$$I_P = \begin{cases} 0 & \text{when } I_C < 0.5; \\ 2(I_C - 0.5) & \text{when } I_C \geq 0.5. \end{cases} \tag{3.2}$$

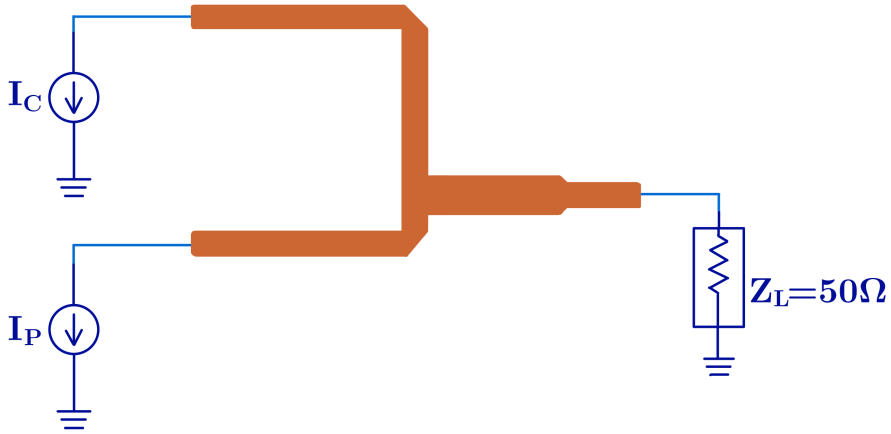


Figure 3.23: Schematic used to simulate the dynamic impedances seen from the current sources.

The impedances seen from the current sources (represented in Figure 3.24) can be calculated from the voltages and currents of those ports.

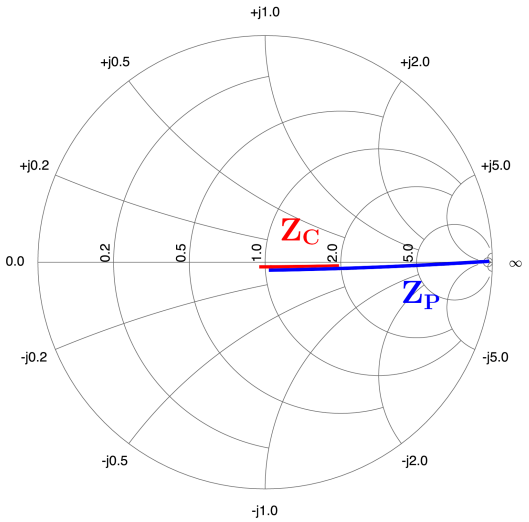


Figure 3.24: Dynamic impedances seen from the ideal current sources.

The impedance Z_C, in port 1, varies from nearly 100 to 50 Ω and Z_P, in port 2, varies from ∞ to 50 Ω, as desired.

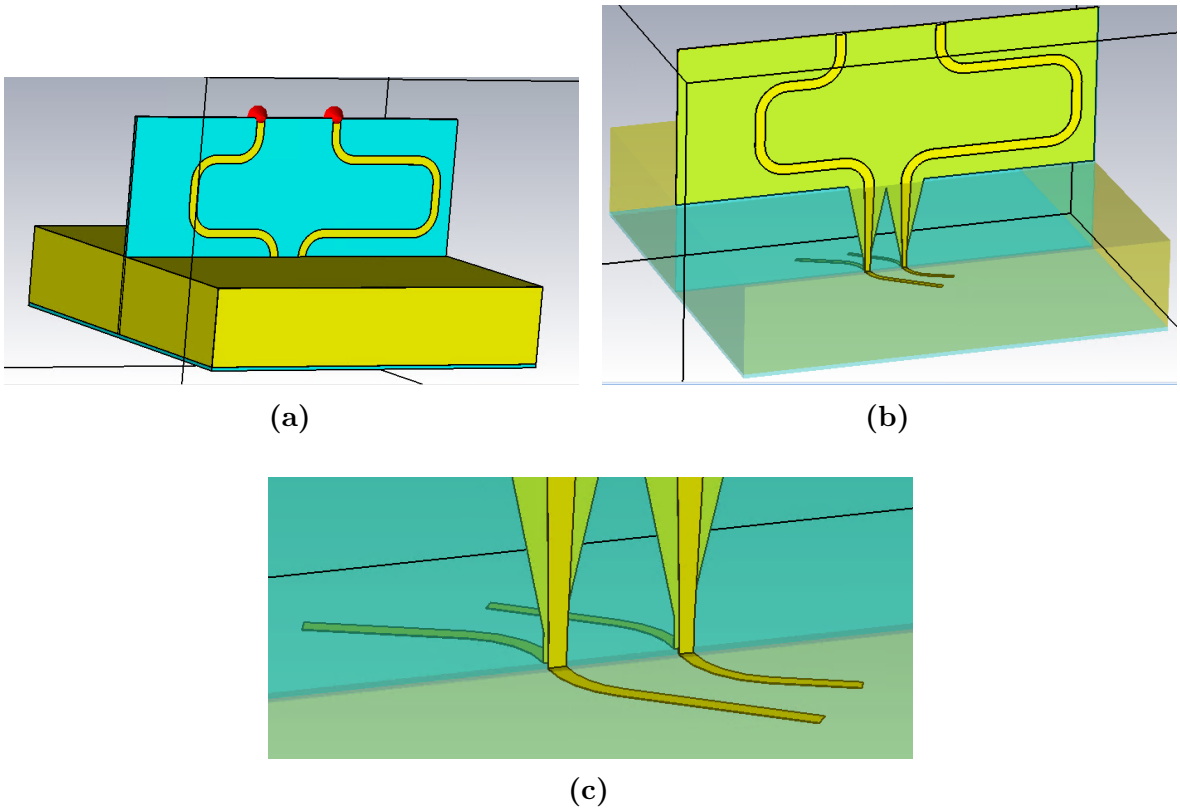
3.8 Design of an Antenna-Combiner

One of the purposes of the designed DhPA is to test the possibility of including in only one element the output combiner and the antenna to which the DhPA's output is to be connected. The idea behind merging the antenna and the combiner is, in one hand, to reduce the required space for these structures (in line with the compactness objectives towards which current telecommunication technology is following) and, on the other hand, to take advantage of the wideband characteristics of some antennas to, using electromagnetic coupling between antenna elements, develop wider bandwidth combiners that would ultimately contribute to increasing the bandwidth of the overall amplifier.

Even though the development of an antenna-combiner structure was not the main purpose of this work (but to provide a Doherty amplifier that, among other tests, would permit experimenting such compact elements), it was made a tentative to design a reasonably simple structure that could be used as a proof of concept. Actually, several antenna structures were considered for the development of this unit (from wideband ones as spiral antennas, to simpler elements as dipoles – where a better design control was intended), but this task proved to be significantly harder than initially thought. The idea was to design an electromagnetic structure that, built around a double antenna (two antenna elements), would have two input ports – one for the carrier amplifier and another for the peaking – whose S-parameters would be as close as possible to those of the conventional Doherty combiner (i.e., S_{11}, $S_{12} = S_{21}$ and S_{22} with -6 dB of magnitude, and a phase of 0º, -90º and -180º respectively). As it is known that two nearby antenna elements suffer from electromagnetic coupling, it was intended to use that phenomenon to create the coupling between the carrier and peaking output ports.

After initially testing different (double) antenna structures in the Computer Simulation Technology (CST) electromagnetic simulation software (from Dassault Systèmes) and realizing the challenging requirements of this structure, it was decided to follow a simpler, more controllable, approach (in detriment of performance indices, such as bandwidth). Thus, a pair of dipole elements was considered for the radiating part, which would connect to the carrier and peaking outputs through two microstrip lines tuned for this effect. An additional interface was also included to perform the connection between the microstrip lines and the two dipoles, to make an adequate conversion from unbalanced to balanced elements. Figure 3.25 shows three 3D views of the implemented

antenna-combiner structure. It consists mainly of two PCB boards, one with the radiating elements (the two dipoles) and, orthogonal to it, another one with the routing lines from the DhPA outputs to the two dipole elements. The output edge of the DhPA board is placed right next to the input edge of the interfacing microstrip line board (the top edge shown in Figure 3.25a, where the red elements (two discrete ports for EM simulation) correspond to the points where the carrier (red point on the right) and peaking (red point on the left) outputs will connect (the distance between these two entry ports is equal to that of the spacing between carrier and peaking out lines - 19 mm)), and the contact of both PCBs as soldered (both the carrier and peaking lines on top layer, and also the ground plane on the bottom layer).



(a) **(b)**

(c)

Figure 3.25: 3D views of the considered antenna-combiner structure: (a) side view of the structure (the radiating dipoles are in the bottom surface, which is 80x80 mm); (b) view of the copper lines (metal box around the antenna in transparent mode); (c) close view of the tuned dipole elements, in the bottom plane.

Each half of the two dipole elements have the dimension of approximately a quarter-wavelength at 4.5 GHz (to guarantee signal radiation at this frequency), and the antenna bottom metal plane was also distanced of a quarter-wavelength (this plane has the objective of blocking the radiation in the direction of the amplifier board). The simplicity of the chosen structure was intended to provide distinct tuning parameters which would individually tackle each of the resulting S-parameters. The distance between the two

dipoles controls the level of coupling between them, thus impacting directly on the magnitude of S_{12} parameter. The width of the lines of each dipole (and of the lines connecting the balun outputs to the dipoles) has a direct impact on the magnitude of the S_{11} and S_{22} respectively. The length of the each microstrip line of the interfacing PCB adequately adjusts the phase of S_{11} and of S_{22} (these microstrip lines have their characteristic impedance near 50 Ω). The parameter that showed to be harder to control was the S_{12} phase, namely it seemed difficult to create an independent degree of freedom between that parameter and the phase of S_{11} or S_{22}. As a tentative to create such new degree of freedom, asymmetric curvature was added to the dipole elements, together with the possibility of placing their feed-point off-centered (this will also change the impedance presented by each dipole, with impact also on S_{11} an S_{22}).

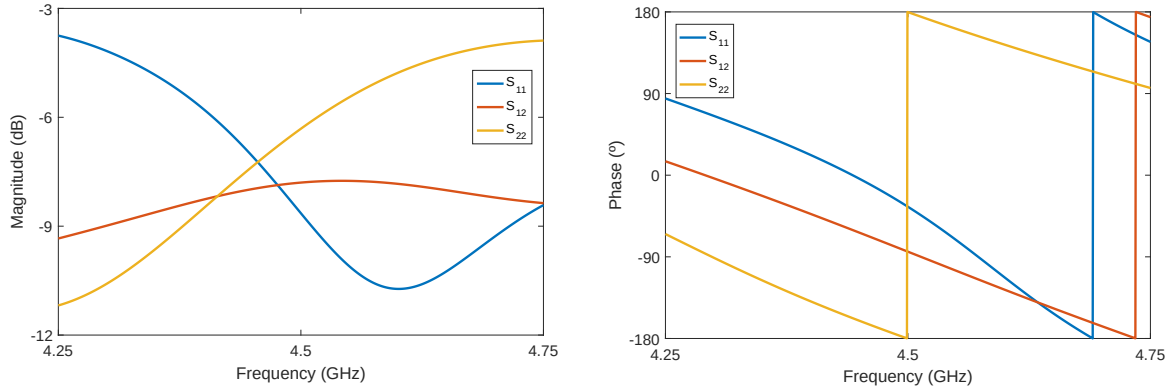
These parameters were then tuned in CST and, for each combination, an electromagnetic simulation was carried out (where two 50 Ω discrete ports were placed at the two input ports of the structure). Naturally, when one of the parameters was changed, even though it dominantly modified the characteristic of the S-parameter it was designed to control, it also changed the values of other characteristics of the measured S-parameters. Therefore, an iterative optimization process was carried out in order to lead the S-parameters to the desired values. Unfortunately, as each simulation took around 25 to 35 minutes to execute, this was a very long and time-consuming process.

Even though this considered structure was designed for simplicity and controllability of its S-parameters, interdependency of the distinct S-parameters on the several parameters under tuning made it difficult to reach a completely satisfactory solution. As mentioned above, it was very difficult to simultaneously set the desired values of the phases of S_{12}, S_{11} and S_{22} (in fact, it was easy to set all the parameters to their target values, except when considering the phase of S_{12} in this optimization process).

After a long optimization process, the best compromise solution that was encountered (corresponding to the structure shown in Figure 3.25) presented the S parameters of Table 3.11 for the 4.5 GHz frequency, and in Figure 3.26 are the S-parameters for a frequency range of 500 MHz around 4.5 GHz.

$\boldsymbol{S_{11}}$		$\boldsymbol{S_{12}}$		$\boldsymbol{S_{22}}$	
Mag (dB)	Phase (°)	Mag (dB)	Phase (°)	Mag (dB)	Phase (°)
-8.6	-34.5	-7.8	-84.3	-6.3	-180

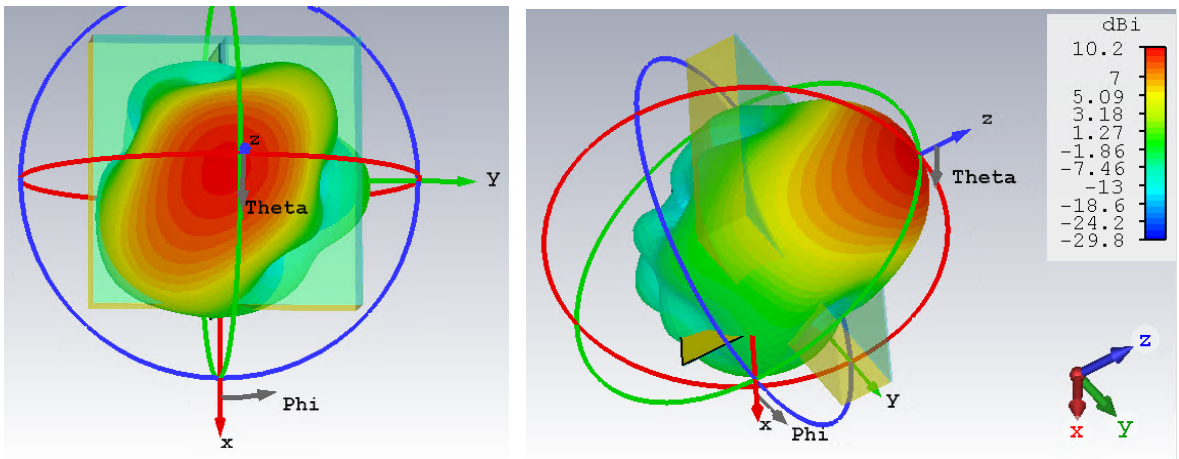
Table 3.11: Achieved S-parameter values for the 4.5 GHz frequency.



(a) **(b)**

Figure 3.26: Obtained S-parameter for a 500 MHz frequency band around 4.5 GHz: (a) magnitude and (b) phase.

Besides maintaining the length of each dipole arm close to a quarter-wavelength, the iterative optimization process did not take into account the radiating characteristics of this antenna structure, nor did it consider the composition of the two radiated fields from the two dipoles. Once again, this antenna structure was only developed for supporting the purpose for which the DhPA presented in this work was conceived – to test its behavior with distinct output combiner structures. To assess the radiating properties of the designed antenna structure, the farfield analysis was conducted in CST, generating the radiation diagram of Figure 3.27, which presents an antenna gain of 10.2 dBi in its direction of maximum gain. In this analysis, the signal sent through the peaking port (port 2) had a -90º phase shift with respect to that of the carrier, to simulate its behavior when connected to an ideal Doherty amplifier. In Table 3.12 are the main characteristics of the antenna, obtained from the CST farfield simulation.



(a) **(b)**

Figure 3.27: Radiation diagram of the simulated antenna structure, for the 4.5 GHz frequency: (a) top view and (b) side view.

Directivity	10.18 dBi
Antenna gain	10.2 dBi
Radiation efficiency	-0.094 dB
Total efficiency	-0.321 dB

Table 3.12: Main characteristics of the designed antenna structure, at 4.5 GHz, obtained from the CST farfield simulation.

3.9 Simulation Results

Harmonic balance simulations were performed to determine the gate bias voltage of the peaking PA. V_{GS} was varied between -7 and -4 V and it was selected $V_{GS} = -5.4$ V for a compromise between efficiency at back-off and linearity.

Several harmonic balance simulations were performed to obtain the characteristic curves of gain and efficiency both as a function of the output power and of the frequency. Initially, the amplifier represented in Figure 3.19 was tested with an ideal Doherty power combiner i.e., two ideal lines with the desired characteristic impedance and electrical length for each tested frequency. Then, the designed power combiner with microstrip lines replaced the ideal one. Later on, the Doherty amplifier was simulated with the antenna combiner. The results of those simulations can be found in the following subsections.

3.9.1 Doherty Power Amplifier with the Ideal Power Combiner

With the ideal power combiner, Figure 3.28 shows the simulated gain, drain efficiency and PAE for the center frequency, 4.5 GHz. Figure 3.29 the simulated gain, drain efficiency and PAE curves for the 4.25 to 4.75 GHz band, and Figure 3.30 the simulated small-signal gain, drain efficiency and PAE (both at full power (43 dBm) and at the output back-off (37 dBm)) as a function of the frequency - from 4.25 to 4.75 GHz.

The simulated amplifier shows suitable characteristics in the considered band: the small-signal gain variation is approximately 2 dB and the efficiency, from the OBO to the full-power, is higher than 50%. However, for higher frequencies, the gain compression is higher.

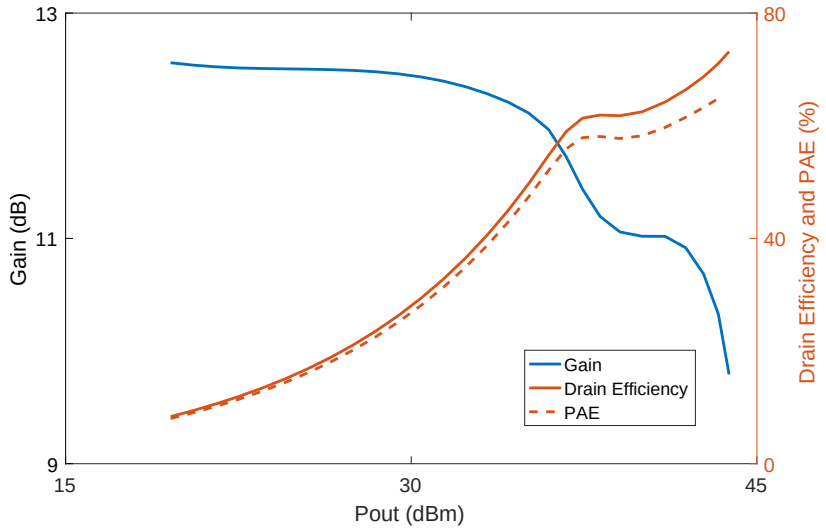


Figure 3.28: Simulated gain, drain efficiency and PAE curves for the project frequency, 4.5 GHz, using the ideal power combiner.

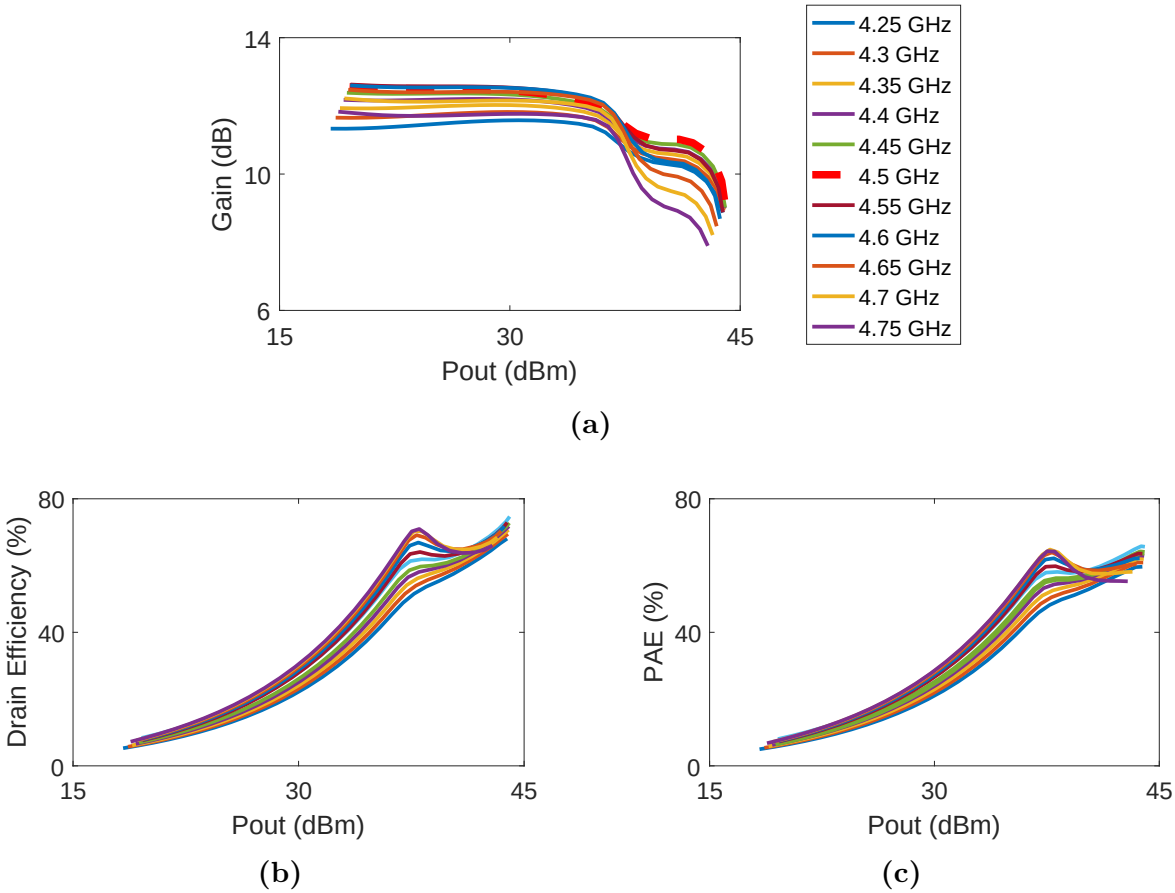
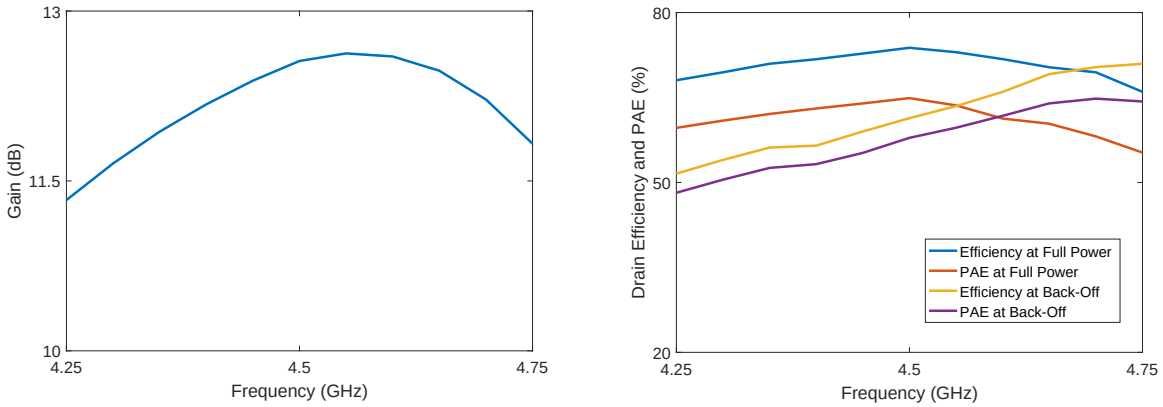


Figure 3.29: Simulated gain (a), drain efficiency (b) and PAE (c) curves - from 4.25 to 4.75 GHz - using the ideal power combiner.



(a) **(b)**

Figure 3.30: Simulated small-signal gain (a), drain efficiency and PAE (b) versus frequency - from 4.25 to 4.75 GHz - using the ideal power combiner.

3.9.2 Doherty Power Amplifier with the Traditional Power Combiner

Using the designed traditional power combiner (the layout model), Figure 3.31 shows the simulated gain, drain efficiency and PAE for the center frequency, 4.5 GHz, Figure 3.32 the simulated gain, drain efficiency and PAE curves for the 4.25 to 4.75 GHz band, and Figure 3.33 the simulated small-signal gain, drain efficiency and PAE (both at full power (43 dBm) and at the output back-off (37 dBm)) as a function of the frequency - from 4.25 to 4.75 GHz.

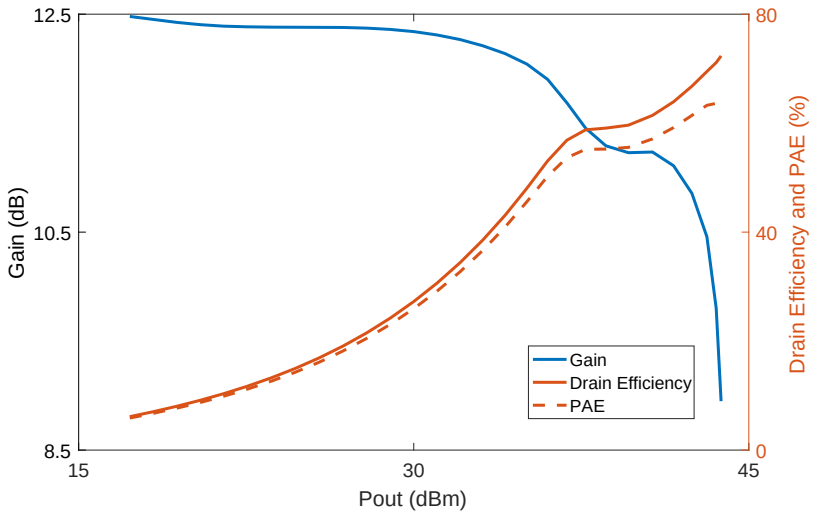
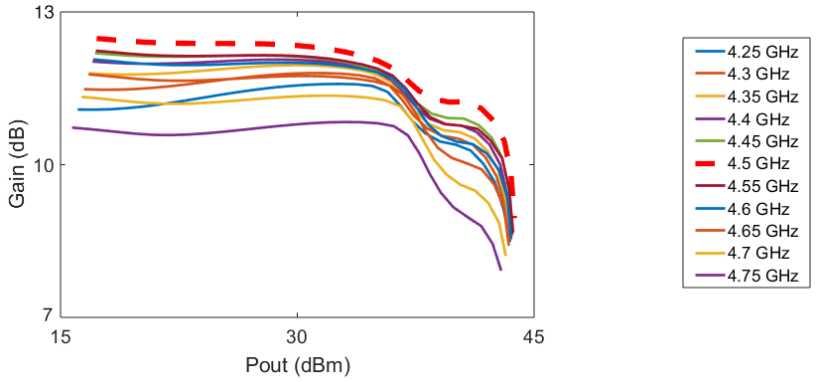
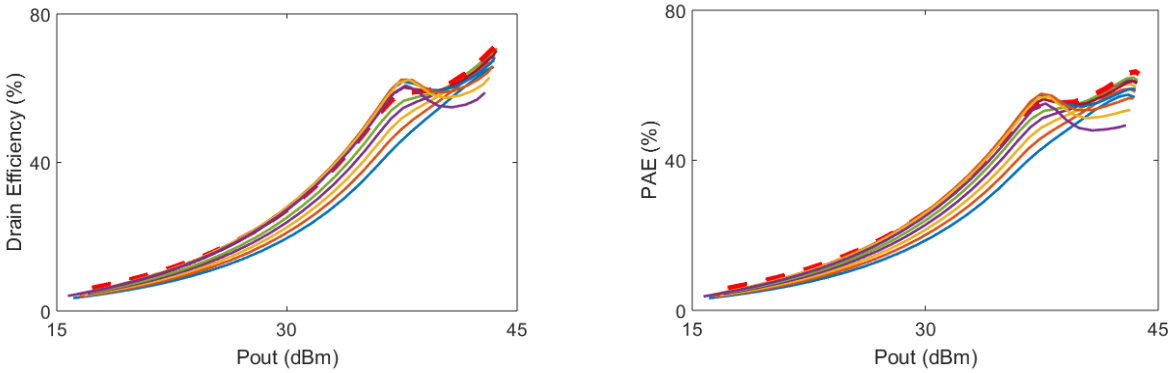


Figure 3.31: Simulated gain, drain efficiency and PAE curves for the project frequency, 4.5 GHz, using the layout power combiner.

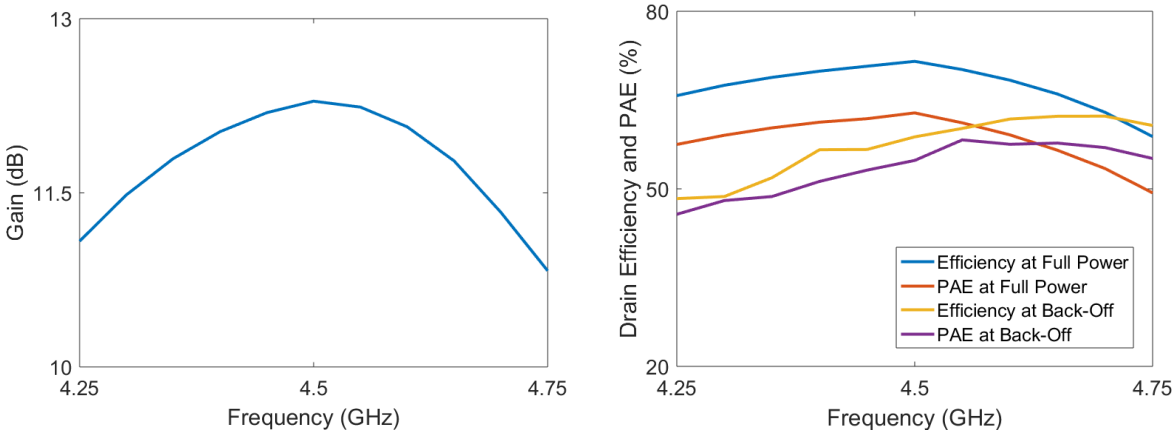


(a)



(b) **(c)**

Figure 3.32: Simulated gain (a), drain efficiency (b) and PAE (c) curves - from 4.25 to 4.75 GHz - using the layout power combiner.



(a) **(b)**

Figure 3.33: Simulated small-signal gain (a), drain efficiency and PAE (b) versus frequency - from 4.25 to 4.75 GHz - using the layout power combiner.

When comparing to the ideal combiner case, the small-signal gain and the overall efficiency of the DhPA slightly decreased. However, the gain variation remains close to 2 dB and the efficiency, from the OBO to the full-power, is higher than 45%.

3.9.3 Doherty Power Amplifier with the Antenna-Combiner

Using the designed antenna combiner (the S-parameters model), Figure 3.34 shows the simulated gain, drain efficiency and PAE for the center frequency, 4.5 GHz, Figure 3.35 the simulated gain, drain efficiency and PAE curves for the 4.25 to 4.75 GHz band, and Figure 3.36 the simulated small-signal gain, drain efficiency and PAE (both at maximum output power and at the output back-off) as a function of the frequency - from 4.25 to 4.75 GHz.

The obtained results show that the simulated amplifier, when connected to the designed antenna-combiner structure, behaves clearly as a Doherty amplifier, as expected, especially in the neighborwood of 4.5 GHz (where the antenna-combiner structure was optimized). In this region, no relevant difference in the overall amplifier behavior is observed, when compared to the case of the conventional output combiner element. Even though the optimized antenna-combiner structure presents S-parameter values, around 4.5 GHz, which are not exactly over the target values (0^o, -90^o and -180^o for the phase of S_{11}, S_{12} and S_{22}, and -6 dB for their magnitude), these results clearly demonstrate that the implementation of Doherty amplifiers with antenna-combiner elements in their output, instead of the conventional output combiner (cascaded with the antenna), are feasable and can present the performance typically expected from these amplifiers. Notice, however, that this analysis does not evaluate the behavior at the farfield, inspecting how the fields originated from the carrier and peaking branches combine in a possible receiver, located somewhere. As was mentioned in Section 3.8, and looking at the results obtained for frequencies in the edges of the tested range, these results also indicate that the antenna-combiner structure should, in the future, be further improved to present, in a wider bandwidth, S-parameter characteristics that are close to the target values, extending, in this way, the desired Doherty behavior and performance. Nevertheless, the intention of this part of the work was simply to serve as proof-of-concept.

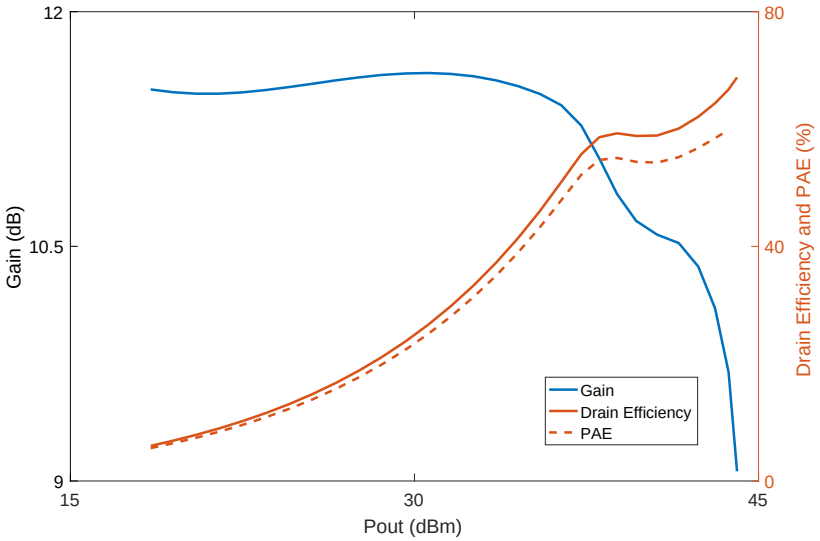
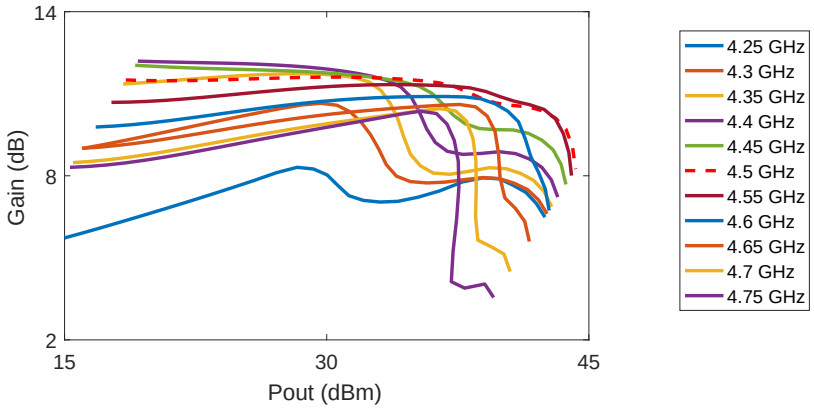
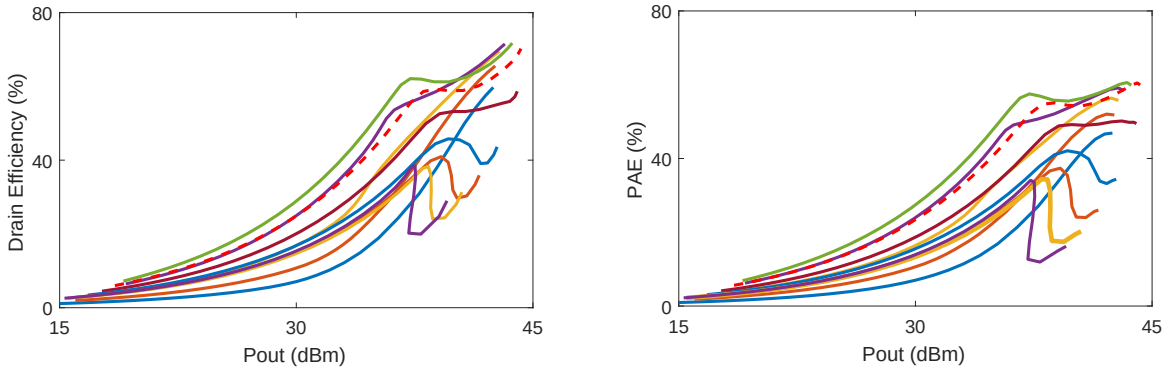


Figure 3.34: Simulated gain, drain efficiency and PAE curves for the design frequency, 4.5 GHz, using the antenna-combiner.

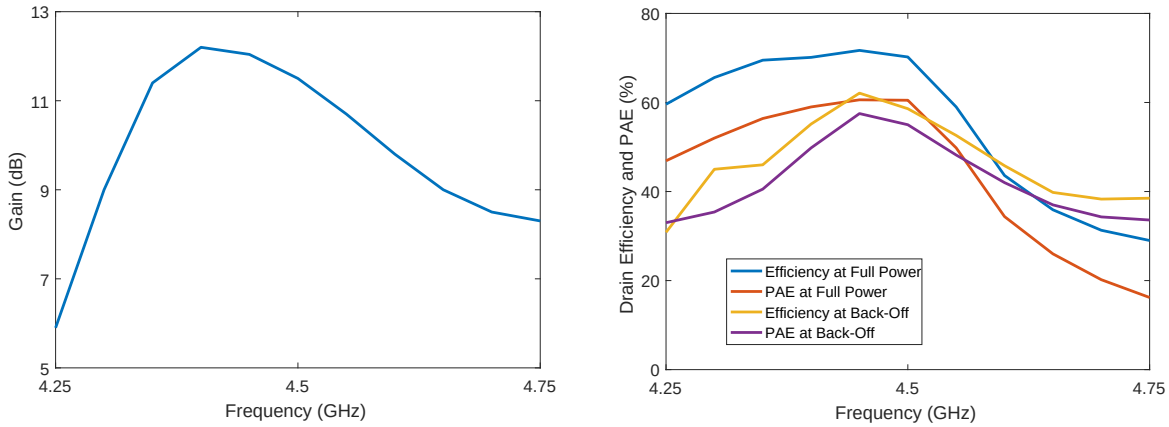


(a)



(b) **(c)**

Figure 3.35: Simulated gain (a), drain efficiency (b) and PAE (c) curves - from 4.25 to 4.75 GHz - using the antenna-combiner.



(a) **(b)**

Figure 3.36: Simulated small-signal gain (a), drain efficiency and PAE (b) versus frequency - from 4.25 to 4.75 GHz - using the antenna-combiner.

CHAPTER 4

Measurement Results

4.1 Initial Tests

The designed two boards of the Doherty amplifier (one containing the input power splitter and both carrier and peaking amplifiers; and the other containing the traditional output power combiner) were produced. To measure the S-parameters of the output power combiner, a replica of the second board was also implemented, to which was soldered SMA connectors, allowing its S-parameter characterization using a Vector Network Analyzer (VNA).

Figure 4.1 shows the connectorized power combiner PCB, where a 50 Ω load was connected to the third port, and in Figure 4.2 and Table 4.1 are the obtained measurement results, where Z_1 and Z_2 are the impedances seen from port 1 and 2, respectively. Naturally, both VNA ports were calibrated, and the additional electrical length introduced by the two SMA connectors as taken into account, so that the reference planes for the S-parameters measurements were at the edge of the PCB.

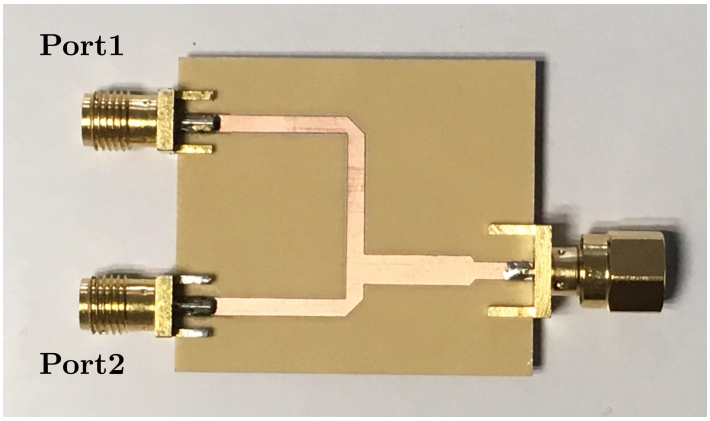
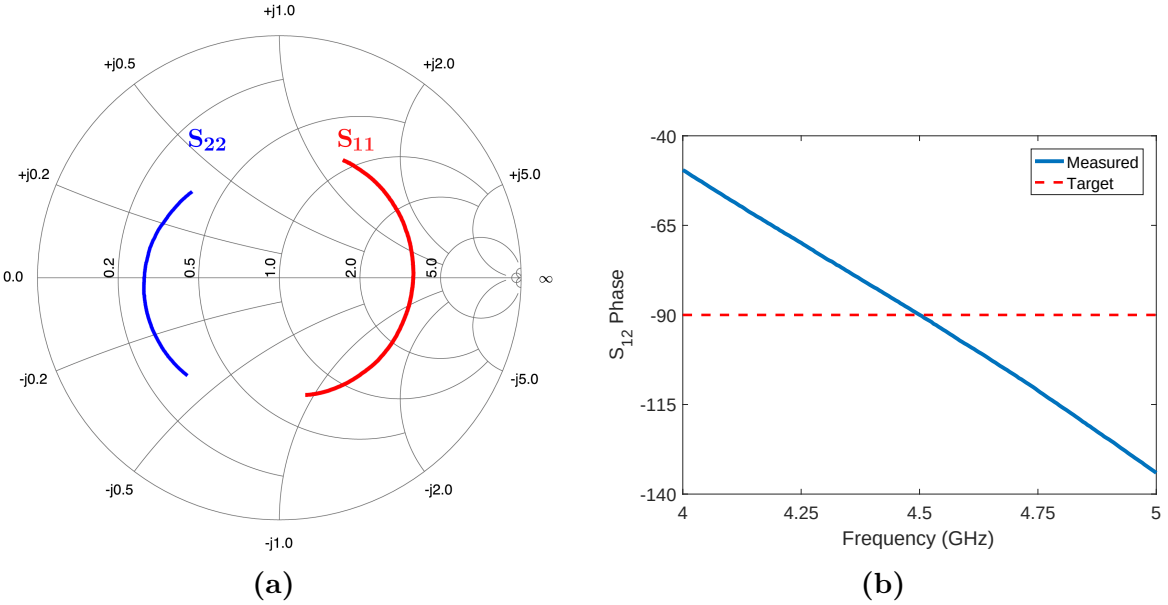


Figure 4.1: Fabricated output power combiner board.



(a) **(b)**

Figure 4.2: Measured S_{11} and S_{22} (a) and phase of S_{12} (b).

Z_1 (Ω)	Z_2 (Ω)	Phase (S_{12}) (^{o})
173.04 + j 7.42	14.65 + j 2.10	89.96

Table 4.1: Measured impedances and phase difference between the two ports at the central frequency - 4.5 GHz.

The impedances Z_1 and Z_2 slightly deviated from the simulated values (specially the imaginary part).

The produced Doherty amplifier with the traditional output power combiner soldered to it can be seen in Figure 4.3. This amplifier was set up in the laboratory, and the first tests were conducted. Firstly, the carrier amplifier operation was evaluated. The two amplifiers were biased at cut-off from the gate side, and the 28 V V_{DD} voltage was applied to their drains. Then, with a spectrum analyzer measuring the output signal spectrum (connected to the combiner output SMA through a 30 dB attenuator), the carrier gate bias level was gradually increased (no input signal was being applied to the PA). In this procedure, it was observed that, after the gate voltage crossed a determined value, the PA output signal presented significant energy at distinct frequency regions, from the sub-GHz range to some units of GHz - this amplifier was oscillating, due to instability.

Despite of the stability analysis previously considered (and described in Chapter 3), the developed amplifier was unstable. Therefore, the stability of the amplifiers was, again, studied in detail in simulation. In the previous analysis, it was only studied the stability of a single PA and the stability circles were only seen from the transistor's gate. This was proved (from the practical results obtained) to be insufficient. Therefore, in

the new simulations, the total system was analyzed - the Rollet stability factor [40] was calculated and stability circles were drawn for the input (before the input power splitter) and for the output (after the output power combiner). Assuming a 50 Ω termination in both ports, for the system to be unconditionally stable the center of the Smith Chart must be in the stable region of the stability circles for all frequencies.

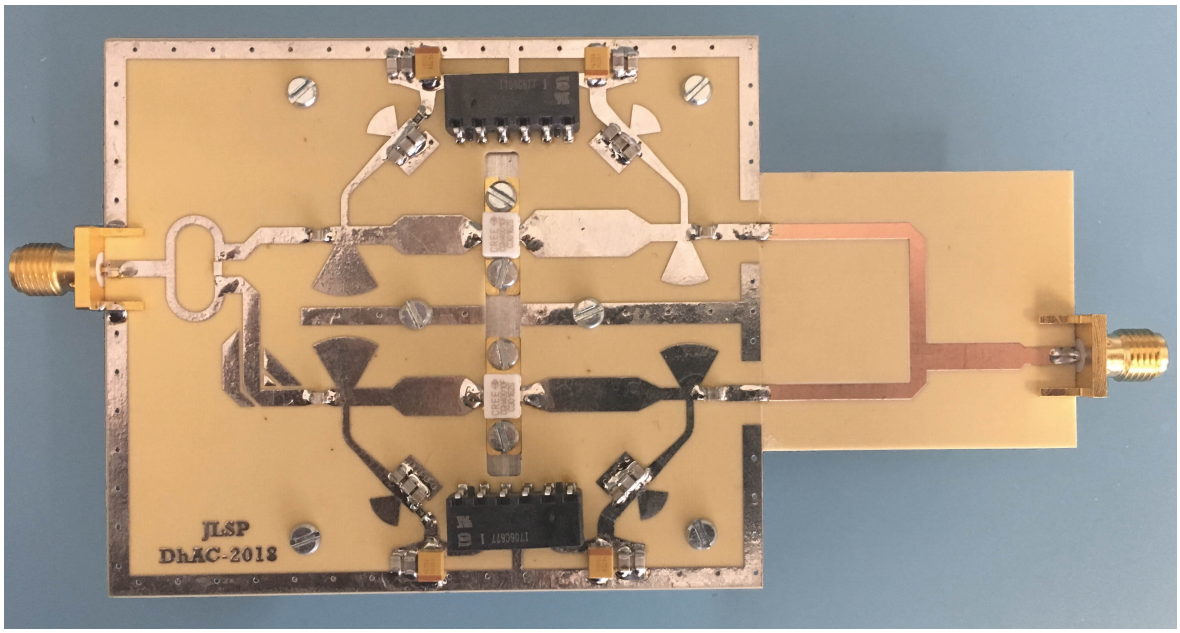


Figure 4.3: Fabricated DhPA with traditional output power combiner board.

From the Rollet factor results, Figure 4.4, the system was potentially unstable in three regions: from 550 to 850 MHz, from 975 MHz to 1.8 GHz and from 4.5 to 4.6 GHz. In the 4.5 to 4.6 GHz band, the stability circles crossed the Smith Chart, however they were far from the center (50 Ω). In the other bands, the system was unstable.

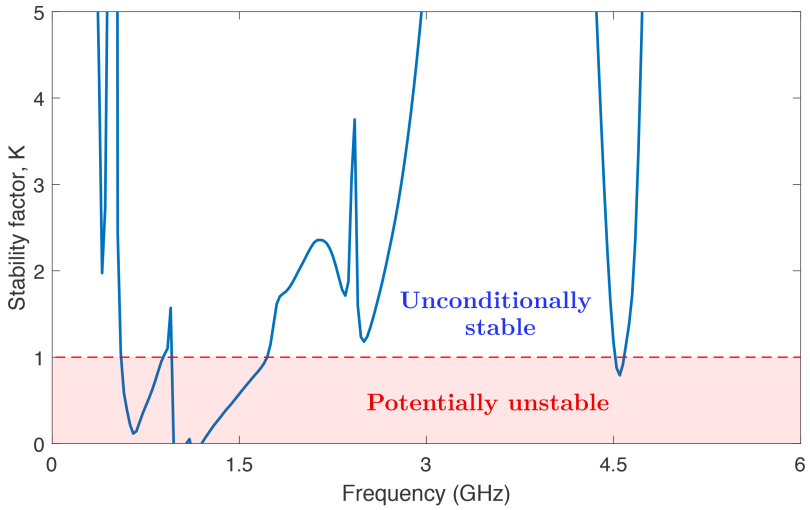


Figure 4.4: Simulated stability factor of the DhPA.

Faced with these results, several procedures were tested (in the simulation environment) to guarantee the stability of the system for all frequencies, such as:

- introducing a series resistor at the beginning of the input bias networks (near the first C_0 in Figures 3.9 and 3.13);
- adding a resistor in parallel with a capacitor in the RF path (it was tested before and after the capacitor used as DC block (C_0) and for both amplifiers or just for the carrier or peaking PAs);
- introducing a series resistor in parallel with a capacitor before the input power splitter;

For each test, harmonic balance simulations were also performed to determine which solution would guarantee stability without compromising too much the figures of merit of the designed DhPA. From the simulation results, it was concluded that it would be required to add a series resistor at the beginning of each input bias network and a resistor in parallel with a capacitor in the RF path of the carrier amplifier. The gain at the center frequency decreased almost 2 dB and the bandwidth was significantly affected (from over than 500 MHz to 200 MHz).

The initial board, Figure 4.3, was then modified according to the new layout shown in Figure 4.5 for the carrier PA (a similar modification was included in the peaking PA design). It was decided to place a 100 Ω series resistor at the beginning of each bias networks and test the circuit before placing lumped components in the RF path, even though the amplifier was unstable in simulation.

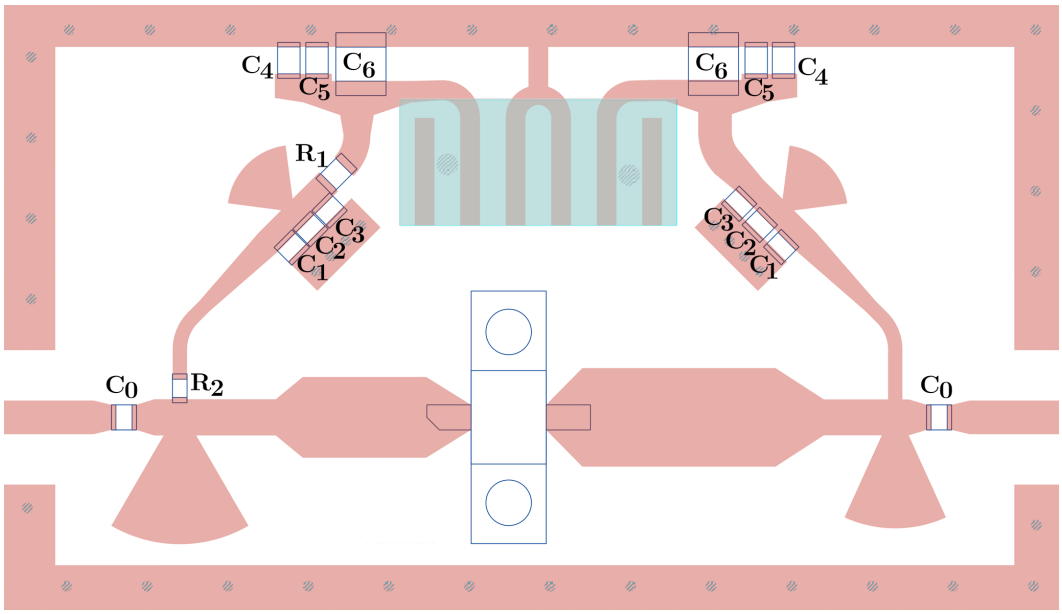


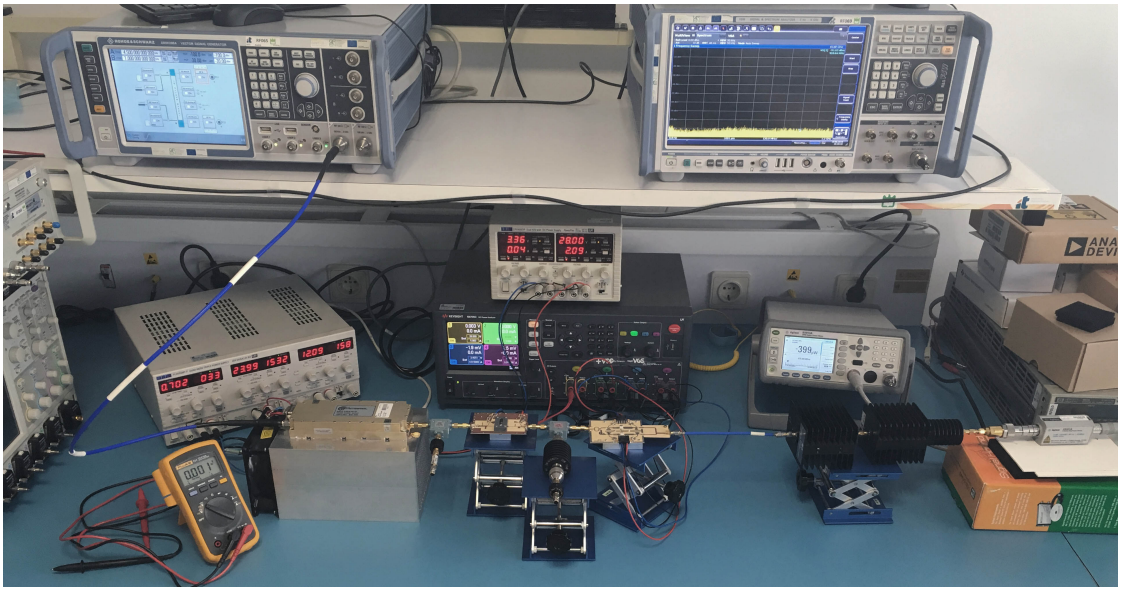
Figure 4.5: Modified layout of the carrier amplifier.

The amplifier was, then, tested and the measured performance is described in the following section.

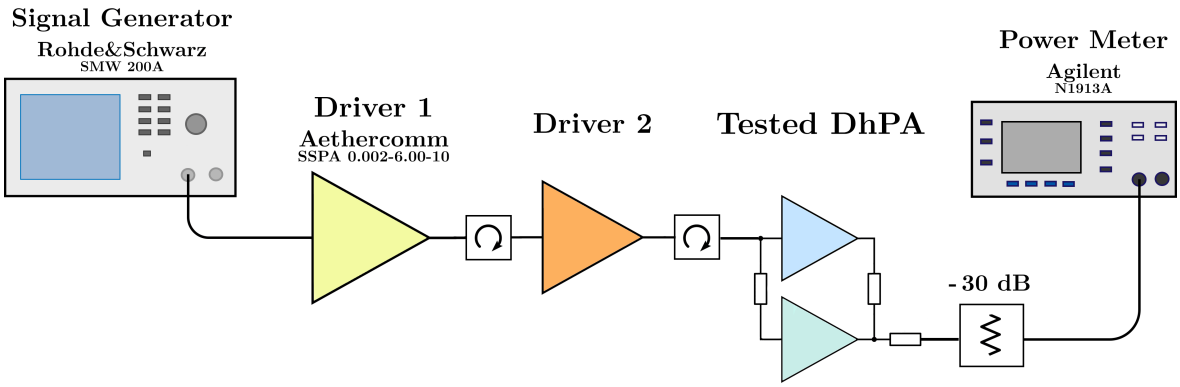
4.2 Doherty Power Amplifier with the Tradition Output Combiner

The transistors were biased at the selected biasing points, which slightly deviated from the simulation values. For the carrier PA, for an $I_{DS} \approx 22$ mA, it was required a $V_{GS} = -2.74$ V. With no signal applied at the input of the DhPA, the modified system was stable.

A one tone signal at 4.5 GHz was applied at the input of the DhPA and the system remain stable and amplified the signal. The measurement setup consisted of a Vector Signal Generator (VSG), three power supplies, two drivers, two circulators, a cascade of attenuators of -30 dB and a power meter, Figure 4.6.



(a)



(b)

Figure 4.6: Measurement setup (a) photograph and (b) schematics.

4.2.1 CW Characterization

In order to obtain the PA's characteristics (and compare them with the simulation results) Continuous Wave (CW) measurements were performed.

Initialy, a small-signal gain analysis was considered. With a fixed input power, the frequency of the tone signal was varied. Figure 4.7 shows the measured small-signal gain of the amplifier.

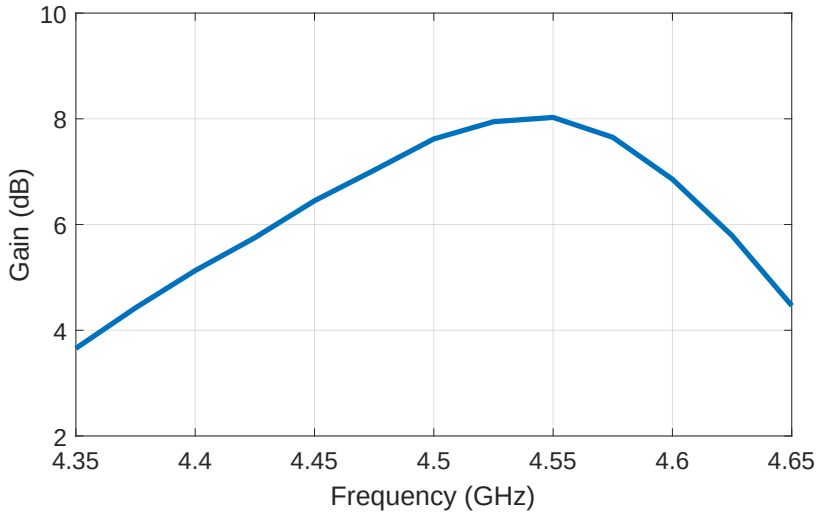


Figure 4.7: Small-signal gain of the DhPA - from 4.35 to 4.65 GHz.

The first findings from this measurement was that the small-signal gain was lower than the simulated one; the best results of power gain were obtained for 4.55 GHz (approximately 1% of frequency shift from 4.5 GHz) and that the bandwidth is approximately 230 MHz.

Power sweep was performed from 4.45 to 4.6 GHz with a 25 MHz step (it was necessary to restrict this test to this frequency range because the gain of the DhPA was low and the driver stage was not capable of delivering sufficiently high power to test the DhPA compression outside this range).

Figure 4.8 shows the measured gain, drain efficiency and PAE curves at 4.55 GHz and Figure 4.9 the measured gain, drain efficiency and PAE curves for the 4.45 to 4.6 GHz band.

When compared to the simulated results, the measured gain was considerably lower, the measured maximum output power was higher than the simulated one (higher than 43.5 dBm $\approx$ 22.4 W) and the gain compression was lower. Moreover, the measured drain efficiency was considerably high (near 75% at full power for all tested frequencies and higher than 45% at the OBO). The PAE results reflect the low gain of the amplifier – for some frequencies the PAE is 20% lower than the drain efficiency.

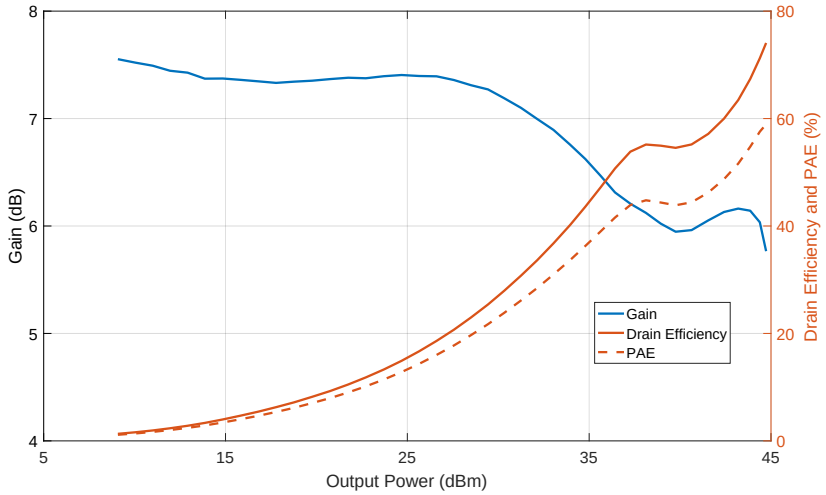


Figure 4.8: Gain, drain efficiency and PAE curves for 4.55 GHz.

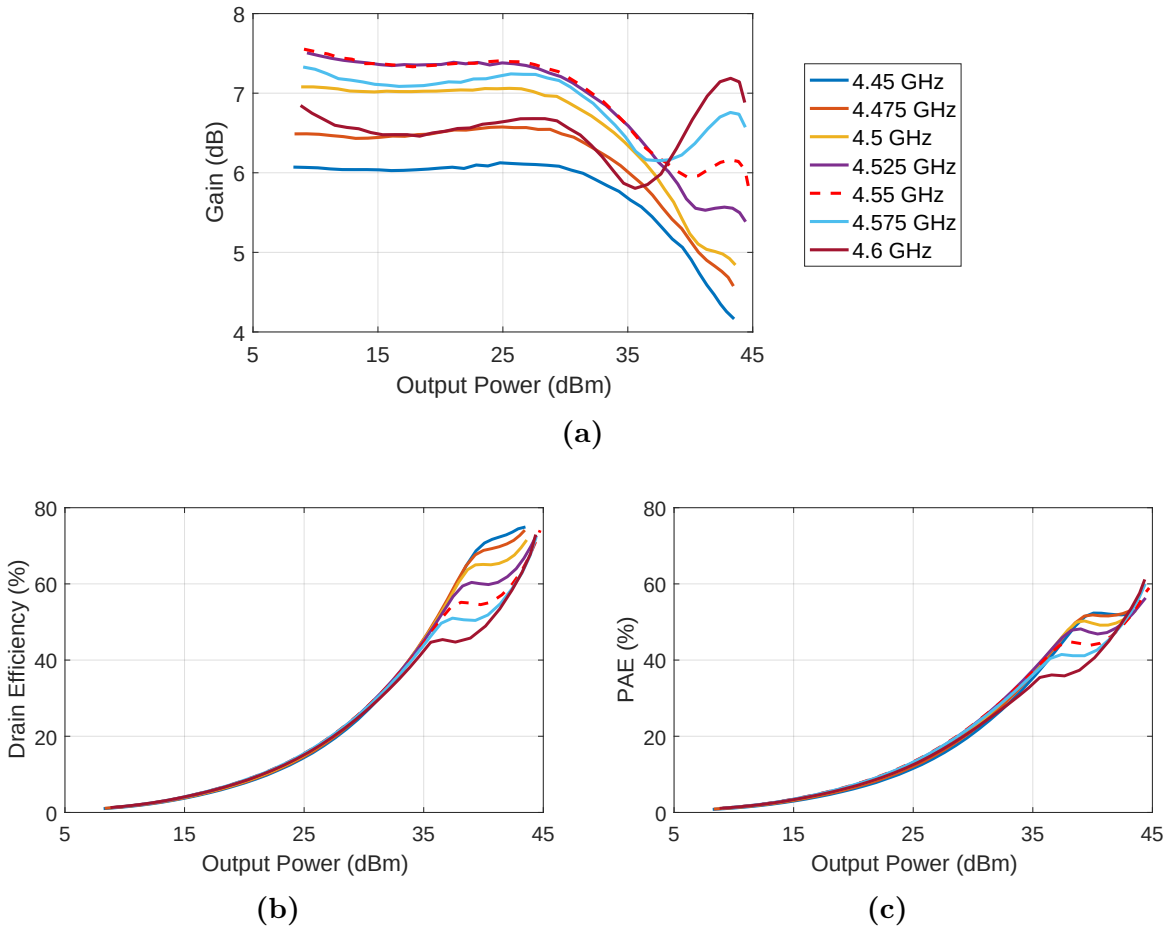


Figure 4.9: Measured gain (a), drain efficiency (b) and PAE (c) curves - from 4.45 to 4.6 GHz.

4.2.2 Linearization Tests

During the design stage of the implemented DhPA the main targets were the delivered output power and the efficiency of the amplifier. Similarly to what is usually done, the linearity of the PA was only evaluated in a later stage. To further test the implemented amplifier and its usability in a realistic telecommunications system, some brief linearity and linearizability tests were performed.

For this purpose, a Orthogonal Frequency-Division Multiplexing (OFDM) signal was generated in Matlab and sent (from the VSG) to the amplifying chain. The output signal of the amplifier was measured (after a 46 dB attenuation) using a Vector Signal Analyzer (VSA). In order to compensate and reduce the observed spectral regrowth, a Digital Predistorter (DPD), based on the Generalized Memory Polynomial (GMP) model [41], was implemented.

In the GMP model, equation 4.1, where x(n) is the complex envelope of the input signal that is to be amplified, and $y_{GMP}(n)$ is the complex envelope of the signal transformed by the GMP model (which is, then, applied to the PA input after modulation), both nonlinear and memory effects (and their cross terms) are taken into account for the calculation of the new (and predistorted) input signal for the amplifier. Iteratively, the parameters of the DPD are calculated and (hopefully) the spectral regrowth is reduced.

$$\begin{aligned} y_{GMP}(n) = & \sum_{p=0}^{P-1} \sum_{l=0}^{L-1} a_{pl} x(n-l)|x(n-l)|^p \\ & + \sum_{k=0}^{K-1} \sum_{l=0}^{L-1} \sum_{m=0}^{M-1} b_{klm} x(n-l)|x(n-l-m)|^k \\ & + \sum_{k=0}^{K-1} \sum_{l=0}^{L-1} \sum_{m=0}^{M-1} c_{klm} x(n-l)|x(n-l+m)|^k. \end{aligned} \tag{4.1}$$

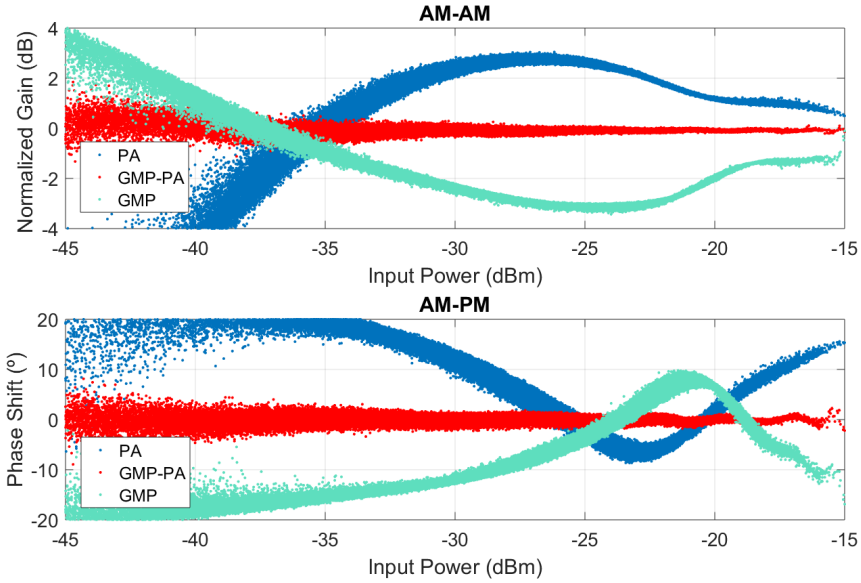
The linearity can also be seen and evaluated through Amplitude to Amplitude conversion (AM/AM) and Amplitude to Phase conversion (AM/PM) tests. The goal, in the AM/AM test, is to have linear amplification (linear gain) throughout all input power levels, and, for the AM/PM case is to have a 0^{o} of phase shift for all input power levels. Increasing the polynomial order, P, might contribute to a better fitting of the gain/phase curve and, for high hysteresis curves, the memory depth of the model is increased.

For the developed DhPA, the tuned configuration parameters for the GMP model are presented in Table 4.2. Figures 4.10 and 4.11 show the linearization results of the DhPA for a 10 and 20 MHz OFDM signal, respectively.

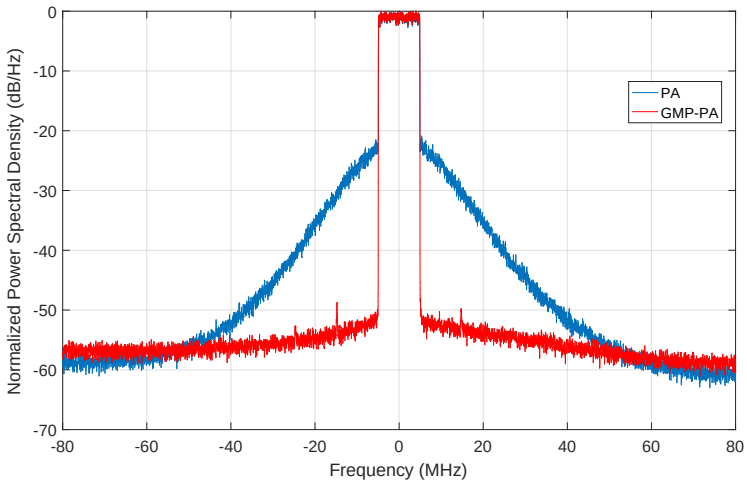
Polynomial Order (P)	11
Memory Depth (M)	5
Cross-Term Order (K)	3
Cross-Memory Depth (L)	1

Table 4.2: Considered configuration parameters for the GMP model.

The coefficients of the GMP DPD were determined through a direct learning iterative process. After a few iterations, the Adjacent Channel Power Ratio (ACPR) was reduced from approximately -25 dBc to -55 dBc, in the 10 MHz signal case (Figure 4.10b), and to -50 dBc, in the 20 MHz signal case (Figure 4.11b).

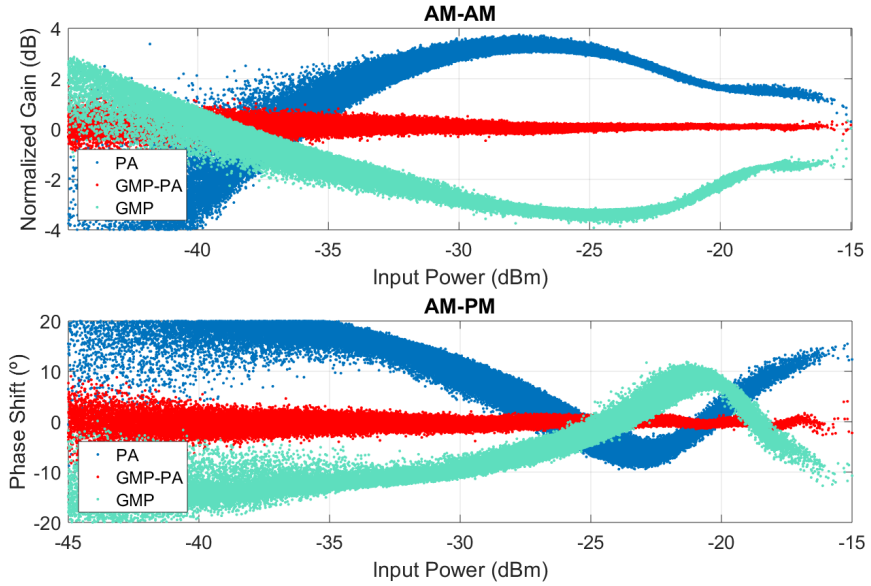


(a)

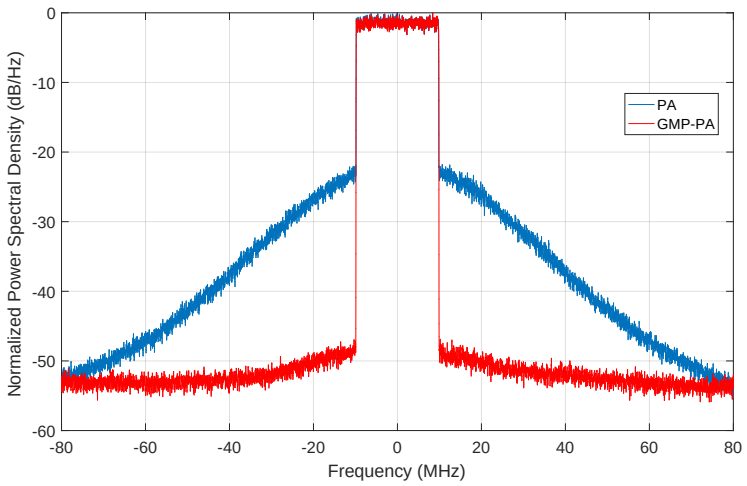


(b)

Figure 4.10: Linearization results of the DhPA subjected to a OFDM signal of 10 MHz bandwidth: (a) AM/AM and AM/PM and (b) spectra.



(a)



(b)

Figure 4.11: Linearization results of the DhPA subjected to a OFDM signal of 20 MHz bandwidth: (a) AM/AM and AM/PM and (b) spectra.

CHAPTER 5

Conclusive Remarks

5.1 Discussion and Conclusions

The focus of this work was to study, design and implement a Doherty power amplifier to operate on RF signals centered at the 4.5 GHz carrier frequency, which would allow testing distinct combiner solutions. A Doherty amplifier was successfully designed and tested in the RF laboratory, presenting desirable characteristics in terms of output power, efficiency and linearizability.

Throughout the study, design and implementation of this work, a significant amount of knowledge on specific issues of the Doherty architecture were progressively learnt and acquired. Therefore, and since the time available for it was limited, some decisions had to be made still at an early stage, where some operational details of this amplifier were not yet fully matured. At the end of this project, and looking back to the implemented solutions, it seems reasonable to mention some points which could have been slightly modified to lead to a final Doherty amplifier with an improved performace. Thus, in the following text, suggestions are made on the considered design solutions that could have been followed in this work to reach a better amplifier.

Uneven power splitting could have been used to improve the dynamic load modulation of the carrier PA, as the output current of the peaking amplifier could reach its maximum value. Although this would lead to an overall lower gain of the DhPA, at higher output power, the gain compression would be reduced - leading to a more linear amplifier. Also, the efficiency at full power would increase.

The stabillity analysis could have been more detailed, in the initial design stage, and the stabillity of the total system should have been evaluated a priori. Doing that would allow, in the design stage, to optimize the input bias networks and IMN by

taking into account the lumped components used for stabillity, improving the amplifier's characteristics.

A different structure of the matching networks could have been considered, allowing a reduction of the distance between the two amplifiers, and, possibly the traditional output combiner could be directly implemented without the offset lines. Also, the transistors could be replaced by the CGH40010P version, where the source terminal is smaller (further contributing to a reduction of the used space).

5.2 Future Work

Since this amplifier was designed for testing different output combiners, a natural follow up of this work would be the design and implementation of distinct power combiners which would be composed of transmission lines, with lines and stubs to achieve a certain performance, and/or different antenna structures that would contribute to the acquisition of specific knowledge and experience in electromagnetic coupling and its impact on the performance of a Doherty power amplifier. An additional objective for persuing with this work would be to investigate ways to increase the bandwidth of the conventional DhPA by adequately designing output coupling structures. And this could also be done simultaneously with the tentative reduction of the space required by both combiner and antenna, by merging these two elements together.

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