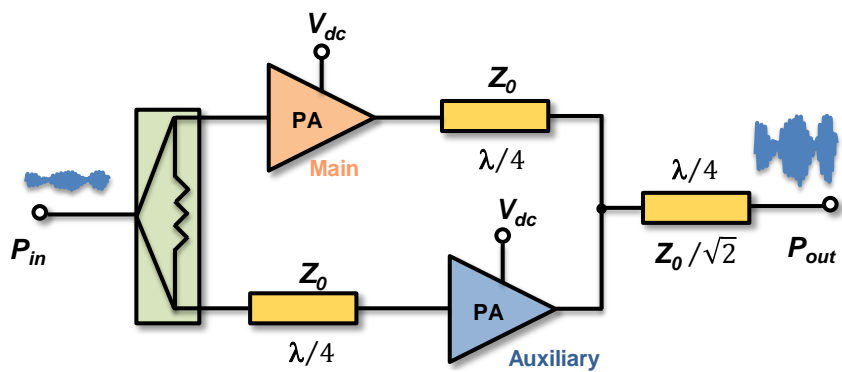




Luís Carlos Cótimos  
Nunes

## Mecanismos de Geração da Distorção Não-Linear em Amplificadores Doherty

### Nonlinear Distortion Generation Mechanisms in Doherty Amplifiers







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Doherty Amplifiers**

Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Electrotécnica, realizada sob a orientação científica do Doutor Pedro Miguel da Silva Cabral, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro e sob a coorientação científica do Doutor José Carlos Esteves Duarte Pedro, Professor Catedrático do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

Apoio financeiro da Fundação para a Ciência e a Tecnologia (FCT) no âmbito de uma bolsa de investigação, ref. SFRH/BD/89941/2012, e do projecto EXPL/EEI-TEL/0851/2013.

Apoio financeiro da Fundação Luso-Americana para o Desenvolvimento (FLAD) através de uma bolsa à participação de oradores portugueses nos EUA, ref. 2015/CON11/CAN9.



Dedico este trabalho à minha namorada, aos meus pais e à minha irmã pelo incansável apoio.



## **O júri / The jury**

Presidente / President

Doutor Luis Filipe Pinheiro de Castro  
Professor Catedrático da Universidade de Aveiro

Vogais / Examiners committee

Doutor Francesc Purroy Martin  
Senior Expert, Huawei Technologies, Sweden AB

Doutor João Manuel Torres Caldinhas Simões Vaz  
Professor Auxiliar do Instituto Superior Técnico da Universidade de Lisboa

Doutor José Alberto Peixoto Machado da Silva  
Professor Associado da Faculdade de Engenharia da Universidade do Porto

Doutor João Nuno Pimentel da Silva Matos  
Professor Associado da Universidade de Aveiro

Doutor Pedro Miguel da Silva Cabral  
Professor Auxiliar da Universidade de Aveiro (orientador)



## **Agradecimentos / Acknowledgments**

Em primeiro lugar gostaria de agradecer aos meus pais, por uma vida de esforço e dedicação. À minha irmã pela sua preocupação e amizade. Aos três pelo incansável apoio, encorajamento e exemplo que sempre me proporcionaram em todas as situações da minha vida, tanto profissionais como pessoais. Sem eles nada disto teria sido possível.

Aos meus orientadores Prof. Pedro Miguel Cabral e Prof. José Carlos Pedro por todos os conhecimentos que me transmitiram, pelo apoio, motivação e orientação que sempre me deram. Agradeço também o excelente ambiente de trabalho que me foi proporcionado e o exemplo que me transmitiram, levando-me a procurar sempre a excelência.

A todo o grupo de Circuitos e Sistemas de Rádio do Instituto de Telecomunicações de Aveiro, por todas as sugestões, discussões e pelo ótimo ambiente de trabalho durante todo o meu percurso.

À Huawei technologies por me ter proporcionado a oportunidade de trabalhar para um projecto muito desafiante e que muito contribui para melhorar o meu trabalho. Nomeadamente gostaria de agradecer ao Dr. Francesc Purroy, Dr. Oleg Pozdeev and Mr. Zeng Zhixiong por todas as sugestões e discussões que tivemos durante o meu trabalho.

Agradeço também à Universidade de Aveiro, ao Departamento de Electrónica, Telecomunicações e Informática e ao Instituto de Telecomunicações por me terem facultado todos os meios e ambiente de trabalho necessários. Assim como a todos os colaboradores destas instituições que contribuíram para o meu trabalho.

À Fundação para a Ciência e Tecnologia pelo apoio financeiro concedido sob a forma de uma bolsa de Doutoramento.

À Fundação Luso-Americana para o Desenvolvimento (FLAD) por me ter subsidiado uma das viagens aos Estados Unidos para participação num congresso.

Gostaria também de agradecer a amizade de todas as pessoas que me apoiaram e me deram forças para continuar, mostrando-se sempre presentes.

Por fim, não poderia deixar de agradecer à minha namorada pelo seu incondicional apoio, encorajamento e compreensão nos momentos mais difíceis. Sem a sua força tudo teria sido muito mais complicado.

A todos o meu muito Obrigado!



## **palavras-Chave**

AM/AM, AM/PM, Amplificadores de Potência, Amplificadores Doherty, Distorção Não-Linear, Eficiência Elevada, Linearidade, Modulação da Carga, Modelação de Dispositivos

## **resumo**

Presentemente, os sistemas de comunicações sem fios exigem uma maior mobilidade e elevadas taxas de transferência. Para além disso, a necessidade de eficiência espectral obriga ao uso de esquemas de modulação de envolvente variável. Consequentemente, o desenvolvimento de amplificadores de elevada eficiência, com uma elevada largura de banda e, ao mesmo tempo, lineares, tornou-se num dos maiores desafios para os engenheiros de projeto de amplificadores de potência. Por forma a cumprir estes requisitos muito rigorosos, o amplificador em configuração Doherty parece ser a técnica mais promissora. Contudo, devido à sua complexa operação, os seus mecanismos de geração de distorção não linear não são ainda completamente conhecidos. Atualmente, apenas interpretações heurísticas estão a ser usadas para justificar os fenómenos observados. Nesse sentido, o principal objetivo deste trabalho é desenvolver um modelo capaz de descrever os mecanismos de geração da distorção não linear em amplificadores Doherty, permitindo assim, a optimização do seu projeto, tendo em conta as especificações de linearidade e eficiência. Para além disso, esta abordagem permitirá uma ponte entre dois mundos diferentes: projecto de amplificadores de potência e pré-distorção digital, uma vez que o conhecimento recolhido da operação do Doherty ajudará na escolha de modelos de pré-distorção mais adequados.



**keywords**

AM/AM, AM/PM, Device Modelling, Doherty Amplifiers, High Efficiency, Linearity, Load Modulation, Nonlinear Distortion, Power Amplifier

**abstract**

Nowadays, wireless communications systems demand for greater mobility and higher data rates. Moreover, the need for spectral efficiency requires the use of non-constant envelope modulation schemes. Hence, power amplifier designers have to build highly efficient, broadband and linear amplifiers. In order to fulfil these strict requirements, the practical Doherty amplifier seems to be the most promising technique. However, due to its complex operation, its nonlinear distortion generation mechanisms are not yet fully understood. Currently, only heuristic interpretations are being used to justify the observed phenomena. Therefore, the main objective of this work is to provide a model capable of describing the Doherty power amplifier nonlinear distortion generation mechanisms, allowing the optimization of its design according to linearity and efficiency criteria. Besides that, this approach will allow a bridge between two different worlds: power amplifier design and digital pre-distortion since the knowledge gathered from the Doherty operation will serve to select the most suitable pre-distortion models.



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## List of Acronyms

ADS	Advanced Design System
AM	Amplitude Modulation
AM/AM	Amplitude Modulation to Amplitude Modulation
AM/PM	Amplitude Modulation to Phase Modulation
CAD	Computer Aided Design
CW	Continuous Wave
DC	Direct Current
DLM	Dynamic Load Modulation
DHT	Doherty
DPA	Doherty Power Amplifier
DPD	Digital Pre-Distortion
DSP	Digital Signal Processing
GaN	Gallium Nitride
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
FET	Field Effect Transistor
H-EER	Hybrid-Envelope Elimination and Restoration
HB	Harmonic Balance
HEMT	High Electron Mobility Transistor
IMD	Intermodulation Distortion
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long-Term Evolution
LUT	Look-Up Table
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSCAP	Metal Oxide Semiconductor Capacitor
MESFET	Metal-Semiconductor Field Effect Transistor
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PD	Pre-Distortion
PM	Phase Modulation
RF	Radio Frequency
RFPA	Radio frequency Power Amplifier

Si	Silicon
VoHB	Volterra on top of Harmonic-Balance
W-CDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access

# 1. Introduction

## 1.1. Background and Motivation

Energy consumption is one of the most important issues in all kinds of applications. Wireless communication systems are no exception, considering that a remarkable effort has been put in increasing the efficiency of their building blocks in order to decrease the overall energy consumption of the whole architecture. Fig. 1.1 represents a general block diagram of a conceptual wireless communication base station transmitter, which is composed of four main blocks: signal processing and control section, RF conversion and power amplification part, power supply system and cooling sector.

The most challenging part of a base station, in terms of energy consumption, is the final stage of the RF power amplification (about 40% of overall energy consumption [1]). Therefore, it is very important to increase the efficiency of the power amplifier, which translates into a direct reduction in its energy consumption. In addition, this efficiency enhancement of the power amplifier also allows for a reduction in the power consumption of the cooling system or even eliminate it [2].

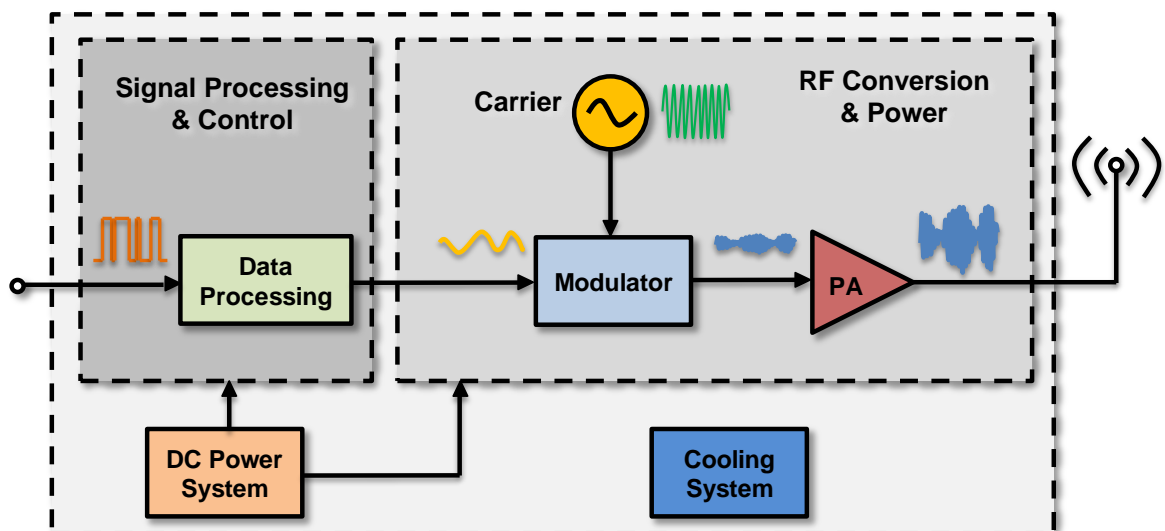


Fig. 1.1 – Block diagram of a conceptual wireless communication base station transmitter link.

In addition, modern wireless communication systems try to find solutions to solve problems that appeared with the rapid growth of data rates and with the increased

demand for mobility. Moreover, the very strict spectral masks imposed by telecommunication regulators, lead to the development of complex modulation formats, such as Wideband Code Division Multiple Access (W-CDMA), Long-Term Evolution (LTE) and Worldwide Interoperability for Microwave Access (WiMAX).

These new signals, modulated in amplitude, AM, and phase, PM, have large peak-to-average power ratios (PAPR) [3] – i.e., the ratio between the average and peak power values (it can reach up to 12 dB) – and whose relative bandwidths may reach, in extreme cases, 20% of the carrier frequency. This being the case, conventional current-mode power amplifiers are no longer a solution, since they are extremely inefficient when operated in back-off mode [4], as is illustrated in Fig. 1.2.

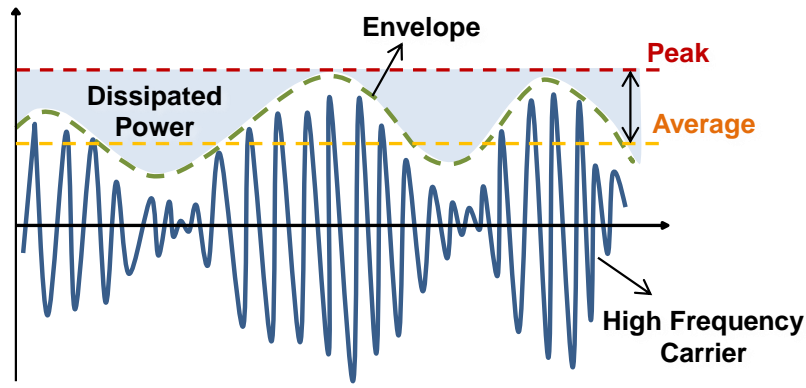


Fig. 1.2 – Illustration of the PAPR problem.

In this scenario, over the last decades, new techniques have appeared to improve the average efficiency of power amplifiers without degrading their linearity [5]–[9]. Actually, these techniques became new radio frequency transmitter architectures and they can be divided in two different strategies: PA supply voltage modulation and load modulation.

To understand the operating principle of these new techniques, let us concentrate on a classical class B power amplifier, whose efficiency is a function of amplitude,  $V_i(t)$ , given by:

$$\eta = \frac{P_{out}(t)}{P_{dc}(t)} = \frac{\pi R_L}{8 V_{dc}} G_m V_i(t) \quad (1.1)$$

where  $R_L$  is the load impedance,  $V_{dc}$  is the supply voltage and  $G_m$  is the transconductance of the transistor. To ensure linearity, the maximum PA signal excursion is limited by the knee voltage,  $V_K$ , otherwise the transistor enters the triode zone. Therefore, if the analysis is restricted to the case of fixed load and power supply voltage, the maximum efficiency is only obtained when the envelope peaks are equal to (1.2).

$$V_{i,Max} = 2 \frac{V_{dc} - V_K}{G_m R_L} \quad (1.2)$$

In order to solve the problem mentioned above, the supply voltage modulation technique dynamically reduces  $V_{dc}$  with the decrease of the amplitude envelope, whereas in the case of the load modulation technique it is the load that dynamically decreases with the increase of the amplitude envelope. As can be seen from (1.1) and from the illustration of the conceptual  $i_{DS}/V_{DS}$  characteristics of these techniques, in a class B power amplifier (Fig. 1.3), the amplifier will always be at the maximum efficiency point, thereby eliminating the waste of power consumption in zones of high output power back-off.

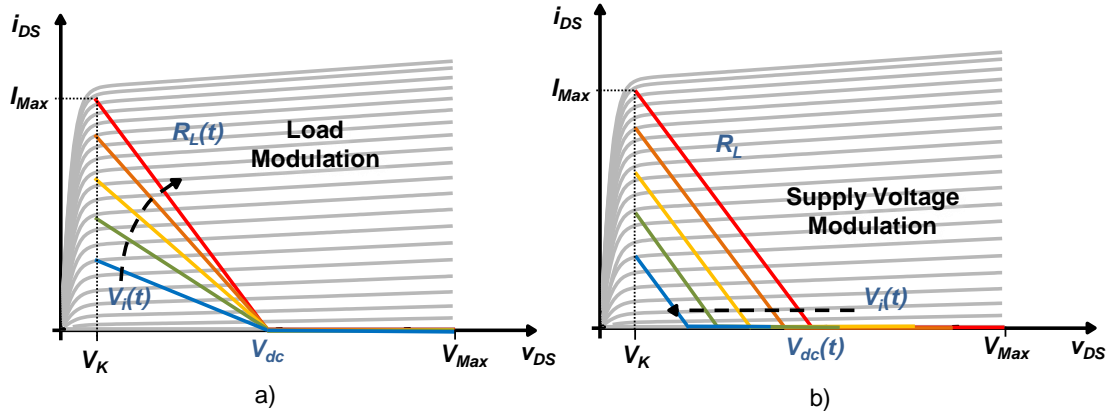


Fig. 1.3 – Conceptual  $i_{DS}/V_{DS}$  characteristics of efficiency enhancement techniques by a) load modulation and b) supply voltage modulation.

On one hand, regarding efficiency enhancement techniques by power supply voltage modulation, there are the EER [5][10], ET [11]–[14], H-EER [9][15] and Polar architectures [7]. On the other hand, recognized load modulation techniques in literature are the Doherty [16], Chireix Outphasing [17], and Dynamic Load Modulation architectures (DLM) [18]–[20]. Fig. 1.4 shows a comparison of the efficiency of all these techniques (when class B operation mode is considered for the main amplifier) as a function of envelope amplitude.

The Doherty architecture has been considered one of the most powerful architectures to extend the PA high efficiency operation region by the scientific community and the industrial community. The Doherty architecture was proposed in the 30s by W. H. Doherty [16] and today it is again reconsidered. It is based on the principle of active load modulation and the classical topology of this architecture uses two power amplifiers called the main and auxiliary amplifier, as shown in Fig. 1.5. Nevertheless, it is possible to use more than one auxiliary amplifier, which results in the so-called N-way Doherty or N-stage Doherty, depending on how the peaking amplifiers are interconnected [21]–[24]. The auxiliary amplifiers collaborate with the main amplifier so that it maintains a high efficiency for lower levels of input power and without saturating for high values of input power.

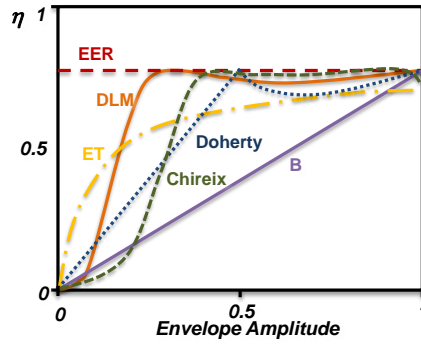


Fig. 1.4 – Efficiency of the efficiency enhancement techniques (when class B operation mode is considered for the main amplifier) as a function of envelope amplitude.

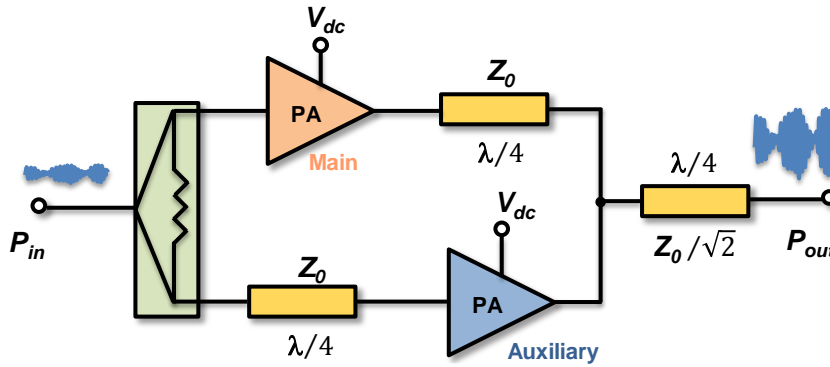


Fig. 1.5 – Classical block diagram of the Doherty architecture.

Although the Doherty amplifier presents a high efficiency for a wide range of input power levels, as well as it allows the use of new signals with high bandwidth, the practical Doherty amplifier presents a nonlinear behaviour due to the imperfect load modulation and the nonlinear behaviour of each of its amplifiers [22].

The nonlinear phenomena observed in the Doherty amplifier are explained in the literature [21], [25], [26] based on the behaviour of active devices operating in small signal, i.e. in the linear regime, and considering only the amplitude modulation to amplitude modulation (AM/AM) characteristics. This theory is centred on the fact that the main amplifier operates in class AB and the auxiliary amplifiers operates in class C, presenting compressive and expansive AM/AM characteristics, respectively. The auxiliary amplifiers compensate the compressive behaviour of the main amplifier resulting in a minimum of intermodulation distortion of the entire Doherty amplifier. However, even this justification which addresses only the AM/AM characteristic, is invalid because the Doherty amplifier is commonly used for very large signals, when their amplifiers are already very nonlinear.

The industry makes the amplifiers operate in a very nonlinear regime for energy efficiency optimization reasons. Therefore, as the mechanisms of nonlinear distortion

generation and control in the Doherty Amplifier are not yet fully understood, the linearization schemes used until now (in most cases digital pre-distortion) are chosen following a purely heuristic approach [27]–[30] and, consequently, with only a moderate probability of success. This way, the main objective of this PhD thesis work is to provide a model capable of describing and explaining the distortion generation mechanisms of a Doherty amplifier based on the most common RF transistor technologies presently used in power amplifiers for cellular infrastructures: the Si LDMOS and the GaN HEMT. This will enable the design of an amplifier with a better compromise between efficiency and linearity and the establishment of linearization schemes more suited to the compensation of these distortion generation mechanisms.

## **1.2. State-of-the-Art**

This section is dedicated to present an overview of the state-of-the-art regarding the Doherty power amplifier. It starts by a brief description of the ideal Doherty power amplifier architecture, presenting its main blocks and how they interact to obtain the desired high efficiency without compromising the linearity.

Secondly, the aspects of a practical Doherty power amplifier implementation that differ from the aforementioned theoretical analysis are presented. On this regard, the published studies concerning nonlinear distortion, for single-ended power amplifiers used to build the Doherty architecture, are discussed. After that, single-ended nonlinear distortion interactions in a Doherty arrangement are addressed.

Finally, the Doherty PA efficiency optimization, namely on what concerns techniques to improve the efficiency at higher back-off levels (beyond the 6dB of the conventional design) are presented.

### **1.2.1 Doherty Power Amplifier Architecture**

Doherty amplifier has been the most promising wireless communications PA architecture for base-stations. It was proposed in 1936 by W. Doherty [16] as a solution to the problem of efficiency degradation in the presence of a fully modulated signal in the Chireix architecture. Doherty attributed this reduction of efficiency to the fact that the Chireix arrangement does not work on completely resistive loads as his system does [16]. Therefore, the Doherty amplifier emerges as an architecture based on the principle of active load modulation capable of providing a high efficiency without compromising the linearity.

The classical arrangement of the Doherty amplifier (2-Way) can be seen in Fig. 1.5. It consists of a power splitter that divides the input signal into two branches, and then it uses two amplifiers (the main and auxiliary amplifiers), which are interconnected through a quarter-wavelength line. The main amplifier (also known as the carrier amplifier) is normally biased in class B, while the auxiliary amplifier (also known as the peaking amplifier) is biased in a moderate or deep class C. Thus, when the input power is very low it is assumed that the peaking amplifier is cut-off, i.e. the output current provided by the peaking PA,  $I_P$ , is equal to zero. Therefore, for low levels of input power, there is only the carrier PA, operating as a single-ended class B PA except that it is terminated by a load that is exactly twice the one expected in a conventional class B.

With the increase of the power level of the excitation signal, the efficiency of the main amplifier will increase until it reaches its peak (ideally 78.5%). It should be noted that, as the load impedance is twice the one expected in a conventional class B PA, this maximum peak is expected when the input voltage reaches half of the admissible excursion signal,  $V_{in,max}/2$ , as shown in Fig. 1.4 and Fig. 1.6.

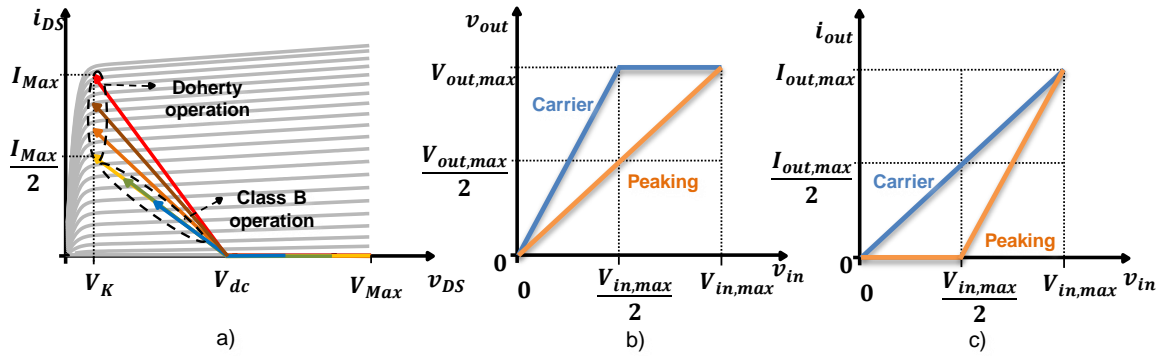


Fig. 1.6 – a) Load Lines of the carrier amplifier in the Doherty architecture; b) Voltages and c) Currents of the carrier and peaking amplifiers as function of the input voltage.

In order to prevent the carrier amplifier from entering the triode zone, when the input voltage becomes higher than  $V_{in,max}/2$ , the peaking amplifier becomes active providing the necessary current to reduce the load impedance of the carrier amplifier. Actually, the peaking and carrier amplifiers behave as active loads to each other. From this point on, the main amplifier will operate as a voltage source and with a constant efficiency. When, finally the auxiliary amplifier reaches its maximum efficiency, the second point of maximum efficiency of the Doherty amplifier is obtained, as shown in Fig. 1.4.

In practice, there are some aspects to take into account that differ from the theoretical analysis described above. Firstly, a class B amplifier introduces distortion even before reaching the triode zone. In addition, a class C amplifier does not provide the

desired abrupt transition from the cut-off region to the region of perfectly linear operation, and the current gain provided by the class C peaking amplifier is less than the one of a class B amplifier. These nonlinear contributions from each amplifier will also degrade the theoretical load modulation, which results in a further nonlinear behaviour [8].

### **1.2.2 Distortion Analysis of the Doherty Amplifier**

As mentioned above, the Doherty amplifier combines two amplifiers (supposedly current-mode amplifiers) through a quarter-wavelength line, where each sub-amplifier has its associated nonlinear distortion. Therefore, in order to understand the nonlinear distortion of the whole Doherty amplifier, first it is necessary to understand the distortion generation mechanisms in each amplifier individually and then understand how these nonlinear phenomena interact in a Doherty arrangement.

#### **A. CARRIER AND PEAKING DISTORTION ANALYSIS**

Two very important characteristics of an amplifier that are recognized to assess its linearity are the Amplitude-induced amplitude variation, AM/AM, and the amplitude-induced phase variation, AM/PM, characteristics. So, it is important to study the causes of distortion in these two characteristics of a power amplifier when it is subjected to complex amplitude and phase modulation formats.

The AM/AM characteristic has been a highly regarded topic by the scientific community and for many years was considered sufficient to assess the PA intermodulation distortion (IMD) performance [31]–[34]. The performed studies were based on small-signal analysis with Volterra series and then extrapolated to large signal, commonly using Describing Functions (DF) techniques [35].

In these studies, for a static analysis, it is assumed that the output current of an active device can be described with a low order Volterra series, or its memoryless subset, the Taylor series:

$$I_{out}[v_{in}(t)] = I_{DC} + G_{m1} \cdot v_{in}(t) + G_{m2} \cdot v_{in}(t)^2 + G_{m3} \cdot v_{in}(t)^3 \quad (1.3)$$

where  $v_{in}$  is the RF input voltage and the  $G_{mx}$  coefficients are the  $x^{\text{th}}$ -order expansion coefficients of the nonlinear transconductance. In Fig. 1.7 it can be seen the typical variations of these coefficients as a function of input voltage up to the 3rd order expansion for a FET.

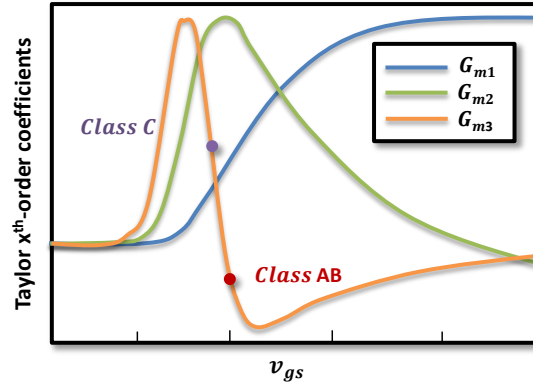


Fig. 1.7 – Normalized coefficients of the FET's nonlinear transconductance up to 3rd-order.

The odd coefficients of the output current expansion in Taylor series are the only ones that cause in-band distortion because these are the only ones that produce mixing-products coincident with the fundamental. Therefore, focusing only on the  $G_{m3}$  coefficient, the variations that exist on it according to the bias point determine the existing changes in the 3<sup>rd</sup> order IMD.

These analyses about the impact of the bias point on the intermodulation distortion and, consequently, in the AM/AM characteristic, help us understand and clarify the classes of operation near the threshold voltage,  $V_T$ . Thus, the class B operation is defined when the transistor is biased exactly in the null of  $G_{m3}$ , which results in a minimum of the IMD3 (the so-called small-signal IMD sweet-spot). Positive values of the  $G_{m3}$  result in a gain expansion (class C behaviour), while for negative values of the  $G_{m3}$  the gain is compressive (class AB behaviour) [36].

Although these studies only address the AM/AM characteristic, they were able to predict most of PA distortion behaviour, namely the so-called IMD sweet-spots, despite neglecting the possible AM/PM conversion of the amplifier. However, in order to be able to expand this analysis to large signal, it is assumed that the large-signal distortion in a PA can be represented by Describing Functions [31], which is not always easy to perform. In addition, it is also assumed that the overall PA distortion is the sum of the small-signal response with the large-signal response, which is not always correct.

Recently, some large-signal studies have been published addressing the AM/AM as well as the AM/PM distortion in a PA [37], [38]. In these studies, it is also used a Volterra analysis but now built on top of a harmonic balance simulation. Unfortunately, as their authors did not derive any analytical model for the amplitude and phase nonlinear distortion generation mechanisms, and for their potential relationship, they were unable to connect these simulated nonlinear distortion sources to the PA measured characteristics.

## ***B. DISTORTION ANALYSIS OF THE OVERALL DOHERTY AMPLIFIER***

The analysis using the Taylor expansion can also be applied in the study of the nonlinear phenomena observed in the Doherty amplifier [22], [25], [26]. Actually, this is the state-of-art of the theoretical analysis of the nonlinear distortion of Doherty amplifiers.

From the studies carried out on current-mode PAs operating in small-signal, it is known that the nonlinear distortion of an active device is strongly dependent on the bias point, i.e. the operation class. Thus, as the main amplifier is normally biased in a class AB regime, i.e. a negative  $G_{m3}$ , it exhibits a gain compression characteristic over the entire range of input power. On the other hand, the auxiliary amplifier is normally biased in a class C regime, i.e. a positive  $G_{m3}$ . So, it exhibits a gain expansion characteristic for low levels of input voltage. Therefore, by adding up these distinct nonlinear behaviours, namely a positive and negative  $G_{m3}$ , it is possible to cancel the IMD3 of the whole Doherty amplifier and, consequently, producing an amplifier with a gain characteristic much more flat [21].

Once again, the previous study neglected possible AM/PM conversions of the amplifiers and how they affect the nonlinear load modulation. Moreover, as mentioned in the Background and Motivation, the issues of reducing energy consumption in base stations lead the PA's designers to design amplifiers focusing predominantly on the efficiency performance and, consequently, the amplifiers will operate close to saturation. Unfortunately, this prevents the cancellation of the nonlinear distortion generation mechanism based on the main and auxiliary amplifiers producing a strongly nonlinear behaviour, which fails the strict wireless communication standards. In order to solve this, the industry usually uses digital pre-distortion techniques but not always successfully. Thus, it is very important to know why the digital pre-distortion fails and the only way to do that is to fully understand the nonlinear distortion generation mechanisms of a Doherty amplifier. This is precisely the main objective of this PhD Thesis.

### ***1.2.3 Efficiency Enhancement Techniques in the Doherty Amplifier***

Since the introduction of the Doherty amplifier, the wireless communication signals have constantly evolved to keep up with the strong demand for higher transmission rates and fulfil the strict spectral masks. Naturally, both the scientific and the industrial communities have been putting efforts in the design of Doherty amplifiers even more efficient than the classical one, as well as in the development of techniques to improve their linearizability. This section is dedicated to the new efficiency and linearizability

enhancement techniques that are applied to the Doherty amplifiers to accommodate the modern wireless communication signals.

A classic Doherty with one auxiliary amplifier can produce two peaks of efficiency, one at the maximum input power and another one at 6 dB below this point. However, the new wireless communication signals have a PAPR higher than this value, sometimes as high as 12dB. Therefore, to solve this problem, a new topology appeared in the literature, the so-called N-Way Doherty [21], [39], which uses more than one auxiliary amplifier. Fig. 1.8 illustrates this topology of the Doherty amplifier as well as the efficiency characteristic as a function of the auxiliary amplifiers that are used.

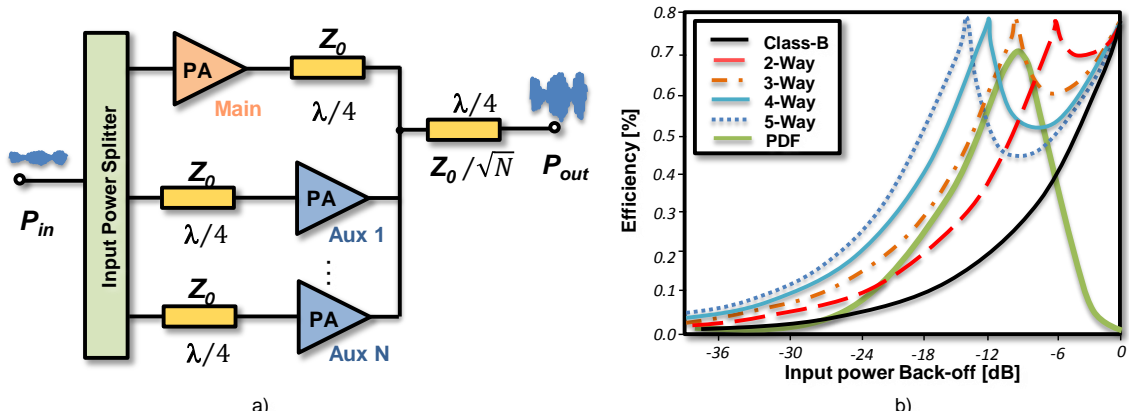


Fig. 1.8 – N-Way Doherty Amplifier: a) N-Way block diagram; b) N-Way efficiency characteristic and the PDF of a W-CDMA signal with 10 dB of PAPR.

In Fig. 1.8 b) it is possible to see the improvement of the average efficiency using the N-Way Doherty arrangement. For example, the 3-Way Doherty has the first maximum peak exactly at the maximum peak of the probability distribution function (PDF) of a W-CDMA signal with 10 dB of PAPR. However, with the increase of the number of auxiliary amplifiers, the efficiency between the two peaks will be increasingly degraded. Therefore, an alternative topology has been considered, the N-Stage Doherty amplifier [22]–[24], [40], [41].

In the literature, there are two different arrangements of the three-stage Doherty amplifier as shown in Fig. 1.9. In the first one, the carrier amplifier has the structure of a Doherty amplifier and the other auxiliary amplifier modulates its load. In the second one, it is used a Doherty amplifier to modulate the load of a single-ended carrier amplifier. In these topologies the auxiliary amplifiers are turned on sequentially allowing three peaks on the efficiency characteristic, as show in Fig. 1.9 c). Although both three-stage topologies present the same efficiency characteristic, the first one requires an active power splitter due to earlier carrier PA current saturation and so, the second one seems to be preferred because it presents a better linearity performance [22],[42].

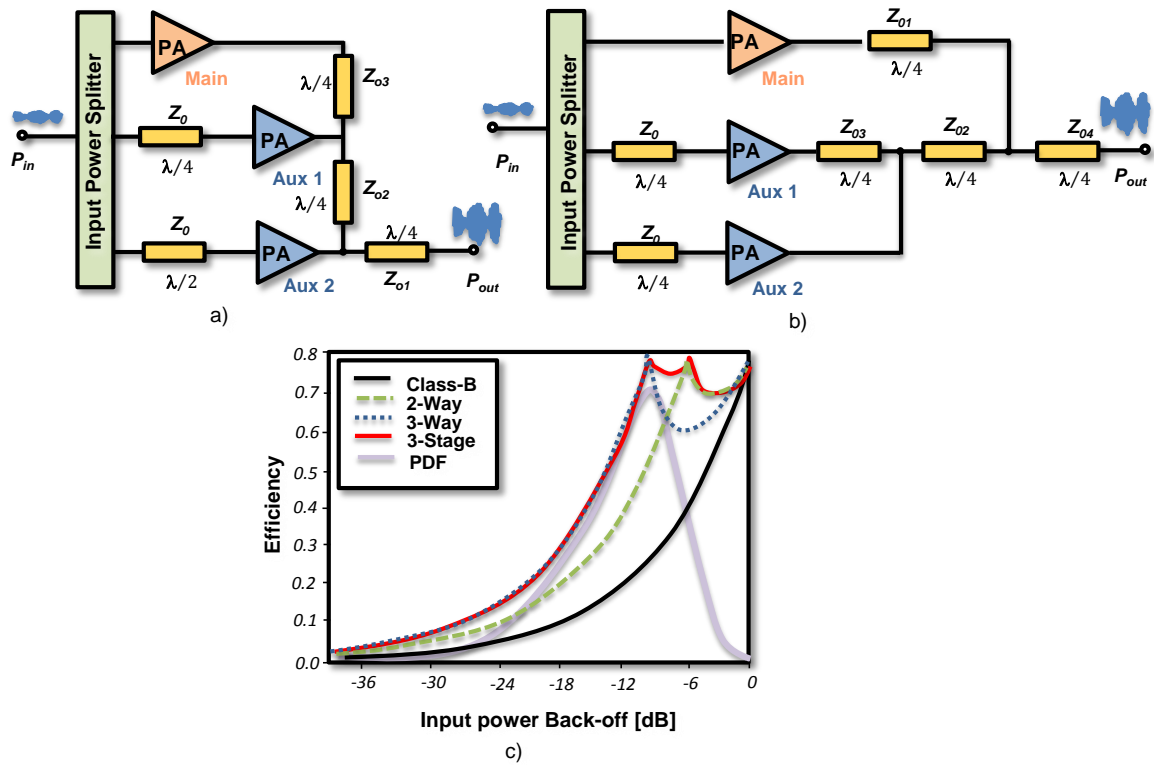


Fig. 1.9 – Three-Stage Doherty Amplifier: a) and b) different types of a Three-Stage arrangements; c) Three-Stage efficiency characteristic and the PDF of a W-CDMA signal with 10 dB of PAPR

Unfortunately, although the theoretical calculations of the Doherty PA efficiency for all above arrangements predict that the efficiency peak at back-off is equal to the one obtained at full-power, in practical Doherty implementations the efficiency peaks vary with the back-off power level. It is observed that efficiency starts to increase as the back-off level is increased and then there is an efficiency degradation for higher back-off levels. In an attempt to explain this efficiency dependency on the back-off power levels, some transistor models with artificial series and parallel losses have been presented [43], [44].

The series losses are used to describe the initial efficiency increase with the back-off and the parallel losses are used to justify the efficiency degradation for higher back-off levels. However, although the series losses can have a physical support in the FET's channel resistance,  $R_{on}$ , the model with parallel losses does not have a physical meaning since the device package is almost purely reactive. Therefore, a physically consistent efficiency model capable of predicting the efficiency dependency on the back-off power levels, namely the efficiency degradation, would be helpful to optimize the Doherty power amplifier design.

In addition, all the Doherty arrangement topologies most often use the auxiliary amplifiers in class C regime so that they come into conduction only for large signal.

However, as it is known, a class C amplifier has a soft turn on as well as a lower current gain. These nonlinear phenomena will produce an imperfect load modulation causing a nonlinear behaviour in the Doherty amplifier. To solve these problems, in the literature there were proposed some approaches, such as the use of an unequal power divider at the input [45], [46], different transistor peripheries [47]–[50], asymmetrical drain voltages [51], [52] or more complicated solutions such as using drivers before the main and auxiliary amplifiers [53], [54], changing the gate bias digitally [40], [55], [56] and independent paths for the main and auxiliary amplifiers [57], [58].

In addition to the efficiency and linearizability enhancement techniques applied to the Doherty amplifier [56], [59], [60], the digital pre-distortion (DPD) techniques are indispensable to fulfil the strict linearity requirements imposed by the wireless communication operators. Unfortunately, as previously mentioned, these linearization schemes are not always successful, mainly because the PA designers usually attribute more weight to the efficiency enhancement when designing the Doherty PAs. Moreover, as the nonlinear distortion generation mechanisms of the Doherty PA are not yet fully understood, when the DPD techniques fail, the PA designers do not know how to improve the linearity of their Doherty PAs. Thus, it is essential to increase the knowledge of the nonlinear distortion mechanisms of the Doherty, so that it is possible to develop new PA design methodologies that improve the efficiency without compromising the linearity. This is precisely the main objective of this PhD Thesis.

### **1.3. Objectives and Thesis' Organization**

As mentioned in the Background and Motivation, the scientific and industrial communities have been putting significant efforts in obtaining power amplifiers with higher efficiency, higher linearity and higher bandwidth. At the moment, the approach that is usually taken consists in the design of power amplifiers optimized for efficiency in a wide bandwidth (often they are designed for multi-bands) and then use digital pre-distortion techniques in order to fulfil the stringent spectral masks.

The problem with this philosophy of efficiency maximization is that, as the linearization schemes are chosen following a purely heuristic approach [27]–[30], there is only a moderate probability of success. Therefore, it is necessary to change this approach and return to the theoretical foundations based on the mathematical modelling of circuits.

Thus, the overall objective of this PhD Thesis is to understand the physical operation of active devices as well as understanding the nonlinear distortion generation mechanisms in 2-Way Doherty amplifiers. For that, it is fundamental to have circuit level

nonlinear models of active devices able to predict the most important nonlinear characteristics of power amplifiers.

In order to accomplish all the objectives of this PhD work the following specific goals were defined:

- Develop nonlinear equivalent circuit models (of the most common transistor technologies) able to reproduce the observed AM/AM and AM/PM characteristics in practical power amplifiers
- Study the nonlinear distortion generation mechanisms of a current mode single-ended power amplifier operating in class AB, B and C.
- Study the nonlinear interaction between the main and auxiliary amplifiers which constitutes the load modulation process.
- Develop a nonlinear distortion behavioural model of a Doherty amplifier, based on the individual behaviour of each of its constituent blocks, as well as on the load modulation process.

With these objectives in mind, this PhD thesis is organized as follows:

Chapter 1 provides the motivation to this work and the state-of-the-art concerning the Doherty PA nonlinear distortion, as well as its efficiency optimization. In addition, the main objectives of this PhD work and the most relevant scientific contributions achieved are presented.

Chapter 2 is dedicated to the extraction of power transistor nonlinear models essential to the nonlinear distortion analysis performed in the next chapters. It starts with a generic model extraction methodology suitable for both GaN HEMT and Si LDMOS devices, followed then by a novel extraction methodology to incorporate the observed trapping effects in the GaN HEMT.

Chapter 3 identifies and explains the main nonlinear distortion generation mechanisms of the carrier and peaking PAs operating individually, as single-ended PAs, based on Si LDMOS and GaN HEMT. This is accomplished by presenting a semi-analytical model sufficiently accurate to predict their AM/AM and AM/PM PA characteristics.

Chapter 4 is devoted to the nonlinear distortion analysis of the overall Doherty arrangement based on both Si LDMOS and GaN HEMT technologies. It is also presented a nonlinear behavioural model based on swept power passive load-pull data using LUTs, which is able to predict the nonlinear distortion of a high-power Doherty PA. Beyond that, a simple model that describes the Doherty PA efficiency dependency on its load-pull ratio is also developed. For that, a justification for the higher efficiencies observed in PAs

based on GaN HEMTs, when subjected to wider load-pull ratios as compared with the one obtained with Si LDMOS based Doherty PAs, is presented.

Chapter 5 closes this PhD Thesis summarizing its most important conclusions and presenting possible future research topics.

### 1.4. Main Contributions

This PhD work originated important contributions for:

- 1) Active device modelling (GaN HEMTs);
- 2) Doherty PA design and for its individual cells nonlinear distortion analysis.

On what GaN HEMT modelling is concerned, a new nonlinear equivalent circuit model extraction methodology for a GaN HEMT subject to trapping effects was presented [C6]. Despite its simplicity, the model is capable of reproducing the fundamental GaN HEMT dynamic distortion characteristics.

Actually, the knowledge acquired during this modelling work also contributed to explain the observed GaN HEMT soft-compression characteristic and its envelope bandwidth related nonlinear memory [C5]. In addition, based on this physical behaviour knowledge, a method of attenuating the observed self-biasing of GaN HEMT based PAs was presented [J3].

Regarding the Doherty nonlinear distortion, a comprehensive and physically based analysis of the AM/AM and AM/PM nonlinear distortion generation mechanisms in both Si LDMOS and GaN HEMT based carrier and peaking PAs, operating individually as single-ended PAs, was developed [J1][C1]. The identification of the main Doherty individual cells nonlinear distortion sources was very useful to understand the Doherty nonlinear distortion mechanisms, namely the ones that affect the AM/PM characteristic [C2][C4].

Beyond these nonlinear distortion studies, a physically consistent explanation of the observed efficiency dependence on the Doherty load-pull ratio was presented [C3], identifying which is the best load modulation that maximizes the Doherty efficiency. This work was then extended to be able to predict the efficiency and output power load-pull contours of a class B power amplifier [J2].

It was also explained the impact of the trapping effects on GaN HEMT based Doherty PA load-pull ratios [C7], showing that this is the reason of the higher efficiencies commonly obtained from GaN HEMT based Doherty power amplifiers when subjected to wider load-pull ratios, as compared with their Si LDMOS counterparts.

The achievements obtained during this PhD were published in the most relevant international journals and conferences in the addressed scientific research areas (see below).

### Papers in International Journals

- [J1] **L. C. Nunes**, P. M. Cabral, and J. C. Pedro, "AM/AM and AM/PM Distortion Generation Mechanisms in Si LDMOS and GaN HEMT Based RF Power Amplifiers", *IEEE Trans. on Microw. Theory and Tech.*, vol. 62, no. 4, pp. 799 – 809, April. 2014.
- [J2] J. C. Pedro, **L. C. Nunes**, and P. M. Cabral, "A simple method to Estimate the Output Power and Efficiency Load-Pull Contours of Class B Power Amplifiers", *IEEE Trans. on Microw. Theory and Tech.*, vol. 63, no. 4, pp. 1239 – 1249, April. 2015.
- [J3] P. M. Cabral, **L. C. Nunes**, T. Ressurreição, and J. C. Pedro "Trapping Behavior of GaN HEMTs and its Implications on Class B PA Bias Point Selection," *Int. J. Numer. Model. Electron. Networks, Devices Fields*, (accepted for publication)

### Papers in International Conferences

- [C1] **L. C. Nunes**, P. M. Cabral, and J. C. Pedro, "A Physical Model of Power Amplifiers' AM/AM and AM/PM Distortions and Their Internal Relationship", *IEEE MTT-S Int. Microw. Symp. Dig.*, Seattle, WA, USA, Jun. 2013.
- [C2] **L. C. Nunes**, P. M. Cabral, and J. C. Pedro, "Study of the GaN HEMT Doherty Power Amplifier Distortion", *Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC)*, Leuven, Belgium, April 2014.
- [C3] J. C. Pedro and **L. C. Nunes**, "Efficiency Dependence on the Load-Pull Ratio of a Doherty PA", *IEEE MTT-S Int. Microw. Symp. Dig.*, Tampa, FL, USA, Jun. 2014.
- [C4] **L. C. Nunes**, P. M. Cabral, and J. C. Pedro, "AM/PM Distortion in GaN Doherty Power Amplifiers", *IEEE MTT-S Int. Microw. Symp. Dig.*, Tampa, FL, USA, Jun. 2014.
- [C5] J. C. Pedro, **L. C. Nunes**, and P. M. Cabral, "Soft Compression and the Origins of Nonlinear Behavior of GaN HEMTs", *European Microwave Conference (EuMC)*, Rome, Italy, Oct. 2014
- [C6] **L. C. Nunes**, P. M. Cabral, and J. C. Pedro, "A New Nonlinear Model Extraction Methodology for GaN HEMTs Subject to Trapping Effects", *IEEE MTT-S Int. Microw. Symp. Dig.*, Phoenix, AZ, USA, May. 2015

- [C7] **L. C. Nunes**, P. M. Cabral, and J. C. Pedro, "Impact of Trapping Effects on GaN HEMT Based Doherty PA Load-Pull Ratios", *Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC)*, Taormina, Italy, October 2015.

## **2. Nonlinear Modelling of Power Transistors useful for Nonlinear Distortion Analysis**

Since the main objective of this thesis is to study the nonlinear distortion generation mechanisms in a Doherty power amplifier, it is fundamental to have nonlinear models that are able to accurately reproduce the nonlinear phenomena of the RF power transistors. This being the case, the circuit level models are preferable due to their high prediction capabilities, where every circuit node can be analysed. This type of nonlinear model is also useful to individually study a particular nonlinear distortion source since the others can be removed.

As it was already mentioned, this thesis is focused on the two main RF power transistor technologies used to build power amplifiers for base stations, the Si LDMOS and GaN HEMT. The core of the model extraction methodology for these two types of RF power transistors is not substantially different. What most distinguishes these two technologies, in what modelling is concerned, is the low-frequency dispersion observed in the GaN HEMTs subject to trapping effects. This being the case, this chapter starts by presenting a generic model extraction methodology without trapping effects being suitable for GaN HEMT and Si LDMOS (with some modifications) devices and then, a novel extraction methodology to incorporate the trapping effects in the GaN HEMT Model is presented.

For validation purposes of the generic extraction methodology, a single GaN HEMT die with 3mm of gate width was used, which a measurement based model was extracted. This generic extraction methodology was also validated for high power devices using a GaN HEMT packaged 6-Cell x 2.7mm device, where the model was obtained by scaling the 3mm device model previously extracted. Both models were validated by comparing the predictions with the CW measurements over a class AB PA: AM/AM, AM/PM, output power and efficiency Load Pull contours. The trapping effects extraction methodology for GaN HEMT devices was also validated using the same devices.

## 2.1. General Nonlinear Model Extraction

### 2.1.1 Extraction Procedure

A GaN HEMT die can be modelled by the equivalent circuit presented in Fig. 2.1, which is composed by the extrinsic parasitic elements and by the intrinsic elements [61]. It should be noted that for Si LDMOS there is no input diode. Since the extrinsic elements are linear, the intrinsic reference plane, needed to extract the bias-dependent intrinsic elements, can be obtained using known de-embedding techniques. Thus, the proposed methodology to extract a model for a GaN HEMT die (without considering the observed long-term memory effects) has the following steps:

1. Extract the extrinsic elements
2. De-embed the extrinsic and extract the bias-dependent small-signal intrinsic elements.
3. Fit the intrinsic elements with physically meaningful nonlinear functions.
4. Implement the large-signal model
5. Validate the obtained model

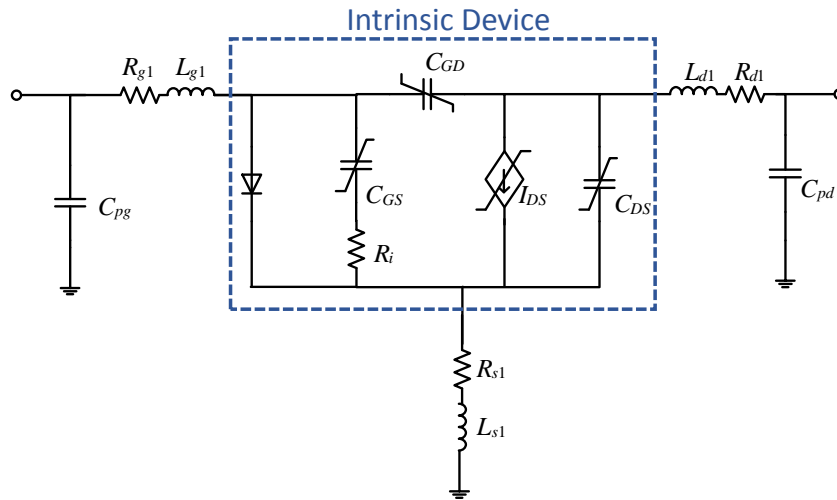


Fig. 2.1 – The adopted GaN HEMT die equivalent circuit

In the following sub-sections it is explained with more detailed this extraction methodology showing some examples for each extraction procedure step.

#### A. EXTRACTING OF THE EXTRINSIC ELEMENTS

From the physical knowledge of the device, a suitable equivalent circuit topology of the extrinsic components for the GaN HEMT die [61] was chosen, which is presented in Fig. 2.1.

The extraction of the extrinsic components can be conducted using analytical methods [62]–[67] or nonlinear optimization [68]–[72]. In general, the first ones are preferred because the extraction is faster than using optimization methods. However, for GaN-HEMT devices, there is no analytical methods to extract, completely and independently, all extrinsic elements, namely a method to separate the channel resistor,  $R_c$ , from the parasitic drain resistor,  $R_d$ , as it will be explained later on.

Although the analytical methods cannot provide a correct solution, they can be used to obtain a good first estimation or to get boundaries so that these results can be used in the optimization process. Therefore, this section starts with a brief introduction on how to get the initial conditions using analytical methods and then the optimization process to extract the complete extrinsic elements will be addressed.

### ***Extrinsic Element Extraction Using Analytical Methods***

The FET channel can be modulated by a distributed RC network when  $V_{DS}=0$  [73]. According to the theory described in [73], the impedance parameters  $Z_{ij}$  of the two-port network that stands for the intrinsic channel – where the input port is located at the gate-source nodes and the output port at the drain-source nodes –, can be given by [62]:

$$Z_{11in} = \frac{R_c}{3} + \frac{R_{dy}}{1 + j\omega C_y} \approx \frac{R_c}{3} + R_{dy} = \frac{R_c}{3} + \frac{nkT}{qI_g} \quad (2.1)$$

$$Z_{12in} = Z_{21in} = \frac{R_c}{2} \quad (2.2)$$

$$Z_{22in} = R_c \quad (2.3)$$

where  $R_c$  is the channel resistor,  $n$  the ideality factor,  $k$  the Boltzmann constant,  $T$  the temperature,  $q$  the electron charge and  $I_g$  the dc gate current.

As the device is a small die, the influence of the  $C_{pg}$  and  $C_{pd}$  parasitic capacitances is negligible (otherwise it is necessary to extract the  $C_{pg}$  and  $C_{pd}$  first) and so, the Z-parameters of the extrinsic FET can be written as [62]:

$$Z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nkT}{qI_g} + j\omega(L_s + L_g) \quad (2.4)$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{2} + j\omega L_s \quad (2.5)$$

$$Z_{22} = R_s + R_d + R_c + j\omega(L_s + L_d) \quad (2.6)$$

After the Z-parameters resistive part extraction (from measurements) for the bias points where  $V_{DS}$  is equal to zero and for all  $V_{GS}$  values in which the gate current can be measured, a curve fitting to the  $Re(Z_{11})$  vs  $1/I_g$  can be applied to obtain the  $R_s+R_g+R_c/3$  value, eliminating the equivalent impedance of the gate-channel Schottky junction,  $nkT/qI_g$ . As it is shown in Fig. 2.2, the curve fitting results in  $R_s+R_g+R_c/3=1.47\Omega$ .

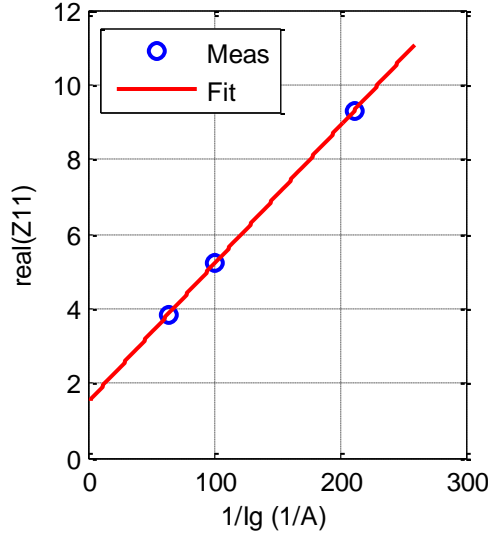


Fig. 2.2 – Curve-fitting of the real part of  $Z_{11}$  versus the inverse of the gate current.

From averaging  $Re(Z_{21})$  and  $Re(Z_{22})$ , the  $R_s+R_d/2=0.36\Omega$  and  $R_s+R_d+R_c=2.05\Omega$  can be obtained, respectively.

At this point, there are three equations and four unknowns and so, to extract the  $R_s$ ,  $R_g$ ,  $R_d$  and  $R_c$  another equation is necessary. Fukui proposed a method to obtain the required equation [74].

In order to apply the Fukui method a lot of measurements in the triode zone are necessary to represent the  $Re(Z_{22})$  vs  $X(V_{GS})$ , in which  $X(V_{GS})$  is the function that models the intrinsic channel resistor ( $R_c$ ):

$$X(V_{GS}) = \left( 1 - \sqrt{\frac{V_{GS} - V_{bi}}{V_{po}}} \right)^{-1} \quad (2.7)$$

Since this method was developed for MESFET devices, it cannot be guaranteed that the channel resistance of HEMT devices follows (2.7), and so the  $V_{bi}$  and  $V_{po}$  values are not well defined. To circumvent this problem, the best values that make the  $Re(Z_{22})$  linearly dependent with the  $X(V_{GS})$  function were chosen, as is shown in Fig. 2.3. With this method, all resistors  $R_g=1.13\Omega$ ,  $R_d=1.58\Omega$  and  $R_s=0.25\Omega$  can be estimated.

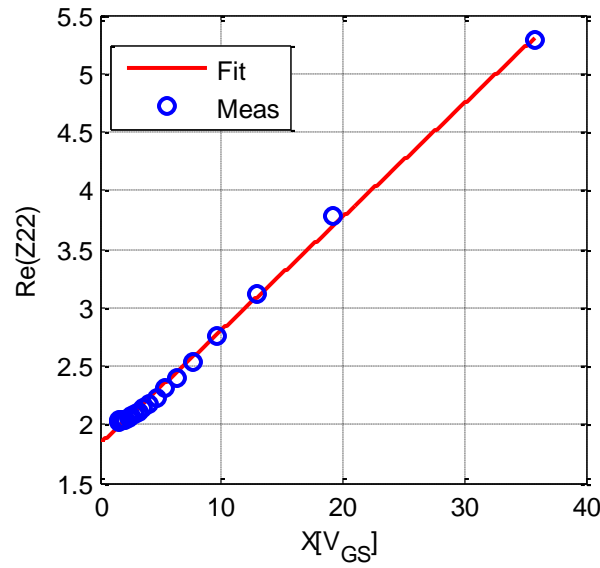


Fig. 2.3 – Real part of  $Z_{22}$  in triode zone to extract  $R_c$  and ( $R_d$  and  $R_s$ ).

It should be noted that for Si LDMOS devices the above methods cannot be directly applied since the gate of these devices is DC isolated. However, other analytical methods have been applied successfully to Si LDMOS devices [65],[66].

In order to extract the extrinsic inductors,  $L_g$ ,  $L_d$  and  $L_s$ , a curve-fitting was applied to the Z-parameters imaginary part measured in “forward bias” regime ( $V_{DS}=0$  and  $V_{GS} \gg V_T$ ) giving more weight to high frequencies where the inductors have more impact.

The obtained all extrinsic components’ values are presented in Table 2.1.

Table 2.1 – Extracted extrinsic components using the analytical method.

$R_g$	$R_d$	$R_s$	$L_g$	$L_d$	$L_s$
1.13 $\Omega$	1.58 $\Omega$	0.25 $\Omega$	54.73pH	164.04pH	7.06pH

As it was already mentioned, the obtained extrinsic values with this analytical method are only useful to obtain a good first estimation to use in the optimization process. In order to check if this first estimation of the extrinsic values is good, in Fig. 2.4 it is possible to observe the S-parameters after de-embedding the extracted extrinsic components. The obtained values for the resistors seem to be higher than their correct values since they lead to intrinsic (after de-embedding)  $S_{11}$  and  $S_{22}$  that fall out of the Smith chart (estimated  $|S_{ii}| > 1$ ).

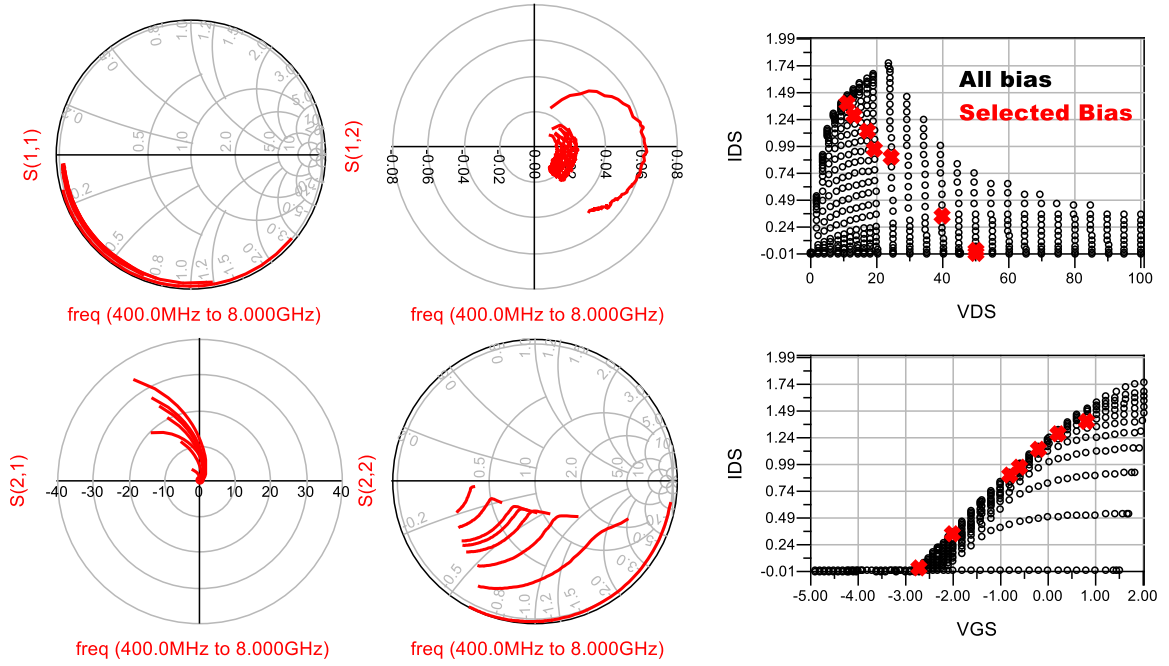


Fig. 2.4 – Estimated intrinsic S-parameters after de-embedding the extracted extrinsic components obtained using the analytical method.

In addition, since the FET channel for  $V_{DS} = 0$  and  $V_{GS} \ll V_T$  can be modelled by the equivalent circuit presented in Fig. 2.5 [75], for high frequencies the channel capacitances are short-circuited and so, the values of  $R_s + R_g$  and  $R_d + R_s$  can be estimated directly from the real part of  $Z_{11}$  and  $Z_{22}$ , as shown in Fig. 2.6, and use these values to check how far the extracted values stand from the correct ones. It should be noted that this method is very sensitive to the measurement quality, as any wrong calibration can easily corrupt the parasitic resistors' extraction.

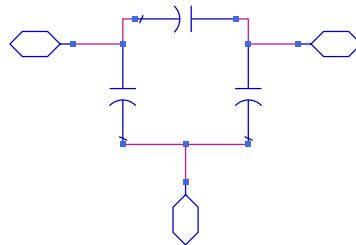


Fig. 2.5 – FET channel equivalent circuit for  $V_{DS} = 0$  and  $V_{GS} \ll V_T$ .

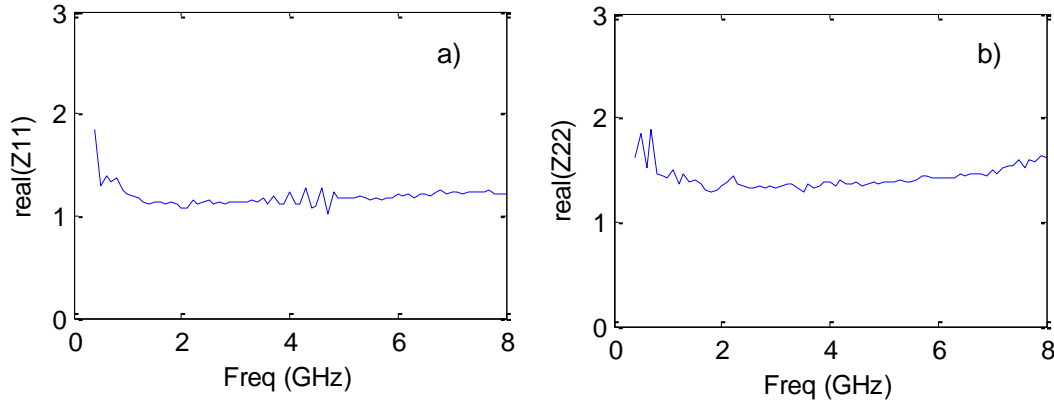


Fig. 2.6 – Real part of a)  $Z_{11}$  and b)  $Z_{22}$ .

The extracted values of  $R_s+R_g$  and  $R_d+R_s$  are equal to  $1.16\Omega$  and  $1.39\Omega$ , respectively. These results are different from the ones previously extracted. These discrepancies lead us to consider that the intrinsic channel resistance,  $R_c$ , is, indeed, modelled with a different  $X(V_{GS})$  function than the one proposed by Fukui. Therefore, the extracted extrinsic values are only used to get a first estimate (initial condition) for the extraction technique based on optimization, which it will be presented next.

### ***Extrinsic Element Extraction Using Optimization methods***

In theory, the optimization should be done for all bias points in order to constrain even more the curve fitting of S- and Y-parameters to the adopted model. However, this is extremely time-consuming and its practical usefulness is questionable. Therefore, it is necessary to choose few adequate bias points to perform a fast and correct optimization. In order to perform this optimization it is also necessary to select a model for the intrinsic FET that is suitable for all bias points considered in the optimization process.

It was found that only two bias points are enough to extract reasonable values for the extrinsic elements, as it will be shown later on. The selected bias points were both in “Cold FET” operation, i.e.  $V_{DS} = 0$ , with  $V_{GS} \ll V_T$  and another one with  $V_{GS} \gg V_T$ . With these bias points, the optimization is constrained to correctly fit the parallel and series elements at the same time, since the first one leads to a high impedance state of the intrinsic network, while the other leads to a low impedance state.

The adopted equivalent model was a  $\pi$ -network, that already includes the resistive part when the FET is biased in “Forward bias” condition [76], i.e.  $V_{GS} \gg V_T$ , as shown in Fig. 2.7, and it can be reduced for the capacitive  $\pi$ -network model already presented for  $V_{GS} \ll V_T$  in Fig. 2.5.

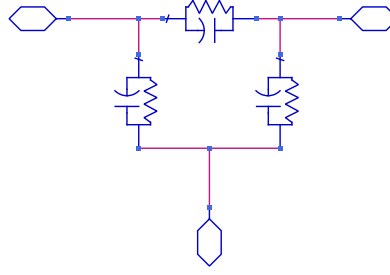


Fig. 2.7 – FET channel equivalent circuit for  $V_{DS} = 0$  and  $V_{GS} \gg V_T$ .

Different bias points result in different intrinsic values, whereas the extrinsic elements are the same. Therefore, the two schematics presented in Fig. 2.5 and Fig. 2.7 were optimized with the same extrinsic elements at the same time. In order to constrain even more the optimization and to get values with physical meaning for the extrinsic elements, the curve fitting should be done at the intrinsic and extrinsic reference planes. Fig. 2.8 shows the curve fitting results for the 3mm device die while Table 2.2 shows the correspondent extrinsic values.

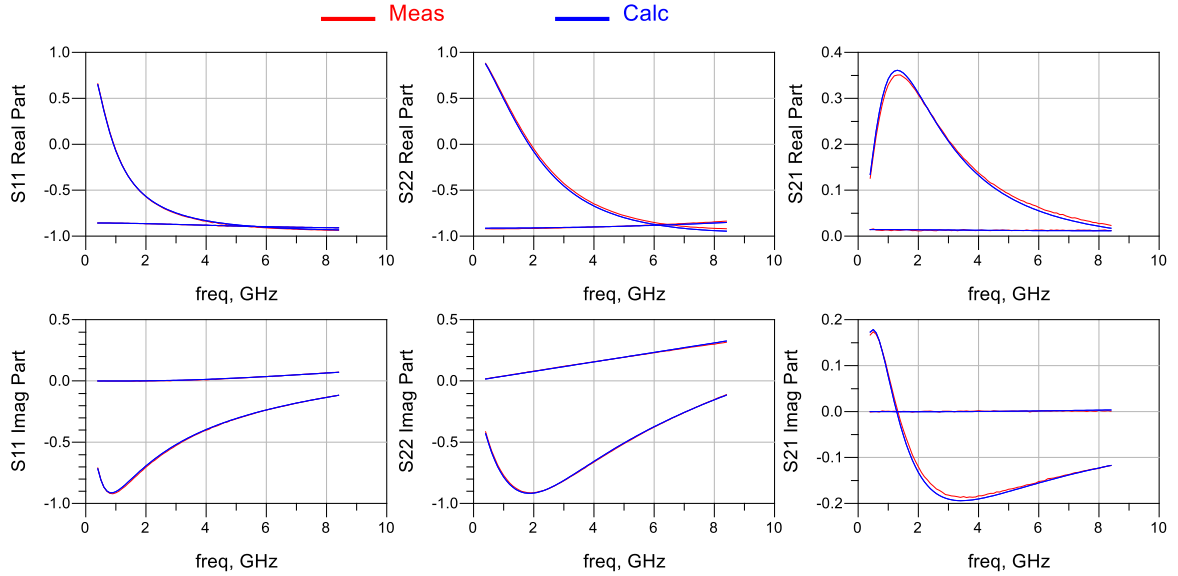


Fig. 2.8 – Curve-fitting to the S-parameters to extract all extrinsic components.

Table 2.2 – Extracted extrinsic components using optimization methods.

$R_g$	$R_d$	$R_s$	$L_g$	$L_d$	$L_s$	$C_{pg}$	$C_{pd}$
$1.29 \Omega$	$0.93 \Omega$	$0.09 \Omega$	$54.1 \text{pH}$	$167.3 \text{pH}$	$4.95 \text{pH}$	$26.6 \text{pF}$	$68.8 \text{pF}$

After the extrinsic elements extraction and de-embedding, the S-parameters of the assumed intrinsic model can be obtained for all bias points shown in Fig. 2.9. Now, both  $S_{11}$  and  $S_{22}$  are inside of Smith chart which is an indication that the extracted extrinsic values are correct (or, at least, physically consistent).

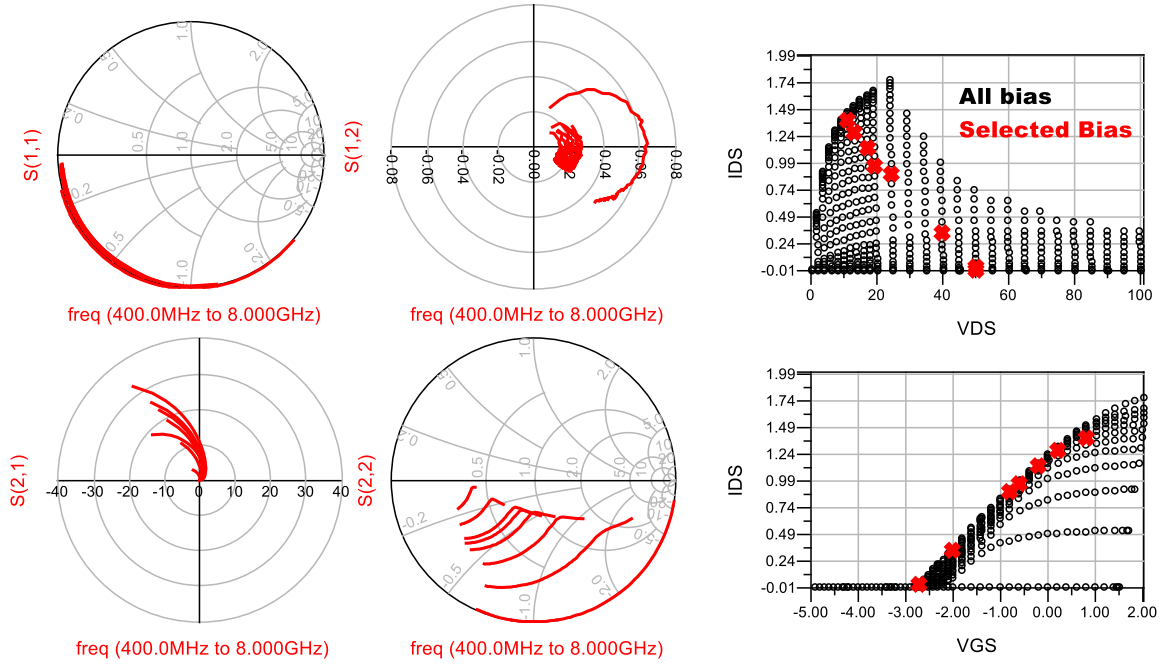


Fig. 2.9 – Estimated intrinsic S-parameters after de-embedding the extracted extrinsic components obtained via optimization.

In order to test the implemented optimization robustness, it was repeated the process with random initial conditions several times and, the obtained values were almost the same. The optimization using more bias points was also tried and the results were very similar. Therefore, it is not necessary to include more bias points, reducing this way the computational time required for the extraction.

#### B. EXTRACTION OF THE BIAS-DEPENDENT SMALL-SIGNAL INTRINSIC ELEMENTS

To extract the bias-dependent small-signal intrinsic elements it is necessary to choose a small-signal equivalent model for the intrinsic device. The adopted model has eight parameters:  $C_{gs}$ ,  $C_{gd}$ ,  $C_{ds}$ ,  $R_{gd}$ ,  $R_{gs}$ ,  $G_m$ ,  $G_{ds}$  and  $\tau$ , and it is presented in Fig. 2.10.

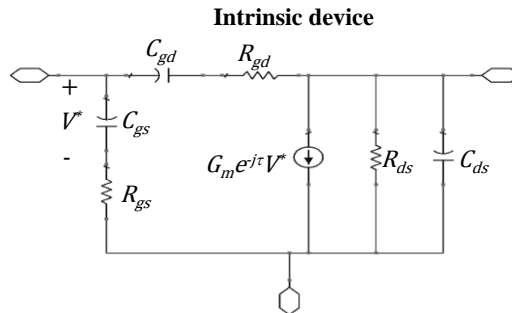


Fig. 2.10 – Adopted model for the small-signal intrinsic device.

With this simple model the intrinsic Y-parameters can be calculated:

$$Y_{intrinsic} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} Y_{gs} + Y_{gd} & -Y_{gd} \\ Y_m - Y_{gd} & Y_{ds} + Y_{gd} \end{bmatrix} \quad (2.8)$$

where  $Y_{gs}$ ,  $Y_{ds}$ ,  $Y_{gd}$  and  $Y_m$  are given by:

$$Y_{gs} = \frac{\omega^2 \tau_{gs} C_{gs}}{1 + \omega^2 \tau_{gs}^2} + j \frac{\omega C_{gs}}{1 + \omega^2 \tau_{gs}^2}, \quad \tau_{gs} = R_{gs} \cdot C_{gs} \quad (2.9)$$

$$Y_{gd} = \frac{\omega^2 \tau_{gd} C_{gd}}{1 + \omega^2 \tau_{gd}^2} + j \frac{\omega C_{gd}}{1 + \omega^2 \tau_{gd}^2}, \quad \tau_{gd} = R_{gd} \cdot C_{gd} \quad (2.10)$$

$$Y_{ds} = g_{ds} + j\omega C_{ds} \quad (2.11)$$

$$Y_m = g_m e^{j\omega\tau} \left\{ \frac{1 - j\omega\tau_{gs}}{1 + \omega^2 \tau_{gs}^2} \right\} \quad (2.12)$$

The next step is to calculate the measured  $Y_{gs}$ ,  $Y_{ds}$ ,  $Y_{gd}$  and  $Y_m$  using the measured Y-parameters, (2.13), (2.14), (2.15) and (2.16), respectively. With the admittances of each branch, all parameter values can be analytically extracted for all bias points.

$$Y_{gd} = -y_{12} \quad (2.13)$$

$$Y_{gs} = y_{11} + y_{12} \quad (2.14)$$

$$Y_{ds} = y_{22} + y_{12} \quad (2.15)$$

$$Y_m = y_{21} - y_{12} \quad (2.16)$$

The  $C_{gd}$  and  $R_{gd}$  values can be extracted using a Matlab nonlinear curve fitting tool to fit the real and imaginary part of  $Y_{gd}$  at the same time. The same procedure can be applied to  $Y_{gs}$  to extract the  $C_{gs}$  and  $R_{gs}$ . To extract the  $C_{ds}$  and  $g_{ds}$  a linear curve-fitting can be applied to the real and imaginary parts, respectively. The  $g_m$  and  $\tau$  can be obtained by averaging the results provided by (2.17) and (2.18), respectively. Fig. 2.11 shows the obtained curve fitting results for some bias points.

$$g_m \leftrightarrow \left| \frac{Y_m \cdot Y_{gs}^*}{\text{Im}(Y_{gs})} \right| \quad (2.17)$$

$$\omega\tau \leftrightarrow -\frac{\pi}{2} + \angle Y_m - \angle Y_{gs} \quad (2.18)$$

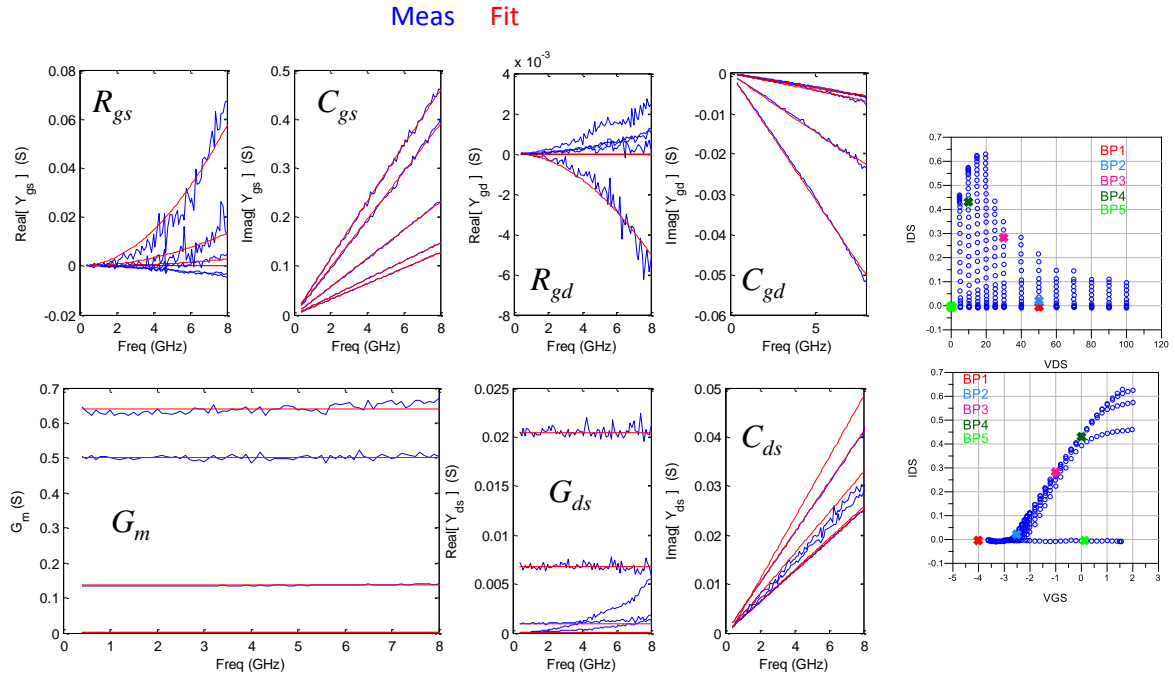


Fig. 2.11 – Obtained Y-parameters curve fitting results for some bias points.

The obtained profiles of the  $C_{gs}$ ,  $C_{gd}$ ,  $C_{ds}$ ,  $g_m$  and  $g_{ds}$  are shown in Fig. 2.12. These intrinsic elements values variation with  $V_{DS}$  and  $V_{GS}$  is in agreement with the known physical behaviour of GaN-HEMT devices, which provides a high confidence on the obtained values, and so, on the extraction procedure.

In order to compare the S-parameters of the extracted model with the measurements, a bias-dependent small-signal intrinsic equivalent circuit model was implemented in ADS with Look-Up-Tables (LUTs). The obtained results can be shown in Fig. 2.13, where it is possible to see an excellent accuracy between the small-signal model and the measurements.

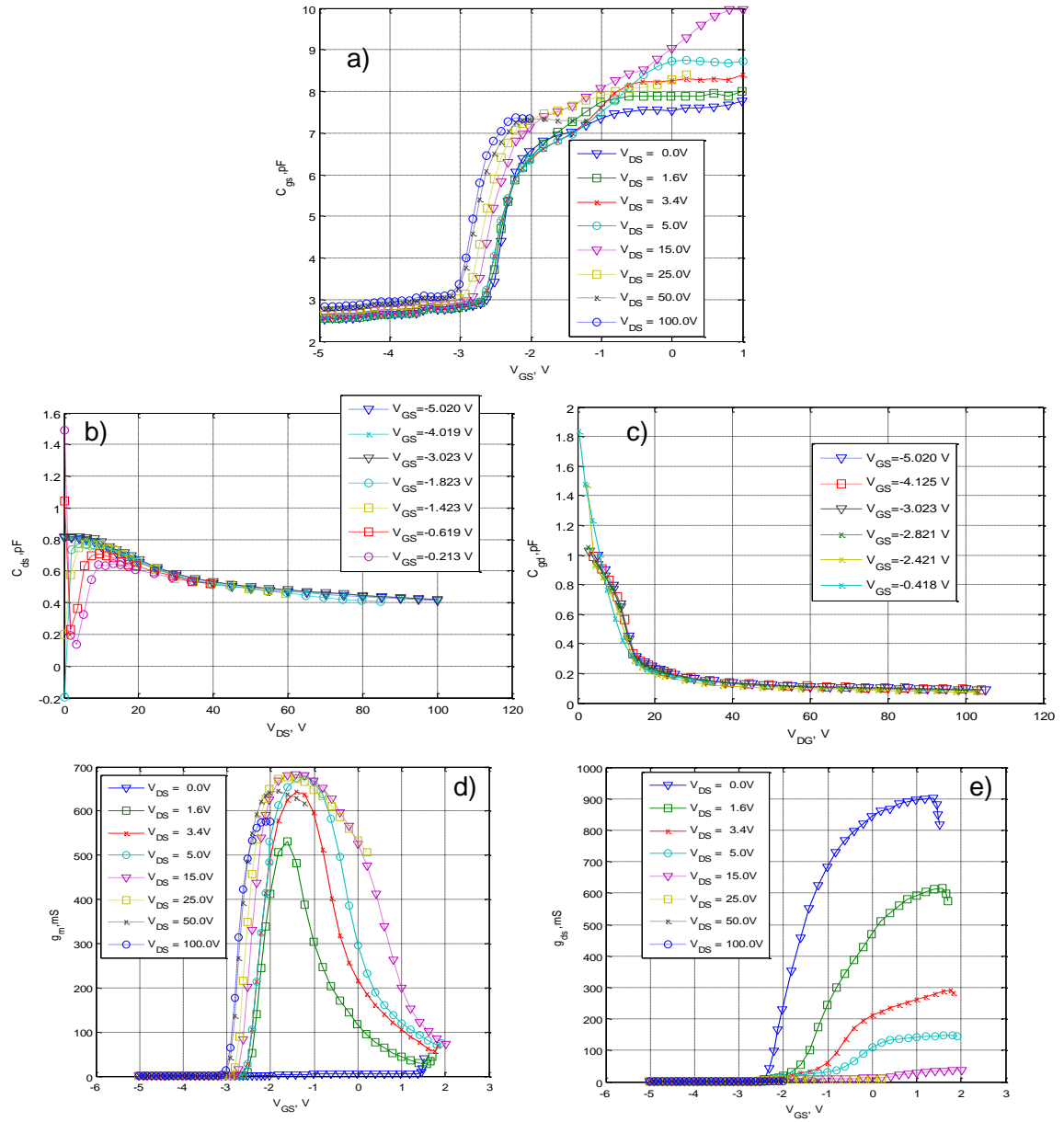


Fig. 2.12 – Extracted a)  $C_{gs}$ ; b)  $C_{ds}$ ; c)  $C_{gd}$ ; d)  $G_m$  e)  $G_{ds}$  profiles.

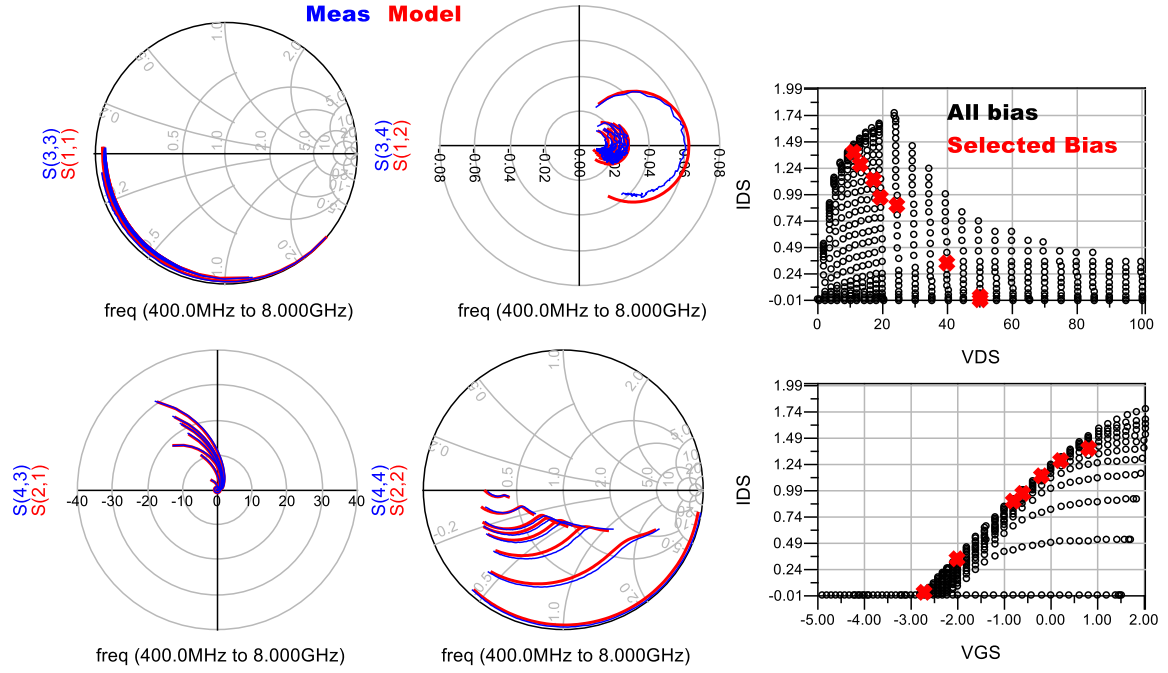


Fig. 2.13 – Comparison between the S-parameters obtained from measurements with the ones obtained from simulations of the small-signal bias dependent model.

### C. LARGE-SIGNAL FORMULATION AND IMPLEMENTATION

The most important task for obtaining a nonlinear model of the device is to choose a suitable large-signal formulation that is capable to predict the measurements, otherwise a good fit between the measurements and the model will never be obtained. This being the case, first it is necessary to look to the extracted bias-dependent small-signal intrinsic elements' variation with  $V_{DS}$  and  $V_{GS}$  and then choose an appropriated large-signal formulation to fit the extracted profiles.

Regarding the drain-to-source current,  $i_{DS}(v_{GS}, v_{DS})$ , the adopted model was the Fager-Pedro model firstly developed for LDMOS [33] devices which was then extended to GaN HEMTs devices [34]:

$$V_T(v_{GS}, v_{DS}) = V_{T0} + \gamma \tanh(\alpha_T \cdot v_{DS}) \quad (2.19)$$

$$V_{GS1}(v_{GS}, v_{DS}) = v_{GS} - V_T(v_{GS}, v_{DS}) \quad (2.20)$$

$$V_{GS2}(v_{GS}, v_{DS}) = v_{GS1} - \frac{1}{2} \left( v_{GS1} + \sqrt{(v_{GS1} - VK)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2} \right) \quad (2.21)$$

$$V_{GS3}(v_{GS}, v_{DS}) = VST \cdot \ln(1 + e^{v_{GS2}/VST}) \quad (2.22)$$

$$I_{DS}(v_{GS}, v_{DS}) = \beta \frac{V_{GS3}^2}{1 + \frac{V_{GS3}}{V_L}} \cdot (1 + \lambda V_{DS}) \cdot \tanh\left(\frac{\alpha V_{DS}}{V_{GS3}^{psat}}\right) \quad (2.23)$$

It should be noted that the adopted model has a slight modification from the one presented in [34], namely the threshold voltage variation with  $V_{DS}$  as expressed (2.19), to obtain better curve fitting results.

In order to obtain better predictions of the nonlinearity and the efficiency, the optimization should be conducted to fit the extracted bias-dependent  $G_m$  and  $G_{ds}$  with the respective derivatives of (2.23) with respect to  $v_{GS}$  and  $v_{DS}$ . Fig. 2.14 and Fig. 2.15 show the achieved fit of the large-signal model with the measurements and, the correspondent parameters of the  $i_{DS}(v_{GS}, v_{DS})$  model are shown in Table 2.3.

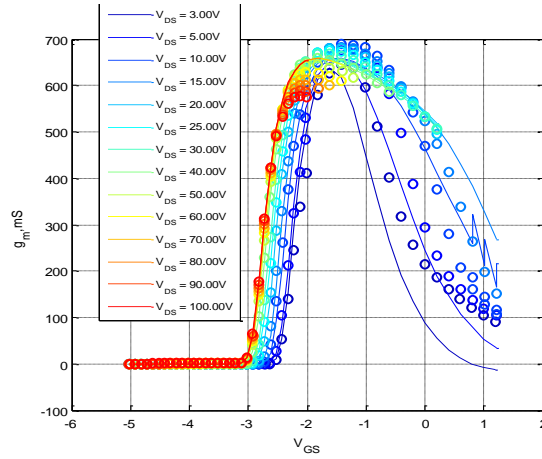


Fig. 2.14 – Achieved fit of the large-signal model with the measured  $G_m$ .

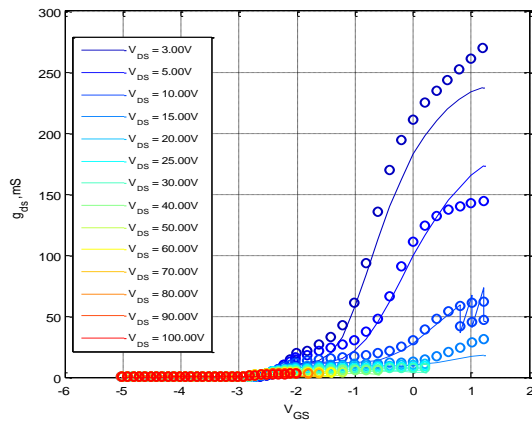


Fig. 2.15 – Achieved fit of the large-signal model with the measured  $G_{ds}$ .

Table 2.3 – Parameters of the  $i_{DS}(V_{GS}, V_{DS})$  large-signal model

$V_{T0}$	$VK$	$\Delta$	$VST$	$plin$	$VL$	$\alpha$	$psat$	$\lambda$	$\beta$	$\gamma$	$\alpha_T$
-2.36	3.95	0.96	0.095	1.219	0.786	0.4	1.228	0	1.165	0.842	0.00948

It was found that due to long-term memory effects the  $G_m$  and  $G_{ds}$  are inconsistent [77], i.e. do not obey the equality (2.24). Therefore, if the  $G_m$  and  $G_{ds}$  were integrated, distinct  $i_{DS}(V_{GS}, V_{DS})$  are obtained and so, it is impossible to obtain a perfect fit at the same time to the  $G_m$  and  $G_{ds}$ . Thus, the extracted  $i_{DS}(V_{GS}, V_{DS})$  function corresponded to a compromise between them. This issue will be focused on the second part of this Chapter, in which long-term memory effects, observed in GaN HEMTs were addressed, presenting a solution to circumvent the  $G_m$  and  $G_{ds}$  inconsistency.

$$\frac{\partial G_m(v_{GS}, v_{DS})}{\partial v_{DS}} = \frac{\partial G_{ds}(v_{GS}, v_{DS})}{\partial v_{GS}} \quad (2.24)$$

On what capacitances are concerned, practically the same formulation was adopted for all capacitances, as shown in (2.25), (2.26) and (2.27). Only the  $C_{gs}$  formulation has a second term in order to obtain a better fit for high  $V_{GS}$  voltages. Although the formulation is practically the same for all capacitances, the parameters of the equations are completely different (see Table 2.4), namely the  $KC_{gsx}$ ,  $KC_{gd0}$  and  $KC_{ds0}$  which determine the slope of the hyperbolic tangents.

$$C_{gs}(v_{gs}) = C_{gs0} + \frac{A_{gs0}}{2} [1 + \tanh(K_{gs0}[v_{gs} - VC_{gs0}])] + \frac{A_{gs1}}{2} [\tanh(1 + K_{gs1}[v_{gs} - VC_{gs1}])] \quad (2.25)$$

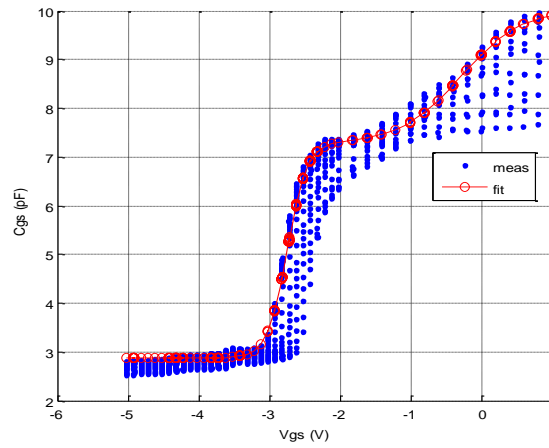
$$C_{ds}(v_{ds}) = C_{ds0} + \frac{A_{ds0}}{2} [1 + \tanh(K_{ds0}[v_{ds} - VC_{ds0}])] \quad (2.26)$$

$$C_{gd}(v_{dg}) = C_{gd0} + \frac{A_{gd0}}{2} [1 + \tanh(K_{gd0}[v_{dg} - VC_{gd0}])] \quad (2.27)$$

For the  $C_{gs}$ , by observation of the measured data (Fig. 2.16), it is possible to see that the  $C_{gs}$  starts with a constant low value, then increases until reaching a constant high value, and, finally, for high  $V_{GS}$  voltages, the  $C_{gs}$  rises again until it stabilizes in its highest value. Therefore, two hyperbolic tangent functions can fit this measured data with positive  $KC_{gs}$ . The consideration of  $C_{gs}$  variation with  $V_{DS}$  was not taken into account, since this model complexity increase does not correspond to a significant accuracy improvement.

Table 2.4 – Parameters for all large-signal models of the capacitances.

$C_{gs0}$	2.878	$C_{ds0}$	0.398
$A_{gs0}$	4.395	$A_{ds0}$	1.123
$K_{gs0}$	3.625	$K_{ds0}$	-0.0156
$VC_{gs0}$	-2.748	$VC_{ds0}$	-24.975
$A_{gs1}$	2.768	$C_{gd0}$	0.1
$K_{gs1}$	1.159	$A_{gd0}$	1.162
$VC_{gs1}$	-0.285	$K_{gd0}$	-0.0756
		$VC_{gd0}$	5.738


Fig. 2.16 – Achieved fit of the large-signal model with the measured  $C_{gs}$ .

Regarding the  $C_{ds}$  and  $C_{gd}$ , it is possible to observe in the measured data (Fig. 2.17 and Fig. 2.18, respectively) that both  $C_{ds}$  and  $C_{gd}$  start with a high value to then slowly decrease to a small value. If a negative  $KC_{ds}$  and an appropriate breakpoint,  $VC_{ds}$ , are used, a hyperbolic tangent function can be also used to fit the measured data. It should be noted that it was assumed that the transistor will not operate with a negative  $V_{DS}$  voltage.

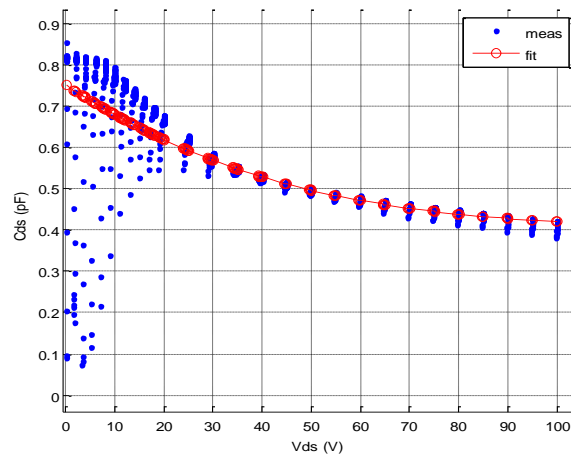


Fig. 2.17 – Achieved fit of the large-signal model with the measured  $C_{ds}$ .

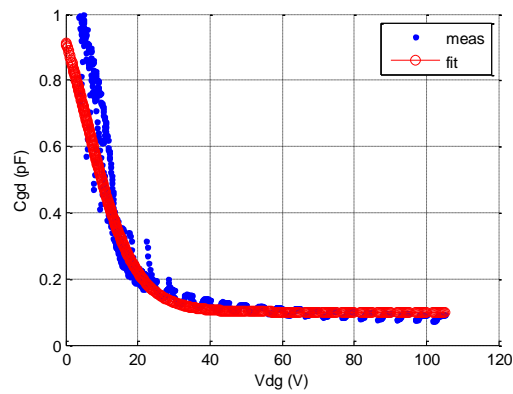


Fig. 2.18 – Achieved fit of the large-signal model with the measured  $C_{gd}$ .

The S-parameters of the large-signal model in comparison with the measured ones indicate that there is a good agreement between them, as shown in Fig. 2.19.

Large-Signal model    Measurements    Small-Signal LUT model

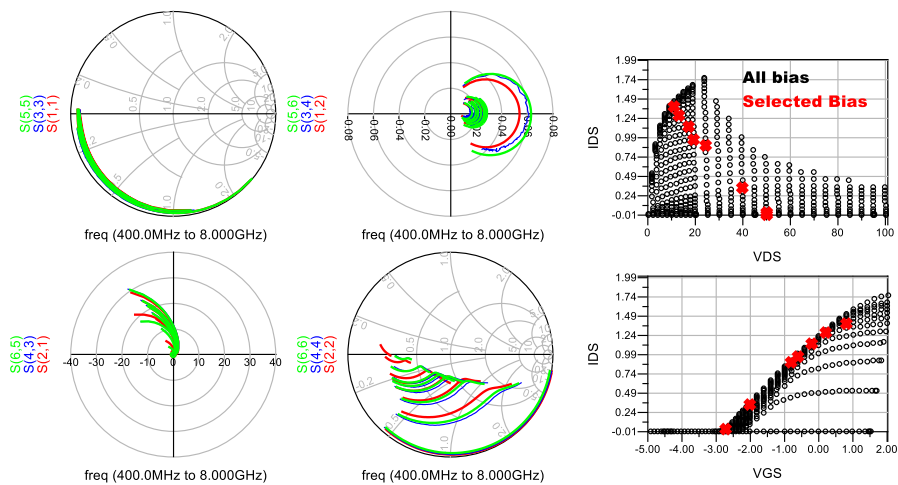


Fig. 2.19 – S-parameters of the large-signal model in comparison with the measured ones and with the ones obtained with small-signal bias dependent model.

#### D. LARGE-SIGNAL MODEL VALIDATION ON A 3MM GAN HEMT DEVICE

The last step to conclude the 3mm GaN HEMT device modelling task was the validation of the implemented large-signal model. The first test performed was the comparison between the model predictions and the measured output power and efficiency load-pull contours. Fig. 2.20 shows the obtained results where it is possible to see the remarkable good agreement between the model predictions and the corresponding measurements. Only slight errors are visible for loads that are far from the optimum output and efficiency loads.

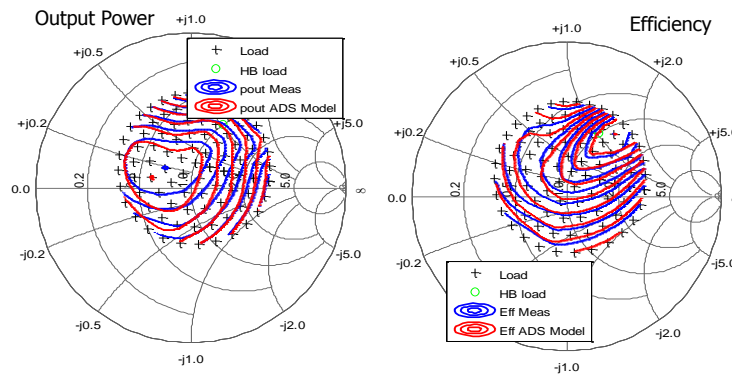


Fig. 2.20 – Simulated efficiency and output power load-pull contours in comparison with measurements for the 3mm device.

The previous experimental test only validates the efficiency and output power load-pull contours. However, it is also necessary to check their absolute values. Otherwise, despite the possible good prediction of the contours' shape, the absolute value predictions can be wrong. This being the case, the absolute values of the efficiency, output power and dc current are presented in the following figures, where it is also possible to see the reasonably good accuracy of the model:

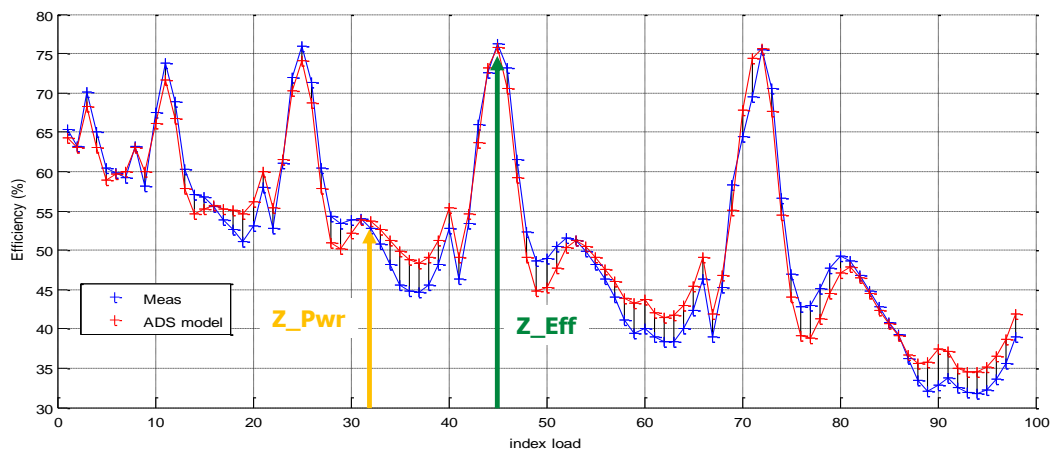


Fig. 2.21 – Simulated efficiency in comparison with the measurements for different load impedances.

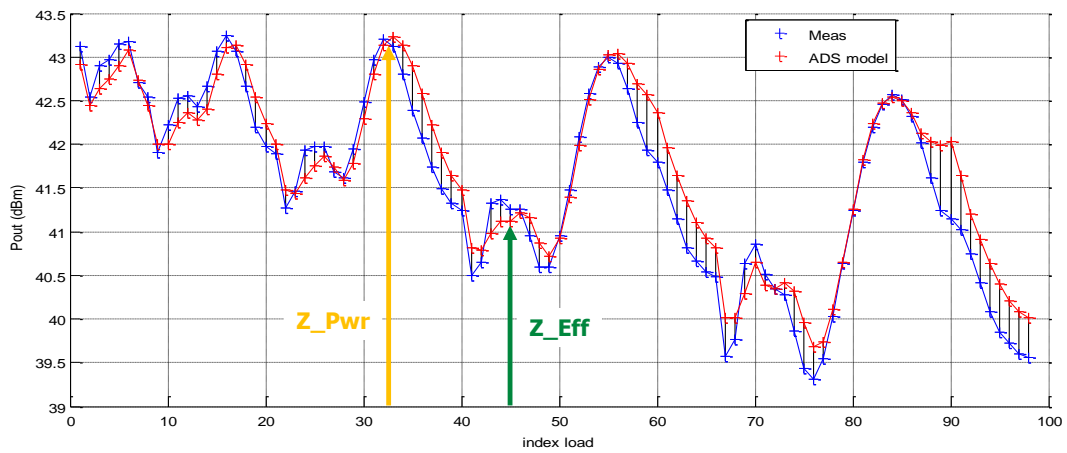


Fig. 2.22 – Simulated output power in comparison with the measurements for different load impedances.

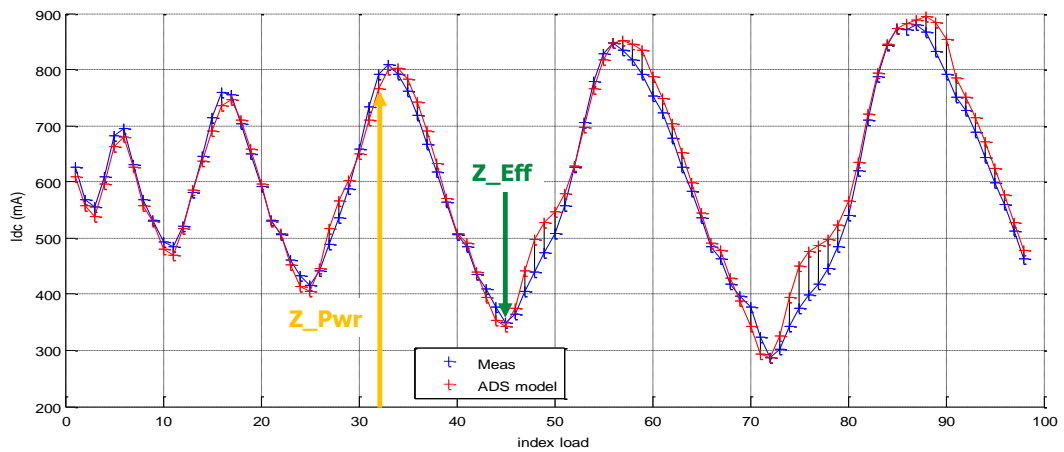


Fig. 2.23 – Simulated dc drain current in comparison with the measurements for different load impedances.

Then it was performed a comparison between the model predictions and the measured gain and efficiency versus output power for a particular load impedance between the optimum efficiency and output power load impedance. As it is possible to see in Fig. 2.24, the gain and output power predictions by the model are very accurate, only the predicted efficiency is 3% lower than the measured one in full power regime.

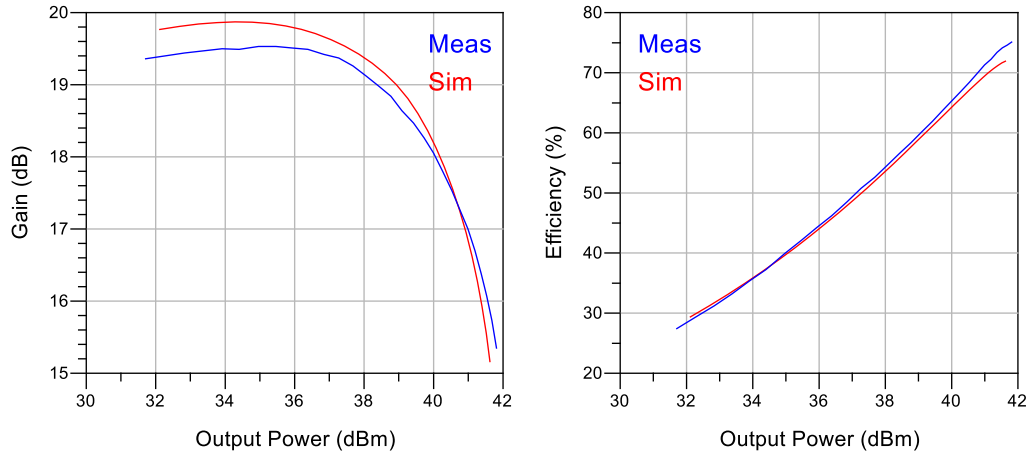


Fig. 2.24 – Simulated Gain and efficiency versus output power in comparison with the measurements.

### 2.1.2 Practical Example of High Power Device Modelling

#### A. SCALING RULES AND PACKAGE EXTRACTION

Most of the times the extraction capability is limited to small devices. Therefore, to extract models for high power devices, some scaling rules are needed to obtain the desired model for large devices from the small ones.

High power devices have a higher gate periphery due to an increase of the number of gate fingers and/or to an increase of the gate width. As shown in the illustration of the FET device depicted in Fig. 2.25, the parameter values should change in a different way from a small to a large transistor, depending on whether the device has higher gate width or several FET's in parallel. Consequently, there are two different scaling factors:

- 1) related to the gate width:

$$sf_{Wg} = \frac{Wg^{new}}{Wg} \quad (2.28)$$

- 2) related to the number of gate fingers:

$$sf_{Ng} = \frac{Ng^{new}}{Ng} \quad (2.29)$$

where  $Wg_{new}$  and  $Ng_{new}$  denote the new gate width and the new number of gate fingers, respectively. As an example, to scale the 3mm single die to a 6-Cell 2.7mm device the scaling factor  $sf_{Wg}$  should be equal to  $2.7/3=0.9$  and the  $sf_{Ng}$  scaling factor equal to 6.

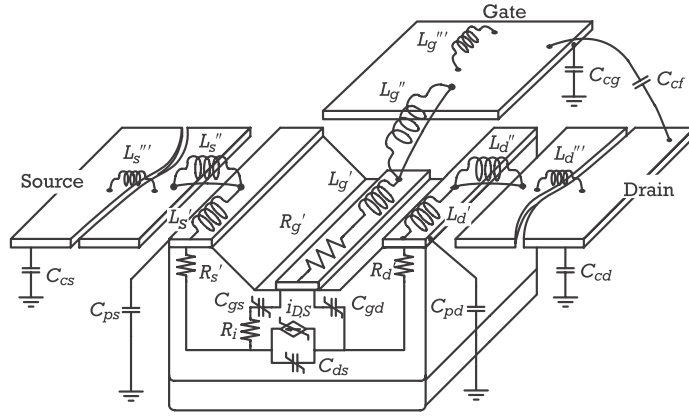


Fig. 2.25 – Illustration of a FET device, from [3].

Since it was not measured any more S-parameter from other devices with different gate peripheries, commonly scaling rules [78], [79] were applied:

For capacitors and  $I_{DS}$ :

$$P^{new} = P_0 \cdot sf_{Wg} \cdot sf_{Ng} \quad (2.30)$$

For inductors and  $R_g$ :

$$P^{new} = P_0 \cdot \frac{sf_{Wg}}{sf_{Ng}} \quad (2.31)$$

For the other resistors:

$$P^{new} = \frac{P_0}{sf_{Wg} sf_{Ng}} \quad (2.32)$$

where  $P_{new}$  is the scaled version parameter of the new device.

## B. HIGH POWER GAN HEMT DEVICE MODELING

This sub-section concludes the modelling procedure for high power GaN-HEMT devices without considering the long-term memory effects. A packaged 6-Cellx2.7mm was used for the experimental validation of the extraction procedure in a high power device.

### Package Extraction

Since this is a packaged device with a large gate-periphery and with pre-matching circuits (at least at the input), it is expected that the extrinsic equivalent circuit elements now play a determinant role on the overall device behaviour. Therefore, it is necessary to know the package structure in order to translate it into a suitable equivalent circuit obtaining a good S-parameters curve-fit.

Fig. 2.26 illustrates the package structure of the 6-Cell 2.7mm device, which it is translated in the large-signal equivalent circuit model presented in Fig. 2.27.

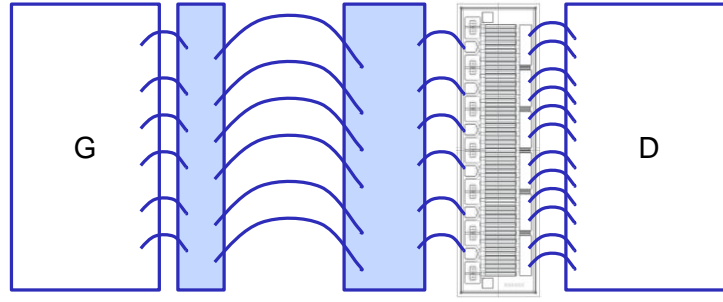


Fig. 2.26 – Illustrative high power device structure.

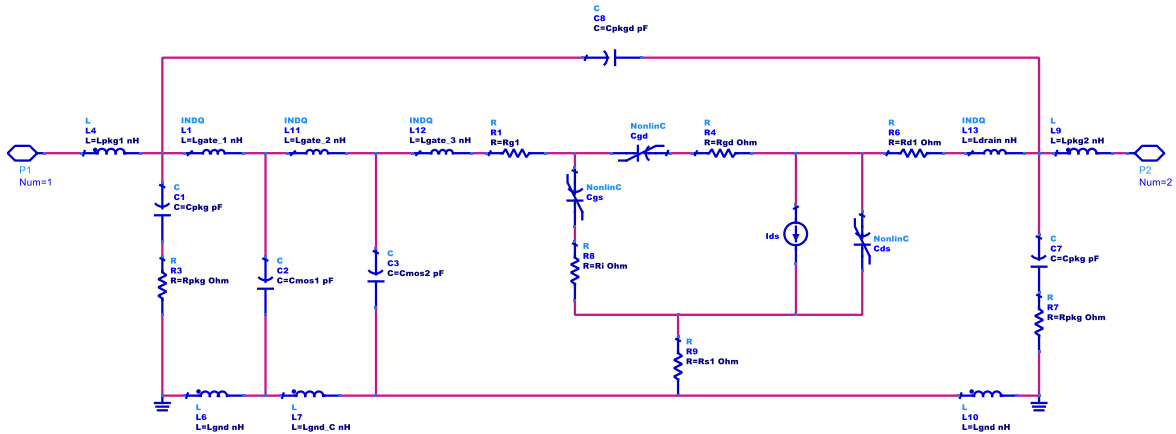


Fig. 2.27 – Package 6-Cell device equivalent circuit.

The extraction of the package element values can be done using two different ways:

- 1) made by measuring “dummy” devices where the die was replaced by a known MOSCAP keeping the bond wire connections as equal as possible to the ones used in the die connection and where the die was simply removed. These “dummy” devices allow the extraction of the package elements made separately from the intrinsic elements;
- 2) made by measuring the entire device (including the die) and perform the package optimization with the intrinsic elements.

The first extraction technique is the preferred one since the optimization is done separately from the intrinsic elements and so, there is no error propagation. However, most of the times it is impossible to obtain measurements of the “dummy” devices because it is necessary to ask the foundry to build this “dummy” device.

Consequently, the second approach was adopted, where the intrinsic elements were first scaled from the previously extracted 3mm device model to obtain the respective high power 6-Cellx2.7mm device. Then, it was performed an optimization of the package elements to fit the measured S-parameters of the entire device. In order to constrain even more this optimization process, at the same time, it was also performed an optimization of

the pulsed CW small-signal gain for several load impedances between the optimum efficiency and output power impedances. The obtained S-parameters and the CW small-signal gain are presented in Fig. 2.28 and Fig. 2.29, respectively.

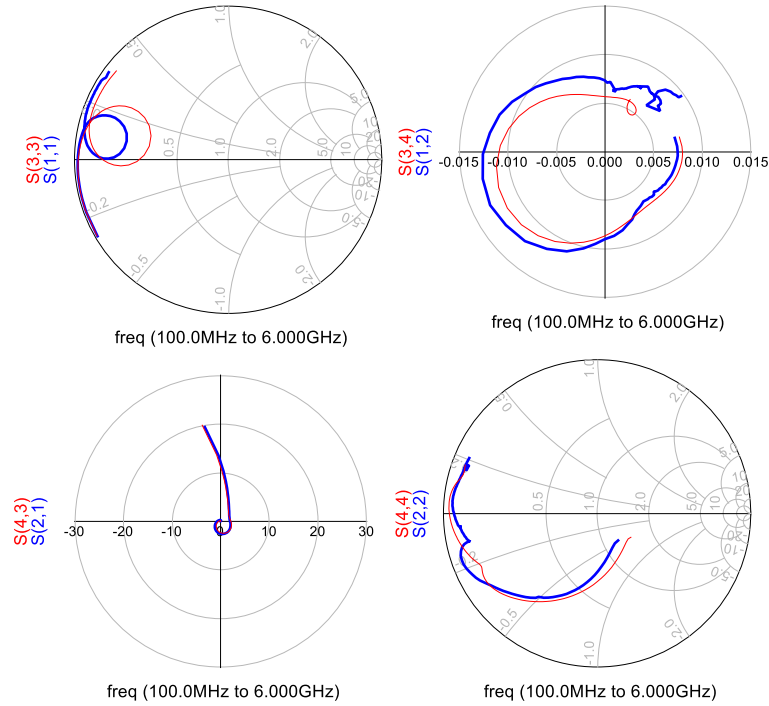


Fig. 2.28 – Simulated S-parameters (for  $V_{DS}=50$  V and  $I_{dq}=100$ mA) of the model – when the package was extracted with a compromise between the S-parameters of the entire device and the small-signal from the swept input power data – in comparison with the measurements.

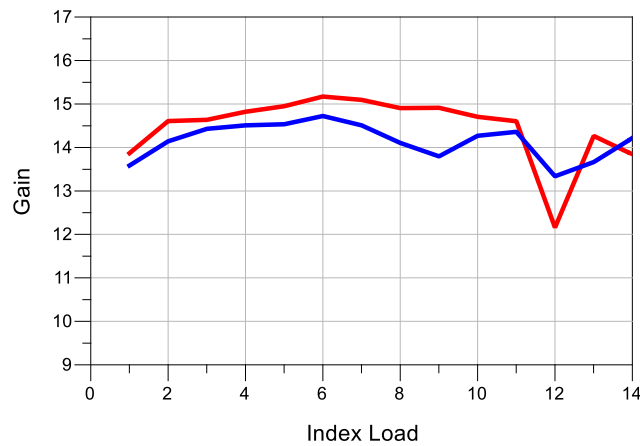


Fig. 2.29 – Small-Signal gain of the final model for different loads.

### Experimental Validation

The linear predictions of the model were already validated during the package extraction. Now, it is necessary to validate the nonlinear predictions, starting by the validation of the AM/AM, AM/PM and efficiency versus input power for different load impedances between the optimum efficiency and output power loads. Fig. 2.30 shows the good agreement between the predictions and measurements of these characteristics for the two optimum loads.

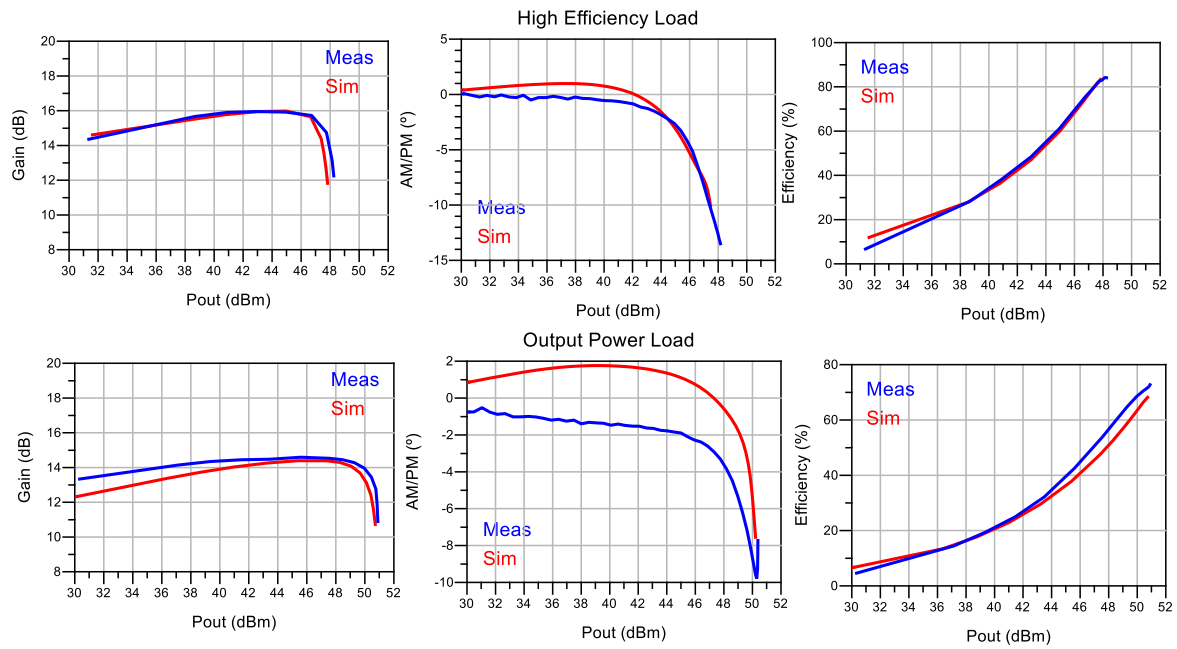


Fig. 2.30 – Simulated gain, phase shift and efficiency versus output power in comparison with the measurements of the 6-Cellx2.7mm GaN HEMT device.

The next validation step is the comparison between the model predictions and the measurements of the efficiency and output power load-pull contours, which are presented in Fig. 2.31. Although the fit between the predictions and the measurements of the load-pull contours with the load variation is not perfect, it is believed to be already sufficiently accurate to allow the use of this model in power amplifier designs, namely Doherty architectures.

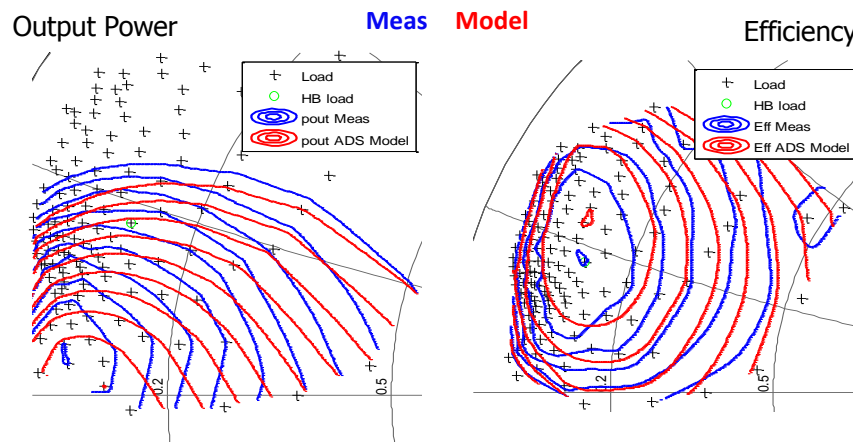


Fig. 2.31 – Efficiency and output power load-pull contours predictions in comparison with the measured ones of the 6-Cellx2.7mm GaN HEMT device.

Again, in the following figures, it is also tested the absolute values for each load impedance, showing also the reasonably good agreement between the predicted and measured values:

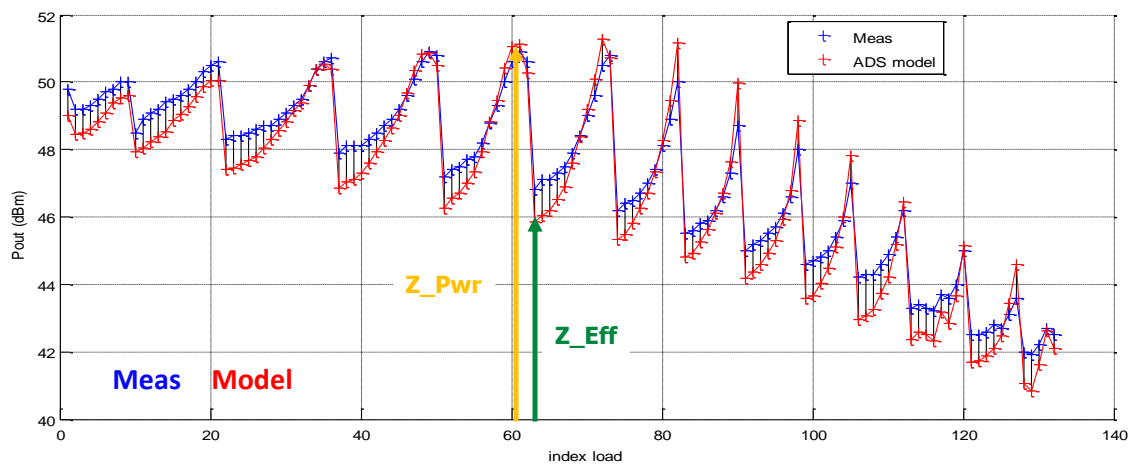


Fig. 2.32 – Simulated output power in comparison with the measurements for different load impedances for the 6-Cellx2.7mm GaN HEMT device.

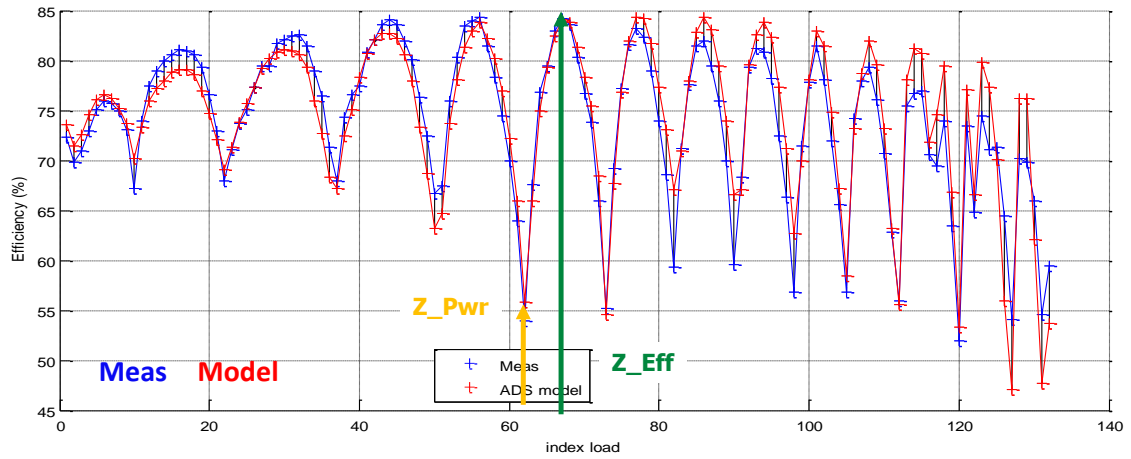


Fig. 2.33 – Simulated efficiency in comparison with the measurements for different load impedances for the 6-Cellx2.7mm GaN HEMT device.

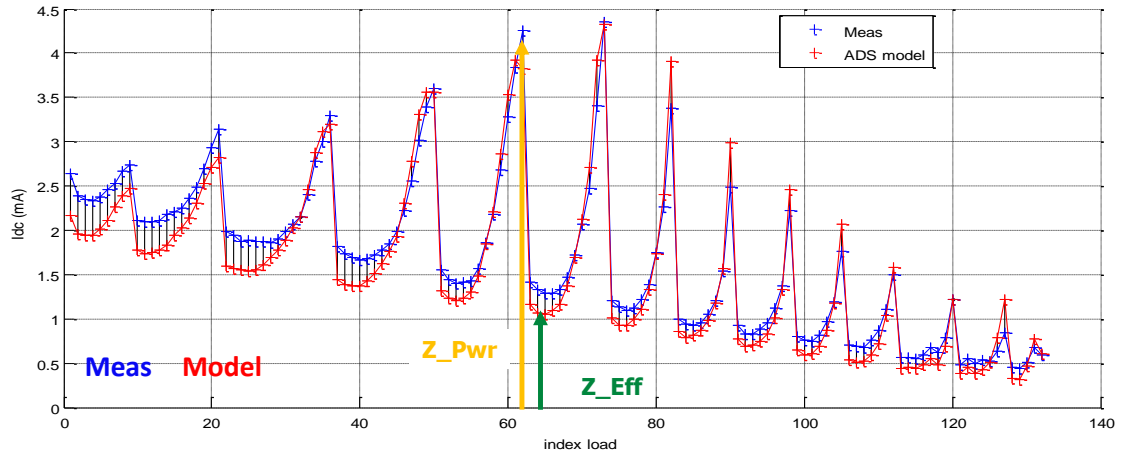


Fig. 2.34 – Simulated dc drain current in comparison with the measurements for different load impedances for the 6-Cellx2.7mm GaN HEMT device.

## 2.2. Nonlinear Model Extraction Methodology suitable for GaN HEMTs

In the previous sub-section, a model extraction methodology, without considering any trapping effects, was presented. However, since in GaN HEMT devices these effects are very noticeable, some approximations were needed to obtain a model capable of predicting the load-pull contours, namely the compromise between the  $G_m$  and  $G_{ds}$ .

Now, in this second part, this issue is addressed presenting an extraction methodology that can circumvent this problem using a double pulse technique to extract a GaN HEMT model with trapping effects. For this, it was first extracted a model for the 1mm device, and then the static and dynamic characteristics were validated using a 3mm device.

### 2.2.1 GaN HEMT Trapping Effects

The charge carrier trapping has been known since the GaAs devices. It is caused by the deep level states in the forbidden band, between the valence and conduction bands, and is due to layer mismatches, crystals imperfections or presence of impurities [80], [81]. As it is illustrated in Fig. 2.35, the surface traps are the cause of a virtual gate, which is responsible for the observed gate-lag phenomena, whereas the buffer and the substrate traps result in a so-called back-gating, which is responsible for the drain-lag phenomena [82]. Thus, according to the known physics understanding of these phenomena, all trapping effects contribute to modify the gate-channel transversal field via a “new gate” or a modified intrinsic threshold voltage. In fact, several equivalent circuit models have been proposed to model these trapping effects by changing the intrinsic threshold voltage,  $V_T$ , [83], [84].

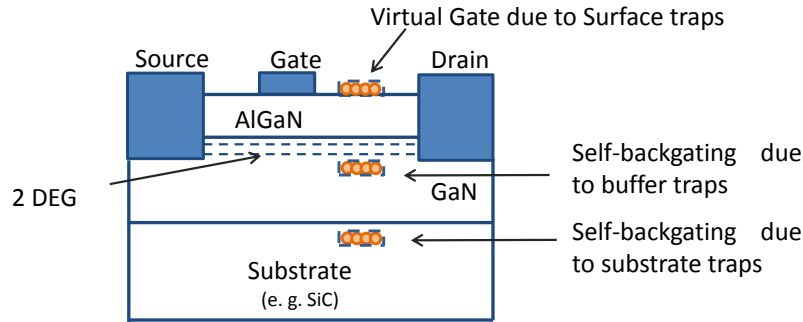


Fig. 2.35 – Illustration of the virtual gates in GaN HEMT devices due to the trapping effects.

On what gate-lag is concerned, its effect can be observed when the  $V_{GS}$  is changed (applying a  $V_{GS}$  step in the transistor) and measured the  $I_{DS}$  current response from different  $V_{GS}$  quiescent points,  $V_{GSQ}$ . As it is illustrated in Fig. 2.36, since the traps associated to the gate-lag are donor-like, when the  $V_{GS}$  is increased, it is observed a detrapping process that induces a positive charge in the virtual surface gate, leading to a slow increase of  $I_{DS}$  instead of an abrupt change. On the other hand, when the  $V_{GS}$  is decreased, the  $I_{DS}$  current decreases slowly for a lower level than the expected if the transistor would not suffer from trapping effects.

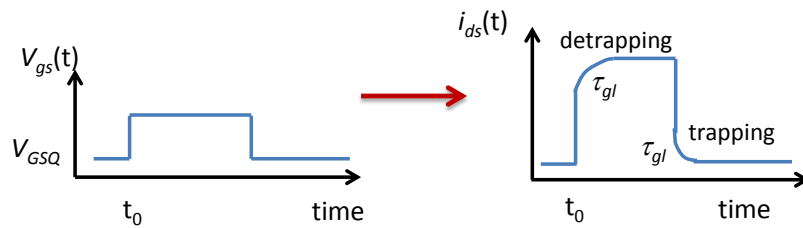


Fig. 2.36 – Illustration of the  $V_{GS}$  step up and step down and the respective  $I_{DS}$  response.

Regarding the drain-lag, its effects can be observed when the  $V_{DS}$  changes abruptly and the measured  $I_{DS}$  current is not consistent with the  $V_{DS}$  variation. Moreover, the observed inconsistency in the  $I_{DS}$  response varies with the quiescent bias point,  $V_{DSQ}$ . As it is illustrated in Fig. 2.37, contrary to the gate-lag, when the  $V_{DS}$  steps up the instantaneous  $I_{DS}$  current is higher than in the steady-state. This is due to the fact that the traps associated to the drain-lag are acceptor-like, and so, the charge carriers are gradually captured in the deep levels, the substrate or buffer layer traps (virtual gate) becomes negatively charged, leading to a channel current decrease. When the  $V_{DS}$  steps down, this virtual gate takes a long time to release its captured electrons, which is observable as a long recovery of the  $I_{DS}$  current [80] from a minimum just after the step down to its much higher steady-state value. The time associated to this  $I_{DS}$  recovery (detrapping process) is normally much higher than the time constant associated to the trapping process [85].

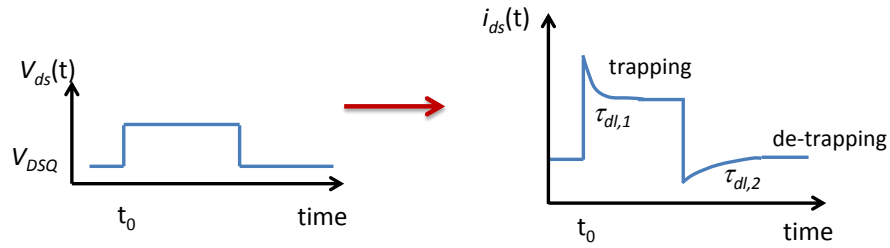


Fig. 2.37 – Illustration of the  $V_{DS}$  step up and step down and the respective  $I_{DS}$  response.

### 2.2.2 Drain-lag Phenomenon and its Effects on the $I/V$ curves

Nowadays, with the progress in the manufacturing process of the GaN HEMT devices, namely using passivation and/or surface treatment and gate field plating, the gate-lag effects can already be significantly reduced or even eliminated [86][87]. Fig. 2.38 presents a set of  $i_{DS}$  pulses collected when  $V_{GS}$  was pulsed for different values (from -5V to 0V) and  $V_{DS}$  was kept constant and equal to 25V. As it is possible to see, aside from a transient response due to the pulsing system, gate-lag effects are indeed not visible.

On the other hand, the drain-lag phenomenon remains, which introduces several problems on the power amplifier linearizability. As an example, in Fig. 2.39 are shown the  $i_{DS}$  pulses when the  $V_{GS}$  is kept constant and equal to -2.6V and the  $V_{DS}$  is pulsed to different values (from a  $V_{DSQ} = 20V$ ). The significant change of the quiescent current for different  $V_{DS}$  is definitely a manifestation of the drain-lag effects.

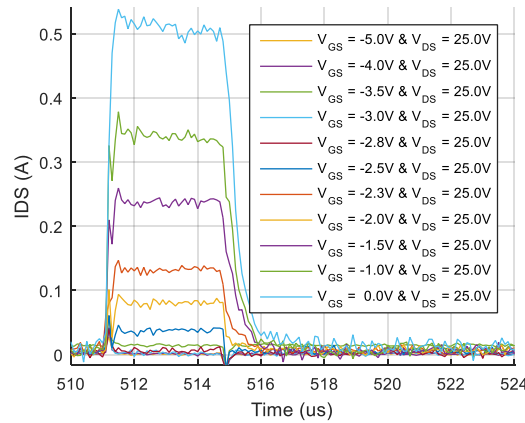


Fig. 2.38 – Zoom of the  $i_{DS}$  pulses when  $V_{GS}$  was pulsed for different values (from -5V to 0V with  $V_{GSQ}=-5V$ ) and  $V_{DS}$  was kept constant and equal to 25V.

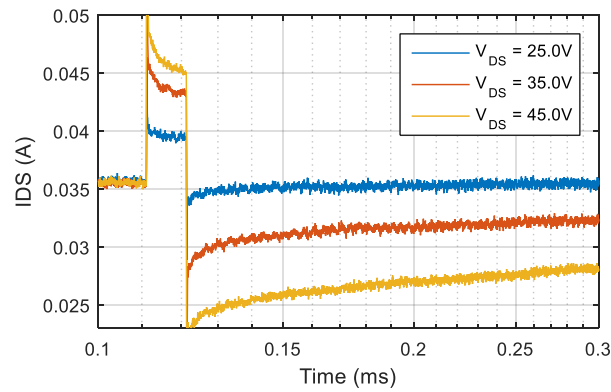


Fig. 2.39 – Zoom of the  $I_{DS}$  pulses when the  $V_{DS}$  is pulsed for different values (from a  $V_{DSQ}=20V$ ) and the  $V_{GS}$  is kept constant and equal to -2.6V.

In addition, it is observed that the pulsed  $I_{DS}$  waveform response when  $V_{DS}$  is pulsed always for the same value – for example 25V, as presented in Fig. 2.38 – does not change with different  $V_{GS}$  pulses. Therefore, from these observations, it is assumed that the drain-lag can be completely identified by the instantaneous  $v_{ds}$  and the quiescent  $V_{DSQ}$  values. This means that the trap charge state is neither dependent on  $v_{gs}$  or  $i_{ds}$ .

In Fig. 2.40 it is possible to see, in more detail, the measured  $i_{DS}$  transient responses to step up and step down  $v_{DS}$  stimuli (where first it was pulsed from  $V_{DSQ}=20V$  to a peak  $v_{DS}$  voltage pulse  $V_{dsP}=45V$  and then return to the  $V_{DSQ}=20V$ , whereas the  $V_{GS}$  was kept constant to  $V_{GS}=-2.6V$ ). There, it is clearly shown that the time constant associated to the  $i_{DS}$  recovery (electron release or detrapping process) is much higher than the one associated to the electron capture or trapping process.

Since the minimum pulse width of present high-power I/V pulser systems is higher than the time constants associated to the charge carrier trapping, it is the  $v_{DS}$  peak voltage that imposes the trapping state, whenever  $v_{DS}$  is pulsed from a lower value to a higher one

(step up) [88]. On the other hand, when the  $v_{DS}$  is pulsed from a higher value to a lower one (step down), the instantaneous  $i_{DS}$  value depends on the previous steady-state  $v_{DS}$  voltage due to the long-time constant associated to the detrapping process.

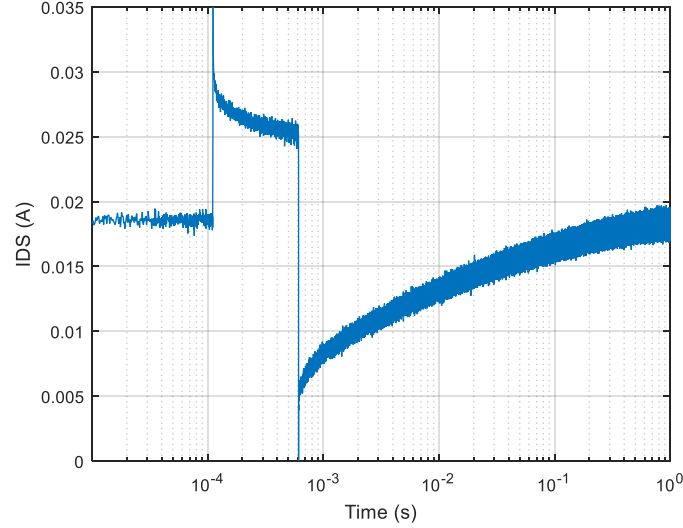


Fig. 2.40 – Measured  $i_{DS}$  responses for a)  $v_{DS}$  step up and b) step down stimuli.

Consequently, these mechanisms produce different pulsed I/V curves depending on whether  $v_{DS}$  voltage is pulsed from a lower value to a higher one or vice-versa. Fig. 2.41 illustrates this by presenting two sets of I/V curves obtained from the same transistor but one with  $V_{DSQ} = 0V$  and another with  $V_{DSQ} = 30V$ . In the first one, the trap state is always changing as it follows the  $v_{DS}$  pulse amplitude. In the second one, however, for  $v_{DS}$  pulses lower than the  $V_{DSQ}$ , the trap state is determined by  $V_{DSQ}$  obtaining a completely different I/V profile, while, for  $v_{DS}$  pulses higher than the  $V_{DSQ}$ , the FET is in the same condition as with  $V_{DSQ} = 0V$ , accompanying that I/V profile.

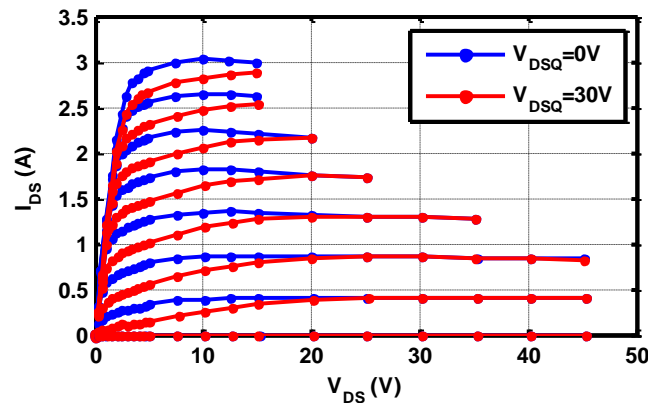


Fig. 2.41 – Comparison between two sets of measured pulsed I/V curves obtained with different quiescent  $v_{DS}$  voltages,  $V_{DSQ}=0V$  and  $V_{DSQ}=30V$ .

It should be noted that, for  $v_{DS}$  values lower than the  $v_{DSQ}$ , the obtained I/V curves can be considered iso-dynamic with respect to the drain-lag effects, whereas in other conditions the I/V curves are not iso-dynamic, which complicates the modelling task.

### 2.2.3 Nonlinear Model Formulation

As it was already mentioned, if the trapping charge changes with the pulses, inconsistent  $G_m$  and  $G_{ds}$  curves can be obtained (which is an evidence of a non-quasi-static model) resulting in the inequality (2.33), i.e. the obtained  $i_{DS}$  curves by  $G_m$  or  $G_{ds}$  integration are different, as shown in the example presented in Fig. 2.42 (the path integration of  $i_{DS}$  depends on the selected trajectory in the  $v_{GS}$ ,  $v_{DS}$  plane).

$$\frac{\partial G_m(v_{GS}, v_{DS})}{\partial v_{DS}} \neq \frac{\partial G_{ds}(v_{GS}, v_{DS})}{\partial v_{GS}} \quad (2.33)$$

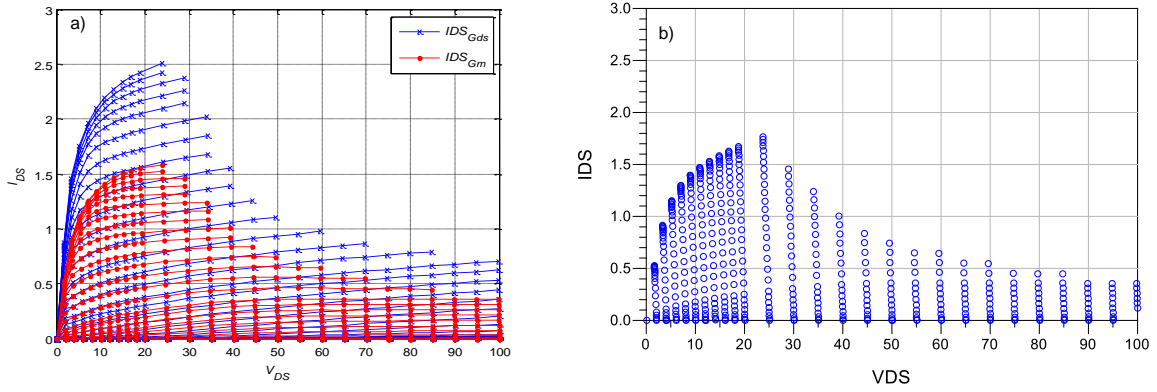


Fig. 2.42 – I/V curves a) obtained by integration of the  $G_m(v_{GS}, v_{DS})$  and  $G_{ds}(v_{GS}, v_{DS})$  and b) dc I/V curves.

Therefore, it is necessary to implement a procedure to extract a quasi-static model of the channel current and charges and then incorporate the long term memory in this model.

The adopted model is a parametric function of the instantaneous values of  $v_{GS}$  and  $v_{DS}$ , and whose parameter vector  $\theta$  (which includes all  $i_{DS}$  model parameters that vary with the trapping charge state – for example  $\beta$ ,  $\alpha$ ,  $V_T$ , etc.) is a function of the trap charge, herein represented by the trapping-state control voltage  $v_C$ , which plays the role of the model controlling parameter:

$$i_{DS}(t) = f\{v_{GS}(t), v_{DS}(t), \theta[v_C(t)]\} \quad (2.34)$$

As a parametric model,  $f(\cdot)$  is a unique static function (i.e., it obeys the quasi-static assumption), and  $v_C(t)$  is the control voltage,  $v_C$ , across the capacitor of a nonlinear RC network with a diode-switch [83], as illustrated in Fig. 2.43, which has associated two

time-constants: the faster charging time-constant and the much slower discharging one. It should be noted that the transfer function of the filter that converts the  $v_{DS}$  voltage into the  $v_C$  voltage is being approximated by a simpler differential equation, which is equivalent to a nonlinear low pass filter transfer function, with only two time constants. However, the real transfer function can be more complicated and, probably, depending on the device, it could be necessary more than one cell of this nonlinear low pass filter presented in Fig. 2.43.

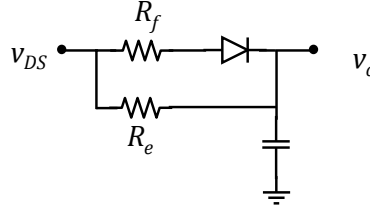


Fig. 2.43 – Trap charge and discharge equivalent circuit.

Being a parametric model,  $f(\cdot)$  can be interpreted as a large set of  $K$  static  $i_{DS}(v_{GS}, v_{DS})$  models, each one dependent on a particular parameter vector  $\theta_k$  defined by its corresponding  $v_{C\_k}$  trap charge state, or quiescent  $v_{DSQ}$ . With this in mind, the dynamic, or non-quasi-static, model has its origins on the evolution with time of  $v_C(t)$ , and so of  $\mathcal{A}[v_C(t)]$ , or of  $\theta_k(v_{C\_k})$  if  $\mathcal{A}[v_C(t)]$  were defined in  $K$  discrete points.

Although the following discussion on the model format and its extraction is focused on the  $i_{DS}$  model, it can be easily extended to the model of  $Q_g(v_{GS}, v_{DS})$  and thus to  $C_{gs}(v_{GS}, v_{DS})$ ,  $C_{gd}(v_{GS}, v_{DS})$  and  $C_{ds}(v_{GS}, v_{DS})$ . Actually, the objective is to obtain a quasi-static model of the channel current and charges.

## 2.2.4 Extraction Procedure

### A. EXTRACTION METHODOLOGY INTRODUCTION

According to what was above explained,  $i_{DS}(v_{GS}, v_{DS})$  can be uniquely defined – so that its form is constant regardless of the path along which it is tested – as long as  $v_C(t)$  is kept constant. However, as  $v_C(t)$  is dependent on  $v_{DS}(t)$ , the only way that  $v_{DS}$  can be swept to extract a quasi-static  $i_{DS}(v_{GS}, v_{DS})$  model, and thus keeping constant  $v_C[v_{DS}(t)]$ , is to take advantage of the widely separate trap charging and discharging time-constants. The S-parameters measurements with pulsed  $v_{DS}$  should therefore always be conducted for  $v_{DS}$  values smaller than the quiescent  $v_{DSQ}$  (i.e., using step down excitations), and when the discharging processes have not yet started. This guarantees that the trap state is always kept constant and determined by the  $v_{DSQ}$ .

For example, setting  $v_{DSQ}$  at 150V and pulsing  $v_{DS}$  down to 60V (see Fig. 2.44) would allow us to extract a pulsed I/V model where  $i_{DS}(v_{GS}, v_{DS})$  is quasi-static and represented by:

$$f\{v_{GS}, v_{DS}, \theta[v_C(V_{DSQ} = 150V)]\} \quad (2.35)$$

where  $v_C(V_{DSQ}=150V)=150V$ .

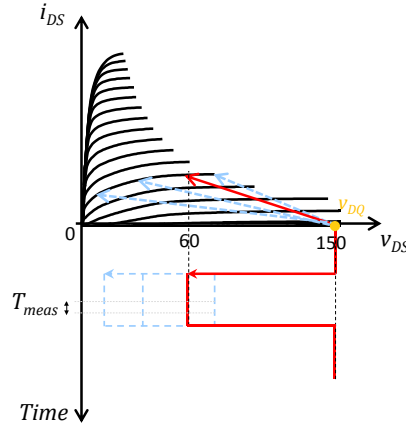


Fig. 2.44 – Illustration of the proposed measurement technique to obtain a quasi-static FET model.

Unfortunately, breakdown or quiescent dissipation power conditions may prevent pulsing from such a high  $V_{DSQ}$ . If that is the case, a double-pulse technique [88] can be used, as is illustrated in Fig. 2.45, where a first pulse is used to set the desired high  $V_{DSQ}$ , whose duration is considerably higher than the trap charging time-constants, but sufficiently smaller than the self-heating time constants, or, at least, sufficiently small to prevent burning the device.

Then, for extracting the  $i_{DS}[v_{GS}, v_{DS}, \theta(v_C)]$  model threshold voltage dependence on the parameter  $v_C$ , it is necessary to sweep this  $v_C$  in a controllable way. For that, the above extraction will be repeated for as many quiescent points  $V_{DSQ}$  as desired, starting at the wanted maximum  $v_{DS}$  voltage, and obtaining several sets of I/V curves with the respective trap state imposed by the used  $V_{DSQ}$ .

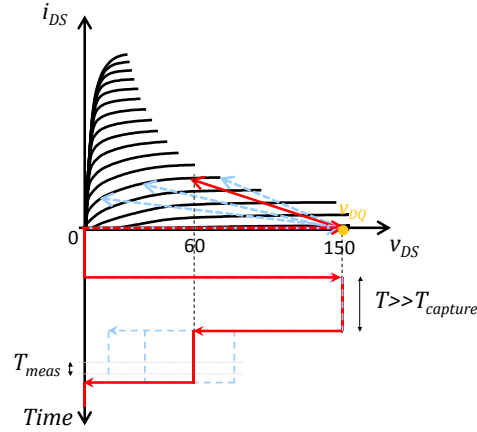
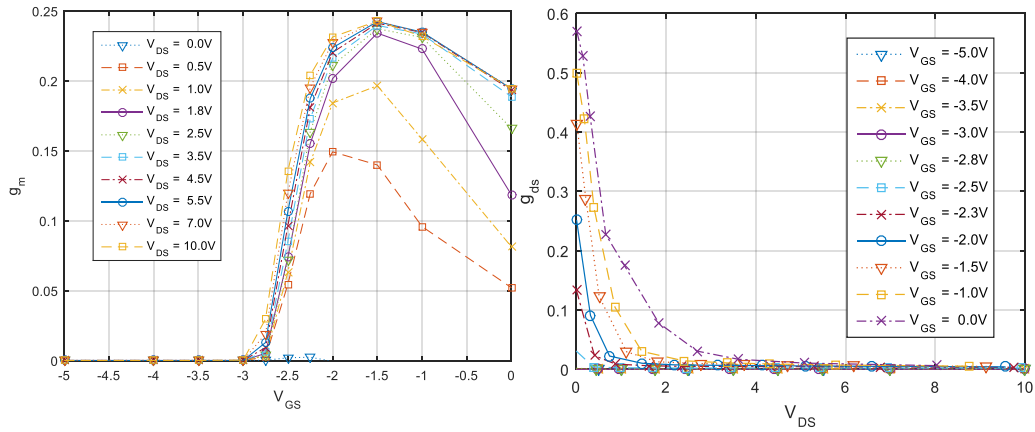


Fig. 2.45 – Illustration of the proposed double-pulsed measurement technique to obtain a quasi-static model without damaging the device by excessive power dissipation.

### B. PULSE BIAS S-PARAMETERS MEASUREMENT RESULTS

Using the extraction methodology described above and, after the extrinsic component values extraction for the 1mm GaN HEMT die, it is possible to have access to the bias dependent S-parameters at the intrinsic reference plan for different trapping states imposed by the used  $V_{DQs}$  voltages. In the following figures the  $G_m$  and  $G_{ds}$ , obtained from the bias-dependent small-signal extraction for several  $V_{DQs}$  voltages [10V, 25V and 45V], are presented:



a)

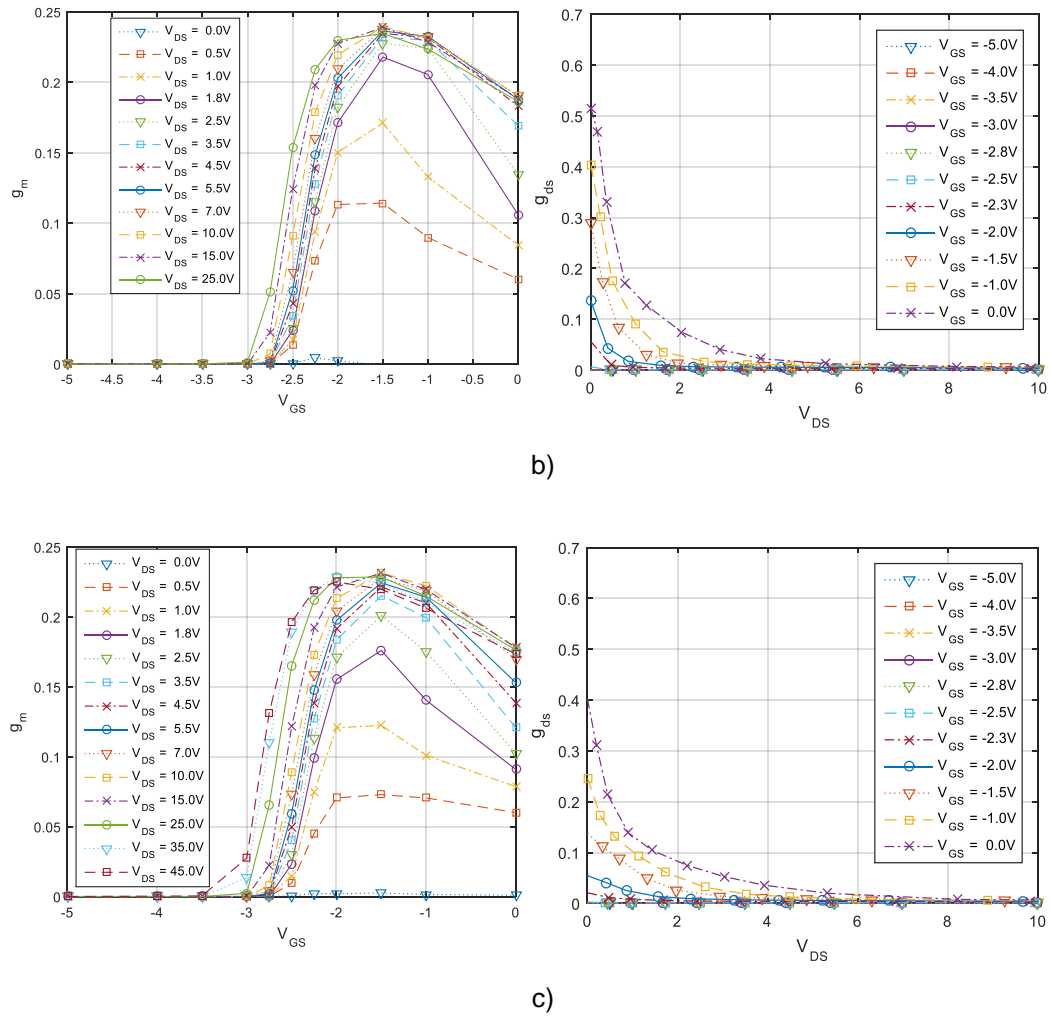


Fig. 2.46 – Obtained  $G_m$  and  $G_{ds}$  from the bias-dependent small-signal extraction for several  $V_{DQs}$  voltages: a)  $V_{DQ}=10V$ ; b)  $V_{DQ}=25$ ; c)  $V_{DQ}=45$ .

With these sets of  $G_m$  and  $G_{ds}$  curves for several  $V_{DQs}$ , the quasi-static nature of these measurements can be tested by verifying if the  $[G_m(V_{GS}, V_{DS}), G_{ds}(V_{GS}, V_{DS})]$  “field” is conservative, i.e if the I/V curves obtained by integration of  $G_m$  and  $G_{ds}$  are unique – not depending on the integration path. In Fig. 2.47 it is possible to see that the I/V curves obtained by integration of the  $G_m$  and  $G_{ds}$  are almost identical. Only small differences due to temperature are still evident, showing that the used extraction methodology is indeed very effective.

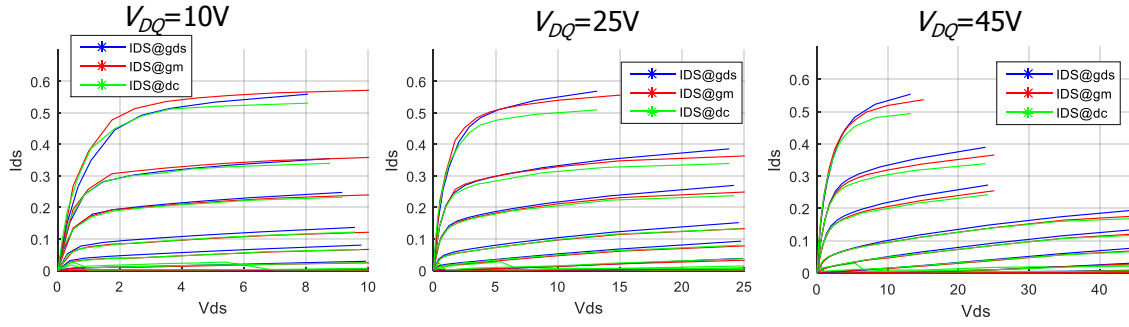


Fig. 2.47 – Obtained I/V curves by integration of the  $G_m$  and  $G_{ds}$  in comparison with the measured pulsed dc I/V curves.

### C. EXTRACTION OF THE QUASI-STATIC $I_{DS}(V_{GS}, V_{DS}, \theta(V_C))$ MODEL

Before moving to the nonlinear model extraction, it is necessary to look at the bias-dependent small signal  $G_m$  and  $G_{ds}$  to verify which parameters of the model should vary with the trapping control voltage.

One of the most visible effects of trapping in the GaN HEMTs is the  $V_T$  variation as it is possible to see in the extracted bias-dependent  $G_m$  for different pre-set voltages ( $V_{DSQ}=10V$  and  $V_{DSQ}=45V$ ) presented in the Fig. 2.48. Therefore, the parameter that controls the  $V_T$  should vary with the trapping voltage control.

In addition, the used devices also reveal a decrease in the FET's output conductance for higher pre-sets that is known as knee walkout, as shown in Fig. 2.49. Consequently, the parameter that controls the  $i_{DS}$  knee should also vary with the trapping voltage control.

Accordingly, the  $i_{DS}(V_{GS}, V_{DS})$  model adopted to fit all sets of I/V points for each  $V_{DSQ}$  was the one of [34], where all model coefficients are fixed for all  $V_{DSQ}$ , except the threshold voltage coefficient,  $V_T$ , and the parameter  $\alpha$  that controls the  $i_{DS}$  knee voltage, which are dependent on the trapping state control voltage,  $v_C(t)$ . It was observed that the model of the  $V_T$  and  $\alpha$  dependence can be modelled with a hyperbolic tangent, such as:

$$V_T[v_C(t)] = V_{T0} + \frac{1}{2} A_{V_T} (1 + \tanh[K_{V_T}(v_C(t) - V_{V_T})]) \quad (2.36)$$

$$\alpha[v_C(t)] = \alpha_0 + \frac{1}{2} A_{\alpha_T} (1 + \tanh[K_{\alpha_T}(v_C(t) - V_{\alpha_T})]) \quad (2.37)$$

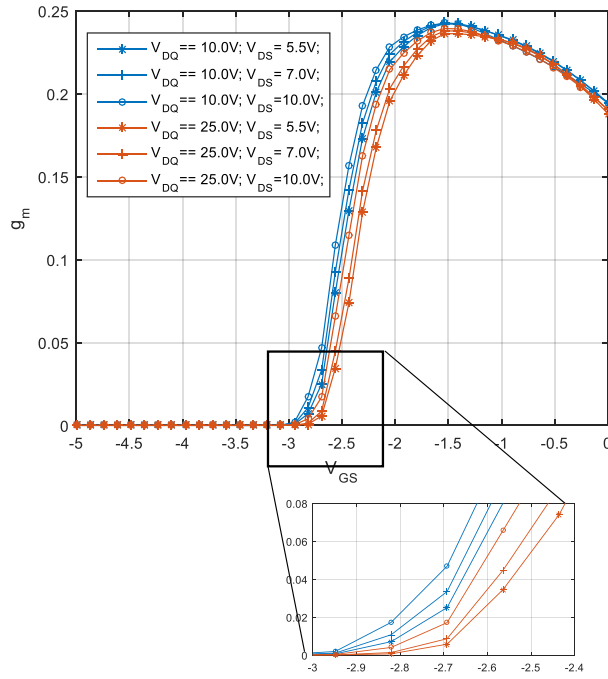


Fig. 2.48 – Observation of the threshold voltage variation in the extracted bias-dependent  $G_m$  for different pre-set voltage ( $V_{DSQ}=10V$  and  $V_{DSQ}=45V$ ).

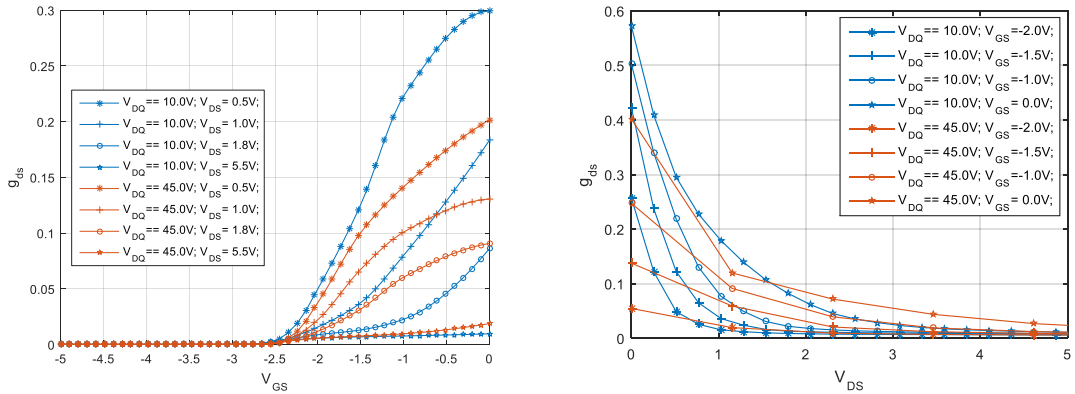


Fig. 2.49 – Knee walkout observation in the extracted bias-dependent  $G_{ds}$  for different pre-set voltages ( $V_{DSQ}=10V$  and  $V_{DSQ}=45V$ ).

Fig. 2.50 shows the obtained curve-fitting results of the I/V curves for several  $V_{DSQ}$  voltages. It should be noted that the measured  $i_{DS}$  points with  $V_{DS}$  higher than the pre-set  $V_{DSQ}$ , are not iso-dynamic. Hence, these values are not included in the curve-fitting process.

The coefficients' variation resulting from the model extraction and fitted through (2.36) – for the threshold voltage – and (2.37) – for the  $\alpha$  – are shown in Fig. 2.51. It should be noted that the model was extrapolated for  $V_{DSQ}$  values higher than 45V since this is the maximum voltage that the implemented drain pulser can excite. This extrapolation was made so that the model could fit the measured RF performance.

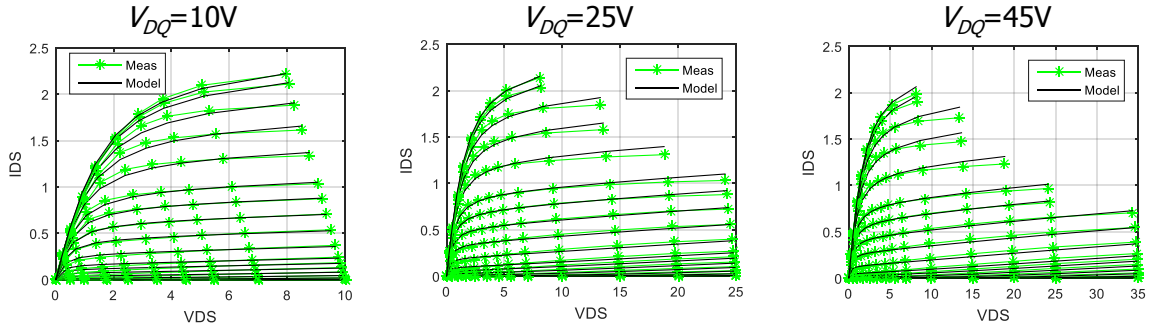


Fig. 2.50 – Modelled and measured I/V curves for different  $v_{DS}$  preset pulses of the 1mm GaN HEMT die.

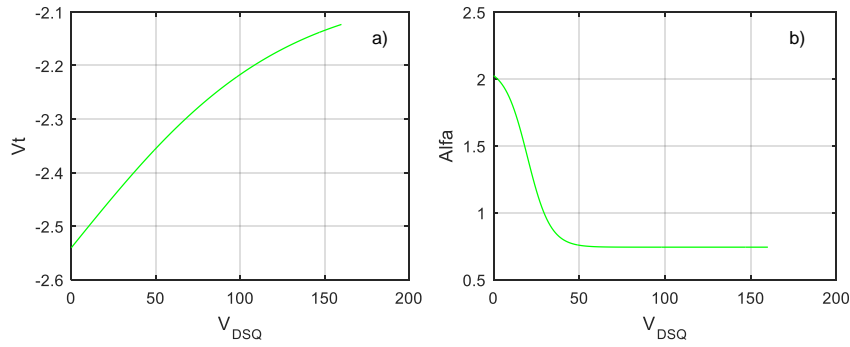


Fig. 2.51 – Extracted threshold voltage and  $\alpha$  variations with the  $v_{DS}$  preset pulse, or the intended  $V_T[v_c(t)]$  and  $\alpha[v_c(t)]$ , respectively.

For extracting the trapping state voltage,  $v_c(t)$ , dynamics, several voltage steps (up and down) were performed to observe the time constants associated to the trapping and de-trapping processes, respectively. Fig. 2.52 shows the  $i_{DS}$  recovery response when the  $V_{DS}$  is a step-down from 45V to 25V with a low and constant  $V_{GS}$  voltage equal to -2.6V (close to the  $V_T$  voltage) to avoid thermal effects.

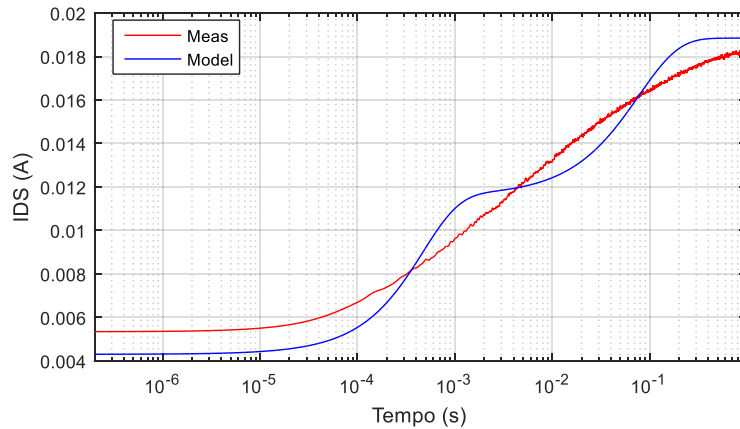


Fig. 2.52 –  $i_{DS}$  recovery response when the  $V_{DS}$  was stepped-down from 45V to 25V with a low and constant  $V_{GS}$  voltage equal to -2.6V to avoid thermal effects. In comparison, it is also plotted the respective model fitting.

As it was already mentioned, this  $i_{DS}$  recovery is not a simple RC filter response. Therefore, to obtain a better fitting, two nonlinear RC filters were used and so, two time constants (70ms and 300us) for the recovery. The obtained fitting for the  $i_{DS}$  recovery is shown in Fig. 2.52.

Following the same procedure for the  $i_{DS}$  step-up response, the time constants associated to the trapping charge process can be determined, which are equal to 2ms and 30μs. It should be noted that it is very difficult to separate thermal effects from the trapping effects and, probably, the slowest trapping time constant is mixed up with some transients due to thermal effects. The obtained curve-fitting to the  $i_{DS}$  step-up response is shown in Fig. 2.53.

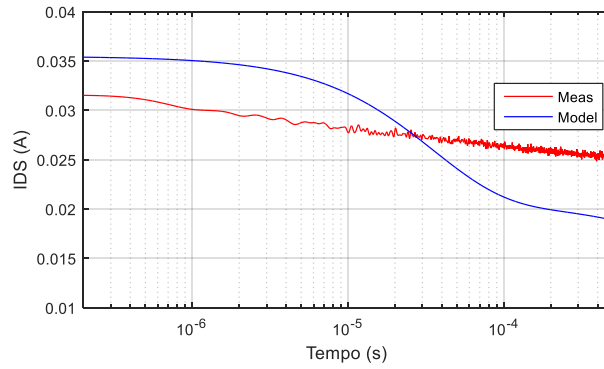


Fig. 2.53 –  $i_{DS}$  trapping response when the  $v_{DS}$  was stepped up from 25V to 45V with a low and constant  $v_{GS}$  voltage equal to -2.6V to avoid thermal effects. In comparison, it is also plotted the respective model fitting.

On what thermal modelling is concerned, the coefficient that controls the gain of the  $i_{DS}$  function,  $\beta$ , was changed according to:

$$\beta = \beta_0 + \beta_{Th} T_h \quad (2.38)$$

where  $\beta_0$  is the initial value extracted and  $\beta_{Th}$  is the coefficient that scales the effect of the temperature,  $T_h$ , in the  $i_{DS}$  current. To represent the electro-thermal dynamics, a simple RC circuit (only one pole) was used, in order not to unnecessarily complicate the model. The obtained coefficients are [ $R_{Th}C_{Th} = 130\text{ms}$  and  $\beta_{Th} = -1.3014\text{e-}3\text{A/}^\circ\text{C}$ ] and the obtained curve-fitting results are shown in Fig. 2.54.

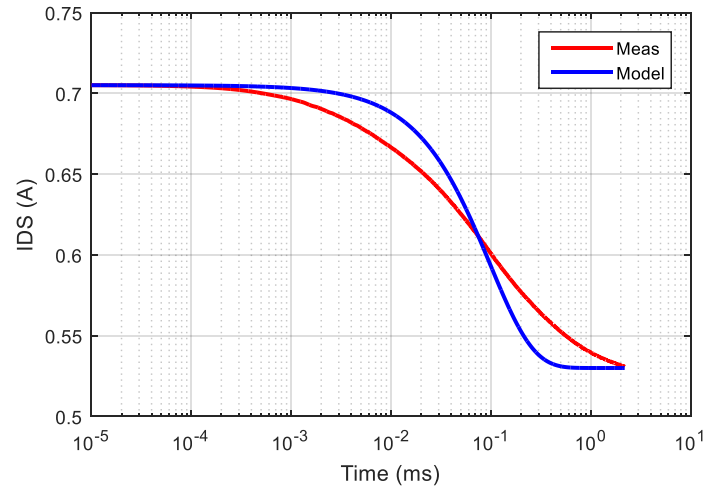


Fig. 2.54 – Modelled and Measured electro-thermal dynamics.

## 2.2.5 Model Validation

### A. CW STATIC VALIDATION

After including trapping effects in the extracted 3mm GaN HEMT model, it is necessary to validate again the updated CW characteristics over a class AB PA through: AM/AM, AM/PM, output power and efficiency Load Pull contours:

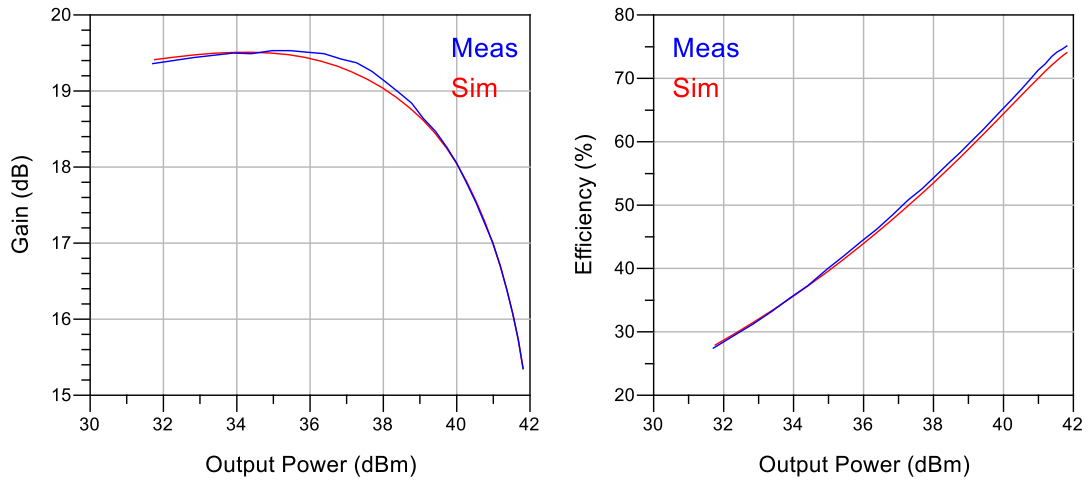


Fig. 2.55 – Simulated gain and efficiency versus output power, after the inclusion of the trapping effects, in comparison with the measurements.

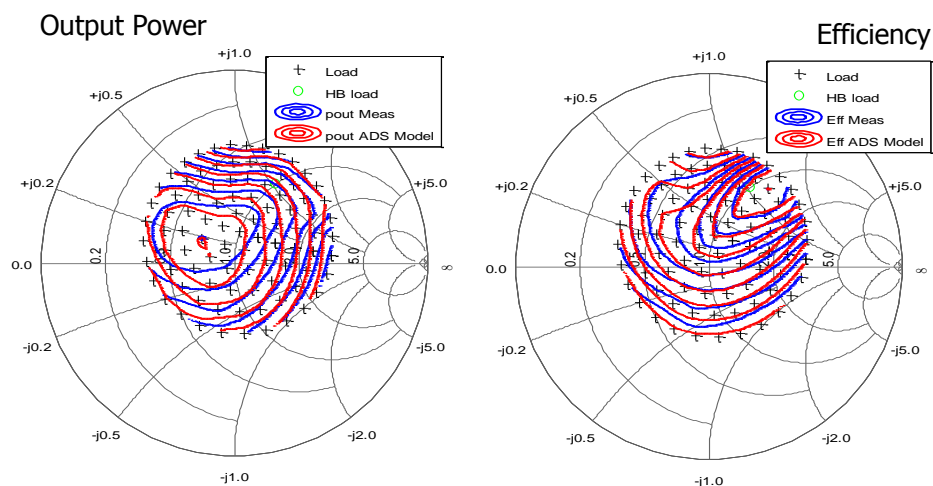


Fig. 2.56 – Simulated efficiency and output power load-pull contours after the inclusion of the trapping effects, in comparison with the measurements.

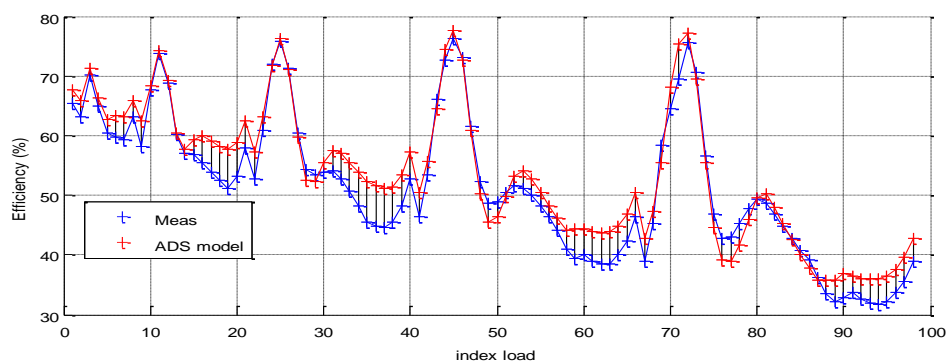


Fig. 2.57 – Simulated efficiency after the inclusion of the trapping effects, in comparison with the measurements.

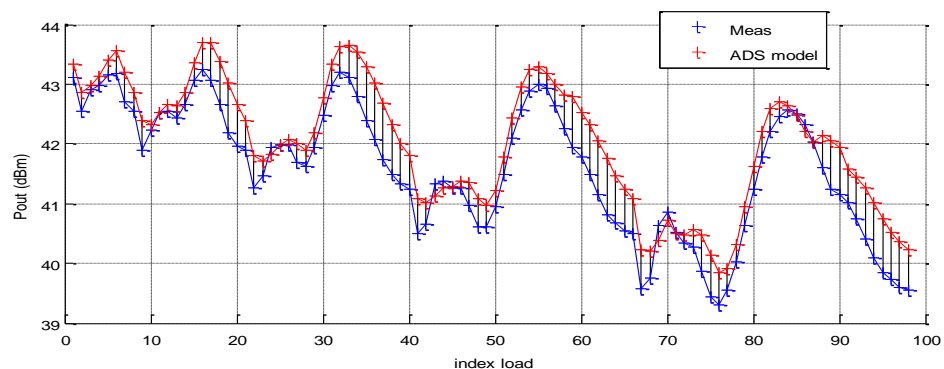


Fig. 2.58 – Simulated output power after the inclusion of the trapping effects, in comparison with the measurements.

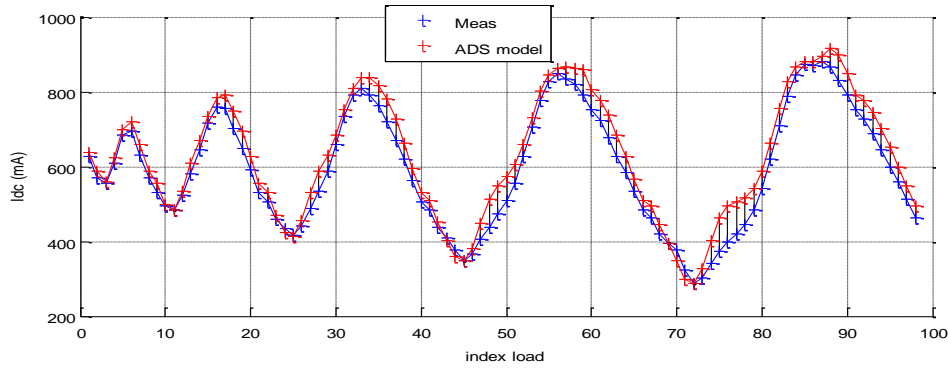


Fig. 2.59 – Simulated dc drain current after the inclusion of the trapping effects, in comparison with the measurements.

As it is possible to see, the obtained load-pull predictions of the 3mm device model are practically the same when it is not considered the trapping effects as it is expected since in CW measurements the trapping state is imposed by the maximum  $V_{DS}$  peak voltage.

### B. DYNAMIC VALIDATION

For demonstrating the extracted model capability to predict the low-frequency dispersion effects observed in GaN HEMT PAs, and their most relevant impact on PA linearity, a 2100MHz 20W PA, using 3mm GaN HEMT, was designed and tested. Fig. 2.60 shows measured and simulated dynamic gain profiles when the PA was excited with two-tone stimuli of different peak powers. As it is possible to see, although there are some differences between the model and the measurements, the model can still reasonably predict the so-called GaN HEMT soft compression, which is actually due to a self-biasing change from class AB to class C behaviour due to the device's drain-lag, as previously advanced in [89].

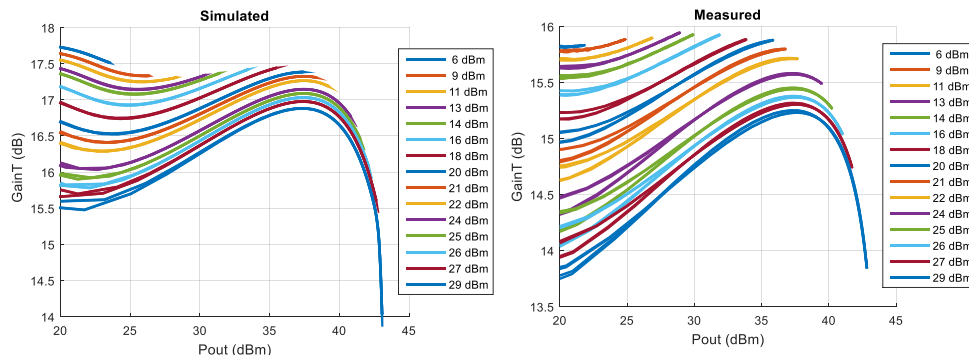


Fig. 2.60 – Measured and simulated dynamic gain profiles with two-tones of various peak-envelope-powers.

In addition, the extracted model was also used to predict the dynamic gain profiles when the PA was excited with two-tones, but now with different frequency separation,  $\Delta f$ , as shown in Fig. 2.61. Although the model does not predict the slight increase of the output power observed for higher  $\Delta f$ , it can predict the dispersion with the  $\Delta f$ . For very small  $\Delta f$  comparatively to the trap discharge time-constant, the gain will dynamically change with the  $v_{DS}(t)$  amplitude, and the PA shows evident memory effects. On the other hand, for high  $\Delta f$  (for this device, higher than 175kHz),  $V_T$  cannot follow the instantaneous  $v_{DS}(t)$ , remaining constant and equal to the respective value given by the  $v_{DS}$  peak. The PA is now memoryless but self-biased into a much more nonlinear class C operation. This self-biasing shift induced by the two-tone frequency separation is an evident proof of trapping, as no other memory effect of equal rise and fall time-constants (either due to bias circuitry or thermal behaviour) can be used to explain it.

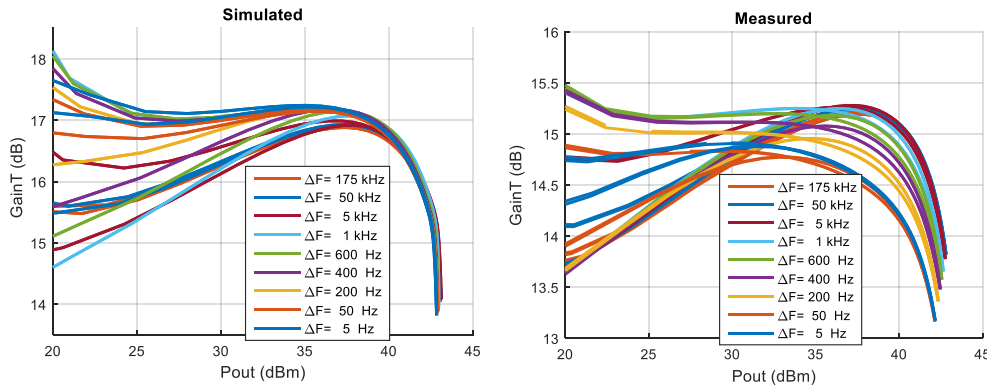


Fig. 2.61 – Measured and simulated dynamic gain profiles with two-tones of constant peak-envelope-power and of various frequency separations.

## 2.3. Summary

This chapter started by presenting a generic model extraction methodology for Si LDMOS and GaN HEMT devices, where any trapping effects observed in the GaN HEMTs were not considered. For validation purposes of this extraction methodology, it was used a single die with 3mm. The extraction methodology was also validated in a high power packaged 6-Cell x 2.7mm device, where the model was obtained by scaling the extracted 3mm device model.

On what the 3mm GaN HEMT device modelling is concerned, since this is a bare die device, the extraction of the extrinsic equivalent circuit elements through (guided) optimization provided results with a physical significance. The obtained profiles of the bias-dependent intrinsic elements – after the de-embedding of the extrinsic components – are also consistent with the device physical behaviour, thus providing good small-signal results.

The extraction of a large-signal model from bias-dependent small-signal  $C_{gs}$ ,  $C_{gd}$ ,  $C_{ds}$ ,  $G_m$  and  $G_{ds}$  led to a very good accuracy on load-pull output power, efficiency and dc drain current. Static nonlinear distortion characteristics evaluated in terms of AM/AM and AM/PM also proved the validity and usefulness of the obtained large-signal model.

On what the packaged 6-Cell 2.7mm device modelling is concerned, although the obtained results are slightly worse than the ones obtained for the 3mm Cell bare die, the model can also be used to correctly predict the output power and efficiency load-pull contours.

At this point, no long-term trapping effects had taken into account. As a consequence, the  $G_m$  and  $G_{ds}$  are inconsistent, resulting in different I/V curves if they are integrated in  $v_{GS}$  or  $v_{DS}$  paths, respectively, which led us to make a compromise between the  $G_m$  and  $G_{ds}$  fits.

Therefore, in the second part of this chapter, a direct GaN HEMT model extraction technique based on double-pulse iso-dynamic measurements was presented, obtaining the desired consistency between the  $G_m$  and  $G_{ds}$  curves.

The long-term memory effects induced by the trapping, namely the drain-lag phenomenon, were modelled with two parallel nonlinear diode-switch RC filters to represent four different time-constants – two for the trapping process and two for the de-trapping process.

Although the trapping behaviour was represented by a very simple shift in the threshold voltage,  $V_T$ , and in the knee voltage,  $V_k$  – actually  $\alpha$  which is approximately equal to  $1/V_k$  – the model was capable of reproducing the essential GaN HEMT dynamic distortion characteristics such as the so-called soft-compression and the envelope bandwidth related nonlinear memory.

In order to improve the dynamic predictions, the thermal effects were also modelled. For that, the temperature dependency in the coefficient that controls the  $i_{DS}$  current gain,  $\beta$ , was included in the model. To represent the electro-thermal dynamics, a simple RC filter was used.

Given the obtained results, the state-of-the-art, and the available pulsed I/V and pulsed S-parameters measurement capabilities, this model is believed to be a very good compromise between modelling complexity and accuracy. It certainly serves as a basis for PA CAD design, and also to approximate the PA's long-term memory behaviour. Furthermore, this model can also be used to identify and understand the nonlinear distortion generation mechanisms of a power amplifier, which is exactly the main purpose of this PhD thesis.

### 3. Nonlinear Distortion Generation Mechanisms of the Carrier and Peaking Operating as Single-ended Amplifiers

Before studying the nonlinear distortion in a Doherty arrangement it is fundamental to understand its main contributors. For that, the carrier and peaking PAs operating individually as a single-ended were studied. Therefore, the objective of this chapter is to identify and explain the main nonlinear AM/AM and AM/PM PA physical distortion generation mechanisms in the two active device technologies of most practical interest – the Si LDMOS and the GaN HEMT.

This chapter also presents a semi-analytical model sufficiently accurate to produce useful nonlinear distortion predictions that are simple enough to allow qualitative circuit design and performance optimization.

#### 3.1. Semi-Analytical Nonlinear Distortion analysis

Contrary to the traditional Volterra series analysis, in which the nonlinearities are approximated by low-order polynomials, and so whose application domain is restricted to mild nonlinear regimes, the proposed method uses the true nonlinear models but it is assumed that the necessary control voltages are already known. This means that some-kind of sinusoidal steady-state analysis, like the ones performed by the frequency-domain harmonic-balance simulators or the time-domain shooting-Newton engines, is conducted before-hand.

After the determination of these control voltages,  $v(t)$ , the time-domain waveforms of the PA nonlinear current,  $i[v(t)]$ , and charge or capacitor,  $q[v(t)]$  or  $C[v(t)]$ , elements are readily obtained. A Fourier expansion of these time-varying elements then allows the calculation of the in-band linear signal and distortion components from which the AM/AM and AM/PM analytical model is derived. Rigorously speaking, this was called a semi-analytical model because it derives closed form expressions, but it is based on the a-priori knowledge of the time-varying waveforms, which, as above explained, must be obtained from an exact CW numerical simulation.

In this sense, the now proposed technique suffers from the same basic limitation of the Volterra on top of Harmonic Balance (VoHB) method of [37] and [90], providing also an approximate analytical form that requires an a priori iterative numerical solution of the circuits' periodic steady-state regime. However, contrary to the VoHB, the present technique directly deals with the Fourier components of the time-varying nonlinear elements and not of any low order polynomial approximation of their models. So, it is more accurate for the same level of complexity, offers a more direct interpretation of the AM/AM and AM/PM distortion generation mechanisms (in terms of the nonlinear dependence of the elements on their control voltages) and circumvents the issues of the polynomial fitting reported in [37], [90] and [91].

In summary, the proposed analysis can be divided in the following four steps:

- 1) Obtain the control voltages of all active device's nonlinear elements via some sinusoidal large-signal steady-state analysis;
- 2) Calculate the time-domain variation of these nonlinear elements;
- 3) Extract the correspondent Fourier components;
- 4) Calculate the intrinsic FET's fundamental voltages and currents which determine the overall AM/AM and AM/PM characteristics.

For illustration purposes, let us first consider the case of a resistive nonlinearity as the ones found in the FET's drain-source current,  $i_{DS}(v_{GS}, v_{DS})$ . Since this is a bi-dimensional nonlinearity (dependent on two separate control-voltages), it will be assumed that it can be expressed as the product of two one-dimensional functions

$$i_{DS}(v_{GS}, v_{DS}) = f_g(v_{GS}) \cdot f_d(v_{DS}) \quad (3.1)$$

as is the case of a large set of nonlinear FET models. In fact, it accounts for all observed FET I/V features except the possible dependence of the knee voltage (transition between the triode and the saturation regions) dependence on  $v_{GS}$  and the possible dependence of the turn-on, or threshold voltage, on  $v_{DS}$ .

In the following analysis, the input control voltage is represented by the generic form:

$$v_{GS}(A, t) = \frac{1}{2} \sum_{k=0}^K V_{gsk}(A, \omega) \cdot e^{j\omega t} + \frac{1}{2} \sum_{k=-K}^0 V_{gsk}(A, \omega) \cdot e^{j\omega t} \quad (3.2)$$

in which  $\omega = k\omega_0$ ,  $\omega_0$  is the fundamental frequency, and  $V_{gsk}(A, \omega)$  coefficients are the Fourier components of the periodic  $v_{GS}(t)$ , determined by the PA excitation source voltage of amplitude  $A$ .

When the voltage-dependent current source is terminated by intrinsic impedance  $Z_L(\omega)$ , and fed by a dc voltage source  $V_{DD}$ , so that:

$$V_{ds}(V_{gs}, \omega) = V_{DD} \cdot \delta(\omega) - Z'_L(\omega) \cdot I_{dsk}(V_{gs}, \omega) \quad (3.3)$$

(where  $\delta(\omega)$  is the Dirac delta function and the  $I_{dsk}$  are the Fourier components of the periodic  $i_{DS}(t)$  current) and so

$$v_{DS}(V_{gs}, t) = V_{DD} - Z'_L(\omega) \cdot \left[ \frac{1}{2} \sum_{k=0}^K I_{dsk}(V_{gs}, \omega) \cdot e^{j\omega t} + \frac{1}{2} \sum_{k=-K}^0 I_{dsk}(V_{gs}, \omega) \cdot e^{j\omega t} \right] \quad (3.4)$$

then, the frequency-domain representation of the  $i_{DS}[v_{GS}(t), v_{DS}(t)]$  current would be:

$$I_{ds}(V_{gs}, \omega) = \left[ \frac{1}{2} \sum_{k=0}^K F_{gk_1}(V_{gs}, \omega_0) + \frac{1}{2} \sum_{k=-K}^0 F_{gk_1}(V_{gs}, \omega_0) \right] \times \left[ \frac{1}{2} \sum_{k=0}^K F_{dk_2}(V_{ds}, \omega_0) + \frac{1}{2} \sum_{k=-K}^0 F_{dk_2}(V_{ds}, \omega_0) \right] \quad (3.5)$$

where the  $F_{gk_1}$  and the  $F_{dk_2}$  are the Fourier components of the time-varying  $f_g[v_{GS}(t)]$  and  $f_d[v_{DS}(t)]$  waveforms defined by

$$F_{gk_1} = \frac{1}{T} \int_{-T/2}^{T/2} f_g[v_{GS}(t)] \cdot e^{-jk_1\omega_0 t} dt \quad (3.6)$$

and

$$F_{dk_2} = \frac{1}{T} \int_{-T/2}^{T/2} f_d[v_{DS}(t)] \cdot e^{-jk_2\omega_0 t} dt \quad (3.7)$$

For example, the fundamental component of this current would be

$$I_{ds1}(A, \omega_0) = F_{g1}(A, \omega_0) \cdot F_{d0}(A, \omega_0) + F_{g0}(A, \omega_0) \cdot F_{d1}(A, \omega_0) + \frac{1}{2} F_{g2}(A, \omega_0) \cdot F_{d1}^*(A, \omega_0) + \frac{1}{2} F_{g1}^*(A, \omega_0) \cdot F_{d2}(A, \omega_0) + \dots \quad (3.8)$$

which would lead to a fundamental output voltage of

$$V_{ds1}(A) = -Z'_L(\omega_0) \left[ F_{g1}(A) \cdot F_{d0}(A) + F_{g0}(A) \cdot F_{d1}(A) + \frac{1}{2} F_{g2}(A) \cdot F_{d1}^*(A) + \frac{1}{2} F_{g1}^*(A) \cdot F_{d2}(A) + \dots \right] \quad (3.9)$$

where, for notation simplicity, the explicit dependence on  $\omega_0$  was dropped and the dependence of  $V_{gs}$  on the input amplitude  $A$  was implicitly assumed.

As already stated, the proposed distortion analysis method is based on the knowledge of the control voltage waveforms  $v_{GS}(t)$  and  $v_{DS}(t)$  – a-priori determined via a numerical periodic steady-state simulation such as the frequency-domain harmonic-balance or the time-domain shooting-Newton methods –, and thus, of the static nonlinearities  $f_g[v_{GS}(t)]$  and  $f_d[v_{DS}(t)]$ .

If now the input voltage-dependent gate-source accumulated charge,  $q_{gs}(v_{GS})$ , or capacitance,  $C_{gs}(v_{GS})$ , were considered, then its corresponding time-domain current would be given by

$$i_{GS}(t) = \frac{d q_{gs}[v_{GS}(t)]}{d t} = C_{gs}[v_{GS}(t)] \frac{d v_{GS}(t)}{d t} \quad (3.10)$$

whose frequency-domain representation would be

$$I_{gs}(V_{gs}, \omega) = \left[ \frac{1}{2} \sum_{k_1=0}^K C_{gsk1}(V_{gs}, \omega) + \frac{1}{2} \sum_{k_1=-K}^0 C_{gsk1}(V_{gs}, \omega) \right] \times \left[ \frac{1}{2} \sum_{k_2=0}^K j k_2 \omega_0 V_{gsk2} + \frac{1}{2} \sum_{k_2=-K}^0 j k_2 \omega_0 V_{gsk2} \right] \quad (3.11)$$

where the  $C_{gsk}$  coefficients are again the Fourier components of the time-varying  $C_{gs}[v_{GS}(t)]$ :

$$C_{gsk} = \frac{1}{T} \int_{-T/2}^{T/2} C_{gs}[v_{GS}(t)] \cdot e^{-jk\omega_0 t} dt \quad (3.12)$$

Similarly to what was done for the drain-source current nonlinearity, for example, the fundamental component of this gate-source current would be:

$$\begin{aligned} I_{gs1}(V_{gs}, \omega_0) &= j\omega_0 C_{gs0}(V_{gs}, \omega) \cdot V_{gs1} \\ &\quad - \frac{1}{2} j\omega_0 C_{gs2}(V_{gs}, \omega) \cdot V_{gs1}^* \\ &\quad + \frac{1}{2} j2\omega_0 C_{gs1}^*(V_{gs}, \omega) \cdot V_{gs2} + \dots \end{aligned} \quad (3.13)$$

## 3.2. AM/AM and AM/PM on a Si LDMOS FET based PA

### 3.2.1 Equivalent Circuit Model of the LDMOS-PA

Fig. 3.1 represents the functional model of a single-stage Si LDMOS based PA in which  $[V_S(\omega)$  and  $Z_S(\omega)]$  and  $Z_L(\omega)$  constitute the input and output Thevenin equivalent circuits, respectively. The former includes the excitation source, input matching network and the FET's input extrinsic components and the latter incorporates the output load impedance,  $Z_o$ , the output matching network and the FET's output extrinsic components.

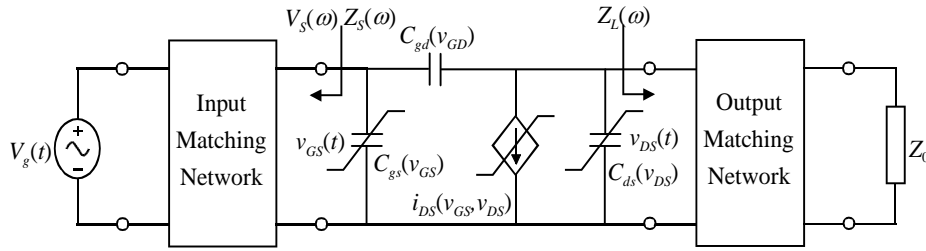


Fig. 3.1 – Graphical representation of the adopted single-stage PA model.

In order to be able to make a physically meaningful evaluation of the PA most significant nonlinear distortion generation mechanisms, typical Si LDMOS elements' values were selected and normalized them in a per Watt basis. The  $f_g(v_{GS})$  and  $f_d(v_{DS})$  functions were derived from the state-of-the-art Fager-Pedro model [33], [92] while the normalized  $C_{gs}(v_{GS})$  and  $C_{ds}(v_{DS})$  modelled profiles were obtained from measured data of an actual high-power LDMOS device. Fig. 3.2 presents both the adopted  $v_{GS}$ -dependent transconductance and  $v_{DS}$ -dependent output conductance, while Fig. 3.3 depicts the  $v_{GS}$ -dependent gate-source capacitance and the  $v_{DS}$ -dependent drain-source capacitance.

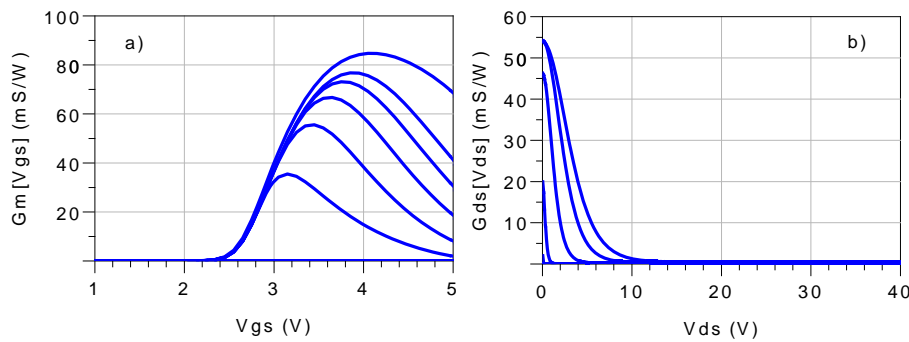


Fig. 3.2 – Si LDMOS normalized a) transconductance  $G_m(v_{GS})$  and b) output conductance  $G_{ds}(v_{DS})$  profiles derived from the adopted  $i_{DS}(v_{GS}, v_{DS})$  model.

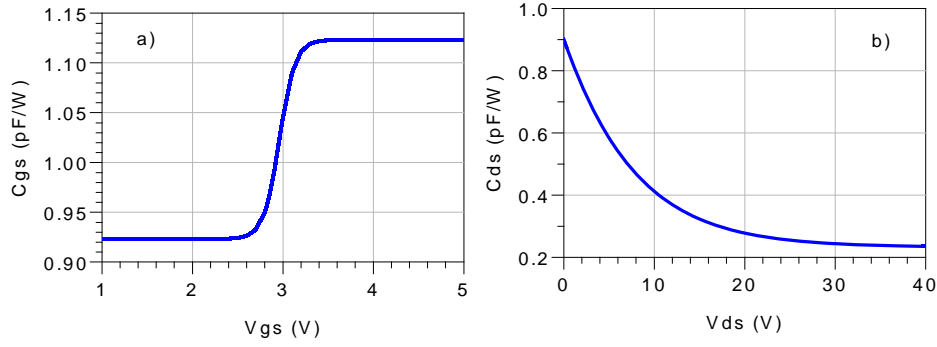


Fig. 3.3 – Si LDMOS normalized a) gate-source capacitance  $C_{gs}(v_{GS})$  and b) drain-source capacitance  $C_{ds}(v_{DS})$  modelled profiles obtained from measured data.

Contrary to the other capacitances, normalized  $C_{gd}(v_{GD})$  was assumed constant (a linear capacitance) at  $C_{gd} = 5$  fF/W, since harmonic-balance simulations showed that the effort of considering its nonlinearity would not increase the distortion model accuracy. In fact, although  $C_{gd}$  varies with the  $v_{GD}$  voltage, as this feedback depletion capacitance is reversed biased with a large voltage, its nonlinearity only manifests itself when the voltage excursion reaches the triode region, where the PA already presents a strong compression. Therefore, its time variation can be considered negligible [93]. However, as this constant feedback capacitance becomes reflected through the Miller effect to the input by  $C_{gd}(1-A_v)$ , and to the output by  $C_{gd}(A_v-1)/A_v$ , and the gate-drain voltage gain,  $A_v$ , depends on the gain compression – which is determined by the input excitation drive,  $A$  –  $C_{gd}$  may still have impact on the PA AM/AM and AM/PM, even if it is considered linear.

For achieving a complete description of the PA AM/AM and AM/PM, the equivalent circuit model of Fig. 3.1 will be further simplified as shown in Fig. 3.4.

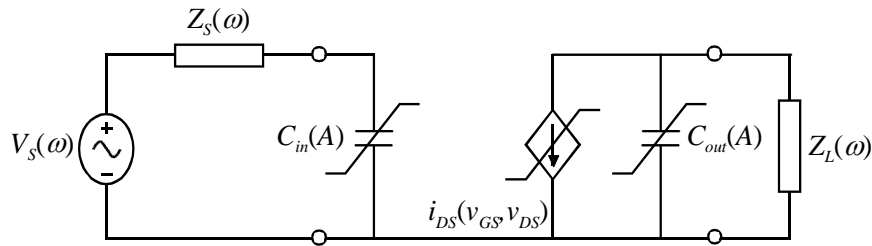


Fig. 3.4 – Simplified unilateral equivalent circuit model of the single-stage power amplifier.

In this figure,  $Z_L(\omega)$  is the load impedance, the input capacitor  $C_{in}(A)$  is given by  $C_{gs0}(A) + C_{gd}[1 - A_v(A)]$  and the output capacitor  $C_{out}(A)$  by  $C_{ds0}(A) + C_{gd}[A_v(A) - 1]/A_v(A)$ . Since the inherent transistor's feedback has now been eliminated, the complete PA nonlinear AM/AM and AM/PM distortion model can be computed as the cascade of five blocks, each one characterized by its own transfer function.

Referring back to the model of Fig. 3.1, the first block is the one that describes the transformation from the generator voltage  $V_g(A, \omega)$  to the input Thevenin voltage  $V_s(A, \omega)$ .

Since it is composed of only linear elements – the input matching network – its transfer function is only dependent on the frequency,  $\omega$ , and not on the excitation amplitude  $A$ . Let us call it  $H_1(\omega)$  and define it as  $H_1(\omega) \equiv V_S(A, \omega) / V_g(A, \omega)$ .

The second block refers to the transformation operated on  $V_S(A, \omega)$  to build  $V_{gs1}(A, \omega)$ , the fundamental voltage component at the  $C_{in}(A)$  terminals. It is characterized by a transfer function  $H_2(A, \omega) \equiv V_{gs1}(A, \omega) / V_S(A, \omega)$ , and determined by the  $C_{in}(A)$  variation.

The  $I_{ds}$  dependence on  $V_{gs1}(\omega)$  is described with the third block, i.e.,  $F_{g1}(A)$ . It is, in fact, given by  $H_3(A) \equiv F_{g1}(V_{gs1}(A, \omega)) / V_{gs1}(A, \omega)$ .

The fourth block provides the drain voltage  $V_{ds1}(A, \omega)$  given the drain current fundamental component,  $I_{ds1}(A, \omega)$ , and its transfer function  $H_4(A, \omega)$  is expressed by (3.9) – in which  $Z_L(\omega)$  must naturally also account for the averaged  $C_{ds}(A)$ , or  $C_{ds0}(A)$ , and the output Miller reflected  $C_{gd}$  – as  $H_4(A, \omega) \equiv V_{ds1}(A, \omega) / F_{g1}(V_{gs1}(A, \omega))$ .

Finally, the fifth block converts this fundamental drain voltage into the PA output voltage and is again represented by a linear transfer function  $H_5(\omega) \equiv V_o(A, \omega) / V_{ds1}(A, \omega)$ .

Given these transfer functions, a complete PA transfer function  $H(A, \omega)$  can be defined:

$$H(A, \omega) \equiv \frac{V_o(A, \omega)}{V_g(A, \omega)} = \prod_{i=1}^5 H_i(A, \omega) \quad (3.14)$$

from which the PA AM/AM and AM/PM distortions can be calculated as:

$$AM/AM \equiv 20 \log |H(A, \omega)| \quad (3.15)$$

and

$$AM/PM \equiv \frac{180}{j\pi} \ln \frac{H(A, \omega)}{|H(A, \omega)|} - \frac{180}{j\pi} \ln \frac{H(A_0, \omega)}{|H(A_0, \omega)|} \quad (3.16)$$

where  $A_0$  stands for a vanishingly small-signal amplitude.

### 3.2.2 $i_{DS}(V_{GS}, V_{DS})$ Induced AM/AM and AM/PM Distortions

From the three represented nonlinearities, the transistor nonlinear drain-to-source current,  $i_{DS}$ , is recognized as the fundamental contributor to the PA nonlinear distortion characteristics [31]–[34]. So, the proposed analysis will be based on the large-signal model description above discussed, where  $i_{DS}(V_{GS}, V_{DS})$  is approximately given by (3.1).

According to what was explained in the previous section, when this bi-dimensional nonlinear voltage-dependent current source is excited by a sinusoidal voltage of amplitude

A, and is terminated by a load-impedance  $Z_L(\omega)$ , it will generate a fundamental output voltage,  $V_{ds1}(A)$ , given by (3.9).

In order to identify which  $V_{ds1}(A)$  components are the most important to the overall LDMOS-PA AM/AM characteristic, it is necessary to restrict the analysis' range by first selecting appropriate quiescent points,  $V_{GG}=V_{GS0}$ ,  $V_{DD}=V_{DS0}$ , and input and output harmonic terminations,  $Z_S(\omega)$  and  $Z_L(\omega)$ .

For getting a wide view of the PA distortion behaviour, three distinct quiescent points were chosen, illustrative of class C, B and AB operation, for which the  $F_{gk}$  and  $F_{dk}$  Fourier coefficient variations with amplitude were studied.

To select a convenient set of intrinsic harmonic terminations, fundamental input and output impedances corresponding to optimum output power and power gain were imposed. Then, a thorough load-pull AM/AM, AM/PM and drain efficiency simulations of the second and third harmonic (purely reactive) terminations – the ones normally used in real PA designs – were performed. These load-pull results led to the conclusions that (i) the AM/AM and AM/PM are almost insensitive to the third harmonic terminations, and (ii) both distortion and drain-efficiency vary significantly with the second harmonic terminations, being the cases  $Z_S(2\omega_0)=0$ ,  $Z_L(2\omega_0)=0$  and  $Z_S(2\omega_0)=j\infty$ ,  $Z_L(2\omega_0)=j\infty$  the only ones of interest since they are the ones for which the drain efficiency is not severely degraded. None of these conclusions is surprising as they result from the fact that third harmonic can only affect 5th order AM/AM and AM/PM distortion via the mixing product  $3\omega_0-2\omega_0$ , while small and moderate distortion levels are mostly conditioned by the fundamental and second harmonic terminations that determine the third order mixing products  $\omega_0+\omega_0-\omega_0$  and  $2\omega_0-\omega_0$ . Furthermore, both second and third harmonic terminations define the  $v_{GS}(t)$  and  $v_{DS}(t)$  control voltage waveforms and so the overall PA drain efficiency. So, from the above identified harmonic terminations, the case  $Z_S(2\omega_0)=0$ ,  $Z_L(2\omega_0)=0$  and  $Z_S(3\omega_0)=0$ ,  $Z_L(3\omega_0)=0$  was selected, as it leads to more manageable analytical forms and has practical relevance corresponding to the common class B PA, and – because of the AM/AM and AM/PM invariance with the third harmonic terminations – it is also a good example of the distortion that should be expected from class F PAs.

Under these selected three quiescent points, and source and load impedance terminations, the  $F_{gk}$  and  $F_{dk}$  coefficients of (3.9) are shown in Fig. 3.5.

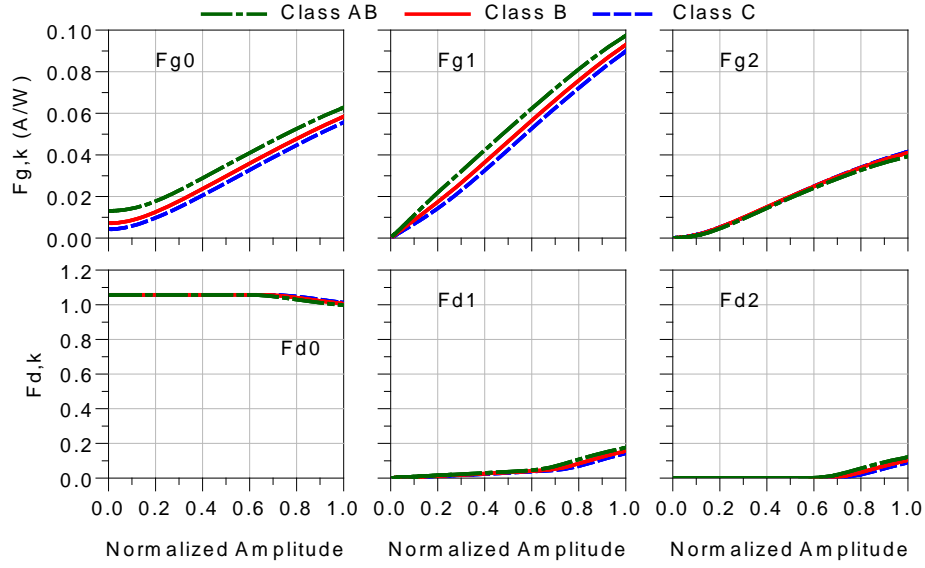


Fig. 3.5 – DC, fundamental and 2<sup>nd</sup> harmonic components of the normalized Si LDMOS time-varying  $f_g(v_{GS})$  (top figure) and  $f_d(v_{DS})$  (bottom figure).

$F_{g0}$ , the dc coefficient, starts at the quiescent current (imposed by the operation class), and as the amplitude  $A$  increases, tends asymptotically to the same constant slope obtained for class B.  $F_{g1}$  is the fundamental coefficient and determines the small-signal gain, which can be either compressive (at class AB bias), constant (at class B) or expansive (at class C). Once again, the slope of  $F_{g1}$  always tends asymptotically to the slope obtained at class B. Finally,  $F_{g2}$  is quite low for small-signal, showing a persistent increase with  $V_{GS}$  amplitude.

The  $F_{dk}$  components have the same shape for all operation classes and can only have impact on  $V_{ds1}$  whenever the  $v_{DS}$  excursion reaches the triode zone. Until then,  $F_{d0}$  is close to unity, and  $F_{d1}$  and  $F_{d2}$  are zero.

Considering the Fourier components' values shown in Fig. 3.5, it is clear that the product  $F_{g1} \cdot F_{d0}$  will be dominant in  $V_{ds1}$ . Actually, since  $F_{d0}$  is close to unity for small amplitudes,  $F_{g1}$  will determine the small-signal AM/AM. But, as the input amplitude increases, there is an  $F_{d0}$  reduction that, with  $F_{g0} \cdot F_{d1}$ , determines the PA gain compression. Hence, these two simple terms should be enough for accurately predicting the small-signal regime and to give a rough estimate of the large-signal AM/AM characteristic.

Fig. 3.6 presents the comparison between the AM/AM plots obtained by HB simulation of the complete PA circuit (identified as PA Gain) and the approximated model only including the nonlinear current source ( $I_{DS}$  Gain) (for the above three mentioned operation classes). Looking into the obtained approximation, it is clear that  $i_{DS}(v_{GS}, v_{DS})$  will indeed be the main source of AM/AM. Nevertheless, if a full description of this nonlinear

distortion amplitude characteristic is desired, it is necessary to include in the model the nonlinear capacitances, as it will be done latter on.

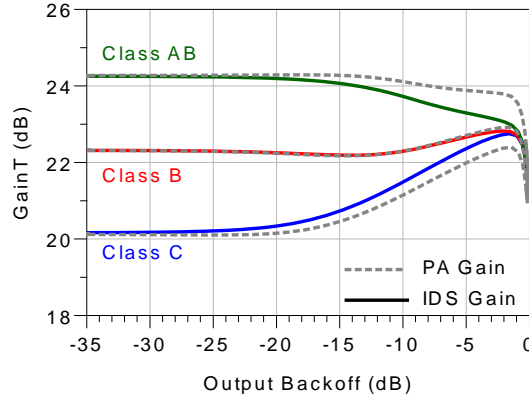


Fig. 3.6 – Simulated and predicted AM/AM characteristics for three different operation classes of a Si LDMOS based PA. The slight differences between the complete PA AM/AM (PA Gain) and the one induced by the drain-source current nonlinearity ( $I_{DS}$  Gain) were attributed to the input capacitance variations.

Since both  $f_g(v_{GS})$  and  $f_d(v_{DS})$  are static nonlinearities, the phase of their corresponding Fourier coefficients can only be either 0 or 180°. So, as shown by (3.9), the only case in which the  $i_{DS}(v_{GS}, v_{DS})$  nonlinearity can generate any AM/PM is when the PA is terminated by a complex load impedance,  $Z_L(\omega_0)$ , and the device is driven to compression. In fact, in the small-signal regime,  $f_d(v_{DS}) = 1$ , the distortion components are independent of the load impedance, and the output drain-source current will always be in opposite phase to the input gate-source voltage, regardless of the excitation drive level. However, under large-signal gain compression, the product  $F_{g0} \cdot F_{d1}$  will be phase-shifted with respect to the dominant  $F_{g1} \cdot F_{d0}$ , and the PA will evidence AM/PM.

If  $Z_L(\omega_0)$  is inductive, i.e., has a positive phase lead of  $\theta$ , both  $V_{ds1}$ ,  $F_{d1}$ , and thus  $F_{g0} \cdot F_{d1}$ , will have a phase of  $180^\circ + \theta$ . So, when this distortion component is added to the signal component  $F_{g1} \cdot F_{d0}$ , it produces an amplitude dependent phase-shift that is negative, and the PA has a phase-lagging AM/PM.

Using a similar reasoning, it is straightforward to conclude that, when  $Z_L(\omega_0)$  is capacitive, the PA presents a positive amplitude-dependent phase-shift, i.e., a phase-leading AM/PM.

### 3.2.3 $C_{gs}(v_{GS})$ and $C_{gd}$ Induced AM/PM Distortion

Before starting with the analysis of the nonlinear capacitance induced distortions, it should be noted that, rigorously speaking, and as was described in [37], [38] the  $C_{gd}$  nonlinearity is not referring to the actual  $C_{gd}$  variation with excitation amplitude, which was found negligible. This nonlinearity arises from the input and output Miller reflections that

are directly dependent on the FET's nonlinear voltage gain – the essential mechanisms responsible for the PA's AM/AM.

Similarly to what was done for the  $i_{DS}(v_{GS}, v_{DS})$  nonlinearity, and according to the methodology above described, the Fourier components of  $C_{gs}[v_{GS}(t)]$  study will also be performed, considering that  $v_{GS}(t)$  is again a periodic waveform of amplitude  $A$ , namely,  $C_{gs0}(A)$ ,  $C_{gs1}(A)$ , and  $C_{gs2}(A)$ . As these have their physical origin in the FET's gate-channel accumulated charge, they must be intrinsically related to the  $f_g(v_{GS})$  function responsible for  $F_{g1}(A)$  [72], [94]. So,  $C_{gs}$  induced AM/PM distortion must again be related to the observed PA small-signal AM/AM conversion.

To quantify these effects, let us start with the equations that give the fundamental and second harmonic of  $v_{GS}(t)$  voltage as a function of the voltage dependent  $C_{gs}[v_{GS}(t)]$  Fourier components, and the input reflected  $C_{gd}$  Miller capacitance, using products up to the second harmonic. Analysing the input mesh of the simplified PA equivalent circuit of Fig. 3.4, it is concluded that

$$V_{gs1} \approx V_S(\omega_0) - j\omega_0 Z_S(\omega_0) \left\{ [C_{gs0} + C_{gd}(1 - A_{v1})] \cdot V_{gs1} - \frac{C_{gs2}}{2} V_{gs1}^* + C_{gs1}^* \cdot V_{gs2} \right\} \quad (3.17)$$

and

$$V_{gs2} \approx -j2\omega_0 Z_S(2\omega_0) \left\{ \frac{C_{gs1}}{4} V_{gs1} + [C_{gs0} + C_{gd}(1 - A_{v2})] \cdot V_{gs2} \right\} \quad (3.18)$$

where, for notation simplicity, the Fourier components' dependence on the input amplitude  $A$  was implicitly assumed and so not explicitly expressed. Thus, solving for the fundamental  $V_{gs1}$  voltage component, leads to:

$$V_{gs1}(A) \approx \frac{V_S(\omega_0) + j\omega_0 Z_S(\omega_0) \cdot \left[ \frac{1}{2} C_{gs2} \cdot V_{gs1}^* - C_{gs1}^* \cdot V_{gs2} \right]}{1 + j\omega_0 Z_S(\omega_0) [C_{gs0} + C_{gd}(1 - A_{v1})]} \quad (3.19)$$

This expression reveals that both  $C_{gs}$  and  $C_{gd}$  will lead to an input AM/AM, but mostly AM/PM distortion, that will be as significant as the gate input matching is resonant and high quality factor,  $Q$ .

In order to identify and describe how the PA's main equivalent circuit elements determine the nonlinearity associated with the fundamental gate-source voltage,  $V_{gs1}(A)$ , the study of the various terms variation of (3.19) versus the input drive level will now be studied, for the same three quiescent points and short-circuit terminations previously considered for the  $i_{DS}(v_{GS}, v_{DS})$  nonlinearity.

Starting with the contribution of  $C_{gs}(v_{GS})$  nonlinearity, Fig. 3.7 a) shows how  $C_{gs0}$  varies with the input amplitude for each operation class. In the small-signal regime,  $C_{gs0}$  has no variation. However, as  $A=|V_{gs1}|$  is raised towards large-signal,  $C_{gs0}$  decreases when the transistor is biased for class AB and increases for class C. The value of  $C_{gs0}$  is almost constant for class B, because, there,  $C_{gs}(v_{GS})$  (as well as the FET's transconductance) presents an almost perfect odd-symmetry. In the asymptotic and very large-signal regime, the value of  $C_{gs0}$  is equal for all operations classes because  $C_{gs}[v_{GS}(t)]$  tends to a square wave. In addition to these observations, it was found that the higher order harmonic components of  $C_{gs}(t)$ , namely  $C_{g1}$  and  $C_{g2}$ , have a negligible impact when compared with the  $C_{gs0}$  contribution.

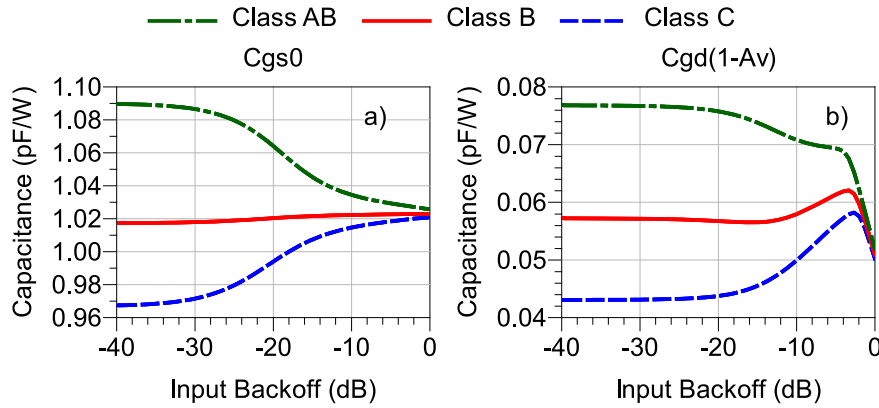


Fig. 3.7 – Shapes of  $C_{gs0}(A)$  component of the LDMOS nonlinear normalized  $C_{gs}$  and normalized input Miller reflected capacitance  $C_{gd}$ .

On what  $C_{gd}$  is concerned, Fig. 3.7 b) shows that the input Miller reflected  $C_{gd}$  is so small in comparison to  $C_{gs0}$  (at least 10 times smaller), that the effect of this feedback capacitance is, for this Si LDMOS device, almost negligible.

### 3.2.4 $C_{ds}(v_{DS})$ Induced AM/PM Distortion

Finally, the analysis will now be focused on the nonlinear  $C_{ds}$  capacitance.

Looking back onto the drain-source output mesh nonlinearity of Fig. 3.4, it is possible to derive the fundamental and second harmonic of  $v_{DS}(t)$  voltage as a function of the voltage dependent  $C_{ds}[v_{DS}(t)]$ , (3.20) and (3.21), respectively. Once again, only products up to the second harmonic were considered.

For evaluating the relative impact that each of the terms of (3.20) has on  $V_{ds1}$ , they were represented versus the input drive level assuming, once again, the same three quiescent points and the short-circuit terminations at all harmonics. Fig. 3.8 shows this variation for  $C_{ds0}$  and  $C_{ds2}$ , where it is possible to see their lack of sensitivity to the operation class, something already expected since  $C_{ds}$  is only a function of  $v_{DS}$ . Besides

that, as the input drive increases, their values suffer a steady rise beyond about -10 dB back off, a consequence of the output excursion swing approaching the FET's triode region, as can be inferred by the direct observation of Fig. 3.3 b).

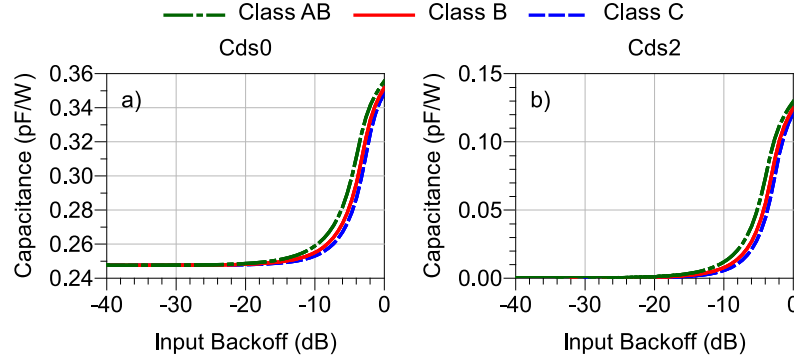


Fig. 3.8 – Shapes of  $C_{ds0}(A)$  and  $C_{ds2}(A)$  components of the normalized LDMOS nonlinear  $C_{ds}$ .

$$V_{ds1} \approx \left\{ j\omega_0 Z_L(\omega_0) \left[ \frac{C_{ds2}}{2} V_{ds1}^* - C_{ds1}^* V_{ds2} \right] - Z_L(\omega_0) I_{ds1} \right\} \times \left\{ 1 + j\omega_0 Z_L(\omega_0) \left( C_{ds0} + C_{gd} \left( \frac{A_{v1} - 1}{A_{v1}} \right) \right) \right\}^{-1} \quad (3.20)$$

$$V_{ds2} \approx \left\{ -j\omega_0 Z_L(2\omega_0) C_{ds1} V_{ds1} - Z_L(2\omega_0) I_{ds2} \right\} \times \left\{ 1 + j2\omega_0 Z_L(2\omega_0) \left[ C_{ds0} + C_{gd} \left( \frac{A_{v2} - 1}{A_{v2}} \right) \right] \right\}^{-1} \quad (3.21)$$

As can be seen from the inspection of the numerator of (3.20), Fig. 3.9, and of its denominator, Fig. 3.10, the relatively large values of  $C_{ds0}$  and  $C_{ds2}$  and of their variation have a significant impact on the LDMOS-PA AM/PM. In fact, a comparative analysis of each of the device AM/PM distortion components has shown that  $C_{ds}(V_{DS})$  is its major contributor, clearly dominating over  $C_{gd}$  or even  $C_{gs}(V_{GS})$ , see Fig. 3.11 a) and b). Consequently, a Si LDMOS based PA may have a mild small-signal AM/PM determined by  $C_{gs}(V_{GS})$ , but tends to evidence a pronounced phase-lagging AM/PM when the device enters the region of gain compression.

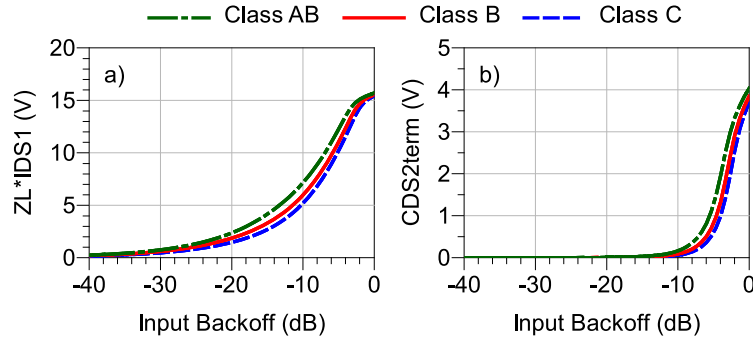


Fig. 3.9 – a) Resistive and b) reactive terms of the numerator of (3.20) for the normalized LDMOS nonlinear  $C_{ds}$ .

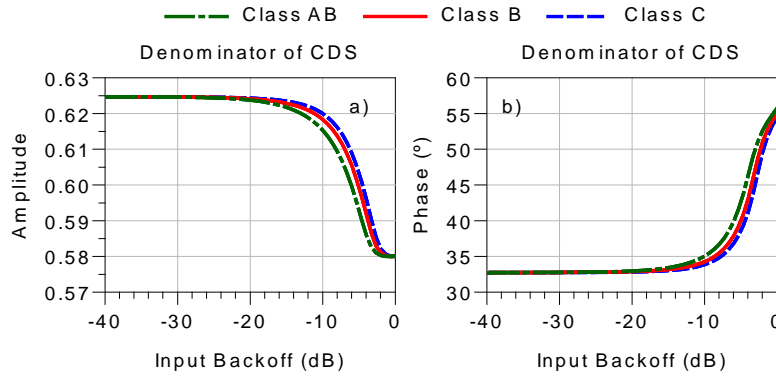


Fig. 3.10 – Amplitude and phase of the denominator of (3.20) for the normalized LDMOS nonlinear  $C_{ds}$ .

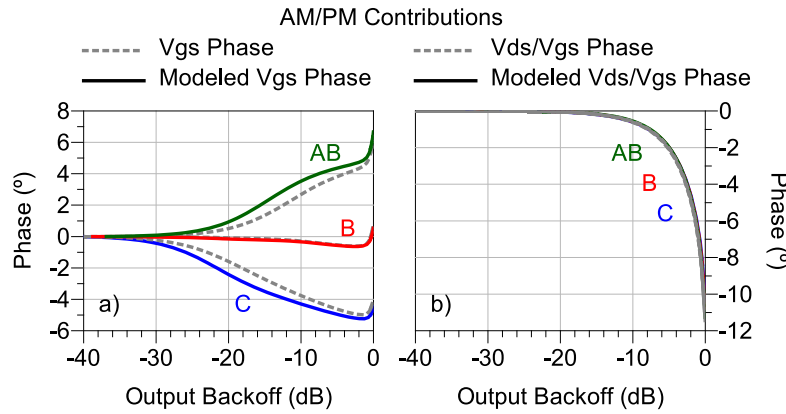


Fig. 3.11 – a) Model predicted (Modelled  $V_{gs}$  Phase) and HB simulated ( $V_{gs}$  Phase)  $C_{gs}$  and  $C_{gd}$  contributions and b) model predicted (Modelled  $V_{ds}/V_{gs}$  Phase) and HB simulated ( $V_{ds}/V_{gs}$  Phase)  $C_{ds}$  contribution to the overall Si LDMOS AM/PM.

Fig. 3.12 presents the overall PA, a) AM/AM and b) AM/PM, characteristics predicted via both a full HB simulation and by the proposed semi-analytical model. The obtained results are very good confirming the identified LDMOS based PA nonlinear distortion generation mechanisms and the above presented conclusions.

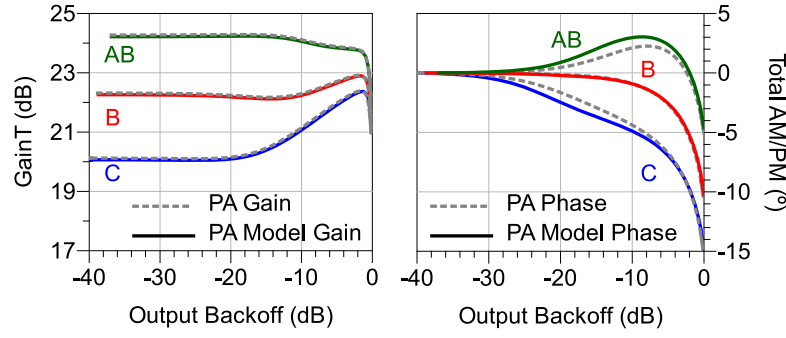


Fig. 3.12 – Overall a) AM/AM and b) AM/PM of the Si LDMOS based PA. Model predictions and HB simulations are shown as continuous or dashed lines, respectively.

### 3.3. AM/AM and AM/PM on a GaN HEMT BASED PA

#### 3.3.1 Equivalent Circuit Model of the GaN HEMT-PA

The topology of the GaN HEMT equivalent circuit model is equal to the one adopted for the Si LDMOS and depicted in Fig. 3.1. However, as is shown in Fig. 3.13 and Fig. 3.14, these normalized values, also extracted from a typical GaN HEMT device characterized in the lab, evidence significant differences when compared to their Si LDMOS counterparts. In fact, and contrary to the transconductance and output conductance profiles that resemble the ones already seen for the LDMOS, the GaN capacitances are smaller. To be precise, both GaN HEMT normalized  $C_{gs}(V_{GS})$  and, in particular,  $C_{ds}(V_{DS})$ , are smaller than the ones already seen for the Si LDMOS, but  $C_{gd} = 23 \text{ fF/W}$  is considerably larger.

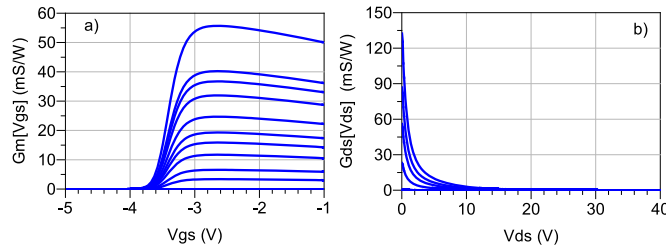


Fig. 3.13 – GaN HEMT a) normalized transconductance  $G_m(V_{GS})$  and b) normalized output conductance  $G_{ds}(V_{DS})$  profiles derived from the adopted  $i_{DS}(V_{GS}, V_{DS})$  model.

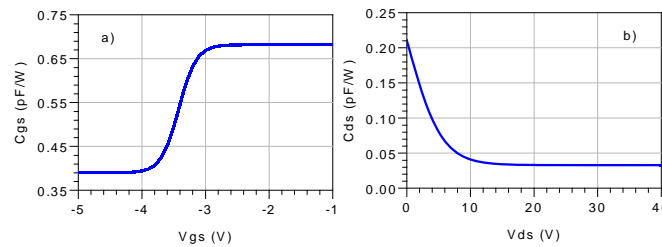


Fig. 3.14 – GaN HEMT normalized a) gate-source capacitance  $C_{gs}(V_{GS})$  and b) drain-source capacitance  $C_{ds}(V_{DS})$  modelled profiles obtained from measured data.

Hence, although it should be expected that the GaN HEMT and the Si LDMOS based PAs have similar AM/AM distortion, significant differences in their AM/PM characteristics are to be expected.

### 3.3.2 $i_{DS}(v_{GS}, v_{DS})$ Induced AM/AM and AM/PM Distortions

As was done for the Si LDMOS, Fig. 3.15 depicts the normalized GaN HEMT  $F_{gk}$  and  $F_{dk}$  Fourier coefficient variations with amplitude drive level, for three distinct bias points, illustrative of class C, B and AB operation.

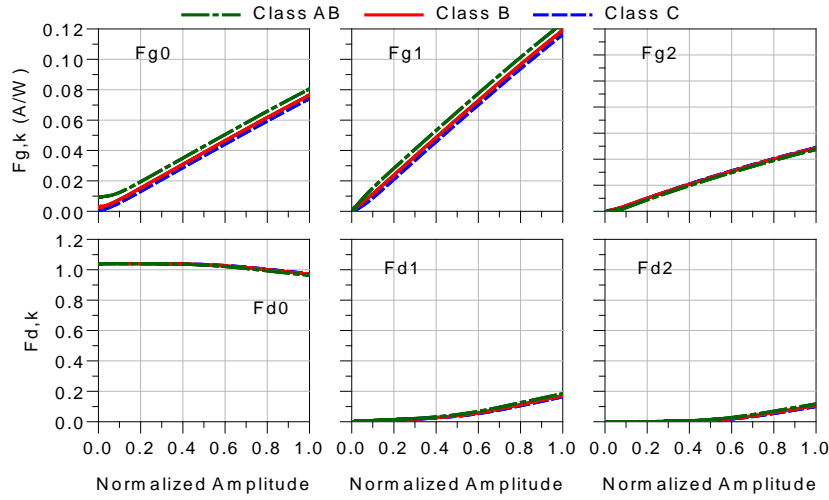


Fig. 3.15 – dc, fundamental and 2nd harmonic components of the GaN HEMT normalized time-varying  $f_g(v_{GS})$  and  $f_d(v_{DS})$ .

Similarly, Fig. 3.16 shows the corresponding  $i_{DS}(v_{GS}, v_{DS})$  induced amplitude distortion contribution, making it clear, once again, that it constitutes the major contributor to the PA AM/AM characteristic. The presented differences between both curves are due to the input capacitance [ $C_{gs0}(A)$  and input Miller reflected  $C_{gd}$ ] variation.

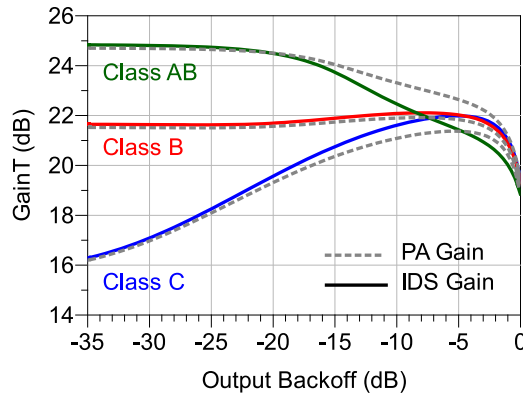


Fig. 3.16 – Simulated and predicted AM/AM characteristics for three different operation classes of a GaN HEMT based PA. The differences between the complete PA AM/AM (PA Gain) and the one induced by the drain-source current nonlinearity ( $I_{DS}$  Gain) are due to the input capacitance variations.

As expected, the evident similarity of Fig. 3.16 with Fig. 3.6 is a direct consequence of the similarity between Fig. 3.15 and Fig. 3.5, and ultimately, between Fig. 3.13 and Fig. 3.2. As a matter of fact, the analogous AM/AM shapes of these two PA technologies is a direct consequence of the similar internal behaviour of their active device's  $i_{DS}(V_{GS}, V_{DS})$ , which has justified the use of the same behavioural model formats [34].

### 3.3.3 $C_{gs}(V_{GS})$ and $C_{gd}$ and $C_{ds}(V_{DS})$ Induced AM/PM Distortion

Moving on to study the impact of the GaN HEMT capacitances, it is found that, contrary to what was seen for the Si LDMOS, GaN HEMT's  $C_{ds0}$  and  $C_{ds2}$  variations with the input drive level, shown in Fig. 3.17, lead to an almost constant (unity) denominator of (3.20) and also a negligible impact on its numerator. This means that the GaN HEMT based PAs will have their AM/PM almost completely determined by the input matching network detuning.

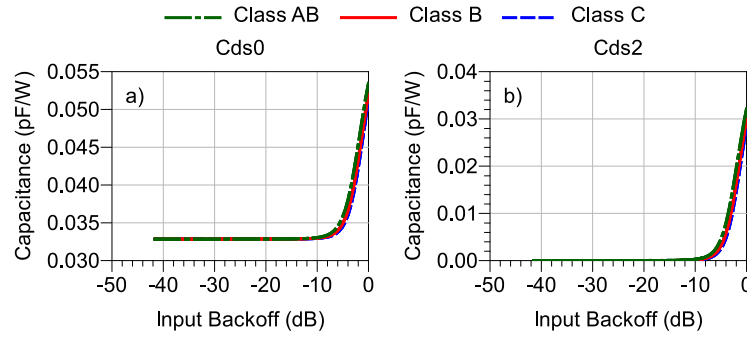


Fig. 3.17 – Shapes of  $C_{ds0}(A)$  and  $C_{ds2}(A)$  components of the normalized GaN HEMT nonlinear  $C_{ds}$ .

Regarding the  $C_{gs}(V_{GS})$  and  $C_{gd}$  capacitances, Fig. 3.18 a) and b) show that, now, the input Miller reflected  $C_{gd}$  variation is comparable to  $C_{gs0}$  shift, which determines a more relevant effect of this feedback capacitance.

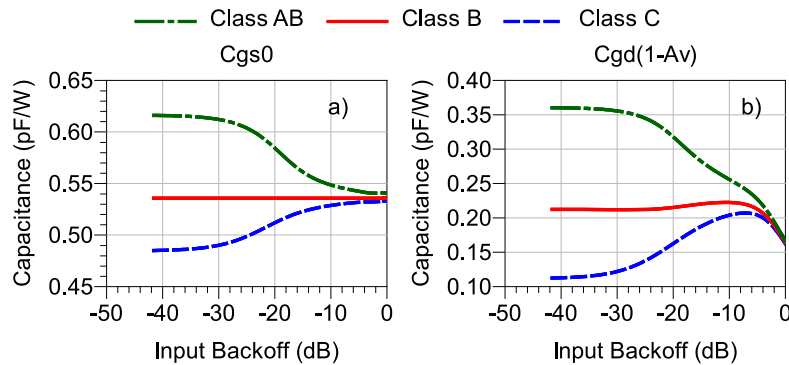


Fig. 3.18 – Shapes of  $C_{gs0}(A)$  component of the GaN HEMT nonlinear normalized  $C_{gs}$  and of the normalized input Miller reflected capacitance  $C_{gd}$ .

In addition, and as was already discussed, the input-reflected  $C_{gd}$  capacitance is directly related to the voltage gain, as is attested by the similarity of  $C_{gd}(1-A_v)$  patterns of Fig. 3.18 b) and the PA gain variations of Fig. 3.16. If this gain expands,  $C_{gd}(1-A_v)$  increases, whereas if the gain compresses,  $C_{gd}(1-A_v)$  also decreases. Therefore, and in a clear opposition to what was concluded for the AM/PM of Si LDMOS based PAs, where the AM/PM was almost always of the phase-lagging type, in GaN HEMT based PAs the AM/PM tends to be opposite to the AM/AM shape, revealing an inherent internal relationship between these two different forms of nonlinear distortion [95].

### 3.4. Experimental Validation

In order to provide an illustrative experimental validation of the proposed model, which could confirm the identification of the nonlinear distortion generation mechanisms and the semi-analytical model previously presented, two off-the-shelf power amplifiers were selected, one using a 200 W Si LDMOS transistor (operating at 1.8 GHz) and another one using a 15 W GaN HEMT device (operating at 0.9 GHz). Fig. 3.19 and Fig. 3.20 present the simplified layout structure of both of these PAs.

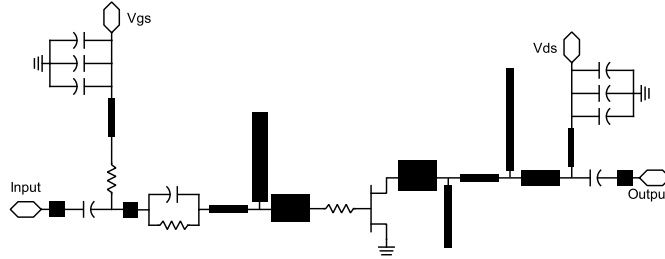


Fig. 3.19 – Layout of the implemented and tested 15 W, 900 MHz, GaN HEMT power amplifier prototype.

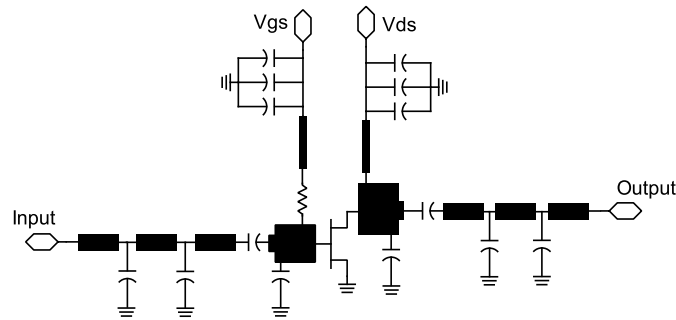


Fig. 3.20 – Layout of the implemented and tested 200 W, 1800 MHz, Si LDMOS power amplifier prototype.

Due to efficiency reasons, the GaN HEMT based PA has an input matching network that presents a nearly short-circuit to both the second and third harmonics, and a class-F output network up to the third harmonic, (i.e., nearly a short-circuit and an open-circuit to the second and third harmonics, respectively). On what the Si LDMOS PA is concerned,

and since it is a very large pre-matched device whose pre-matching networks have a low-pass characteristic, it is almost insensitive to either any source or load harmonic impedance variations present at its terminals (i.e., the intrinsic harmonic terminations are fixed).

Fig. 3.21 and Fig. 3.22 show overall AM/AM and AM/PM characteristics for the GaN HEMT (already presented in [95] with more quiescent points) and Si LDMOS based PAs, respectively. On both figures, it is possible to identify three sets of curves: (i) laboratory measurements; (ii) HB simulations using a full circuit-level nonlinear model, and (iii) predictions using the semi-analytical model.

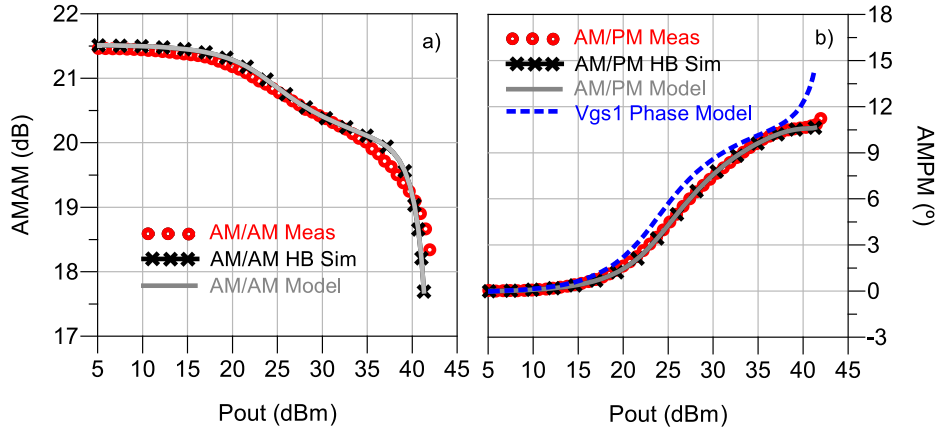


Fig. 3.21 – a) AM/AM and b) AM/PM characteristic from lab measurements, HB simulation of a circuit-level model and predictions from the proposed semi-analytical model for the GaN HEMT based PA. For comparison purposes, fundamental gate-source voltage phase predicted by the proposed semi-analytical model is also plotted.

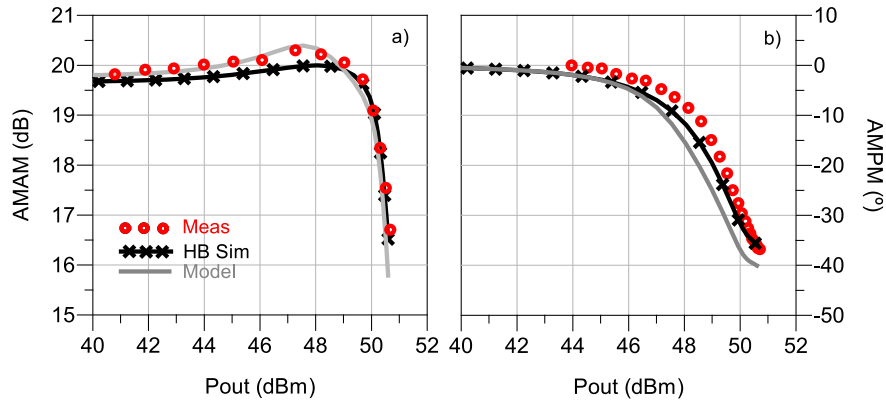


Fig. 3.22 – a) AM/AM and b) AM/PM characteristic from lab measurements, HB simulation of a circuit-level model and predictions by the proposed semi-analytical model for the Si LDMOS based PA.

For the GaN PA, the  $C_{ds}$  was considered linear, i.e.,  $C_{ds0}=C_{ds}$  and  $C_{ds1}=C_{ds2}=0$  in (3.20) since its value was found so small that it could not produce any significant impact on the PA nonlinear distortion. In fact, this approximation is perfectly justified by the very

good agreement obtained between all measured, HB simulated and (3.20) predicted curves. Note that the slight differences between the measurements and the proposed model (which are more evident in deep compression) are already present in the circuit-level simulation. Hence, they are believed to be due to a deficient modelling of the  $i_{DS}(V_{GS}, V_{DS})$  triode region or to a possible manifestation of the GaN HEMT long-term memory effects [85]. However, even more significant is the pattern similarity registered between the AM/AM and AM/PM curves shown in Fig. 3.21 a) and b), respectively, which confirms the internal relationship between these two distortion characteristics theoretically advanced in Section 3.3. In Fig. 3.21 b), also the fundament gate-source voltage phase given by (3.19) is shown, which confirms that most of the AM/PM distortion of a GaN based PA is indeed generated on the FET's input side, due to the variation of the  $C_{gs0}$  and the  $C_{gs}(1-A_v)$ . Actually, the main differences verified between the overall AM/PM and the  $V_{gs1}$  phase are only observed in the compression zone, where the amplifier distortion becomes also dependent on the  $v_{DS}$  voltage variation (in this region, if the load impedance presents an important imaginary part there will be a non-negligible phase shift, as was explained in the previous sections).

Regarding the Si LDMOS PA, and as was predicted,  $i_{DS}(V_{GS}, V_{DS})$  and  $C_{ds}(V_{DS})$  were found to be the dominant AM/AM and AM/PM nonlinear distortion generation mechanisms, respectively. Accordingly, there is also a very good agreement between all measured, HB simulated and (3.20) predicted AM/AM and AM/PM curves shown in Fig. 3.22 a) and b), respectively. The observed differences could be overcome if higher order harmonics were further included in the proposed model.

These results prove the practical usefulness of the proposed semi-analytical model and the identification of the PAs' AM/AM and AM/PM nonlinear distortion generation mechanisms for both PA technologies. They also confirm the expected differences between the AM/AM and AM/PM characteristics of both GaN HEMT and Si LDMOS based PAs discussed throughout the paper.

### 3.5. Summary

In this chapter, the AM/AM and AM/PM nonlinear distortion generation mechanisms in both Si LDMOS and GaN HEMT based single-ended power amplifiers were presented and explained. The transistor nonlinear drain-source current was confirmed to be the major contributor to the AM/AM, while the AM/PM distortion was determined by, either the output nonlinear capacitance, in Si LDMOS devices, or by the FET's input impedance variation due to the nonlinear gate-source and the input Miller reflected gate-drain

capacitances, in GaN HEMTs. Besides these major distortion contributors, it was also shown that the device's load impedance can be an additional source of AM/PM conversion whenever the output matching is out of resonance.

The derived AM/AM and AM/PM semi-analytical large-signal model uncovered the physical connection between all these distortion generation mechanisms and proved to be effective for predicting both the AM/AM and AM/PM characteristics of both a Si LDMOS and a GaN HEMT based PA.

In this model, there is a trade-off between accuracy and simplicity. If, on one hand, very precise results are needed, like the ones obtained with HB simulators, a large number of harmonic components of the time-varying nonlinear elements' Fourier expansions (increasing complexity) will be needed. This will make the identification and understanding of the major nonlinear distortion generation mechanisms more difficult. However, if, on the other hand, the objective is only to identify the main nonlinear distortion generation mechanisms, then the model complexity can be reduced, obtaining a rough estimate of the overall PA behaviour.



## 4. Nonlinear Distortion Generation Mechanisms of the Overall Doherty Amplifier

With the identification of the main nonlinear distortion generation mechanisms of a single-ended PA operating in class AB and class C, the two basic cells of the Doherty arrangement, it is possible to study the Doherty nonlinear distortion, which is exactly the main objective of this chapter. In addition, it is also performed a study of the Doherty efficiency peaks dependency on the back-off power levels.

### 4.1. Theoretical Analysis of a 2-way Doherty PA and its Limitations

Theoretically, the equivalent schematic of an ideal 2-way Doherty PA can be represented as shown in Fig. 4.1, where  $R_{opt}$  is the load that maximizes the carrier and peaking PAs' output power. Both PAs are assumed to be ideal current sources (without any nonlinear or linear intrinsic capacitances),  $I_C(t) = jG_m V_{gs}(t)/2$  and  $I_P(t) = -j\alpha I_C(t)$ , respectively, being  $G_m$  the transconductance of the transistors,  $V_{gs}$  their input envelope controlling voltage and  $\alpha = |I_P|/|I_C|$  the peaking-to-carrier current ratio.

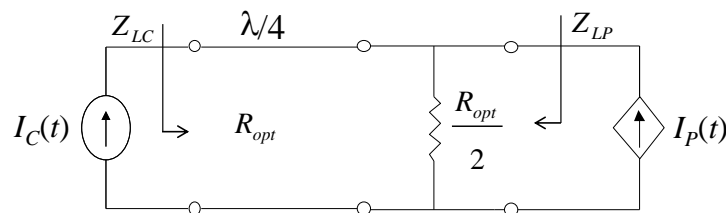


Fig. 4.1 – Equivalent schematic of an ideal 2-way Doherty PA.

It is possible to further simplify this schematic by considering the carrier PA current source Thevenin equivalent calculated after the quarter-wave transmission line,  $V_{Th} = -jR_{opt}I_C(t)$  and  $Z_{Th} = 0$ , resulting in the schematic of Fig. 4.2.

The dynamic load impedances seen by the carrier and peaking PAs can be given by  $Z_{LC} = (2 - \alpha)R_{opt}$  and  $Z_{LP} = R_{opt}/\alpha$ , respectively. For low input powers, the peaking current is equal to zero and for large signal it equals the carrier current. Therefore, the load

impedances presented to the carrier and peaking PAs are always real, varying from  $2R_{opt}$  to  $R_{opt}$  for the carrier PA, and from infinity to  $R_{opt}$  for the peaking PA.

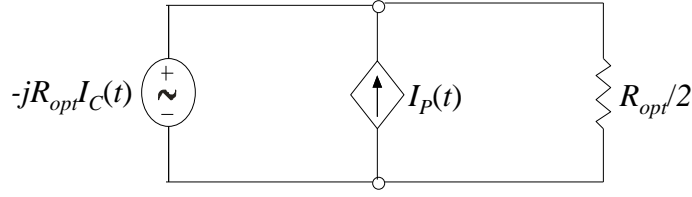


Fig. 4.2 – Simplification of the equivalent circuit schematic presented in Fig. 4.1.

It should be noted that, if the carrier PA current source has no internal conductance, it becomes an ideal voltage source in parallel with the peaking PA and the load. This causes the so-called peaking PA suppression – i.e., the distortion of the ideal 2-way Doherty is determined by the carrier PA – turning the Doherty configuration as linear as its carrier PA.

However, according to the knowledge obtained from the single-ended nonlinear distortion analysis presented in previous Chapter, practical implementations of the carrier and peaking PAs exhibit nonlinear AM/AM and AM/PM distortions. Actually, the class B carrier PA already presents distortion even before reaching the triode-zone saturation limit, since the real transistors do not present an abrupt saturation to triode zone and turn-on transitions. This is further aggravated by the insufficient load modulation provided by the class C peaking PA, which does not turn-on abruptly as would be expected from a class B PA piecewise linear current characteristic.

Furthermore, the transistors also have intrinsic capacitances that are sources of nonlinear distortion, namely of AM/PM. In Chapter 3, it was founded that the AM/PM in a PA based on GaN HEMTs is mostly determined by the phase-shift in the fundamental gate-source voltage, due to the variation of the input Miller equivalent  $C_{gd}$ ,  $C_{gd,Miller}(A) = C_{gd}(1-A_v)$ . Therefore, since the AM/AM is strongly related with the voltage gain,  $A_v$ , when it expands,  $C_{gd,Miller}$  increases, producing phase-lagging, whereas a gain compression imposes a  $C_{gd,Miller}$  reduction imposing a phase-leading curve. Consequently, the AM/PM tends to be opposite to the AM/AM characteristic for single-ended PAs and so, these two characteristics are strongly entangled.

On what the PAs based on Si LDMOS are concerned, the AM/PM distortion is mostly determined by nonlinear output capacitance, producing a pronounced phase-lagging AM/PM when the device enters the region of gain compression.

From the above observations, it could be expected that either Doherty PA based on GaN HEMTs would not show any significant AM/PM – unless the peaking PA suppression was inactive and thus allowing the peaking AM/PM distortion to be dominant – or the

Doherty PA based on Si LDMOS present always a phase-lagging AM/PM characteristic. However, as it will be presented next, the same conclusions derived from single-ended PAs nonlinear distortion cannot be directly applied to the Doherty distortion analysis.

## 4.2. Nonlinear Distortion of a Doherty PA

The Doherty operation can be usually divided in three distinct zones, as it is illustrated in Fig. 4.3.

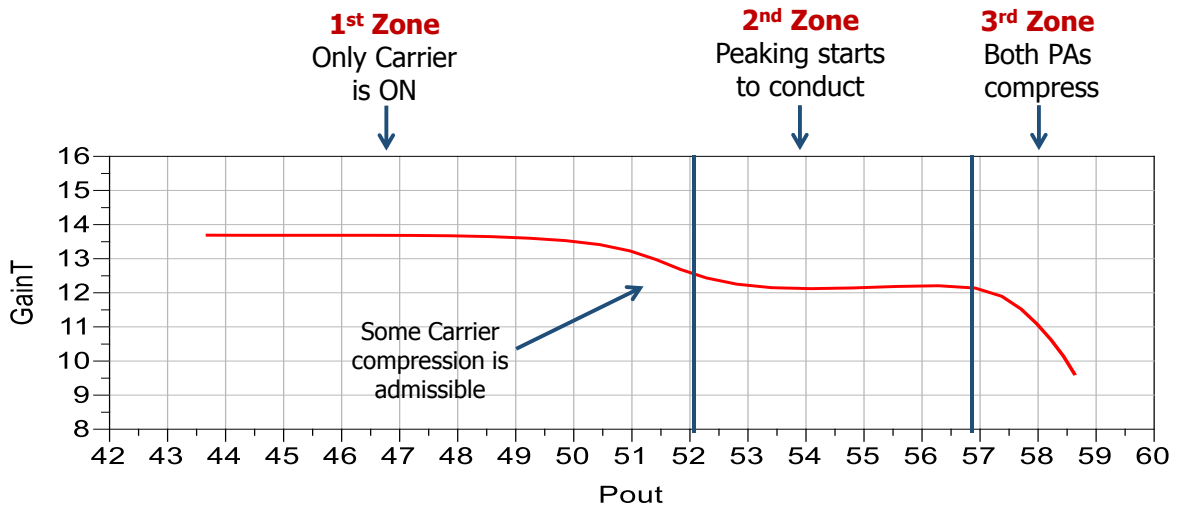


Fig. 4.3 – Typical AM/AM of a Doherty PA with three different operation zones well defined.

For low power regimes, the carrier PA works as a single-ended amplifier terminated with an impedance that maximizes the efficiency for the desired power back-off where the Doherty has the first efficiency peak. This impedance (at small-signal) is imposed by the passive combiner (which includes the OMNs) and by the peaking PA off output admittance,  $Y_{22off}$ . Therefore, in this zone, the conclusions derived to single-ended PAs in terms of nonlinear distortion are also valid for the Doherty.

For mid-power region, the carrier PA begins to operate at a constant output voltage and the peaking provides the necessary current to ensure a flat AM/AM curve. It is in this region that the Doherty has its main advantage over conventional amplifiers in terms of efficiency characteristics, since it presents a high efficiency for a certain power back-off level.

Finally, in the last region, both amplifiers saturate and, in order to obtain the maximum output power that the transistors are capable to provide, the load impedance presented to both PAs must end in the load that maximizes the output power. For that, it is normal to use a device for the auxiliary device twice as large as the one used in the main

PA or different division ratios of the input signal for the main and the auxiliary PAs to produce the necessary  $I_P$  current and thus the desired dynamic load modulation effect.

On what Doherty AM/PM distortion is concerned, in the mid-power region, the  $Z_C$  and ZP starts to depend on the load modulation ratio,  $\alpha = I_P/I_C$ , and since the peaking and carrier PA currents are added in magnitude and phase in the output combiner, as is illustrated in Fig. 4.4, significant phase difference between these currents is responsible for a larger DHT-PA AM/PM distortion, reduced output power (AM/AM distortion) and non-optimal load-modulation. Therefore, it is essential to optimize the output combiner (which includes the OMNs) as well as the input offset lines, to set appropriate a carrier-peaking PAs phase relationship.

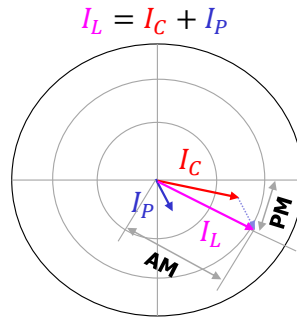


Fig. 4.4 – Illustration of the Doherty carrier and peaking PAs currents combined in magnitude and phase.

In addition to this AM/PM distortion, the nonlinear interaction between the carrier and peaking amplifiers in the Doherty operation along with their inherent nonlinear distortion mechanisms also introduces other AM/PM contributions for the overall Doherty distortion. Since the single-ended power amplifiers based on GaN HEMT and Si LDMOS devices present distinct main sources of AM/PM, these nonlinear distortion contributions to Doherty PAs based on these two device technologies are presented separately in the following two sub-section.

#### 4.2.1 AM/PM Distortion in GaN HEMT Doherty Power Amplifiers

In the above mentioned mid-power region, the AM/AM and AM/PM entanglement observed in GaN HEMT single-ended PAs is broken. In this region, the carrier PA presents a constant output voltage, resulting in a high voltage gain compression and, consequently, in a strong phase-leading characteristic due to the high input  $C_{gd,Miller}$  variation, as shown in (3.19). On the other hand, since the peaking PA output node coincides with the overall Doherty PA output, the peaking voltage gain will be as constant as the overall Doherty gain. Consequently,  $C_{gd,Miller}$  impact on the AM/PM distortion

induced by the peaking PA will be negligible and, thus, the overall Doherty AM/PM will be mostly determined by the carrier PA input phase variation.

In order to demonstrate this, two conceptual Doherty PAs were designed and simulated with: (i) unequal power division; (ii) appropriate quiescent point selection for both carrier and peaking PAs (assuring the needed load modulation); (iii) AM/AM variation below 1 dB.

In the first simulated Doherty PA, say PA-I, the carrier and peaking device equivalent circuits were only composed by a nonlinear  $i_{DS}(V_{GS}, V_{DS})$  current source and by nonlinear  $C_{gs}$  and  $C_{ds}$  capacitances. In the second simulated Doherty PA, PA-II, a linear  $C_{gd}$  capacitance was included in both the carrier and peaking PA device models. In order to keep the simulations physically meaningful, typical GaN HEMT element values were selected. The obtained Doherty AM/AM and AM/PM characteristics for both PAs are shown in Fig. 4.5.

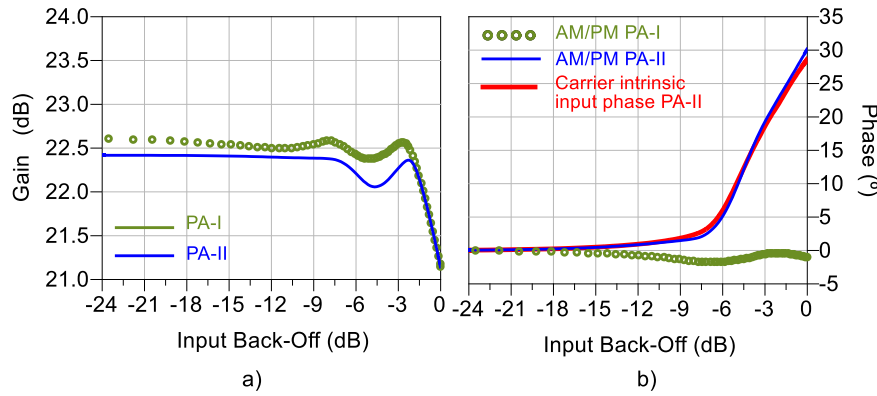


Fig. 4.5 – a) Simulated transducer power gain and b) AM/PM characteristics of both DPAs. For comparison purposes, fundamental gate-source intrinsic voltage phase of the carrier PA-II is also plotted.

In the first simulated Doherty PA (PA-I), both AM/AM and AM/PM characteristics are almost flat. There is only a slight compression in the AM/AM characteristic for large input power drive for optimized efficiency. On the other hand, although the simulated DPA (PA-II) still presents a more or less flat AM/AM characteristic, identical to the first one, it presents a strongly nonlinear AM/PM curve. This severe phase variation, noticed when the  $C_{gd}$  capacitance was included in the carrier and peaking transistor models of the second Doherty PA, clearly indicates that the main contributor to the AM/PM distortion of a Doherty PA based on GaN HEMT devices is the  $C_{gd}$  capacitance.

In order to further demonstrate the influence of the  $C_{gd}$  capacitance on the AM/PM distortion, through its associated input reflected Miller capacitance variation, the carrier PA intrinsic voltage gain was plotted in Fig. 4.6 a) and the correspondent input impedance variation in Fig. 4.6 b). Although the voltage gain,  $A_v$ , is almost constant until -6 dB of input

power back-off, it presents a very hard compression after that. This is due to the load impedance reduction presented to the carrier PA, and induced by the peaking PA, that determines the constant voltage operation of the carrier PA.

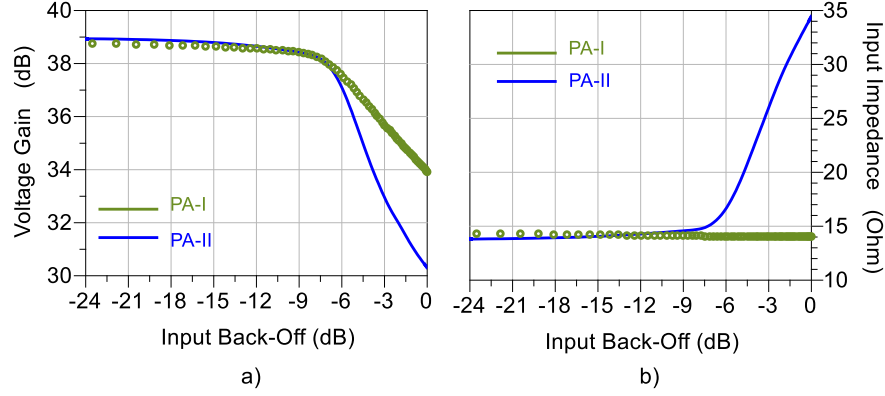


Fig. 4.6 – a) Simulated voltage gain characteristic of the carrier PA and b) correspondent input impedance variation, of both DPAs.

In the second Doherty PA, this voltage gain compression causes a large variation of the input impedance due to the reduction of the input reflected  $C_{gd, Miller}$  capacitance value – producing a further gain compression due to an input mismatch –, which imposes the observed phase variation. On the other hand, in the first DPA (as its device models do not have any  $C_{gd}$  capacitance), there is only a slight variation of the input impedance due to the nonlinear  $C_{gs}$ , which leads to a negligible phase variation.

Therefore, the main conclusion that can be drawn from this analysis is that the overall Doherty AM/PM distortion is mostly induced by the carrier PA input phase variation, as shown in Fig. 4.5 b). Moreover, in a DPA, the class B biased carrier PA suffers a voltage gain reduction much harder than its corresponding single-ended operation power gain. Conversely, the class C biased peaking PA shows a voltage gain that is flatter than what would be expected from a similar PA, but operated as a single-ended amplifier. So, the DPA AM/PM distortion will be significantly different from what would be expected from its single-ended carrier and peaking PAs.

In order to experimentally verify the nonlinear distortion induced by  $C_{gd}$  on the Doherty arrangement, a 900 MHz Doherty amplifier prototype was designed using Cree's CGH35015F (15W GaN HEMT) transistors for both carrier and peaking PAs. Unequal power division was used to obtain the necessary load modulation. A photograph of the actual prototype is shown in Fig. 4.7.

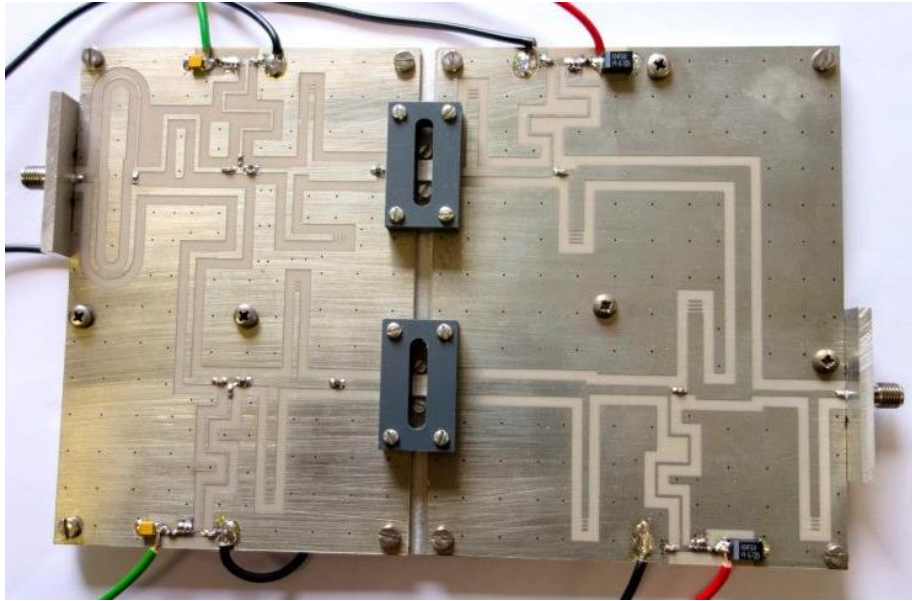


Fig. 4.7 – Photograph of the implemented and tested 900MHz, GaN Doherty PA prototype.

Fig. 4.8 presents the measured and simulated AM/AM and AM/PM characteristics of the implemented Doherty PA, where it is possible to see a remarkable agreement between both curves.

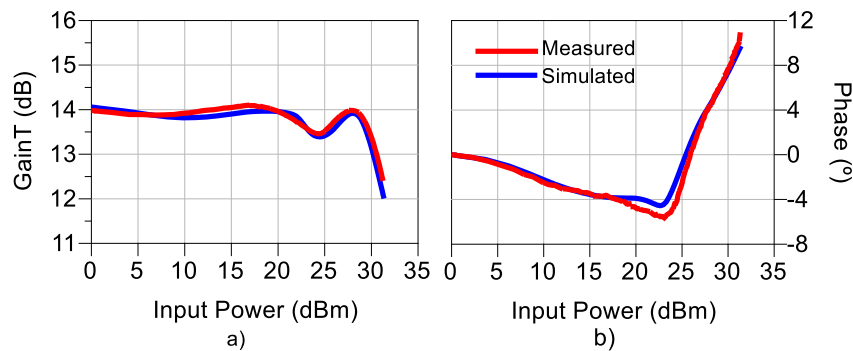


Fig. 4.8 – Measured and simulated a) AM/AM and b) AM/PM characteristics of the implemented Doherty Power Amplifier prototype.

In accordance to what was previously explained, the Doherty PA presents a good AM/AM performance whereas, in terms of the AM/PM characteristic, there is a strong nonlinear behaviour starting at 6 dB of input power back-off, exactly when the peaking enters into operation.

It should be noted that, for small input drive levels, where the peaking is off, the carrier is operating as a single-ended current-mode PA. Therefore, all nonlinear distortion appearing in both AM/AM and AM/PM curves must be induced by it. Consequently, the phase-lagging behaviour in the AM/PM characteristic for those low power levels can be due to a slight expansion of the carrier intrinsic voltage gain along with a non-perfect open

circuit presented by the peaking PA at the junction node where the currents of both amplifiers are added.

#### **4.2.2 AM/PM Distortion in Si LDMOS Doherty Power Amplifiers**

As mentioned in the single-ended nonlinear distortion analysis, the main contributor for AM/PM distortion of a power amplifier based on Si LDMOS is the nonlinear  $C_{ds}(v_{DS})$ , which clearly dominates over  $C_{gd}$  or even  $C_{gs}(v_{GS})$ , producing a pronounced phase-lagging AM/PM characteristic.

However, since the carrier PA presents a constant voltage excursion when the peaking PA enters into conduction, the average nonlinear  $C_{ds}(v_{DS})$  almost does not vary in this region. In addition, the impact of the input  $C_{gd,Miller}$  variation, due to the strong voltage gain compression observed in the Doherty operation, becomes comparable with the other capacitances. Consequently, in Si LDMOS Doherty power amplifiers it is expected that the AM/PM characteristic starts to present the normal phase-lagging behaviour due to the nonlinear  $C_{ds}(v_{DS})$  but, when the peaking enters into operation, it is expected a phase-leading behaviour due to the input  $C_{gd,Miller}$  variation.

Finally, when both the carrier and peaking PAs enter into the gain compression region, the voltage excursion at the carrier terminals is no longer constant, and so the  $C_{ds}(v_{DS})$  variation with its inherent phase-lagging behaviour is superimposed to the effect of the input  $C_{gd,Miller}$  variation.

In order to demonstrate this, similarly to what was done for the GaN HEMT Doherty nonlinear distortion analysis, three conceptual Doherty PAs were designed and simulated. In the first simulated Doherty PA, say PA-I, the carrier and peaking device equivalent circuits were only composed by a nonlinear  $i_{DS}(v_{GS}, v_{DS})$  current source and by nonlinear  $C_{gs}$  and  $C_{ds}$  capacitances. In the second simulated Doherty PA, PA-II, the nonlinear  $C_{ds}$  was replaced by a linear capacitance and a linear  $C_{gd}$  capacitance was included in both the carrier and peaking PA device models. Finally, in the third simulated Doherty PA, PA-III, the carrier and peaking device models were composed by the nonlinear  $i_{DS}(v_{GS}, v_{DS})$  current source, by the nonlinear  $C_{gs}$  and  $C_{ds}$  capacitances and also by the linear  $C_{gd}$  capacitance. In order to keep the simulations physically meaningful, typical Si LDMOS element values were selected. The obtained Doherty AM/AM and AM/PM characteristics for the all PAs are shown in Fig. 4.9.

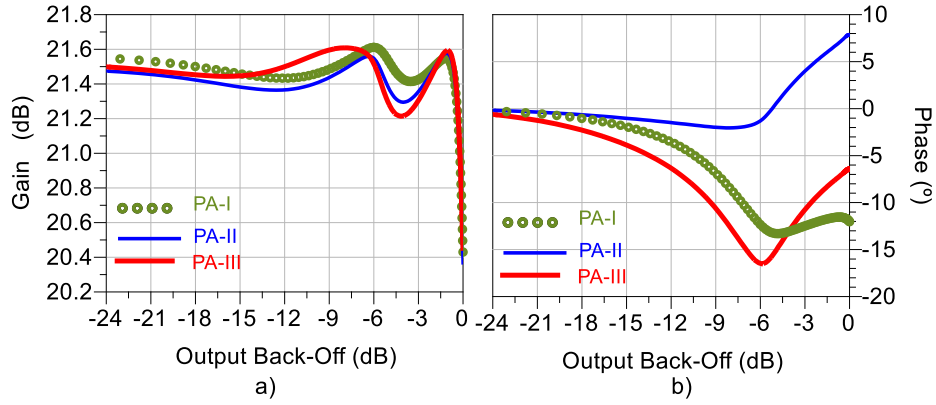


Fig. 4.9 – a) Simulated transducer power gain and b) AM/PM characteristics of all Si LDMOS conceptual DPAs.

The AM/AM characteristics of all simulated Doherty PAs are almost flat. There is only a slight compression for large input power drive for efficiency reasons. On what the AM/PM characteristic is concerned, in the first simulated Doherty PA (PA-I), it is visible the phase-lagging behaviour until the peaking PA enters into operation. After that, the PA-I AM/PM characteristic is almost flat. It only returns to its initial phase-lagging behaviour in the gain compression zone. On the other hand, contrary to what is observed in the first Doherty PA, the second simulated Doherty PA (PA-II) reveals a phase-leading behaviour when the peaking PA enters into operation. The AM/PM characteristic of the third simulated Doherty PA (PA-III) is the combination of the two previous characteristics.

The above observations are in agreement with what was explained and clearly indicate that the nonlinear  $C_{ds}(v_{DS})$  (for small amplitudes) along with the input  $C_{gd,Miller}$  variation (in the Doherty operation) are indeed the main contributors to the AM/PM distortion of a Doherty based on Si LDMOS devices.

In order to experimentally verify these Doherty nonlinear distortion mechanisms, it was designed and implemented a 1800MHz, 700W, asymmetric Doherty amplifier using 230W Si LDMOS devices from Freescale for both the carrier and peaking PAs. Two peaking amplifiers were used to obtain a high efficiency at ~9 dB of output power back-off. Fig. 4.10 presents the measured and simulated AM/AM and AM/PM characteristics of the implemented Doherty PA.

In accordance to what was previously explained, the Doherty PA presents an almost flat AM/AM characteristic (with the gain compression for large power levels for efficiency optimization) whereas, in terms of the AM/PM characteristic, there is the strong initial phase-lagging behaviour due to the nonlinear  $C_{ds}(v_{DS})$  and followed by an almost constant AM/PM characteristic, when the peaking PAs enter into operation.

The fact that the slight phase-leading behaviour due to the input  $C_{gd, Miller}$  variation is not observed, when the peaking PAs enters into operation, can be attributed to either the source and load harmonic impedances – since they are imposed by the device pre-matching networks – or to the difficulty in obtaining a purely real impedance at the fundamental.

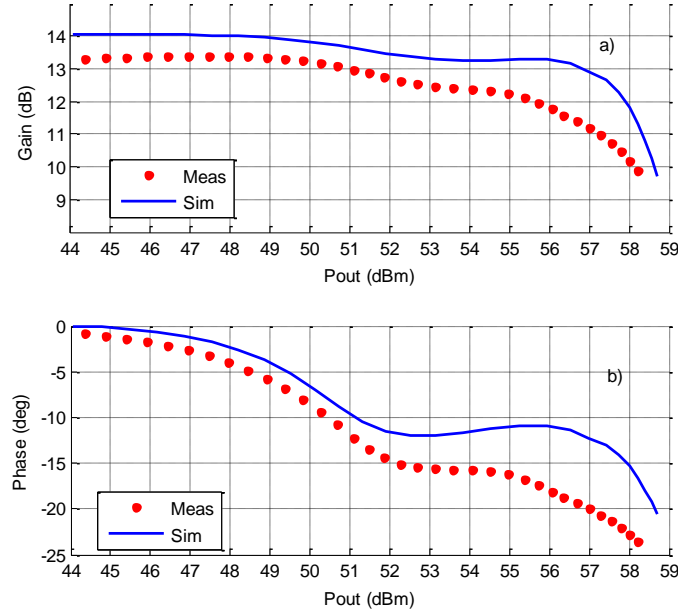


Fig. 4.10 – Measured and simulated a) AM/AM and b) AM/PM characteristics of the implemented Doherty power amplifier prototype.

### 4.3. General Approach for Distortion Analysis

To achieve the desired high power levels in cellular base stations it is necessary to use devices with large gate peripheries. This implies the use of transistors with built-in pre-matching circuitry allowing the transformation of the very low fundamental impedances, at the intrinsic reference plane, to manageable impedance values, at the package plane, making the intrinsic device nodes not observable.

In addition, the desired high-power Doherty power amplifiers are usually made with output matching networks made of very complex and distributed structures, where only a numerical electromagnetic representation or measured S-parameters characterization are available and the output combiner is not made with the canonical quarter wavelength impedance inverters. Consequently, the above characteristics along with the lack of equivalent circuit models for the high power devices, make the high-power Doherty nonlinear distortion analysis very complicated.

This being the case, it is necessary a more general approach where the output combiner can be represent as a general linear N-port network described and where it is not necessary a precise definition of the “junction node”, i.e. a circuit node where the carrier and peaking currents are combined, as it is illustrated in Fig. 4.11 for a case of an Asymmetric 2-Way Doherty PA.

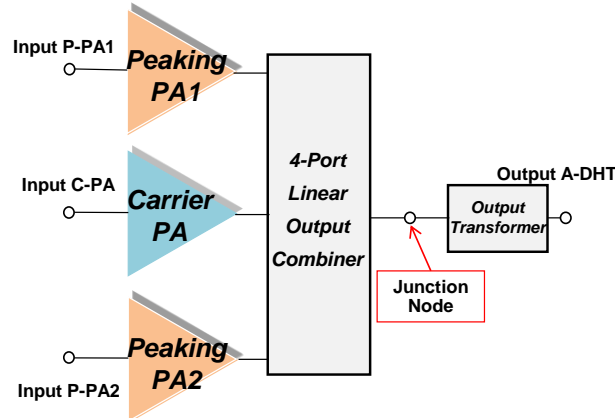


Fig. 4.11 – Asymmetric 2-Way Doherty PA junction node selection example.

As previously mentioned, accurate models for the active devices are necessary to perform a Doherty nonlinear distortion analysis. These models can be of equivalent circuit or behavioural type. Unfortunately, the first type is not always made available by the transistor manufacturer or it is not accurate enough, for all necessary load conditions. On the other hand, nonlinear behavioural models, as the Poly-Harmonic Distortion model (PHD) [96],[97], are suitable for the Doherty distortion analysis, if they are made load impedance dependent. However, they are extremely complicated to extract and so, industry tends to avoid them.

This being the case, active load-pull-based large signal models based on Look-Up Tables (LUTs) with only the fundamental measured data, have been proposed [98]. However, for high power devices it is very complicated and expensive to perform active load-pulling.

Consequently, passive load-pull-based models using LUTs are preferred [99], [100]. Although easier to extract (since it is only necessary to collect swept power passive load-pull data), they fail to predict the DPA load modulation since, for high back-off values, in spite of the peaking being off, it actually draws some current which is not taken into account producing inaccurate predictions [98].

To solve this problem, the peaking output admittance (essential to accurately predict the load modulation trajectories) was included in the Doherty output combiner, described

by its Z-parameters, making it possible to analyse the effects of the carrier and peaking currents separately at the output load.

#### 4.3.1 Behavioural Model Based on Passive Load-Pull Data

The necessary pre-matching circuitry in the high power devices, along with the package, impose the harmonic impedances at the intrinsic reference plane, regardless of the harmonic terminations at the output side. Consequently, the behavioural models extraction for these high power devices becomes simplified, since only the fundamental data is needed.

Actually, to develop the above behavioural models, PA designers can use the swept power load-pull data that they have already been measuring for a long time in the characterization of field-effect transistors. This approach consists in building a behavioural model,  $I_D(V_{in}, Z_L)$ , where the output is the fundamental drain current,  $I_D$ , and the inputs are the fundamental input voltage,  $V_{in}$ , and the load-impedance,  $Z_L = V_D / I_D$ .

As was already mentioned, the passive load-pull approach is preferable in comparison to the active characterization of the device,  $I_D(V_{in}, V_{out})$ , because it reduces the amount of necessary data required for extracting such model. Unfortunately, such a nonlinear PA behavioural model  $I_D(V_{in}, Z_L)$  is not general, because it does not allow active loads, which is exactly the load that is presented to the peaking PA, when it is off or sourcing very low current, as will be explained next.

##### A. OVERCOME THE ACTIVE LOAD IMPEDANCES PROBLEM

During high power devices' characterization, since the input power is swept for each passive load impedance, there are no negative drain currents. However, for the peaking PA, in a Doherty arrangement, some current provided by the carrier PA follows to the peaking, because the carrier PA sees the peaking PA off output admittance,  $Y_{22off}$ . This originates a negative drain current at peaking' terminals, making the  $Z_L$  presented to the peaking active.

To overcome this problem, the peaking PA  $Y_{22off}$  can be embedded in the output combiner [Z] matrix using the model presented in Fig. 4.12. This involves a transformation given by (4.1) and (4.2) of the load impedance,  $Z_p$ , and the collected drain current,  $I_{P,data}$ , at the package reference plane to a virtual intrinsic load impedance,  $Z_p'$ , and a virtual intrinsic drain current,  $I_P'$ , respectively.

$$Z_p' = \frac{Z_p}{1 + Y_{22off} Z_p} \quad (4.1)$$

$$I'_p = \frac{I_{p,data}}{1 - Y_{22off}Z'_p} \quad (4.2)$$

The new calculated current  $I'_p$  is the current that enters into the new  $[Z']$  matrix output combiner. To recover the peaking drain impedance and the drain current, it is necessary to de-embed the peaking PA  $Y_{22off}$ .

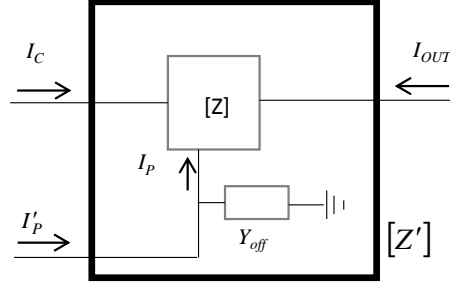


Fig. 4.12 – Schematic representation of the embedding procedure of the peaking PA off output admittance in the combiner  $[Z]$  matrix.

### B. OUTPUT COMBINER AS A GENERAL N-PORT NETWORK

In high power Doherty implementations, where wide transmission lines are used, there is no evident node where the peaking and carrier currents are added up, which complicates the analysis. To solve this problem, the entire output combiner (including the output matching networks and the impedance transformer from the junction to the output) can be modelled as a general N-port network, described by its impedance-parameters, the Z-Matrix:

$$\begin{cases} V_1 = Z_{11}I_1 + Z_{12}I_2 + Z_{13}I_3 \\ V_2 = Z_{21}I_1 + Z_{22}I_2 + Z_{23}I_3 \\ V_3 = Z_{31}I_1 + Z_{32}I_2 + Z_{33}I_3 \end{cases} \quad (4.3)$$

to which the carrier PA is attached to port one, the peaking PA to port two, and the load,  $Z_L$ , to port three.

So, the carrier and the peaking PAs drive the output combiner with currents  $I_1$  and  $I_2$ , when they are terminated by impedances  $Z_C$  and  $Z_P$ , respectively, while the load imposes a boundary condition given by  $V_3 = -Z_L I_3$  or  $I_3 = -Y_L V_3$ . Forcing this load boundary condition into the Z-Matrix leads to:

$$V_3 = \frac{Z_{31}}{1 + Z_{33}Y_L} I_1 + \frac{Z_{32}}{1 + Z_{33}Y_L} I_2 \quad (4.4)$$

which allows to compute the output voltage (or current) flowing to the load as a linear combination of the carrier and peaking PA currents.

Since these PA currents are nonlinear functions of the carrier and peaking PA input drive voltages and load impedances, to compute  $Z_C=V_1/I_1$  and  $Z_P=V_2/I_2$ ,  $I_3$  is first calculated:

$$I_3 = -\frac{Z_{31}Y_L}{1 + Z_{33}Y_L}I_1 - \frac{Z_{32}Y_L}{1 + Z_{33}Y_L}I_2 \quad (4.5)$$

Now, substituting this current into the  $V_1$  and  $V_2$  expressions leads to:

$$V_k = \left(Z_{k1} - \frac{Z_{k3}Z_{31}Y_L}{1 + Z_{33}Y_L}\right)I_1 + \left(Z_{k2} - \frac{Z_{k3}Z_{32}Y_L}{1 + Z_{33}Y_L}\right)I_2 \quad (4.6)$$

Replacing  $k$  by the corresponding port index, the respective relationship of the peaking and carrier voltages with their currents can be obtained, and so:

$$Z_C \equiv \frac{V_1}{I_1} = \left(Z_{11} - \frac{Z_{13}Z_{31}Y_L}{1 + Z_{33}Y_L}\right) + \left(Z_{12} - \frac{Z_{13}Z_{32}Y_L}{1 + Z_{33}Y_L}\right)\frac{I_2}{I_1}, \quad (4.7)$$

$$Z_P \equiv \frac{V_2}{I_2} = \left(Z_{22} - \frac{Z_{23}Z_{32}Y_L}{1 + Z_{33}Y_L}\right) + \left(Z_{21} - \frac{Z_{23}Z_{31}Y_L}{1 + Z_{33}Y_L}\right)\frac{I_1}{I_2}. \quad (4.8)$$

So, the general approach for distortion analysis of the 2-Way Doherty PA can be conducted by reflecting each of the output carrier and peaking PA currents,  $I_C'$  and  $I_P'$ , to the “junction node”, obtaining  $I_C$  and  $I_P$  and then adding them in amplitude and phase to obtain the Doherty AM/AM and AM/PM characteristics.

#### 4.3.2 Application to a Practical Doherty Power Amplifier

In order to validate the proposed behavioural model approach, an 1840MHz, 700W, 2-way asymmetric DPA composed by three 250W LDMOS devices (one for the carrier and two for the peaking PAs that will provide the appropriated load modulation) was designed and implemented. Then, this DPA was compared with a Simulink model that uses the proposed nonlinear PA behavioural models for each device.

These behavioural models were extracted via ADS simulations using the passive load-pull approach:  $I_2(V_1, V_2)=f(V_1, Z_L, V_{GSQ})$  and implemented as LUTs. For this extraction, it was used the same source impedance,  $Z_s$ , as the one of the final Doherty arrangement.

It should be noted that, although two peaking PAs are used, and so an output combiner with three inputs and one output, because the currents of the peaking PAs are equal ( $I_2=I_4$ ), and so are their voltages,  $V_2=V_4$ , this four-port network can be simplified to the three-port representation of (4.3), using  $Z_{12}=2Z_{12}'$ ,  $Z_{22}=Z_{22}'+Z_{24}'$  and  $Z_{32}=2Z_{32}'$  where the  $Z_{kk}'$  denote the four-matrix coefficients.

The final block diagram of the Simulink Model that represents the DPA is presented in Fig. 4.13, where the [Z] block represents equations (4.4), (4.5), (4.7) and (4.8).

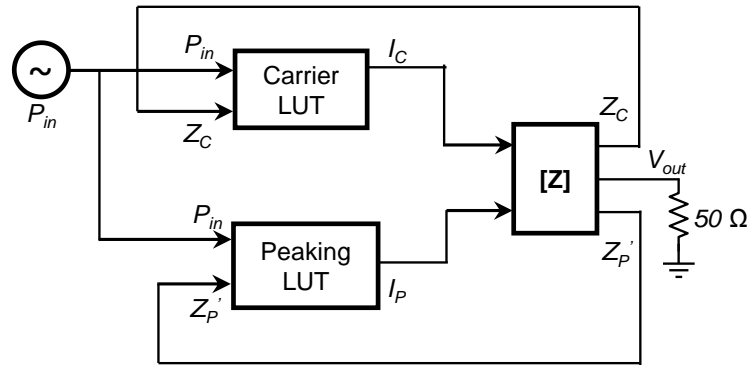
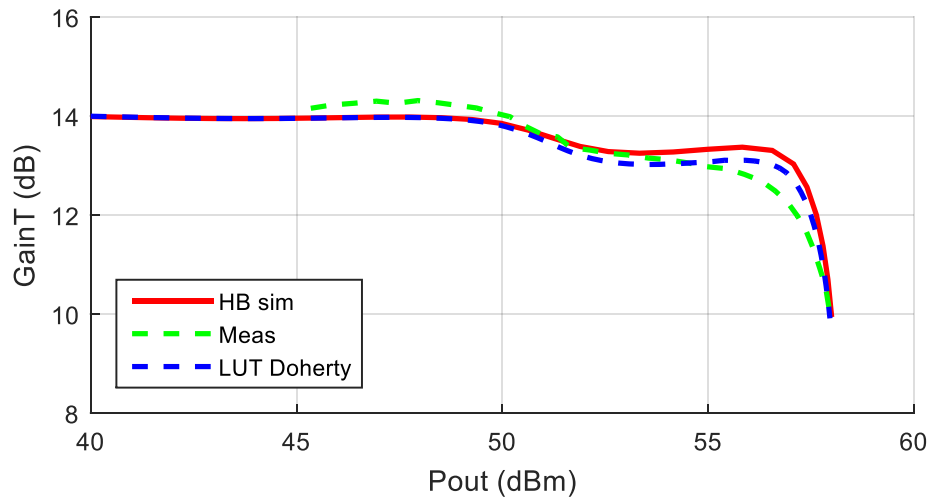


Fig. 4.13 – Block diagram implemented in Simulink to represent the asymmetric Doherty amplifier through LUT behavioural models.

Fig. 4.14 presents the comparison between the AM/AM and AM/PM measurements and simulations (obtained from the ADS harmonic-balance and from the proposed Simulink model). As seen, there is a good agreement between these characteristics in a wide input power range. In Fig. 4.15 it is presented the correspondent carrier and peaking load modulation trajectory predictions obtained by both simulations, showing also a good agreement. These results prove that the proposed general approach can indeed be used for Doherty nonlinear distortion analysis.



a)

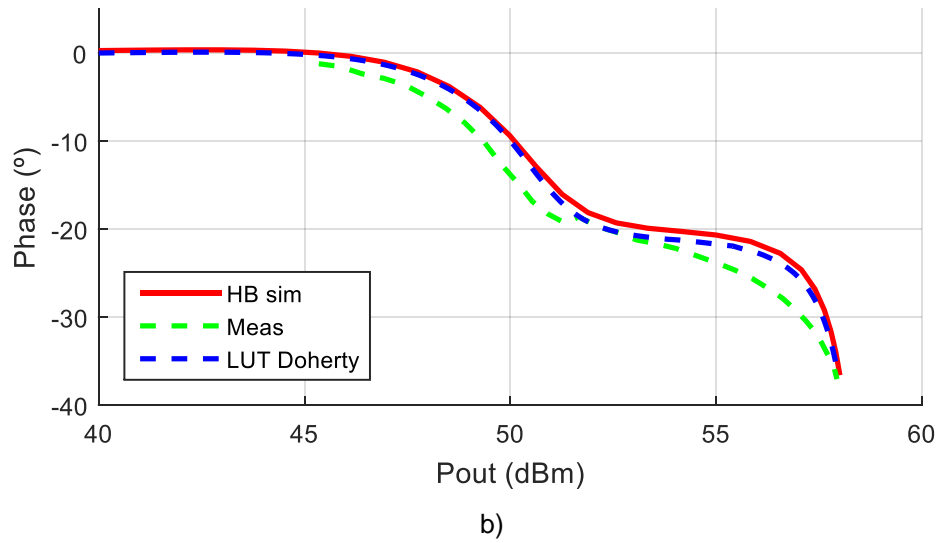


Fig. 4.14 – Comparison between a) AM/AM and b) AM/PM measurements and simulations (obtained with ADS harmonic-balance and the Simulink LUT behavioural models).

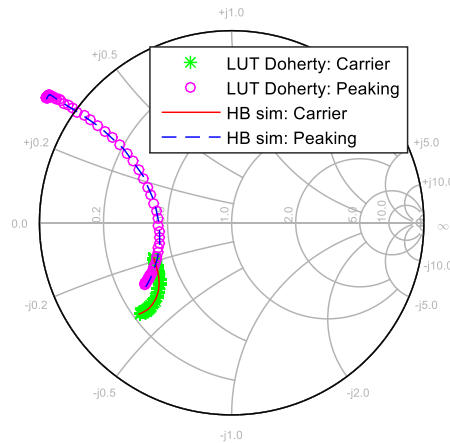


Fig. 4.15 – Load modulation predictions obtained with ADS harmonic-balance and the Simulink LUT behavioural models.

#### 4.4. Efficiency Analysis of the Doherty Amplifier

The Doherty PA has been very attractive since it offers the possibility of highly efficient operation throughout a wide range of amplitudes and this is very important when the PA needs to deal with the new complex modulated signals that have very high PAPRs, sometimes as high as 12dB. Therefore, beyond of the nonlinear distortion analysis, presented in the previous sections, it is also important to keep an eye on Doherty efficiency characteristic, namely the capability of controlling and understanding the first efficiency peak and its position. This being the case, the main objective of this sub-section is to explain the dependence of the Doherty PA efficiency on its load-pull

ratio, the ratio between the small-signal and the full-power load resistances presented to the intrinsic transistor of the carrier.

It is also desired an explanation for the higher efficiencies commonly obtained from GaN HEMT based Doherty power amplifiers (PAs), when subjected to wider load-pull ratios as compared with their Si LDMOS counterparts, the two main players in base-station PA technology.

#### 4.4.1 Efficiency Dependence on the Doherty PA Load-Pull Ratio

As mentioned before, it is very important to guarantee that the Doherty PA presents its first efficiency peak exactly at the power level in which it will operate most of the time. Therefore, the Doherty design starts by selecting the output power back-off level in which it should have the first efficiency peak,  $P_{L,mod}$ , the small-signal carrier PA load impedance that maximizes the efficiency for this power level,  $Z_{L,mod}$ , and the corresponding intrinsic drain impedance,  $R_{d,mod}$ .

Normally, the operation regime for the carrier PA is a class B or shallow class AB. So, if a theoretical FET model is considered, whose  $i_{DS}$  dependence on  $v_{GS}$  is piecewise linear and whose transition between the saturation to triode zones is abrupt with a constant (i.e., independent of  $v_{GS}$ ) knee voltage  $V_K$ , like the one used in the Cripps load-line method [101], [4], the  $i_{DS}$  dc and fundamental components ( $I_0$  and  $I_1$ , respectively), at the onset of saturation, are given by:

$$I_0(|Z_L|) = \frac{I_p}{\pi} = \frac{2}{\pi} \frac{V_{DD} - V_K}{R_{d,mod}} \quad (4.9)$$

$$I_1(|Z_L|) = \frac{I_p}{2} = \frac{V_{DD} - V_K}{R_{d,mod}} \quad (4.10)$$

where  $I_p$  is the class B half-wave sinusoid peak for the maximum voltage excursion,  $V_{1,mod} = V_{DD} - V_K$ , where  $V_{DD}$  is the drain supply voltage. This leads to the corresponding fundamental output power,  $P_{L,mod}$ , and the dc observed power,  $P_{dc,mod}$ :

$$P_{L,mod} = \frac{1}{2} V_{1,mod} I_{1,mod} = \frac{1}{2} \frac{(V_{DD} - V_K)^2}{R_{d,mod}} \quad (4.11)$$

$$P_{dc,mod} = V_{DD} I_{0,mod} = \frac{2}{\pi} V_{DD} \frac{V_{DD} - V_K}{R_{d,mod}} \quad (4.12)$$

At this input power level, the peaking PA should start conduction in order to prevent the carrier PA from entering into the compression regime. Then, at the maximum power level,  $P_{L,pwr}$ , if the Doherty is properly designed, both carrier and peaking PAs should see

the load impedance or drain resistance that maximizes the device's output power,  $Z_{L,pwr}$  or  $R_{d,pwr}$ . Consequently, both carrier and peaking PAs reach the maximum output voltage excursion,  $V_{1,pwr} = V_{DD} - V_K$ , and the consequent second Doherty efficiency peak is obtained.

Now, if the dc and fundamental drain currents were calculated for this power level, this would lead us to conclude that the two theoretical Doherty efficiency peaks would be equal to:

$$\eta = \frac{\pi}{4} \frac{V_{DD} - V_K}{V_{DD}} \quad (4.13)$$

However, not only this is not observable in a practical Doherty, as the first efficiency peak varies with the so-called DHT load-pull-ratio, LPR, defined as the VSWR at the carrier PA device package plane:

$$LPR = \frac{1 + |\Gamma_{L,mod}|}{1 - |\Gamma_{L,mod}|} \quad (4.14)$$

where the  $\Gamma_L$  reflection coefficient refers to the mismatch of  $Z_{L,mod}$  with respect to the conjugate of  $Z_{L,pwr}$ :

$$\Gamma_{L,mod} = \frac{Z_{L,mod} - Z_{L,pwr}^*}{Z_{L,mod} + Z_{L,pwr}^*} \quad (4.15)$$

This LPR is a very important tool for the high power Doherty PA designers, since with that the load impedance path presented to the carrier PA that maximize the Doherty efficiency can be directly mapped onto the measured output power and efficiency load-pull contours. This being the case, it is crucial to understand the reason for the observed variation of the efficiency profile with the load-pull ratio.

#### A. AN IMPROVED EFFICIENCY MODEL USING A VARIABLE KNEE VOLTAGE

So, in order to improve the efficiency model presented above, it was considered the dependence of the knee voltage,  $V_K$ , with the drain current:

$$V_K(i_{DS}) = V_{DD} - \frac{1}{2} R_d I_p = R_{on} I_p \quad (4.16)$$

in which the  $R_{on}$  is the FET's channel resistance in the triode region.

This means that the knee voltage can also be expressed as a function of  $R_d$ :

$$V_K(R_d) = \frac{2R_{on}}{R_d + 2R_{on}} V_{DD} \quad (4.17)$$

Substituting this equation in (4.11) and (4.12) leads to updated output power and dc consumed power of:

$$P_L = \frac{1}{2} \frac{R_d}{(R_d + 2R_{on})^2} V_{DD}^2 \quad (4.18)$$

$$P_{dc} = \frac{2}{\pi} \frac{V_{DD}^2}{R_d + 2R_{on}} \quad (4.19)$$

which results in an efficiency given by:

$$\eta = \frac{\pi}{4} \frac{R_d}{R_d + 2R_{on}} \quad (4.20)$$

With the FET's channel resistance inclusion, a maximum of output power and an efficiency that increases asymptotically with  $R_d$  (or with the DHT LPR) to the theoretical class B efficiency of 78.5% when  $R_d \gg 2R_{on}$  can be observed. Unfortunately, the  $R_{on}$  is incapable of predicting the observed optimum efficiency load and the consequent efficiency degradation when  $R_d$  increases beyond this optimum load.

#### **B. EFFECT OF THE FET'S SOFT TURN-ON**

In practice, since the real transistor drain current presents a soft turn-on [33], [34], to ensure high efficiency and gain flatness, the chosen quiescent gate voltage ( $V_{GS}$ ) usually does not enforce zero drain current but a non-null quiescent value ( $I_{DQ}$ ). With this bias point, it is possible to maintain the class B linearity and so the  $i_{DS}$  fundamental component ( $I_1$ ) is approximately equal to the theoretical class B fundamental current,  $I_1 = I_p/2$ . However, the non-null quiescent current implies that the ratio between the fundamental and the dc component is no longer constant and equal to  $I_1/I_0 = \pi/2$ .

In fact, although for lower load impedances (when the input signal excursion is very high) the quiescent current could be neglected and the theoretical class B  $I_1/I_0$  ratio is asymptotically achieved, for higher loads (for which there is practically no current swing), the non-null quiescent current remains producing a  $I_1/I_0$  ratio approximately equal to zero. Fig. 4.16 shows this  $I_1$  and  $I_0$  behaviour as a function of  $R_d$ , as well as the ratio between them, obtained when it was considered a FET model described by only the  $i_{DS}(V_{GS})$  current source with a smooth turn-on.

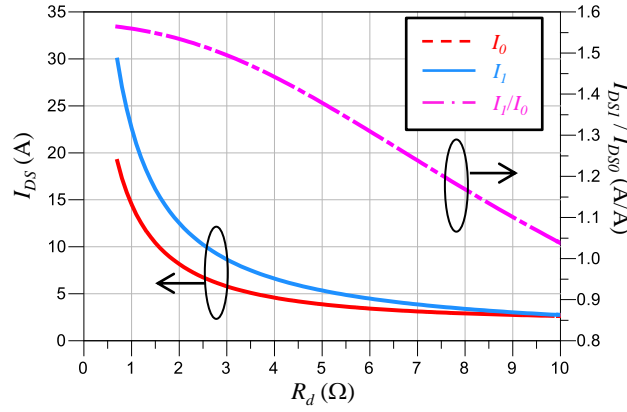


Fig. 4.16 – Simulated dc,  $I_0$ , and fundamental,  $I_1$ , output current components of the FET, described by only the  $i_{DS}(v_{GS}, v_{DS})$  current source with a smooth turn-on. It is also plotted the ratio between  $I_1$  and  $I_0$ , which is the main responsible of the efficiency decrease when  $R_d$  is increased.

As it was explained, the  $I_1$  component dependence on  $R_d$  can be approximated by the theoretical piecewise class B model:

$$I_1(R_d) = \frac{I_p}{2} = \frac{V_{DD}}{R_d + 2R_{on}} \quad (4.21)$$

while to represent the  $I_0$  component dependence on  $R_d$  it is necessary to include the non-null quiescent current. For that, it was found that  $I_0$  can be reasonably well approximated by:

$$I_0(R_d) = \frac{2}{\pi} \frac{V_{DD}}{R_d + 2R_{on}} + \frac{I_{dq}^2}{\frac{V_{DD}}{R_d + 2R_{on}} + I_{dq}} \quad (4.22)$$

Thus, although the output power dependence on  $R_d$  can be still approximately represented by (4.18), the dc power must be updated, resulting in the following efficiency dependence on  $R_d$ :

$$\eta(R_d) = \frac{\pi}{4} \frac{R_d}{R_d + 2R_{on}} + \frac{V_{DD}}{V_{DD} + \frac{\pi}{2} \chi(I_{dq}) \cdot (R_d + 2R_{on})} \quad (4.23)$$

in which  $\chi(I_{dq})$  is the second term of (4.22). Consequently, for lower impedances – where the  $I_{dq}$  has a negligible impact on dc component and so,  $\chi(I_{dq})$  is approximately equal to zero – the efficiency increases with  $R_d$ . However, if  $R_d$  continues to increase, the current swing becomes smaller and smaller, producing the mentioned reduction of the  $I_1/I_0$  ratio, which leads to an efficiency degradation. Therefore, the smooth turn-on, with the consequent non-null quiescent current, is indeed the justification for the efficiency degradation for higher loads (or higher DHT load-pull ratios) and, consequently, the existence of an optimum load that maximizes the efficiency. The comparison between the

simulated and calculated efficiency profiles versus  $R_d$  can be shown in Fig. 4.17, presenting a remarkable agreement.

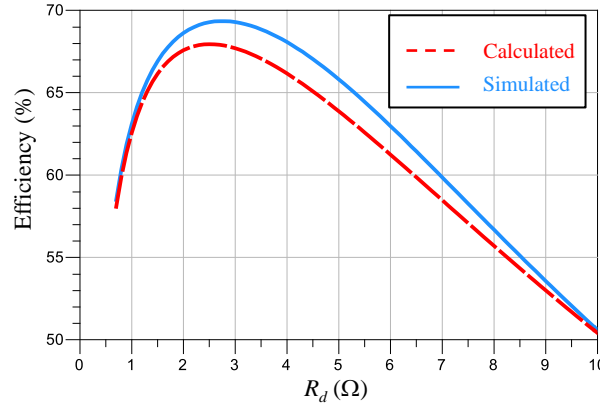


Fig. 4.17 – An illustration of the calculated and simulated [through the smooth turn-on FET model] drain efficiency versus drain resistance profile,  $\eta(R_d)$ .

### C. EFFECT OF THE FET'S $I_{MAX}$ AND THE PRESENCE OF NON-REAL LOAD IMPEDANCES

In order to correctly estimate the efficiency load-pull contours, it is necessary to take into account the FET's current limitation,  $I_{max}$ , when the FET is terminated with non-real load impedances,  $Z_L = R_L + jX_L$ . This being the case, the FET can reach the onset of saturation either by (i) voltage clipping, implying that  $|V_1| = V_{DD} - V_K$ , or by (ii) current clipping, which corresponds to  $|I_1| = I_{MAX}/2$ . Consequently, the fundamental output power,  $P_{out} = (1/2)\text{Re}[V_1 I_1^*] = (1/2)R_L |I_1|^2$ , is approximately equal to

$$(i) \quad P_L = \frac{1}{2} \frac{R_L}{(|Z_L| + 2R_{on})^2} V_{DD}^2 \quad (4.24)$$

or

$$(ii) \quad P_L = \frac{1}{8} R_L I_{MAX}^2 \quad (4.25)$$

depending on whether the FET operates limited in voltage or current, respectively.

Applying this to the dc power consumption, the following equations are obtained:

$$(i) \quad P_{dc} = \frac{2}{\pi} \frac{V_{DD}}{|Z_L| + 2R_{on}} + \frac{I_{dq}^2}{\frac{V_{DD}}{|Z_L| + 2R_{on}} + I_{dq}} \quad (4.26)$$

or

$$(ii) \quad P_{dc} = V_{DD} I_{MAX} \quad (4.27)$$

which leads to efficiency values of

$$(i) \quad \eta = \frac{\pi}{4} \frac{R_d}{|Z_L| + 2R_{on}} + \frac{V_{DD}}{V_{DD} + \frac{\pi}{2} \chi'(I_{dq}) \cdot (|Z_L| + 2R_{on})} \quad (4.28)$$

or

$$(ii) \quad \eta = \frac{\pi}{8} R_L \frac{I_{MAX}}{V_{DD}}. \quad (4.29)$$

These efficiency expressions lead to the constant output power and efficiency contours shown in Fig. 4.18. The remarkable agreement between these calculations with the simulations of a real  $i_{DS}(V_{GS}, V_{DS})$  current source model of the 250W Si LDMOS device used in the validation sub-section, proves that, despite the simplicity of the proposed model, it can predict the output power and efficiency load-pull contours. This model is also useful to conclude that the constant efficiency load-pull contours normally present an approximately oval characteristic, in which their axes are orthogonal to the axes of the constant output power load-pull contours.

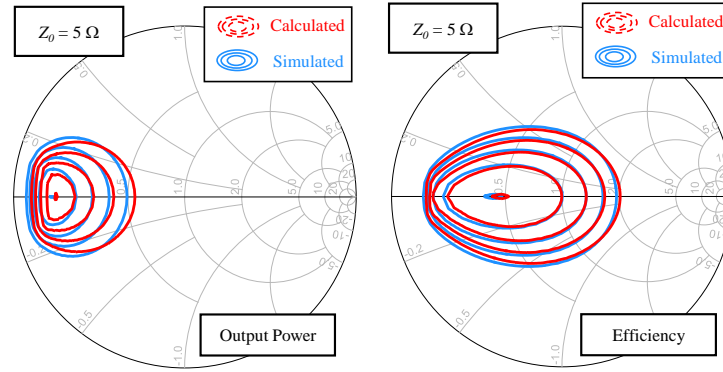


Fig. 4.18 – An illustration of the calculated and simulated [of a real  $i_{DS}(V_{GS}, V_{DS})$  current source model of the 250W Si LDMOS device used in the validation sub-section] drain efficiency load-pull contours ( $\eta_{Step}=5\%$ ,  $\eta_{Max,simulated}=69.3\%$  and  $\eta_{Max,calculated}=67.9\%$ )

#### D. VALIDATION OF THE PROPOSED OUTPUT POWER AND EFFICIENCY LOAD-PULL CONTOURS' MODEL

To validate the proposed output power and efficiency load-pull contours' model, it was used a 1800MHz high power (250W) input and output pre-matched Si LDMOS device from Freescale Semiconductor, Inc., whose intrinsic equivalent circuit model was obtained through optimization of the dc curves and bias-dependent small-signal S-parameters simulated with the encoded nonlinear device model provided by the device's vendor.

The measured output power and efficiency load-pull contours are the ones offered by the device's vendor to its customers at the 1dB compression point. These were compared with the predictions obtained by simulations and derived from the proposed load-pull contours' model calculations. To perform these calculations, a  $R_{on}=0.12\Omega$  and

$I_{MAX}=60A$  parameters were extracted from the simulated I/V curves. The quiescent bias point of ( $V_{GS}=2.95V$  and  $V_{DS}=28V$ ) gives us the missing parameter to have the complete load-pull contours' model, the quiescent current  $I_{dq}=2.3A$ .

Fig. 4.19 and Fig. 4.20 show the comparison between the measured, simulated and predicted output power and efficiency load-pull contours after the transformation to the intrinsic FET reference plane and at the device terminals reference plane, respectively. Although the observed slight differences between the measured and predictions, the proposed model is still capable of predicting the contours behaviour (including the orthogonality of the output power and efficiency contours), as well as the optimum output power and efficiency loads,  $Z_{L,pwr}$  and  $Z_{L,eff}$ , being very useful to select the desired region of the DHT load modulation.

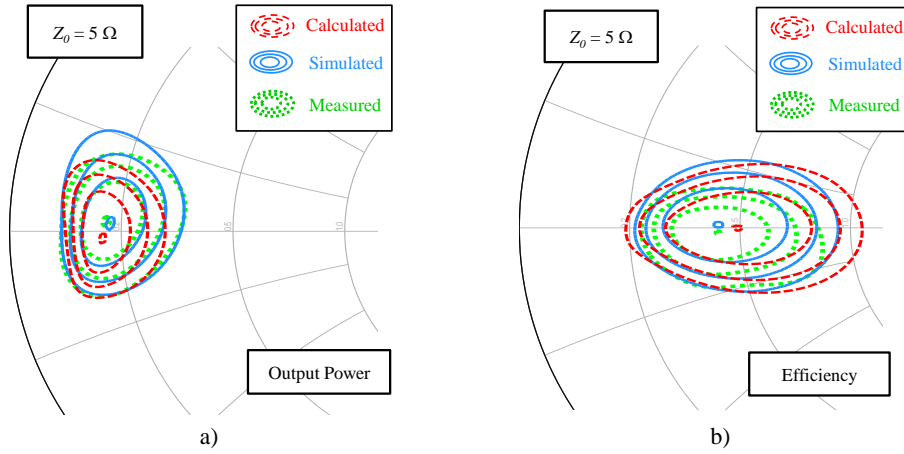


Fig. 4.19 – A comparison between the output power ( $P_{Step}=0.5$  dB,  $P_{Max,simulated}=55.7$  dBm,  $P_{Max,measured}=54.2$  dBm and  $P_{Max,calculated}=54.5$  dBm) a) and efficiency ( $\eta_{Step}=2$  %,  $\eta_{Max,simulated}=74.7$  %,  $\eta_{Max,measured}=70.2$  % and  $\eta_{Max,calculated}=67.9$  %) b) load-pull contours predicted by the proposed theory and measured in the 250 W pre-matched Si LDMOS FET, after transformation to the intrinsic device reference plane.

Note that the observed differences between the measured and the predictions can be derived from the nonlinear capacitances, namely the  $C_{ds}(v_{DS})$ , since with the increase of the output voltage excursion (due to the load impedance variation), the load required to guarantee the needed fundamental termination seen by the intrinsic current source is progressively more inductive than predicted. Beyond that, the pre-matching circuitry along with the package of this high power device impose the harmonic terminations at the intrinsic reference plan (regardless of the impedance presented to the output terminal), and so, it is very difficult to guarantee the necessary class B short circuit at all harmonics.

#### 4.4.2 Impact of Trapping Effects on GaN HEMT Based Doherty PA Load-Pull Ratios

Presently, as was already mentioned, base-station PAs rely on either GaN HEMTs or Si LDMOS and it has been observed that GaN devices present higher efficiencies when subjected to wider LPRs than their Si LDMOS counterparts. However, no justification for that has yet been presented, which is exactly the objective of this sub-section.

In the previous sub-section it was demonstrated that the FET' soft turn-on with its inherent non-null quiescent current,  $I_{DQ}$ , has a determinant impact on the efficiency degradation with the increase of the drain load resistance (see Fig. 4.17). It was also presented that this efficiency dependency can be modelled by (4.23).

To further illustrate the quiescent current impact on the efficiency variation with the load impedance, several  $I_{DQ}$  values were chosen in (4.23) – all around class B operation – where the above model is still valid, and observed the efficiency variation with the load impedance. The obtained results are shown in Fig. 4.20, where it is possible to see that, although  $I_{DQ}$  is very small, when compared with the maximum current, it has a severe impact on the LPR. Actually, the simulated efficiency is higher in a wider LPR range when the device is biased for shallow class C operation than for shallow class AB.

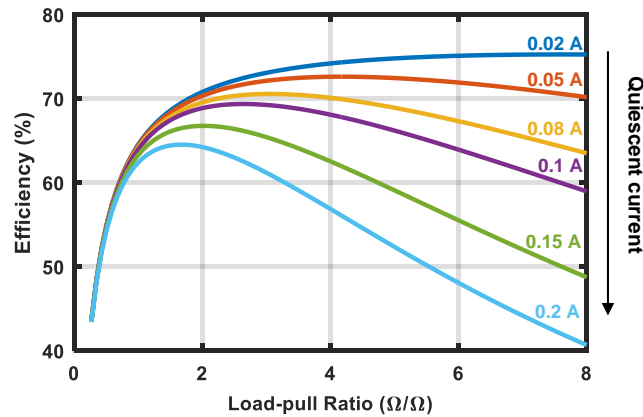


Fig. 4.20 – Illustrative behaviour of the efficiency variation with the load impedance for increasing quiescent currents.

The devices based on GaN suffer from charge-trapping effects, namely drain-lag, in which the  $i_{DS}$  current does not instantaneously follow a fast  $v_{DS}$  variation. As a consequence,  $i_{DS}$  presents slow transients in which its value is determined by the trapping charge state imposed by the  $v_{DS}$  peak voltage [83]. These effects can be understood as a back-gating phenomenon resulting in a severe self-biasing effect. In [85] and [89] the authors showed that when performing AM/AM CW measurements, for increasing CW

amplitudes (i.e., for increasing  $v_{DS}$  peak voltages), the transistor actually changed its real bias point, leading to a  $I_{DQ}$  reduction.

Since load-pull characterization is usually done at the onset of saturation (corresponding to very high  $v_{DS}$  peak voltages), the efficiency is actually being measured for a self-biased shallow class C PA (a fact evidenced by the AM/AM profiles that reveal a significant gain expansion when the PA is excited with a fast modulated signal). Therefore, as it was shown above, with this operation class change, and consequent  $I_{DQ}$  reduction, GaN transistors maintain high efficiencies for a wider load impedance range, reason why they present higher efficiencies when subjected to wider load-pull ratios in DPA applications.

To test the presented hypothesis, two 15W transistors were selected: a Si LDMOS (BLF6G21-10G from NXP) and a GaN HEMT (CGH35015F from Cree). The first one was selected because Si LDMOS technology is known for not suffering from trapping effects and could be used to actually validate the proposed theory. Both transistors were tested at 900MHz.

The bias points selected for the load-pull characterization were, for both the GaN HEMT and the Si LDMOS, the ones that provided the flattest gain characteristic (corresponding to class B operation) when the transistors were terminated with their maximum output power load. In order to verify the quiescent current importance in the efficiency variation with the drain impedance, the Si LDMOS device was also tested in shallow class C operation, this way emulating the back-gating phenomenon observed in GaN HEMTs. Fig. 4.21 shows the obtained CW gain curves of both devices for the mentioned quiescent points. For illustration purposes, it is also shown the self-biased class C behaviour that the GaN HEMT reveals when it is excited with a fast (with respect to the trapping time constants) two-tone signal, but biased with the same static (CW) class B quiescent point.

Fig. 4.22 presents the measured Si LDMOS Pout and PAE load-pull contours for the two above mentioned bias points. Although in the Pout contours there is no substantial difference between both bias points, in the PAE contours there is a significant transformation. Fig. 4.23 presents the PAE dependence on the load resistance where the detected differences are more evident.

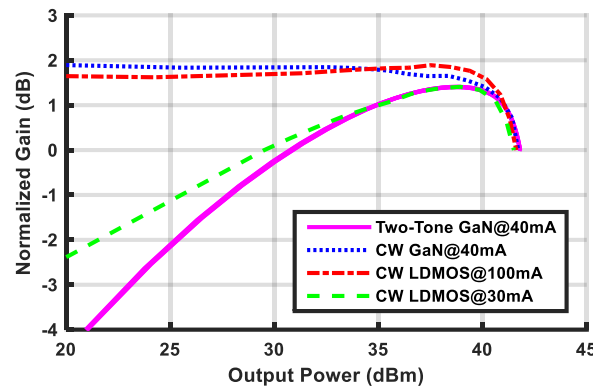


Fig. 4.21 – Comparison between the measured 900MHz CW gain profiles of the GaN HEMT (class B operation) and Si LDMOS (class B and class C) devices terminated with their maximum output power loads. In addition, it is also shown the measured gain profile when the GaN HEMT was excited with a fast two-tone signal.

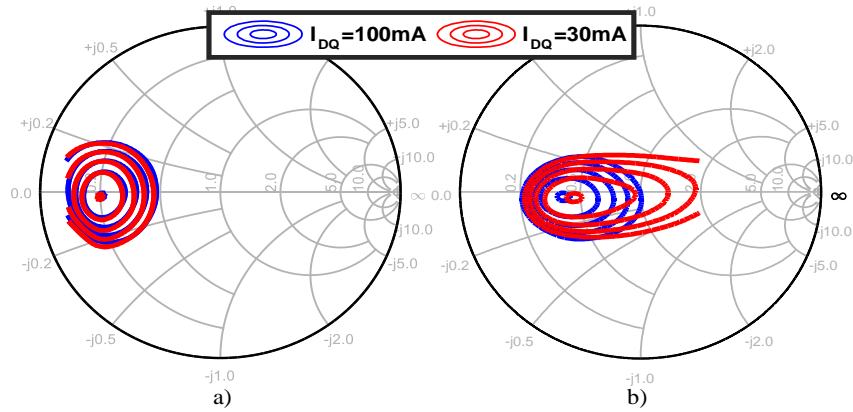


Fig. 4.22 – Measured load-pull a) output power and b) PAE contours of a Si LDMOS device for two different bias points.

For the GaN HEMT transistor, both the  $P_{out}$  and PAE load-pull contours were also measured. Fig. 4.24 presents the obtained PAE variation with the load resistance. The obtained profile is quite similar to the one obtained with the class C LDMOS PA, proving that this enlargement is indeed due the trapping-effects and consequent reduction of quiescent current.

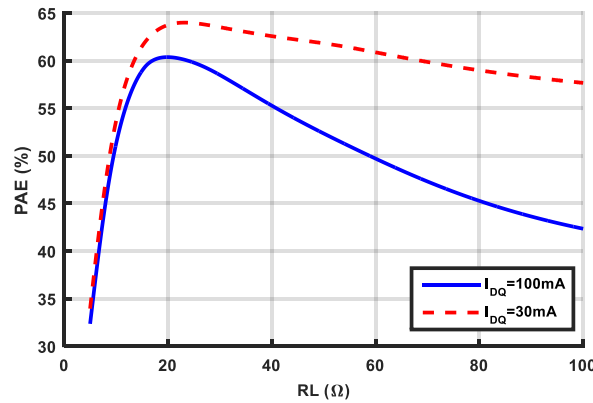


Fig. 4.23 – Measured PAE dependence on the load resistance of a Si LDMOS device for two different bias points.

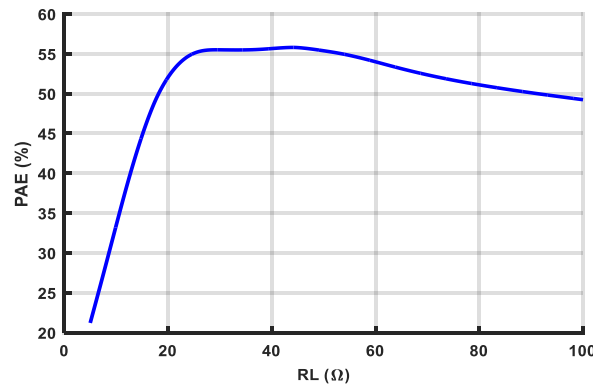


Fig. 4.24 – Measured PAE dependency on the drain impedance of a GaN HEMT device.

## 4.5. Summary

This chapter was dedicated to the nonlinear distortion generation mechanisms in both Si LDMOS and GaN HEMT based 2-Way Doherty arrangement. The transistor nonlinear drain-source current  $i_{DS}(V_{GS}, V_{DS})$  of both carrier and peaking PAs and how these currents are combined in the output combiner are the major contributors to the overall AM/AM Doherty distortion. On what the AM/PM distortion is concerned, it was found that in GaN HEMT based Doherty PAs the major contributor is the FET's input impedance variation due to the input Miller reflected gate-drain capacitance along with the output voltage compression at carrier FET terminals. For Si LDMOS based Doherty PAs, the AM/PM distortion is mostly determined by the output nonlinear capacitance variation.

These Doherty nonlinear distortion mechanisms were successfully verified in a practical 900 MHz Doherty PA using 15W GaN HEMT transistors and in a 1800MHz Doherty amplifier using 230W Si LDMOS transistors.

In addition, in this chapter it was also presented a nonlinear PA behavioural model based on swept power passive load-pull data using LUTs useful to analyse the nonlinear

distortion of a high-power Doherty. Where the peaking output admittance - essential to accurately predict the load modulation trajectories – was incorporated in the Doherty output combiner which was modelled as a general N-port network described by its Z-parameters. This model proved to be effective in the predictions of the AM/AM and AM/PM characteristics of an 1840 MHz 700W asymmetric Doherty power amplifier, as well as on the carrier and peaking load-modulation trajectories.

Beyond that, in this chapter it was also presented a simple model to describe the output and efficiency dependency on the DHT load-pull ratio, demonstrating that the FET channel series resistance,  $R_{on}$ , and soft turn-on are the main reasons for the observed optimum efficiency load resistance. It was also shown that the reactive components on the load impedances produce oval output power and efficiency load-pull contours where their axes are orthogonal to each other. The proposed theoretical model was successfully validated using a commercial 1800 MHz high power (250W) Si LDMOS FET.

A justification for the higher efficiencies observed in GaN HEMT DPAs when subjected to wider load-pull ratios as compared with the one obtained with Si LDMOS based DPAs was also presented. It was found that the trapping-effects observed in GaN HEMTs and their consequent quiescent current reduction are the fundamental reason for this improvement. This theory was validated by comparing the load-pull contours obtained in a 15W GaN HEMT device with the ones obtained using a 15W Si LDMOS with different quiescent currents.

## 5. Conclusion and Future Work

The main motivation for this PhD work was the fact that there was a lack of knowledge about the nonlinear distortion generation mechanisms in a Doherty amplifier, which is essential to its design with optimized efficiency and linearity. Besides that, better linearization schemes could be idealized to compensate the obtained distortion. Thus, the main objective of this PhD work became to develop a simple model capable of describing and explaining the distortion generation mechanisms of a Doherty amplifier based on both Si LDMOS and GaN HEMTs, the two most common RF power amplifier technologies presently used in cellular infrastructures.

This being the case, after a first chapter dedicated to the motivation, background work, and literature review, in Chapter 2, a generic model extraction methodology for Si LDMOS and GaN HEMT devices was presented. These models were very useful to study the nonlinear distortion of a power amplifier, since they allowed to individually analyse the nonlinear distortion arising from different sources also presented.

Besides that, Chapter 2 also presented a new extraction methodology to incorporate trapping effects in GaN HEMT models based on double-pulse iso-dynamic measurements. Despite its simplicity, the extraction methodology and the inclusion of these phenomena on the model produced very good results, predicting the fundamental GaN HEMT long-term dynamics.

The Doherty nonlinear distortion analysis (the main objective of this PhD work) was divided in two steps. Firstly, in Chapter 3, the main AM/AM and AM/PM nonlinear distortion generation mechanisms of the carrier and peaking PAs – the two basic cells of the Doherty arrangement – operating individually as single-ended PA were identified and explained. These studies were carried out on both Si LDMOS and GaN HEMT device technologies and it was found that the transistor nonlinear drain-source current was the major contributor to the AM/AM in both technologies, whereas the AM/PM distortion was determined by, either the output nonlinear capacitance, in Si LDMOS devices, or by the FET's input impedance variation due to the nonlinear gate-source and the input Miller reflected gate-drain capacitances, in GaN HEMTs.

Then, in Chapter 4, the main nonlinear distortion generation mechanisms in both Si LDMOS and GaN HEMT based 2-Way Doherty arrangement were presented. Again, for both device technologies, the transistor nonlinear drain-source current  $i_{DS}(V_{GS}, V_{DS})$  of both the carrier and peaking PAs, and how these currents are added in the output combiner, are the major contributors to the overall AM/AM Doherty distortion. On what the AM/PM distortion is concerned, the strong variation of the Miller reflected gate-drain capacitance due to the output voltage compression at the carrier FET terminals was found to be the major AM/PM contributor in GaN HEMT based Doherty PAs, whereas, for Si LDMOS based Doherty PAs, the AM/PM distortion was determined by the nonlinear drain to source capacitance variation. In addition, a LUT based behavioural model suitable for high power Doherty was presented and found useful to study the nonlinear interaction between the carrier and peaking PAs in the Doherty arrangement when it is not possible to obtain accurate circuit level models for the active devices.

Finally, in the last sub-section of Chapter 4, a simple model to describe the output and efficiency dependency on the DHT load-pull ratio was presented, where it was found that the FET channel series resistance,  $R_{on}$ , and soft turn-on are the main reasons for the observed optimum efficiency load resistance. In addition, it was also found that the quiescent current reduction due to the trapping-effects observed in GaN HEMTs is the main reason for the higher efficiencies observed in GaN HEMT DPAs when subjected to wider load-pull ratios as compared with the ones obtained with Si LDMOS based DPAs.

In summary, this PhD Thesis was successfully completed since the main nonlinear distortion sources in 2-Way Doherty amplifiers were clearly identified and explained – which was the main objective of this PhD work – being the derived models successfully compared against measurements. Actually, combining the active device modelling with the PAs nonlinear distortion analysis revealed to constitute one of the major advantages of this PhD work. On the one hand, the information derived from the modelling work can help the identification of the nonlinear distortion sources and how they contribute to the AM/AM and AM/PM distortion of the PA. On the other hand, the knowledge derived from the understanding of the PA nonlinear distortion mechanisms can also help the modelling work when it is necessary to do some model adjustments.

## **5.1. Future Work**

The knowledge regarding the nonlinear distortion generation mechanisms and control, either in the entire Doherty arrangement or in their individual cell PAs, operating in a single-ended mode, is believed to constitute the major contribution derived from this

PhD work. In fact, with this knowledge, some power amplifier design rules to improve the linearity and efficiency compromise can be derived.

This being the case, one interesting future research topic regarding the power amplifier design, namely the Doherty architecture, is the development of an output combiner and an input splitter, where the aforementioned nonlinear distortion physical generation mechanisms conclusions are taken into account, with the objective of minimizing the AM/AM and AM/PM distortions without degrading the efficiency. This new design methodologies can be further explored using the so-called digital Doherty amplifier, where different digitally synthesized signals are used in each branch.

Actually, the flexibility offered by digital synthesis opens another door for other future research topics. Studying which input signal along with output combiner structures that maximize the power amplifier efficiency and linearity performance is undoubtedly a scientific orientation to be followed. This being the case, it would be very useful an extension of the Doherty efficiency and nonlinear distortion analysis to other architectures as Chireix Outphasing – in which complex load modulations are used – or envelop tracking, if voltage supply adaptation is considered.

In addition, with the necessity of higher and higher data rates and with the increased demand for mobility, the power amplifiers have to handle high bandwidth modulated signals, being frequently required to use more than one carrier. This can be further complicated when the power amplifier, for economic reasons, needs to handle multi-bands – in which the carrier frequencies separation can reach hundreds of MHz – to accommodate different standards. In this scenario the bias networks start to have an important role with respect to nonlinear memory effects. Thus, the previous analysis should be extended to accommodate these multi-band and bandwidth issues.

Moreover, one possible scenario for the fifth mobile generation (5G) is to have a very high density distributed network of small transmitters with a huge bandwidth, being mandatory the optimization of the compromise between cost and performance. Furthermore, since, in this scenario, the power generated by the amplifiers is small, very complicated linearization schemes, where the consumed power is comparable to the power generated by the amplifiers, are not a solution. Therefore, the knowledge either obtained from the nonlinear distortion analysis, or from the circuit modelling task (especially for GaN HEMTs) resulted from this PhD work can be used to develop a power amplifier with a built-in non-expensive high bandwidth analogue pre-distorter.

On what device technologies is concerned, although the Si LDMOS is a very mature and low cost device technology, presenting a high reliability and very good linearity

performance, the continued need to increase the bandwidth and to reduce the wasted energy on power amplifiers leads to an increased attention to GaN HEMT technology – with its inherent higher efficiency – by the industry and the scientific community, even if it is a more expensive solution. However, the long term memory effects, observed in the GaN HEMTs, severely impact the power amplifier linearizability performance and so, more complicated linearization schemes are needed. The physical based model for GaN HEMTs with trapping effects developed during this PhD work along with the knowledge acquired in this process, already contributed to improve these linearization schemes. However, looking in detail to the model predictions and comparing them with the measurements, it seems that there is something missing. Consequently, this modelling work should be continued.

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