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Linearizing an L-Band Power Amplifier for RADAR applications

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Linearização de Amplificador de Potência Banda-L para aplicações RADAR

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requesitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações. Realizada sob a orientação científica do Professor Catedrático Nuno Miguel Gonçalves Borges de Carvalho, Professor do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro, co-orientação do Professor Associado Reza Mahmoudi, Professor do Departamento de Electrónica da Universidade Técnica de Eindhoven, e co-orientação industrial do Engenheiro Hervé Brouzes, Microwaves Specialist na Thales Netherlands, e do Engenheiro Koen Wieringa, Technical Authority na Thales Netherlands.

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Palavras-chave

RADAR, Amplificador de Potência, linearidade, eficiência, dithering de baixa frequência, IMD, simulações de load-pull

Resumo

Esta dissertação de Mestrado têm como principal objectivo aumentar a linearidade de um determinado amplificador de potência, mantendo a sua eficiência.

Primeiramente, depois de escolhida a técnica a implementar (dither de baixa frequência (LFD)), vai ser feita uma análise com base numa dedução matemática seguida de simulações em MATLAB, para provar a sua eficácia.

Simulações usando o modelo do amplificador (fornecido pelo fabricante) e a técnica de LFD vão ser feitas onde as condições necessárias à implementação do dither vão ser extraídas para, posteriormente serem usadas na construção de um prótotipo. Depois do design do prótotipo ser finalizado, e da placa completa ter sido produzida, os resultados das medições, vão ser comparados com as simulações. Medidas de sinal fraco e sinal forte, bem como medidas da distorção de intermodulação vão ser apresentadas e analisadas.

No final, as medições anteriores vão ser utilizadas para comprovar a validade da técnica escolhida na linearização do amplificador para ser usado em aplicações de RADAR.

Keywords RADAR Power Amplifier, linearity, efficiency, low-frequency dithering, IMD, load-pull simulations

Abstract

This thesis attempts to improve the linearity, while keeping the efficiency, of a given power amplifier to be used in RADAR applications.

The thesis is divided in three major parts: first, the theoretical analysis around the chosen linearization technique is done by mathematical deduction and MATLAB simulations. In second place, ADS simulations with low-frequency dithering applied to an amplifier model, provided by the manufacturer of the amplifier, are performed. The desired characteristics found during simulations will be used on the design of the prototype.

Then, using the designed prototype, measurements to compare with the previous simulations, will be done. To prove the concept idea, small and large signal, for a single-tone, and two-tone measurements, with and without dithering, will be performed.

The improvement of the intermodulation distortion products using a dithered amplifier will be shown demonstrating actual linearity enhancement.

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Acronyms

BW Bandwidth.

CAD Computer-Aided Design.

DAC Digital-to-Analog Converter.

DPD Digital Predistortion.

DSP Digital Signal Processing.

DUT Device Under Test.

EER Envelope Elimination and Restoration.

EPA Error Power Amplifier.

FB Feedback.

FFW Feedforward.

GaAs Gallium Arsenide.

GaN Gallium Nitrate.

HEMT High-Electron-Mobility Transistor.

HFD High-Frequency Dithering.

HW Hardware.

IF Intermediate Frequency.

IM3 3^{rd} Order Intermodulation Distortion.

IM5 5^{th} Order Intermodulation Distortion.

IMD Intermodulation Distortion.

LFD Low-Frequency Dithering.

LINC Linearity With Non-Linear Components.

LIT Linearity Improvement Technique.

LNA Low Noise Amplifier.

LUT Look-Up Table.

MMIC Monolithic Microwave Integrated Circuit.

PA Power Amplifier.

PAE Power Added Eficiency.

PAPR Peak-to-Average Power Ratio.

PBO Power Back-Off.

PCB Printed Circuit Board.

RADAR Radio Detection and Ranging.

RF Radio Frequency.

RF HPA Radio Frequency High Power Amplifier.

SMPA Switched Mode Power Amplifier.

SNR Signal-to-Noise ratio.

SP Scattering Parameter.

STC Sensitivity Time Control.

UMS United Monolithic Semiconductors.

VNA Vector Network Analyzer.

VSWR Voltage Standing Wave Ratio.

Chapter 1

Introduction

The goal of this project is to improve linearity of a given power amplifier which is used in Radio Detection and Ranging (RADAR) applications.

RADAR systems radiate electromagnetic energy and detect the echo returned from reflecting objects. Figure 1.1 depicts the basic structure of a RADAR.

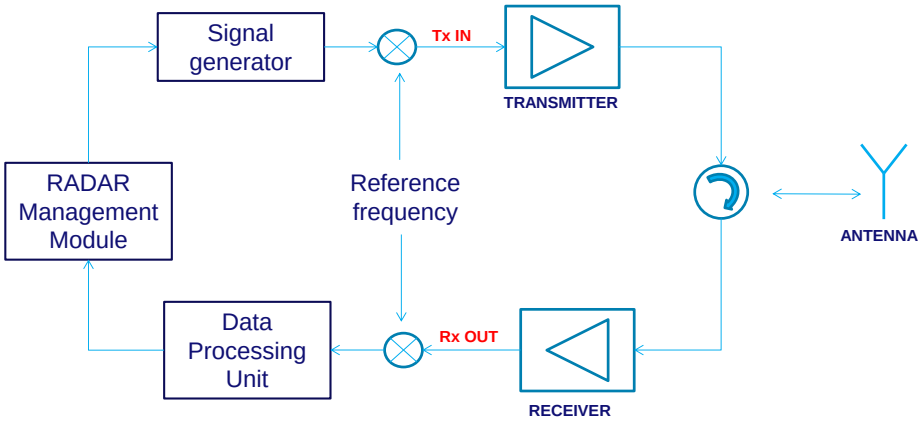


Figure 1.1: *Radar architecture.*

A modulated signal is amplified in the transmitter module and fed into the antenna. In presence of reflecting objects (also called targets), echoes (weak reflected signals) come back to the antenna and are amplified in the receiver channel. The transmitter chain always includes more than one stage of amplification (fig. 1.2), and the input of the receiver includes a limiter (to protect the circuit) followed by the Low Noise Amplifier (LNA) stages.

The received signal is processed and analyzed in the data processing unit and information of the target can be extracted, e.g., its distance, moving speed, shape...

Of course, a lot of intelligence has been put into each block. An enormous number of individual electronic components are combined in order to build these systems that can be portable, or installed on top of ships and are used to track people, fixed targets or missiles.

The most important characteristic of a RADAR is the average transmitted power received by the target rather than the peak power value because it allows to determine the detection range of the radar. According to the dimension and implementation of the RADAR system, they can be used to detect small and slow objects, like small drones, as well as large targets

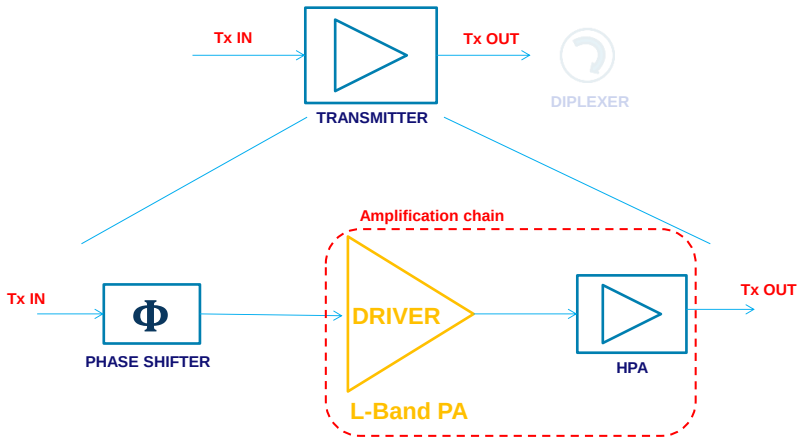


Figure 1.2: *Transmitter block.*

like ships and fast targets such as aircrafts and missiles.

For naval RADAR applications, typically, a sequence of narrow and rectangular-like pulses with a Radio Frequency (RF) carrier is used as a waveform. Figure 1.3 illustrates those pulses.

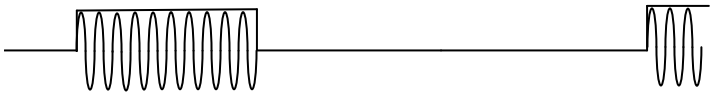


Figure 1.3: *RADAR pulse.*

Pulsed signals are mainly used because a single antenna may be shared for both transmitter and receiver and after the transmitter sends the signal (receiver is off), the transmitter turns off and the complete system is in listening mode. The transmitter must be completely shut down for the receiver to listen the re-transmitted signals that come from the targets, with as less disturbance as possible.

If the transmitter was always on, it would be very hard to keep the transmitter from interfering with the receiver that would be trying to hear faint echoes from distant targets. There exists CW radars which keep the transmitter and receiver channel always on, however these radars use carefully separated transmitter and receivers,with dedicated frequency modulation (FMCW radar).

Although pulsed signals with high power lead to much higher operating voltages (both DC and RF), energy storage problems, the necessity for high-power switching devices and careful thermal conditioning to keep temperature rise inside each pulse at levels that do not cause significant distortion through gain variation along temperature. An advantage of the pulsed radars is the possibility of the receiver sensitivity to be adjusted accordingly with Sensitivity Time Control (STC) - short range and long range echoes arriving at different times.

Within each pulse, an appropriate modulation is chosen according to the nature of the RADAR to increase the range resolution as well as the Signal-to-Noise ratio (SNR). Pulse compression is the signal processing technique mainly used [1]. After the transmission of the coded pulse, the received signal is mixed to an Intermediate Frequency (IF), amplified and processed using a pulse compression filter that consists of a matched filter to achieve maximum SNR.

The use of this technique provides several benefits regarding to range, resolution capability

and transmitted energy. Usually, pulse compression is done by linear frequency modulation (chirping) [1].

Moreover, another important characteristic of the radar systems is the use of saturated amplifier stages to keep output power as constant as possible across operating conditions (instantaneous frequency, temperature, aging,...). Naval radars systems require target detection in the highest range possible and the most accurate precision in the tracking operation therefore, transmitters must guarantee high power with stable waveforms over a wide bandwidth, with high efficiency and high reliability over time. Thus, operating the device in the linear region is not practical because variations over frequency, temperature and manufacturing spread lead to variations in the output power.

1.1 Motivation

The desire for increased overall electromagnetic sensors effectiveness is driving the need for improved interoperability between systems. For example, RADAR systems could also provide communication system features which can only be delivered using high crest factor signals, therefore the need of higher transmitted signal dynamic range.

Using power amplifiers under compression, only frequency modulation can be applied without sacrificing power efficiency. To be able to apply high order amplitude modulation schemes, using the RADAR signal in the linear zone is needed. In this case, the Power Amplifier (PA) is operated in a current steering class (A, AB, B or C), thus in a linear regime that is very in-efficient: increasing linearity means decreasing efficiency.

In the PA design, one can either use a linear PA (poor efficiency) with supply or load modulation techniques to enhance their efficiency while keeping the linearity (using pre-distortion or Cartesian feedback), or try to linearize non-linear but power efficient PAs.

Switched Mode Power Amplifier (SMPA) is a sub-class of efficient amplifiers that is characterized by its fast voltage swing between saturation and off-state. The voltage times current product at the amplifier terminals is always minimal, hence decreasing the power loss and thus, increasing the efficiency. On the other hand, the linearity is intrinsically poor because they switch between cut-off and saturation levels so, they cannot reflect the amplitude variations of the input on the output. Classes D, E, F, F^{-1} are the most common classes of operation for SMPA topologies.

Some linearization techniques of SMPA has been studied: outphasing [2] and Envelope Elimination and Restoration (EER) [3] are two of those techniques. On a side note, EER can be linked to any saturated class of operation, not only SMPA.

Later will be seen that EER can achieve good results although it requires a meticulous work because the complete circuit needs to be perfectly matched. The outphasing technique converts the modulated signal to a summation of two constant-envelope signals, to be further processed by the switched mode PAs (explained in more detail in chapter 2) and its major drawback resigns in the complex signal processing and precise matching between the two amplifiers, otherwise it will degrade the overall linearization efficiency. Thus, dithering was the chosen technique to be applied. A detailed explanation of the technique will be done in chapter 3. Theoretically, this technique allows a combination of the use of the signal under saturation with an enhancement of linearity.

1.2 Document overview

The goal of this thesis is to improve the linearity, while keeping the efficiency, of a given power amplifier to be applied in RADAR transmitter. Thus, in chapter 2, the linearity concept will be introduced followed by a deep study about different linearization and efficiency improvement techniques in order to chose the one to apply to the amplifier. In this chapter, a table with a summary of the state-of-the-art implementations for each one of them will be presented.

After revealing the chosen technique, in chapter 3, a detailed analysis of the dithering technique will be described, starting with a general understanding about the topic and then, diving into the mathematical proof of concept. After that, MATLAB simulations will be used to model a dithered amplifier. A distinction between HFD and LFD will be done.

In chapter 4, first the specifications of the amplifier to be linearized, will be itemized. Following is a description of the practical requirements that need to be defined regarding its specifications, such as its class of operation and the respective bandwidth for both input and dithering signal. Then, model based simulations on MATLAB will be performed and, at last, a check on the stability of the system will be presented.

For an implementation and further test of the prototype board, the design of a complete layout will be described, in chapter 5. Each step of the design process will be explained and confirmed by simulations and after, by measurement results. The measurement results are shown in chapter 6. Small and large signal, for a single-tone, two-tone and pulse-to-pulse phase stability measurements will be performed. Finally, in chapter 7, a discussion of the principal results will be done and some recommendations for potential future work will be given.

Chapter 2

Linearity

This chapter introduces the general topics about linearity. It begins with the mathematical concept and then, goes into the practical-system point of view. After that, a review of the state-of-the-art linearization techniques will be done.

Technological developments are rapidly changing the communications market. Nowadays, there is, more and more, the growing need of transmission multiple signals with as much information as possible, at high data rates, leading to highly complex modulation schemes.

Existence and uniqueness of a solution for a given output; boundedness of the output in case of boundedness of the input and, most important, continuous linear dependence of the output on the input are the properties that characterize the performance of a linear system.

In an analytical point of view, considering the system in figure 2.1 defined by an operator Y that maps an input, $x(t)$, as a function of t, to an output, $s(t)$. It is linear if, for the inputs $x_1(t)$ and $x_2(t)$, the system produce the response $s_1(t)$ and $s_2(t)$, respectively, and for all a and b, constant and time independent, the equation:

$$Y(ax_1(t) + bx_2(t)) = as_1(t) + bs_2(t), \tag{2.1}$$

holds for all inputs. In this case, the system obeys to the superposition and homogeneity (degree 1) properties.

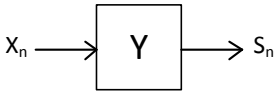


Figure 2.1: *Linear system.*

Distortion and the loss of linearity, in the frequency domain, can be seen as the creation of undesired signal energy at frequencies not contained in the original input signal. This distortion can be produced by amplitude (AM-AM) and/or phase non-linearities (AM-PM).

Amplitude linearity is a measure of how closely the input-output transfer response of an amplifier resembles a straight line [4]. A deviation from a straight line can be represented by a power series:

$$V_{out} = a_1V_{in} + a_2V_{in}^2 + a_3V_{in}^3 + ... + a_nV_{in}^n, \tag{2.2}$$

where a_1V_{in} is the linear amplified original waveform, the product that respects the superposition and homogeneity properties, and the rest are the harmonic distortion products.

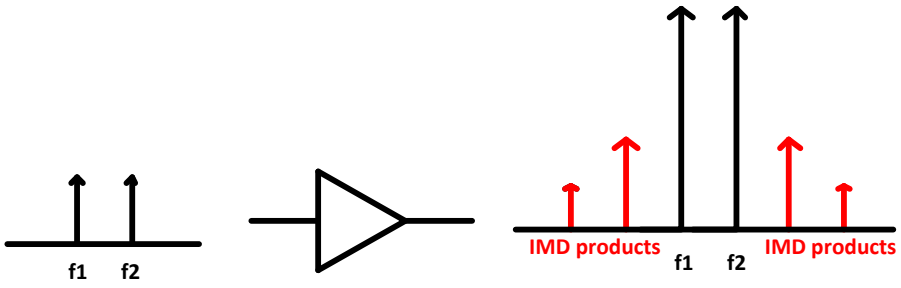


Figure 2.2: *Amplifier output.*

For a single tone, these harmonics may be eliminated by filtering. However, for a multi-tone input signal, this is not so straight forward since, there will be mixing products that will fall into the bandwidth of the input signal. These unwanted signals are known as intermodulation (IMD) products and cannot be easily filtered since they can be near to the desired input signal.

Some of the odd IMD products will fall inside bandwidth, IM3 and IM5 are the third and fifth order intermodulation products which are the most important ones since they are the strongest distortion products.

Phase non-linearity or AM-PM, also contributes to an increase of the system distortion.

In an ideal system, when a signal passes through an non-linear amplifier, the output signal can suffer from phase impairments. The amplifier always introduces a shift in time (phase angle) and although, the phase-shift or time delay should be constant for all power levels of a certain device, there can be a substantial change in phase with the power level. This change will transform the phase variation in the signal level into phase modulation. This issue will take the distortion problem to a different level where the unwanted phase modulation side-bands contribute to the IMD, increasing the unwanted frequencies amplitude.

Thus, phase non-linearity produces IMD products like amplitude non-linearity. To try to circumvent this problem, some techniques can be applied to the system. This is the topic of the next section.

Along this report, the overall circuit will be evaluated according to the classical non-linear metrics such as harmonic level for a single sinusoidal level or P1dB, because of its generality, and intercept point analysis. However, the existing analysis methods have many limitations such as providing necessary information for linearity analysis of a generic modulated input signal with an arbitrary crest factor. In [5], Foad describes a different linearity analysis approach that approximates a system for digitally modulated signals. This analysis will not be applied to the results of this thesis however it could be used in further studies using the same linearization technique, for any specific modulation and for any particular application.

2.1 Linearity and Efficiency Improvement Techniques

In this section, a detailed analysis is made for each technique and later, a comparison between them is presented. After a brief explanation of how each works, its advantages and disadvantages are listed according to the purpose of the project that is being developed.

As Cripps once said [6]:

"Some, if not all, of the linearization goals which challenge the modern RF designer become relatively trivial if efficiency is removed from the equation: (...)"

Even if the main purpose is linearity, barely nothing can be reached if the amplifier doesn't have a usable efficiency ratio. Therefore, as one will see, trying to increase the efficiency of the RF power amplifiers, also the linearity will improve. Further, even a highly efficient and linear setup would be of no practical use if the output power is so much decreased that the system would become too bulky/costly to reach the desired transmitted power. The target is thus to reach the best trade-off between linearity, efficiency and output power.

It is worth to note that all the techniques that will be presented below need a well matched circuit. Only with matched systems, good linearization marks can be obtained. Also, these methods not only improve the linearity and efficiency but also contribute to a more reliable system (semiconductor reliability being highly impacted by temperature rise), for low overall costs (prime power and cooling systems weighting in the overall system cost).

The methods presented here try to improve the non-linear characteristics in gain and phase transfer function of the Radio Frequency High Power Amplifier (RF HPA). All amplitude (AM/AM) and phase (AM/PM) distortion generate at the output harmonics, intermodulation products and phase modulation leading to adjacent channel interference and loss of transmission fidelity. Trying to reduce these issues can be very hard-working!

After the introduction of the back-off technique, the next three techniques presented are more considered as methods to improve efficiency rather than linearity. These techniques came up to try to solve the low efficiency of the power amplifier when backed-off.

2.2 Back-off technique

This technique circumvents the non-linear effects by backing-off an amplifier's output power operating point relative to saturation.

Back-off method is the most simple method to apply and a reference to other techniques. However, it cannot be improved or give such good results as the others.

Advantages

-Simple: no additional components are required,
-Can be combined with other techniques,
-Less thermal dissipation due to the reduction of the output power,
-Maintain the same bandwidth.

Disadvantages

-Efficiency decreases,
-Reduced power added efficiency which increases the demand on power supplies.

2.3 Doherty

In the early era of radio broadcasting, Mr. Doherty proposed a new method to improve the thermal and cost issues of the RF amplifier. Back then, a transmitter that could deliver tens of kilowatts would consume an enormous amount of power, thus some care should be taken in power conservation area.

An efficiency enhancement was the starting point. In 1936, Doherty [7] proposed an active load-pull technique based on a two amplifiers schematic that acted as a variable load.

Superficially, this technique makes use of the "resistive properties" of the transistor applied in a non-conventional way together with an impedance inverter and a RF output load.

Regarding figure 2.3, it is possible to vary this load seen by the other amplifier by applying current from a second phase coherent source.

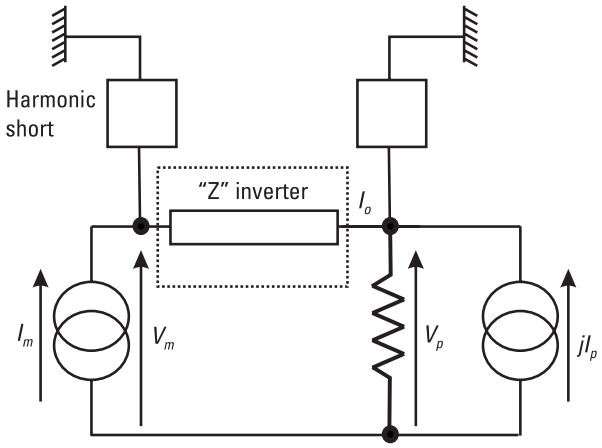


Figure 2.3: *Doherty technique [6]*

The impedance inverter is only used to do a 90 ° phase-shift whose terminal characteristics have the form

$$\begin{bmatrix} V_p \\ I_p \end{bmatrix} = \begin{bmatrix} 0 & jZ_o \\ 1/(jZ_o) & 0 \end{bmatrix} \times \begin{bmatrix} V_m \\ I_m \end{bmatrix}.$$

Assuming that both active devices conduct different currents, and naming one amplifier as "main" and "auxiliary" to the other and by Kirchoff's theory, the voltage appearing across the load resistance is

$$V_L = R_L(I_m + I_p).$$

If the two devices have different bias conditions, the two behaviours can be combined. Using, for example, a "main" class AB amplifier and an "auxiliary" class C amplifier, when the main device is conducting, the auxiliary is inactive and when the auxiliary is active, the main device is held in a constant maximum voltage condition (saturation region). This is the reason why the auxiliary amplifier is also called peaking amplifier.

This can be achieved thanks to the load resistance whose effective value decreases dynamically with increasing the drive level due to the pulling effect of the auxiliary amplifier. Thus, maintaining maximum voltage swing and efficiency [8].

Doherty keeps the linearity of the main amplifier while improves the efficiency for lower input values and from 6 dB back-off (0.5 setting in figure 2.4) up to full power, the efficiency is almost constant.

However, most of the power in this region is given by the peaking amplifier, the dependency of the output power on the input drive signal remains as defined by the main amplifier which can be much more linear, in this case [8]. Although the main device is kept below clipping levels by the action of the auxiliary device, it tends to neglect the quickly rising of the main amplifier voltage, as can be seen in figure 2.4 where V_p represents the output voltage of Doherty's implementation.

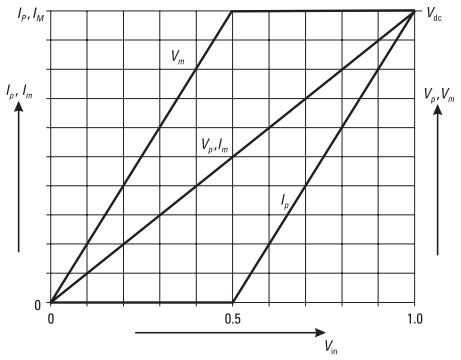


Figure 2.4: *Output curves of the main and auxiliar amplifiers - Doherty technique [6]*

Nevertheless, when both transistors are combined, the IMD performance is impaired. To minimize this effect, N-way Doherty can be used.

The N-way Doherty amplifier is basically the parallel between one carrier amplifier (main) and N-1 numbers of auxiliary amplifiers.

This way, it seems that the use of more devices enables a flatter efficiency over a wide range of Power Back-Off (PBO) because both amplifiers can be driven more in BO and therefore, they will operate more linearly [9] without sacrificing the PAE. However, the greater is the N, the higher biases are required (in order to optimize linearity) and the load modulation is reduced thus, the efficiency improvement of the device is reduced.

In the end, the final maximum RF output power will be the sum of both amplifier's power.

Advantages
-No feedback,
-Simplicity of the circuit,
-Easy configuration, easy to understand,
-Low cost RF circuit,
-Wide bandwidth when compared with EER and Linearity With Non-Linear Components (LINC),
-Most of the output power in the upper range is being supplied by the auxiliary device (a non-linear device will better suit) and the dependency between the output and the input drive signal is defined by the main device characteristic (the more linear the better!).

Disadvantages
-Two amplifier are required: space? power?

2.4 Outphasing or LINC

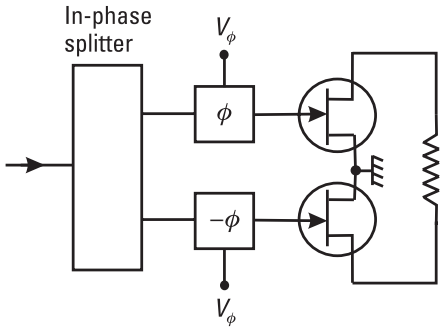


Figure 2.5: *LINC PA configuration [6]*

Also called efficiency-boosting technique, was firstly introduced by Chireix.

Like Kahn EER approach (explained below), this method is based in a transmitter architecture which constructs the required signal at a high power level.

This technique seems to have left behind a legacy of misunderstanding and misconception in the industry as to exactly what the technology has to offer [8]. However, a brief attempt will be presented next.

Two similar RF amplifiers, that can be highly non-linear, will operate at a fixed RF power level.

Figure 2.5 shows two devices, operating in a different class, connected to a same load resistor. The input signal will be split and each will pass through a differential phase shifter, each element has at least 90 ° range. The linearization effectiveness of the method will depend upon two characteristics.

The **first** is the relation between the output voltage and the phase offset. The dependencies on the angle ϕ are:

$$v_o = V\cos(\theta - \phi) - V\cos(\theta + \phi),$$

where V represents the amplitude of the RF sinusoidal of each device.

The voltage in the terminals of the RF load is

$$v_o = 2V\sin(\theta)\sin(\phi).$$

If the phase of the phased shifters could be

$$\phi = k\sin^{-1}(V_\phi),$$

where V_ϕ is the drive signal applied to the phase-shifter, linear changes in the drive signal V_ϕ would produce linear changes in the PA output amplitude.

The **second** is the load-pulling effect.

The impedance viewed by each device as the outphasing angle varies. Taking a deep analysis (fig.2.6), one can conclude [6] that depending on the angle, the load impedance changes and may become highly reactive. A trade-off between the behaviour of the load and the angle value must be done.

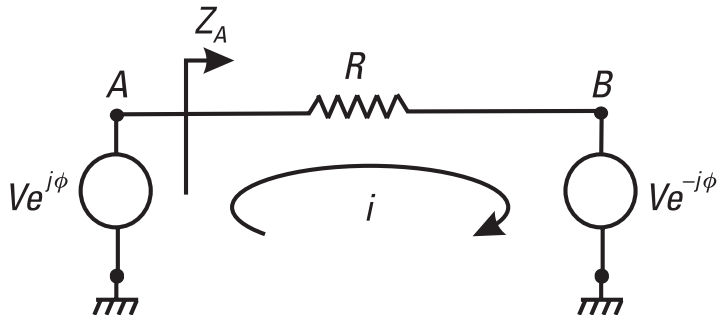


Figure 2.6: *One of the Chireix analysis [6]*

Advantages
-Both amplifiers can be highly non-linear (more efficiency) as opposed to Doherty approach,
-Load modulation can take place between the two active RF devices, which leads to an improved PBO efficiency [8],
-With a digital Look-Up Table (LUT), the resulting amplifier can be very linear [8],
-Do not dissipate too much heat;
-Twice the power.

Disadvantages
-Limited dynamic range is available, especially if reactive compensation is used,
-Calibration required (especially when dealing high dynamic range),
-Complex.

2.5 EER

More considered an efficiency enhancement technique, EER preserves the phase modulation as well as the amplitude.

With this method, Kahn tried to improve efficiency and linearity simultaneously.

In figure 2.7 a simple schematic of the technique is presented. Kahn demonstrated that if the phase and envelope of the input signal were separate and the envelope signal was used to control the high voltage controlled supply of the PA, efficiency and linearity would be conquered. He also proved that passing the phase modulation of the input signal through a limiter, it would be preserved.

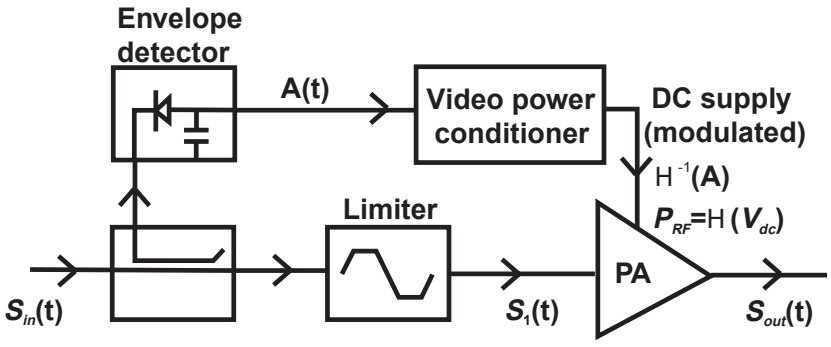


Figure 2.7: *Envelope elimination and restoration technique [8]*

In the schematic, the top branch has the envelope detector that is connected to the power supply of the amplifier and the down branch has the limiter that just let phase modulation pass through. Phase modulation signal will be amplified according to the controlled voltage supply, "restoring" the envelope amplitude of the input signal. The envelope amplitude will be proportional to the modulating supply voltage.

This way, the PA can be saturated and non-linear. Since the power supply is reduced the efficiency can remains constant.

Advantages
-The amplifier can work in the saturated zone as in the outphasing approach, the efficiency of the amplifier remains constant as the voltage supply is reduced,
-"Immune" to RF BW and matching issues unlike outphasing and Doherty,
-Uses a limiter which eliminates the possibility of a AM-PM distortion in the non-linear RF PA.

Disadvantages
-Necessity of a perfect alignment of the envelope and phase signal in the amplifier,
-Large envelope variations can drive the RF PA into cut-off–distortion,
-Extreme wide bandwith is needed to cover the amplitude information,
-Amplifying the detected envelope signal to modulate the PA device will consume a huge amount of power.

2.6 Predistortion

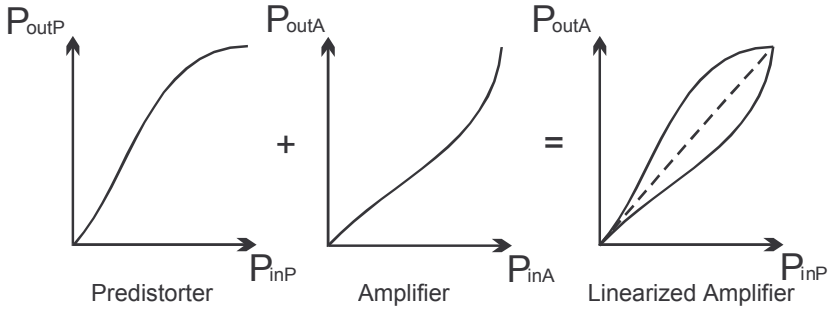


Figure 2.8: *Predistortion principle [10]*

The idea is to include at the input of the PA, a small box that will provide linearization (fig.2.8) and will consume little power. Of course, it seems too simple to be true however, good performances are being obtained [11] [12] in a certain range.

The traditional idea of the predistortion technique is open-loop so, it cannot be straightly compared to the closed-loop systems, one must have in mind that a limited Bandwidth (BW) range needs to be fixed. Also, an increase of the Peak-to-Average Power Ratio (PAPR) at the PA input can be experienced (gain expansion).

The main goal of predistortion is to behave to counteract the PA saturation effects, without interfering in the rest of the circuit. For example (fig.2.9), for a simple input signal V_{in}, the non-ideal amplifier response shows some compression, V_a; an ideally amplifier would give an

output as V_o. So, to have a similar effect to the latter case, the predistorter will increase the input level V_{in} to a higher level V_p.

There are three different types of predistortion: analog, digital and adaptive baseband. Each, with different degrees of success.

Nowadays, Digital Predistortion (DPD) is being more and more routinely used.

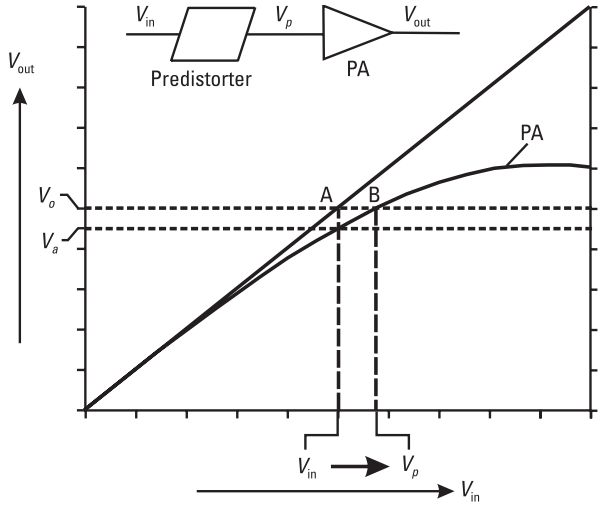


Figure 2.9: *Predistortion technique [6]*

Advantages
-Work with baseband, IF or RF signals,
-Can be implemented with passive components,
-Have a moderate performance compared with other techniques,
-Simply circuitry and lower power consumption compared to Feedforward (FFW) technique [11],
-Stable performance and wider BW compared to Feedback (FB) techniques [11].

Disadvantages
-Increases the BW of the signal that is input to the PA because of the distortion components that will be added to the signal when the drive signal passes through the predistorter − BW expansion,
-When the amplifier saturates, a point with no return is achieved. No matter if the input is increased, the output cannot be restored.

Analog Predistortion

There are two types of analog predistorters. The "simple" one, which usually is a configuration of one or more diodes, and the "compound" predistorters which synthesize the required non- linear characteristics using separated sections to generate the various degrees of distortion.

This is, whereas the "simple" predistorter relies fundamentally on selecting and/or tailoring the non–linear characteristics of the PD device to match, or cancel the PA non-linearities; the compound PD uses a less familiar concept [6].

Diodes, a FET channel or the saturation characteristic of a mesa transistor [1]are examples of simple predistorters. Figure 2.10 illustrates diodes acting as a predistorter: for low input levels, the attenuation is determined by R_a, the diodes do not conduct; for higher drive levels, the diodes start to conduct and a lower value resistor is shunted across the first resistor causing lower amplitude attenuation.

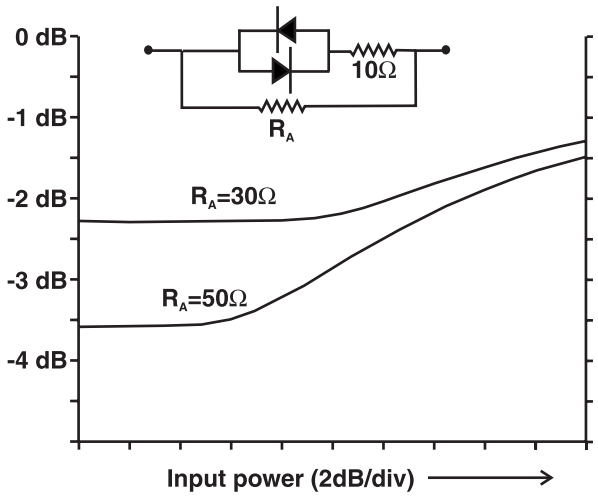


Figure 2.10: *Simple predistorter [8]*

In this case, the use of a shunt capacitance can settle the phase shift (AM-PM).

The "compound" predistorters are more complex than a circuit based on diodes and resistors, as can been seen in figures 2.11 and 2.12. They do not rely on the non-linear elements, they have already specifically tailored characteristics.

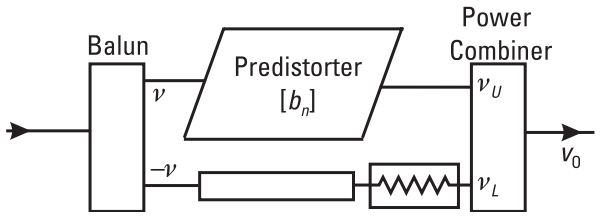


Figure 2.11: *Cuber technique [6]*

Below, one approach of this method is presented.

The method presented in picture 2.11 is known as compound cuber. The basic concept is: the input signal is split, one will pass through a non-linear amplifier and the other by a phase-shifter (180 °) and by an attenuator. After separation, the input signal of the second branch will be phase-shifted 180 ° due to the effect of the balun however, after the phase-shifter the signal will be again in phase with the first branch one. After each signal travelled in each path, both signals will be combined using another balun. Since the combiner will introduce another phase-shift in the second signal, the output will only contain components proportional to the third-, fifth-, and so forth degree powers of the input, the linear components will be cancelled out due to the second path.

[1]**Mesa transistor**- has a general appearance of a saturating MESFET I-V characteristic, but without the gate control.

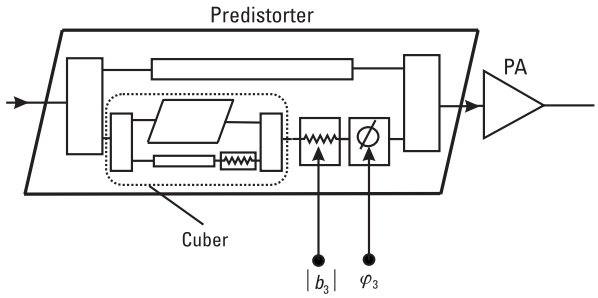


Figure 2.12: *Analog predistorter [6]*

Thereafter, a basic schematic combining the cuber with some other components (fig.2.12) can be drawn in order to obtain a matched third-degree predistorter (assuming that, for BW concerns, only the third degree order distortion term is important, further orders can be neglected).

As depicted in figure 2.12, the input signal is split and then, one part will go into the cuber to be added later with the input signal. After the signal passes through the cuber, it will be phase-shifted and its amplitude will be scaled in order to reduce the distortion introduced by the PA.

At the output of the predistorter, the signal will be formed by the fundamental signal plus the third, fifth, ..., –degree distortion coefficients shifted 180 °. Thus, these distortion spikes will attenuate the ones generated by the PA.

Advantages
-No feedback technique,
-Both methods can correct the amplitude and phase distortion introduced,
-Can be combined with most of the other methods of linearization,
-Control methods can be used to set the third order coefficients in the predistorter.

Simple predistorter
-Simplicity.

Compound cuber
-Ability to generate a precisely scaled and phased 3rd degree effects in the PA,
-Robust linearization performance which consumes little or no power.

Disadvantages
-The stability of various attenuation and phase settings over environmental and input signal conditions.

Simple predistorter
-Less reliable than compound cuber.

Compound cuber
-As for FFW, it is needed to take care and attention to the adaptive software monitoring system,

-Complex Hardware (HW) compared with DPD technique,
-Bandwidth of the circuit depends upon the bandwidth of the several components of the cuber,
-High non-linearities still remains (changes in the cuber can be made in order to avoid those).

Digital Predistortion

Digital Predistortion is an open loop technique, as said before. The figure below shows the first circuit of DPD.

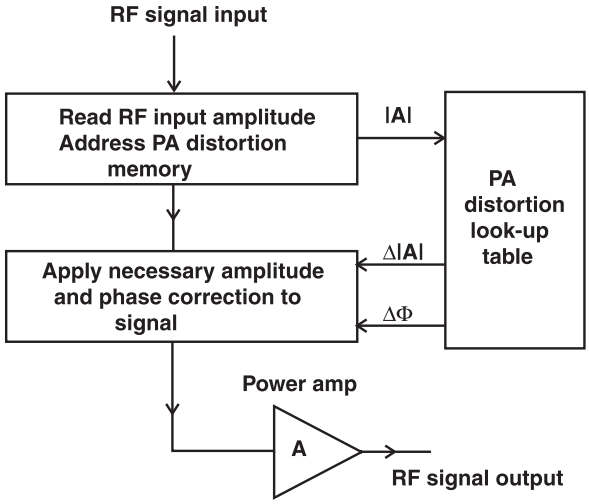


Figure 2.13: *Digital predistortion technique [8]*

It is based in a digital table that stores all the data related with non-distortion behaviour when the RF input signal passes through the first box ("PA distortion LUT"). This box gives the information about the characteristics (amplitude and phase) of the input signal. After, the LUT will provide the amplitude and phase corrections to the signal before it goes into the PA, to compensate the distortion of the power device.

The LUT is the key aspect of this technique. It includes the PA predistortion requirements, the modulator drive requirements and a single composite table entry for an appropriate density of RF drive levels. Thus, it is very important to know how does the device behaves in time. Temperature effects, aging and environmental issues can affect the LUT performance as well as the thermal dissipation can cause some hysteresis and asymmetry. To avoid those problems, one can always try to develop a dynamic LUT refreshing system, thermal problems are defined physically thus can be included into the non-linear models [6].

Also, the calibration of LUT is really important.

Besides that, this technique also suffer from memory effects. To sidestep that issue some improvements are usually done: addition of an adaptation loop in the DPD system which enables continuous monitoring of the linearization integrity and LUT refreshing or use of a DPD algorithms– LUT becomes a Digital Signal Processing (DSP) unit (LUT plus a processing unit) which can correct short-term memory effects through the inclusion of some of the recent "history" of the signal as can be seen in figure 2.14.

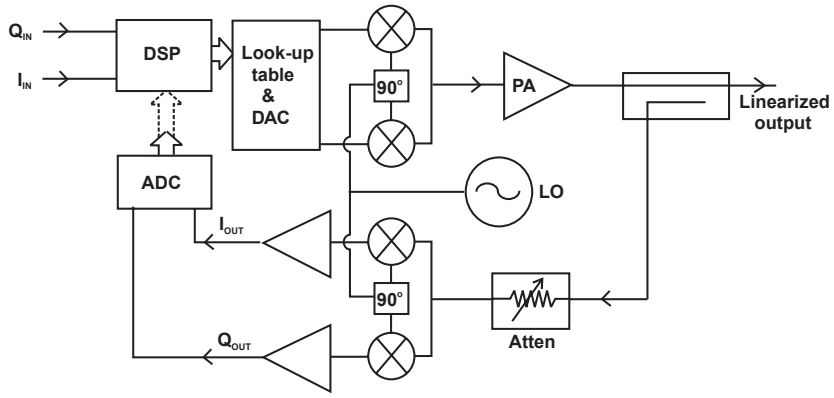


Figure 2.14: *Digital predistortion improvement technique [8]*

With those improvements, fig.2.14 may look like a system with a FB loop however, the LUT refreshment is too slow compared with the feedback loop.

Advantages
-More precise, robust and reliable then RF Envelope FB – more Intermodulation Distortion (IMD) suppression than with analog predistortion,
-Can be build with or without a feedback loop – with feedback, do not need an algorithm to compensate thermal effects,
-Can be combined with almost all techniques,
-Allow amplitude and phase correction.

Disadvantages
-More complex than RF Envelope FB – moderate complex in Linearity Improvement Technique (LIT)s scale,
-Used for an entire transmitter circuit,
-Analog envelope detectors can be a problem when generating the input signal control (accuracy, bandwidth, . . .),
-High sensitivity to delays between the control signals generated by the digital circuitry and the RF signal,
-Any change in the PA characteristic that are not predicted in LUT will rapidly degrade the correction process,
-Can suffer from memory effects,
-Require a prior knowledge of the signal modulator in digital form and a phase coherent sample of the RF carrier used to perform the down conversion,
-At lower levels of PBO, if corrections become small numbers, they will be followed by an increase of precision required from the control signal (with a Digital-to-Analog Converter (DAC) in the circuit, more bits mean less speed!),
-Bandwidth is limited by the digital circuit,
-It entails more requirements and limitations to data converters related with the number of harmonics that the correction signal needs to contain to perform the required predistortion function,
-LUT needs calibration,
-LUT components determine the speed of the system,

-More power consumption due to LUT when compared to analog predistortion.

Adaptive Baseband Predistortion

This technique is a version of digital predistortion. It is a closed loop technique and the predistorter block is a combination of Cartesian FB and a DSP.

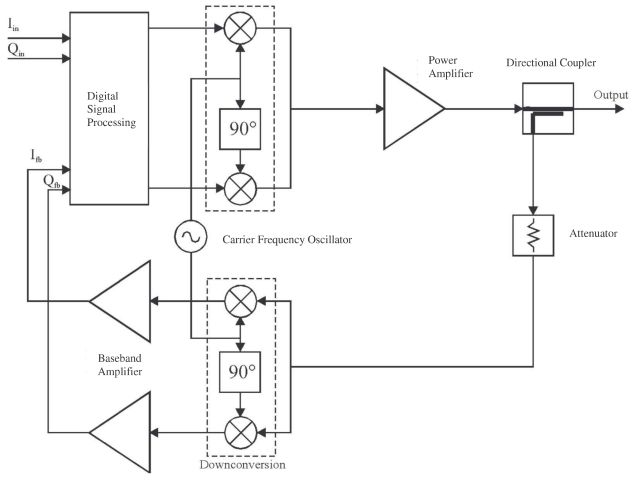


Figure 2.15: *Adaptive baseband predistortion technique [10]*

As depicted in schematic 2.15, I and Q signals, at a baseband level, are fed into the DSP block. The DSP block works as a warehouse as it stores weighting coefficients that can be update by the new coefficients derived from the FB loop. These coefficients will create the predistortion signal when added to the I-Q input signal. The signal is then up-converted and amplified by the PA. Most of the (dis)advantages of the DPD are suitable to this case.

Disadvantages
-Complex compared, for instance, with analog predistortion,
-Bandwidth limitations,
-Accuracy of the DSP,
-More power consumption due to the DSP unit.

2.7 Feedback

These three methods present, next attempt to reduce the non-linear effects by using a well know method: feedback.

Negative feedback

Generally speaking, negative feedback creates stability and improves accuracy as it is used to eliminate or reduce unpredictable behaviour of the circuit.

This method can be rapidly described: a sample of the output is inverted, attenuated (gain of FB loop) and used to correct the input signal. The sum of the input and the FB

signal will result in an input version with less distortion that will be amplified again by the forward amplifier.

The linearity of the device is given by the way that each system preserves the amplitude and phase distortions of the RF carrier, it is clear that FB techniques should be applied at the baseband rather than RF carrier frequencies.

Below will be introduced two of some FB techniques that are mainly used in the market.

Envelope feedback

As can be seen by the picture 2.16, a video amplifier generates an error signal by the subtraction of both envelope signal of the input and output (they are considered envelope signals after the envelop detectors). The output signal of the video amplifier will control the gain of the main amplifier that it is working below saturation. Thus, an improvement of the spectral distortion may be obtained.

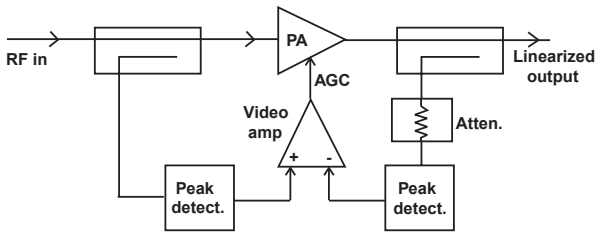


Figure 2.16: *Envelope FB technique [8]*

The main difference between this method and the direct FB is easy to see using small signal, whereas the first uses gain control, the second just controls the input signal by subtraction of the FB signal.

As said before (fig. 2.16), this method cannot be implemented at the end due to the feedback. FB adds some important effects that damage the transmission namely the latency. In [6], Cripps says that latency could eventually be solved if one could combine smaller PA modules (small devices have lower Q-factor) that will scale down in a linear fashion as the power, or number of cells paralleled on the die, decreases.

Advantages

-Simplicity and compactness of the RF detectors compared with the Cartesian FB circuitry (fig. 2.17),
-Compared with direct FB, the problem of delay is alleviated due to the use of envelope signal,
-Thermal effects compensation.

With output power control:

-Free from limitations of predistortion: the control does not itself introduce additional higher-degree effects.

Output power control disadvantages:

-If the controller is a voltage controlled attenuator, there will be a residual attenuation setting in the linear region, in order to provide suitable linearization range [9].

Disadvantages
-With feedback loop,
-Only has an amplitude correction loop: "(...) RF PA distorters, the required amplitude correction at the input escalates as the compression region is reached. This means the AM-PM will be degrading simultaneously as the input amplitude controller strives to correct the gain compression." [6],
-Amplitude correction will introduce phase distortion,
-The envelope detection process generates video signals which have higher BW than the original modulation BW (easily to visualize with a two-carrier RF signal),
-Losses in the power amplifier (but, also FFW technique suffers from that),
-Simple envelope amplitude correction cannot increase the intrinsic power saturation of the device so, the efficiency of the circuit just decreases as the envelope swings into the compression region,
-Delays introduced by the peak detection plus video amplifier can be really hard working and increase with bandwidth,
-For low power levels, the gain of the video amplifier must become higher which may lead to bandwidth and stability problems.

Cartesian feedback

To sidestep the disadvantages of the previous technique, Cartesian FB has been developed. Cartesian FB forces the amplitude and phase of the output to be an amplified version of the input signal, unlike Envelope FB.

From figure 2.17, one can see that a separate I and Q signals are fed through different correcting amplifiers and into I-Q modulators. These modulators will form the RF signal $S(t)$,

$$S(t) = I(t)\cos(w_c * t) + Q(t)\sin(w_c * t),$$

where w_c is the RF carrier frequency.

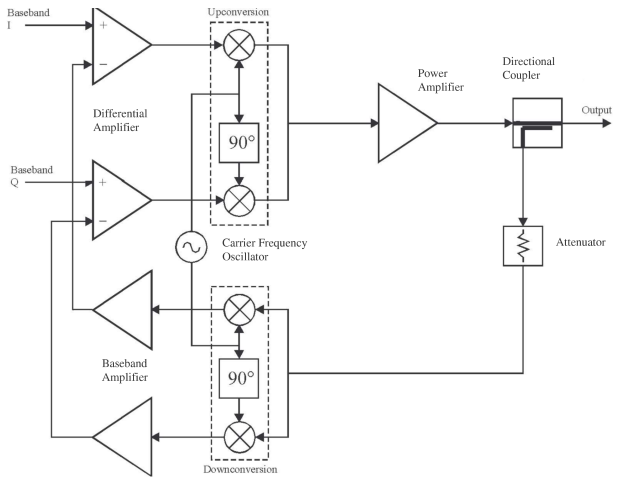


Figure 2.17: *Cartesian FB technique [10]*

This signal is fed into the input and will emerge, with some distortion, at the output, reason to couple the output signal into a downconverter which retrieves the distorted I and Q signals. These signals are directly compared with the undistorted input baseband signals and then, the FB mechanism will force the loop to generate an output signal similar to the originals I and Q at the input.

Therefore, the correctness of the output depends on the gain and the bandwidth of the video circuitry and on the linearity of the downconverter de-modulators.

Advantages
-As the input signal is treated as a I-Q signal, both channels can be processed in well-matched paths, each of which has a BW comparable to the input signal,
-Thermal effects compensation,
-Symmetry of gain and BW in two input paths (asymmetry is one of the main reason of IMD) leads to reduction of the phase distortion between AM-AM and AM-PM processes,
-Amplitude and phase correction.

Disadvantages
-Has feedback loop,
-Implemented for an entire circuit,
-Implement amplitude and phase correction with the cost to work at baseband (or IF) frequency to perform the comparisons between input and output plus the error amplification,
-Video BW and stability precautions limit the capability to handle multi-carrier signals,
-Delays between both paths may produce huge damages: higher the frequency, more delayed is experienced thus the FB system can become unstable at higher frequencies: unwanted oscillations [1]. This problem can be prevented, limiting the BW.

2.8 Feedforward

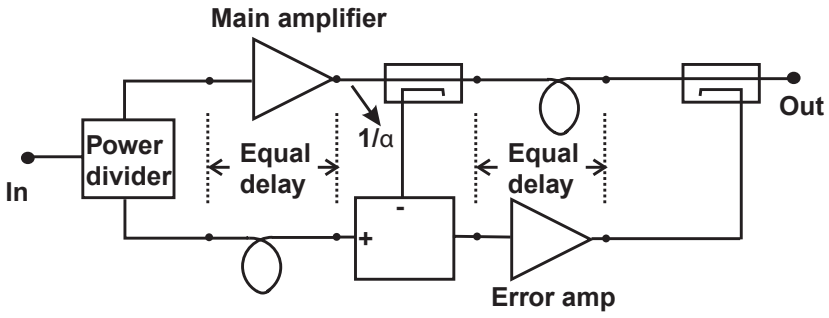


Figure 2.18: *Feedforward technique [8]*

Feedforward is an old technique based in a method similar to the feedback one except that the correction of the signal is applied at the output rather than to the input.

In fig. 2.18 is illustrated the main concept of this technique. Firstly, the input signal is split using a power divider, half of the signal is amplified by the main PA and the other half is delayed and added with a coupled sample of amplified signal that is 180 ° out-of-phase. This will create an error signal with the distortion produced by the main amplifier, including

compression, AM-AM and AM-PM effects. It is important to note that the distortion is 180 °out-of-phase when compared with the amplified signal.

Then, the error signal will be amplified back, by Error Power Amplifier (EPA), to the original level of the amplified signal of the first branch and recombined with a delayed version of it.

Thereby, this approach offers the benefits of FB without the instability and bandwidth issues [8], allowing a deep concentration around the need to maintain accurate gain and phase tracking.

At the end of the system one would have the amplified version of the input signal which means that the bandwidth will only be limited by the tracking capability of the system. Even though, there are some problems that could appear and distort the efficiency of this method.

The delays between paths, distortion of the error amplifier,... can be really troublesome.

There are some variations from the common FFW technique that try to improve some of those issues: in [6] is suggested to double the FFW loop in order to deal with tracking errors more easily; FFW enhanced power combiner – using EPA and PA with the same gain, an increase of the input power by 3 dB is observed and the EPA additionally generates some correction.

Advantages
-No feedback method,
-Immune to memory effects due to the error corrections in real time.

Disadvantages
-Bandwidth depends upon the tracking capability of the system (it can handle modern wide-band multi-carrier signal linearity specifications [6]),
-Two amplifiers are needed,
-The corrections of the signal need to be amplified up to the necessary higher power level - a relation between the amplitude capability of the main and error PA must exist,
-Error amplifier will introduce nonlinear contributions: most of the tracking errors will appear from the gain and phase variations in the error amplifier over frequency and temperature oscillations,
-The correction signal is dependent on the precision with which this tracking can be maintained over frequency, temperature, time and load characteristics; high accuracy in gain, phase and delay needs to be maintained in all the system,
-Power wastage due to the coupling factor of the last coupler: since the error amplifier needs to compensate this coupling factor, lower values of the factor will require a higher powerful amplifier; a trade-off must be done between power and distortion caused by the error amplifier,
-Need to generate the correction signal at a much higher level than the originally required for the other methods thus, worse efficiency.

2.9 Dynamic Gate biasing

Dynamic gate biasing presented in [13] helps to reduce IM3 by increasing the gate bias as the device compresses thereby increasing the gain. The entire procedure is described in

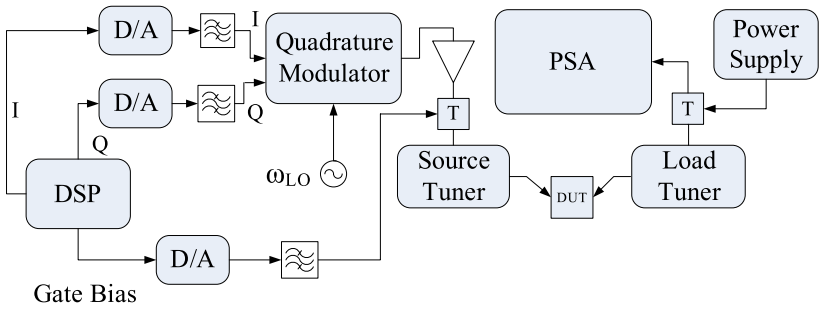


Figure 2.19: *Dynamic gate biasing technique test setup [13]*

the paper mentioned before [13] and shows a reasonable reduction of the IM3 while keeping the efficiency constant. This technique was tested with two tones input and Gallium Nitrate (GaN) HFETs using dynamic gate biasing technique.

Figure 2.19 displays the test setup used in [13], the I-Q input signal are generated and up-converted with a certain tone spacing. The signal is fed into the amplifier (DUT) at the same time that a gate bias signal is generated based on the input, in an open loop fashion.

If the device is tuned to the best matching for a deep class AB bias, the results mentioned before are achieved.

Advantages
-Simple concept, simple implementation,
-Can be combined with other techniques.

Disadvantages
-When the device gets saturated, this strategy loses its effectiveness,
-RF stability,
-High sensitivity: aging and temperature effects can be a serious problem
-Takes extra space.

2.10 Dithering

Or averaging method due to the non-linear characteristics of the output signal: more stable and smoother (less non-linear).

Starting by the meaning of dither, it represents any signal that will be added to the input. Dithers can be periodic or stationary-random functions, analog or digital, correlated or uncorrelated and with frequencies low/above the system cut-off frequency, LFD or HFD respectively. Moreover, if the dither is based in a pseudo-random signal, one can also choose if memory or memoryless.

Regarding each type, for a mathematical analysis to obtain the equivalent non-linearity function a Fourier series can be used: for periodic or low frequency dither, or a statistical averaging series for any kind of dither (pseudo-random or periodic dither).

For a briefly explanation of the technique, it is not necessary to distinguish between LFD and HFD methods, however each approach as particular characteristics ((dis)advantages), listed below.

This open loop technique is very simple to explain, however a deep mathematical research could be needed in order to understand the facts [14]. Dithering relies in an injection of an external signal to a (non)linear system in order to achieve some improvement results, thus it behaves like a moving average filter which smooths the non-linear characteristics of the system.

In paper [15], it is explained and demonstrated that a low frequency dithering improves the non-linear characteristics of the original signal. With a non-linear class D LDMOS amplifier and an input signal at 2.014G Hz, Malekzadeh et all reached an enhancement from 55 to 59 % drain efficiency.

To finalize, in [5], after a fine tuning measurements, the results confirmed that LFD and HFD have the same linearity results however the drain efficiency is improved and the reactive loss is reduced for LFD.

LFD
-The linearization method only will influence the amplitude of the signal thus the system is time variant with respect to the value of the signal,
-With lower frequency than the input signal but should be higher frequency than the envelope BW,
-Envelope amplitude vs non-linear characteristics,
-Reduces the reactive loss,
-Spurious will depend on the frequency of the dither and the input signal,
-The input band pass signal has a maximum bandwidth due to the dither higher order harmonics.

HFD
-It is time invariant with respect to both amplitude and value of the input signal,
-Signal amplitude vs non-linear characteristics,
-Spurious side-bands won't affect the original linearized signal.

Advantages
-Open loop,
-Simply and robust circuitry compared with most linearization techniques,
-Common mode dithering generates in-phase spurious components around the odd order dithering frequency harmonics at the output, which makes the output filter easier to realize [15],
-Can be used to stop undesired behaviour or cycle oscillations in the system,
-Asymptotic stability.

Disadvantages
-For a linear operation, the amplitude of the dither signal must be higher than the amplitude of the input signal,
-The original signal has a maximum bandwidth limitation for the dither may be applied: there is a relation between the frequency of the input signal and the dither ($\approx 1/4$ bellow the input frequency),
-Requires an extra signal.

2.11 Conclusions

In table 2.1 one can find the best performances for each LIT. It is important to mention that all of these techniques were performed for continuous RF waves, contrary to what shall be done in this work. However it is still a rather good approach since almost no work was done in this field, with RADAR pulsed signals.

Table 2.1: *LIT performances.*

Technique	***fc*** (Hz)	**BW**(Hz)	**NL Specs**	**Reference and Notes**
Doherty	2137.5 G ≈2 G	$\pm 5M$ $\pm 5M$	IM3=-60 dBm ACPR=42.5 dBc	[16] [17]
3-way Doherty	2.14 G	$\pm 5M$	ACPR=43.22 dBc	[9]
Cartesian Feedback	1.95 G	$\pm 5M$	ACPR≈50 dBc	[18]
Analog Predistortion	836 M	6M	IM3=IM5=-25 dBm	[11]
DPD	2.4-5 G	$\pm 5M$	ACPR=45.6 dBc	[12]
Feedforward + Predistortion	1.495 G	5M	IM3=-104 dBm	[19]
DPD + Cartesian FB	947.5 M	2K between fundamentals (see note)	SFDR=37 dB	[20]DSB transmission
Dynamic Gate Biasing	814.8 M	200K	IM3=-40 dBm	[13]
Adaptive Baseband	1.8 G	10M	IM3=-17.63 dBm IM5=-35.44 dBm	[21]
EER	100 M	1M	IM3=-40 dBm	[3]
Outphasing	1.96 G	2.5M	ACPR=51 dBc	[2]
Dithering	2.014 G	$\pm 5M$	DSP=30 dBc	[15]

The field "*fc*" represents for the cases with two tones input: the lowest input frequency, for other input cases, the value of the central frequency of the main channel. Respectively, for "BW", for the former case it gives the value between the two tones and for the latter, the distance between the central frequency and one for the borders of the main channel.

IM3 and IM5 are calculate with a power of the fundamental equal to 0 dBm.

Chapter 3

Dithering concept

Previously, some linearity–efficiency techniques were enumerated and explained. Each one of them is used, together with another method or alone, to improve important characteristics of the power element of the transmitter chain (chapter 2).

In this thesis, the goal is to design an amplifier for naval radar applications using dithering as the linearization technique to improve its modulation linearity, while keeping its electrical power efficiency. Therefore, a detailed analysis of the dithering technique will be described in this chapter. Firstly, a general understanding will be written, followed by a mathematical proof of concept.

Dither has been applied in digital systems for many years. Including a wideband noise signal with an amplitude of approximately the step size together with the signal to be quantized is a well-known technique of linearizing the averaged quantizer staircase function. It was firstly employed on mechanical computers on board of planes and lately, extended to analog-to-digital converters and digital audio applications. In [5], a new application is given to the dithering - linearization of SMPAs- and based on his work, a similar method will be applied in a RADAR amplifier.

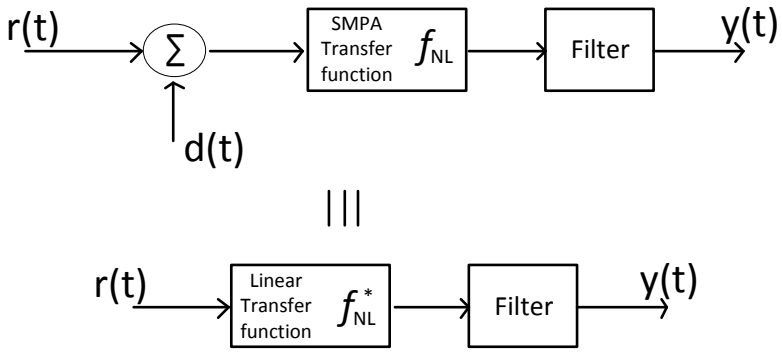


Figure 3.1: *Dithered amplifier (upper branch) and its linearized equivalent (lower branch), with an output filter centered at the frequency of $r(t)$.*

Figure 3.1 shows a block diagram overview of the dithered amplifier. Two input signals are summed and passed through a static non-linear transfer function that resembles a common type of a SMPA (memory effects are not taken into account) and further by a filter. The

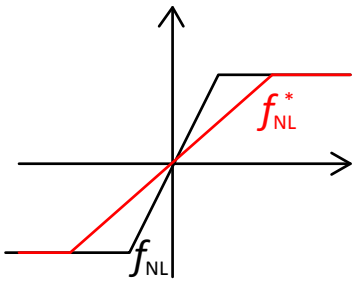


Figure 3.2: *Non-linear transfer functions of SMPA (black) and the dithered system (red).*

combination of the input signal, $r(t)$ with the sinusoidal signal, dither $d(t)$, form the input signal of the amplifier. The output filter is a compulsory element in the complete system since it is responsible for filtering out the dither as well as its harmonics and the intermodulation products of the two tone input signal.

Based on dithering frequency, two different modes can be applied: Low-Frequency Dithering (LFD), in which the dithering frequency is lower than the desired input frequency and High-Frequency Dithering (HFD), where dither has higher frequency than the input signal. The main difference between them is undoubtedly the rate at which LFD and HFD switch. For HFD, the variations of the dither are much higher in frequency than for LFD thus, for the first case, the dithered transfer function is time invariant and these high frequency variations can be easily suppressed by the output filter (fig. 3.1). While for LFD, the dither switching frequency is lower than the input signal which means that it will be slower regarding to the input signal value, the system is time-variant with respect to the RF signal. Therefore, the averaging process, in this case, will be performed on the complex envelope of the input signal: dither frequency should be higher than the envelope bandwidth of the input signal, the system is time-invariant with respect to the envelope of the RF signal. Depending on the nature of the dither, the output filter (fig. 3.1) may be a low pass or a band pass filter in case of HFD or LFD, respectively.

The approach taken in this report is LFD. Using LFD, the prior concern will be the non-linear characteristics introduced in the envelope amplitude of the input signal. Spurious will depend on the relation between the frequency of the dither and the band-pass input signal (explained in more detail in further chapters). Nevertheless, low frequency signals are easier to produce and the reactive power loss associated to the switching frequency of the dither will be lower when compared to HFD.

Analog dither will smoothen the *hard non-linearities of the system*, when it is in compression, by acting like a moving average filter (figure 3.1, lower branch).

In a top-down perspective if, hypothetically, one had only the input signal (r(t)) in the described system, d=0 (fig. 3.1), all dynamics, at the output, would come from the input because the instantaneous non-linear gain will be varying according to the input signal.

When, at the input, there is the same signal but combined with a larger and lower frequency one (dither, d(t)) (figure 3.1), the instantaneous gain of the envelope of the input signal (after the averaging process performed by the filter at the output) will be the derivative of the non-linear transfer function. The output dynamics of the input signal will depend on $r(t)$ but also on the large signal dynamics (dither) because the dither will perform the averaging. The complete picture can be seen like this: the envelope of the input signal can be seen like a vector which is stopped when compared to the dither signal that will move around

it, with $f_r - f_d$ frequency, performing the averaging. The relation between the amplitudes of the input signals is explained below, in section 3.1.

Despite its complex theoretical understanding and the need of an extra input signal in practice, this open–loop technique is rather simple to practically apply. In conclusion, below are listed the two most important limitations of the dither:

- Slope gain: the feasibility of the dither depends upon the zero input slope gain of the block. As long as the PA has a high slope gain, it can be dithered. Therefore, all kinds of SMPA may suit to apply this technique. If the gain is not enough, the dithered gain may drop a lot due to dithering which, consequently will decrease the power added efficiency (gain of the dithered system decreases with the amplitude of the dither). Therefore, it's understandable that the dithering doesn't work so well with linear PA classes, such as A, AB, C or J.

- Reactive power loss: Both high frequency dither and lower frequency dither smoothen the gain function of the amplifier, however applications that use HFD will always lower the efficiency compared to the system without dither. This happens because the higher frequency of the system determines the zero crossing frequency of the output voltage or current and the reactive power loss: CV^2f or LI^2f, if f is higher so the reactive loss will be. While in a HFD, the dither sets the zero crossing frequency, for LFD case, the zero crossing frequency will depend on the frequency and the level of the dither (explained below).

In fig. 3.3, the zero-crossing frequency is plotted versus the ratio between the signal amplitude, r, and the dither amplitude, A. This figure tends to explain the second topic mention above. One can see that, for a LFD system, as the dither amplitude increases, the zero crossing frequency will drop effectively (approaching to the frequency of dither) and so, the reactive power loss will decrease as well. Important to note that the drop in the CV^2f loss value strongly depends on the capacitor C, which is dependent of the process technology [14]. Thus, the more parasitics will have in the process technology, a stronger improvement in the reactive power loss will be noticed.

Hence, performing LFD will reduce the switching frequency so, the loss due to the reactive power will always be less.

3.1 Mathematical proof

This section presents an analytical method to characterize a SMPA, excited by a random input signal, with Gaussian statistics. Both Gelb, in [22], and Foad [5] did a similar analysis but in a more complex way.

Assuming that the system has a static non-linear input-output transfer function that matches the one represented in fig. 3.4: such described system will have a wide spectral output. Note that the system described in fig. 3.4 is ideal, in practice the amplifier won't be only saturated or turned off, it will have a short linear part between the off state and saturation.

The total output of the system can be written as

$$y(t) = y_c(t) + y_u(t) \tag{3.1}$$

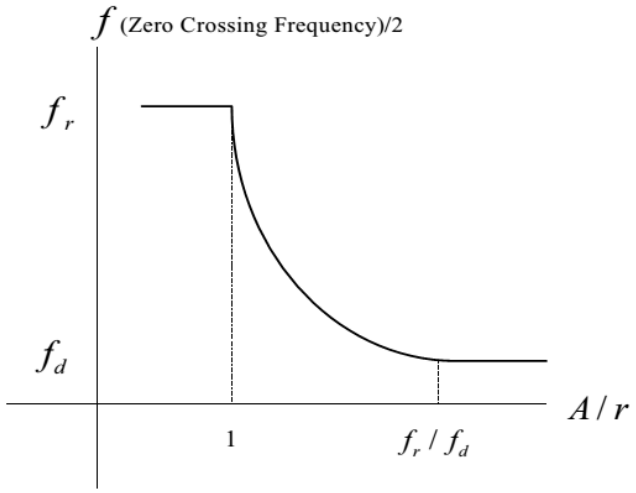


Figure 3.3: *Zero switching frequency versus ratio of dither over input signal amplitude [14].*

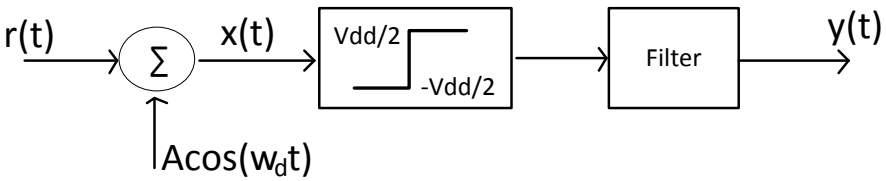


Figure 3.4: *Block diagram of a dithered system.*

where y_c and y_u represent the correlated and uncorrelated outputs. Assuming that the correlated part only represents the linear output of the system while the uncorrelated part characterizes the non-linear behaviour of a SMPA. If a proper selection of the input is done, the spurs won't interfere with the desired signal bandwidth. Therefore, assuming there is no memory effect associated and the system behaves according to this formulation:

For a band limited random input, $r(t)$ (desired RF signal) with a sinusoidal component with a different frequency, $A\cos(\omega_d t)$ (d stands for dither), the instantaneous gain of the system can be expanded in a Fourier series in time as follows:

$$\begin{aligned} y(t) &= f_{NL}(r(t) + A\cos(\omega_d t)) \\ &= g_0(r(t), A) + \sum_{i=1}^{\infty} g_i(r(t), A.\cos(i\omega_d t + \varphi_i)) \end{aligned} \tag{3.2}$$

where the input frequencies are non-commensurable.

According to eq. 3.2, the non-linearities of the system can be divided in two: g_0 represents the non-linearity transfer function zone which represents the linear amplification of the input signal plus the non-linear distortion around it and its harmonics, assuming that the frequencies components do not fall into the band of interest. The second part represents the spurious components around the dither signal and its harmonics. This second part can be neglected

by the use of a proper filter; for LFD, it is of high importance to have a band-pass filter at the output of the amplifier to supress the dither frequencies as well as its harmonics and intermodulation products with the RF signal.

After the band-pass filter, the first part of the eq. 3.2 is what remains.

For an ideal limiter with quantizing step $V_{dd}/2$ and in one dither period, T_d,

$$g_0(r(t), A) \triangleq \frac{1}{T_d}\int_0^{T_d} f_{NL}(r(t) + A\cos(\omega_d t))dt \tag{3.3}$$

Using a *sign* function as non-linear function, g_0 becomes,

$$g_0(r(t), A) = \frac{1}{2\pi}\frac{V_{DD}}{2}\int_{-\pi}^{\pi} sgn(r(t) + A\cos(\theta))d\theta \tag{3.4}$$

If

$$a = \int_{-\pi}^{\pi} sgn(r(t) + A\cos(\theta))d\theta \tag{3.5}$$

$$= \int_{-\pi}^{0} sgn(r(t) + A\cos(\theta))d\theta + \int_{0}^{\pi} sgn(r(t) + A\cos(\theta))d\theta \tag{3.6}$$

By a change of variables,

$$a = \int_{-\pi+\sin^{-1}(\frac{r}{A})}^{-\sin^{-1}(\frac{r}{A})} -d\theta + \int_{-\sin^{-1}(\frac{r}{A})}^{\pi+\sin^{-1}(\frac{r}{A})} d\theta \tag{3.7}$$

$$= \begin{cases} 4\sin^{-1}(\frac{r}{A}) & \text{if } \mid r \mid \leq A, \\ \pm 2\pi & \text{if } \mid r \mid > A. \end{cases} \tag{3.8}$$

Thus, the quasi-static representation of a limiter with a sinusoidal dither of amplitude A is,

$$g_0(r(t), A) = \begin{cases} \frac{V_{DD}}{\pi}\sin^{-1}(\frac{r}{A}) & \text{if } \mid r \mid \leq A, \\ \frac{V_{DD}}{2}sgn(r) & \text{if } \mid r \mid > A. \end{cases} \tag{3.9}$$

Then, the correlated output is the linearly amplified input, as long as $\mid r \mid \leq A$. In figure 3.5, the new non-linear transfer function of the system is shown (in red).

This analysis is based on gain representation of the amplifier characteristics using describing functions. Therefore, if $r(t)$ is a gaussian signal with zero mean, variance σ^2 and θ is uniformly distributed in $[0, 2\pi]$,

$$N_r(\sigma_r, A) = \frac{1}{\sqrt{2\pi}\sigma_r^3}\int_{-\infty}^{\infty} g_0(r(t), A) r e^{-\frac{r(t)^2}{2\sigma_r^2}} dr \tag{3.10}$$

where g_0 was defined in eq. 3.9.

$N_r(\sigma_r, A)$ represents the instantaneous quasi-linear gain of the system:

$$y_c(t) = N_r(\sigma_r, A).r(t) \tag{3.11}$$

For last, but not the least, it is important to note that saturation input level is conditioned by the amplitude of the dither sinusoidal, as well as the gain expansion and compression in g_0 that will lead to harmonic and/or intermodulation distortion: co-channel and adjacent channel non-linearities. According to the red curve of fig. 3.5, when $r = A$ (x=1, in 3.5), the output of the system is no longer changing with the input.

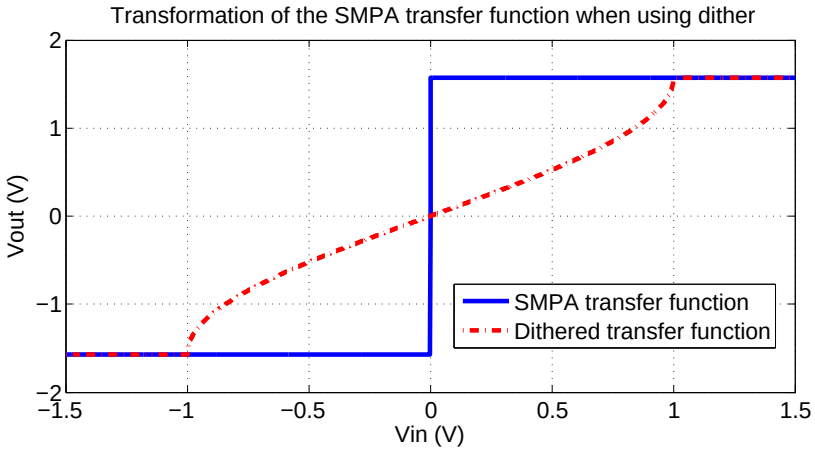


Figure 3.5: *Non-linear transfer function of the system with dither.*

3.2 MATLAB simulations

In this section, time domain simulations using MATLAB[1] simulator will be shown. The MATLAB file used to generate the plots can be found in the appendix, in the end of the report.

In simulation, two tones with and without the extra input(dither), will be applied. Comparisons between both situations will be made and conclusions about the viability of this technique will be presented.

Distinction will be made between a two tones output with and without dither for both LFD and HFD. Figure 3.1 represents the diagram blocks followed while writing the script.

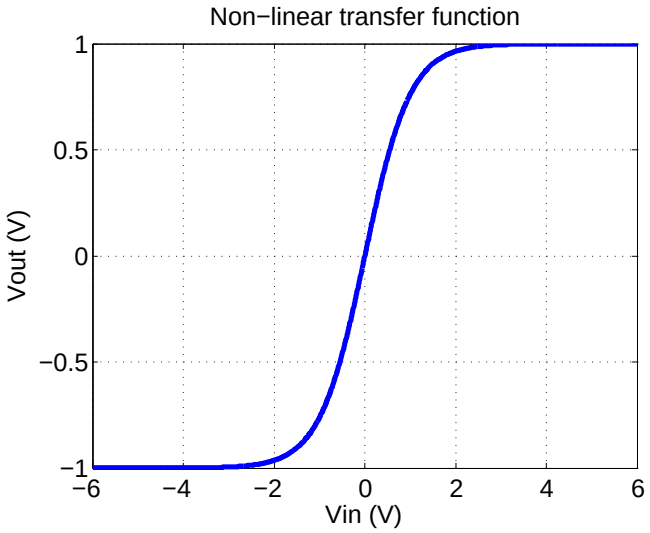


Figure 3.6: *Non-linear transfer function of the system.*

The simulations started by choosing a non-linear function that could resemble the non-linear transfer function of an SMPA. Another important step of the simulations was the choice

[1]MATLAB is a U.S. registered trademark of The Mathworks Inc.

of the filter. It has a fundamental role in the system since it performs the average that leads to the linearization of the system. In simulations, an ideal fir filter was used centred at the the frequency filter of the input signal.

Figure 3.6 shows the non-linear transfer function of the system. It was chosen to be an hyperbolic tangent function to approximate the real system.

Starting with HFD, 198 MHz and 202 MHz were combined at the input and the dither is at 1300 MHz. For all simulations, both HFD and LFD, the dither is a sinusoidal with 2.2 V amplitude. Figure 3.7 shows the difference between a simple two tones (in blue) and a two tones with dither (in red) signal. In this case, the envelope of the two tones dithered system is modulated by the two tones signal.

The output spectrum is shown in figure 3.8 and 3.9. For HFD, there's higher intervention of high frequency spurs due to the intermodulation products between the two tones and the dither and, the two tones harmonics.

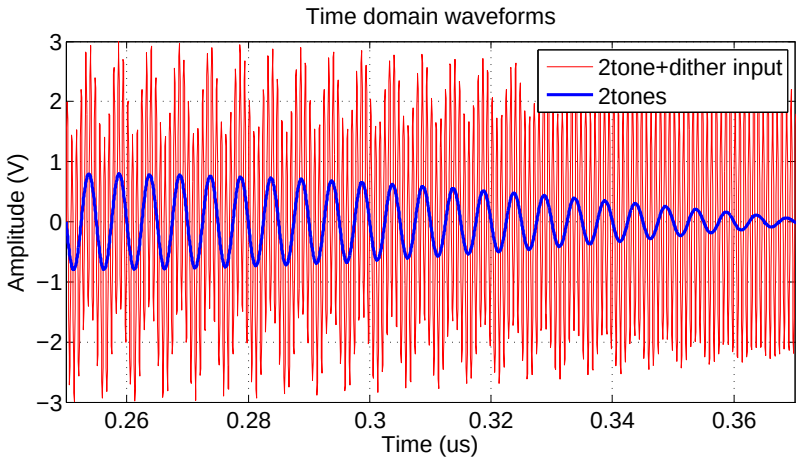


Figure 3.7: *Two tones dithered input vs two tones input for HFD.*

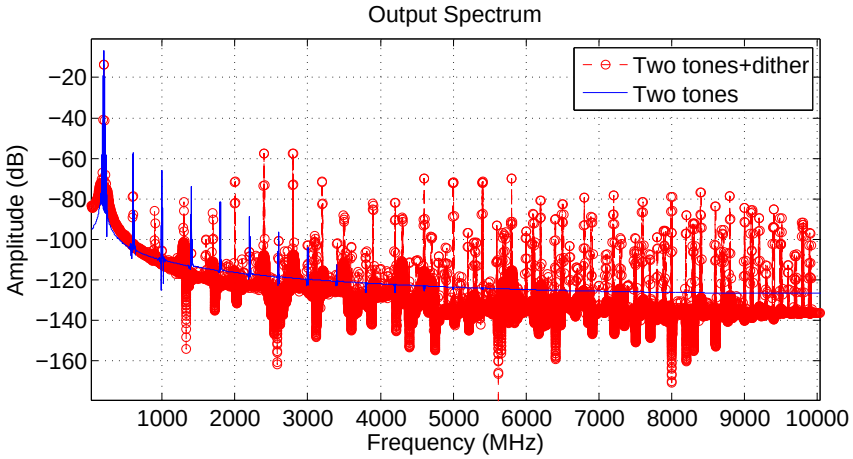


Figure 3.8: *Output spectrum of a dithered system vs system without dither for HFD. The spectrum was computed for a two tone sinusoidal, with 1V amplitude for each tone.*

Still analysing figure 3.9, some conclusions about IM3 can be drawn. It can be seen that

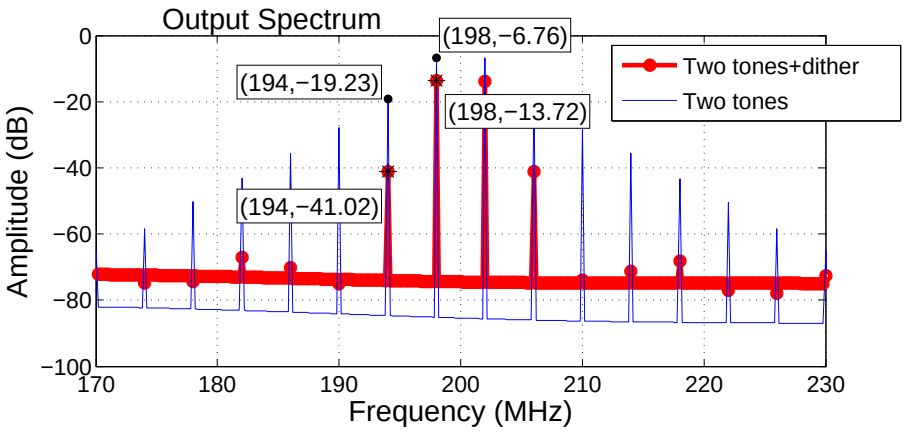


Figure 3.9: *In-band zoom of the spectrum of figure 3.8.*

Table 3.1: *IM3 analysis for HFD system.*

HFD					
Two Tones			**Two Tones dithered**		
Fundamental (dBV)	**3rd order interm (dBV)**	**IM3 (dBc)**	**Fundamental (dBV)**	**3rd order interm (dBV)**	**IM3 (dBc)**
-10.57	-33.81	-23.24	-10.02	-41.46	-31.44
-9.133	-28.81	-19.68	-8.978	-44.69	-35.71

for the same input power, the IM3 level has quite different values for each system. Despite the fundamental amplitude is lower, there's a higher difference in the IM3 value for the dithered system.

In table 3.1, simulation results with the input RF power tuned to get the same output power under the two conditions are shown. It can clearly be seen that the intermodulation products are significantly lower (by 10 dB) when using the high-frequency dithering, thereby demonstrating the effective linearization effects of the dither technique.

For LFD, the same analysis can be done. 1299 and 1301 MHz were the frequencies chosen for the two tones input and the dither is at 358 MHz, the frequency sampling is 10 GHz and the amplitude of the dither is 2.2 V. Figure 3.10, 3.11 and 3.12 are the time domain representation of the input, the output spectrum and a zoom inside the desired bandwidth, respectively. Here, the envelope of the the dithered system will follow the two tones envelope, the envelope carrier is the 2 MHz sinusoidal (1301-1299=2 MHz).

Comparing the output spectrums of both HFD and LFD, LFD has more close to band spurs whereas HFD has more spurs at high frequencies. This phenomena is related with the frequency of the dither and its harmonics since it will be the stronger signal in the system (before saturation). For the HFD case, the harmonics of the dither and the intermodulation products of the two tones and dither will fall above the desired bandwidth while, for LFD, if the dither frequency is not well chosen, one might end with harmonics of the dither inside the desired bandwidth, not to mention the intermodulation products that may also fall within it. In figure 3.11, can be seen a strong spike at 1074MHz, this is an harmonic of the dither

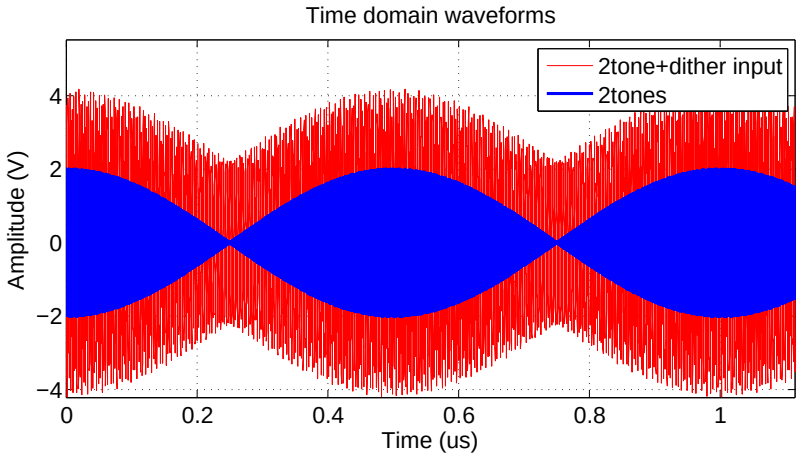


Figure 3.10: *Two tones dithered input vs two tones input for LFD.*

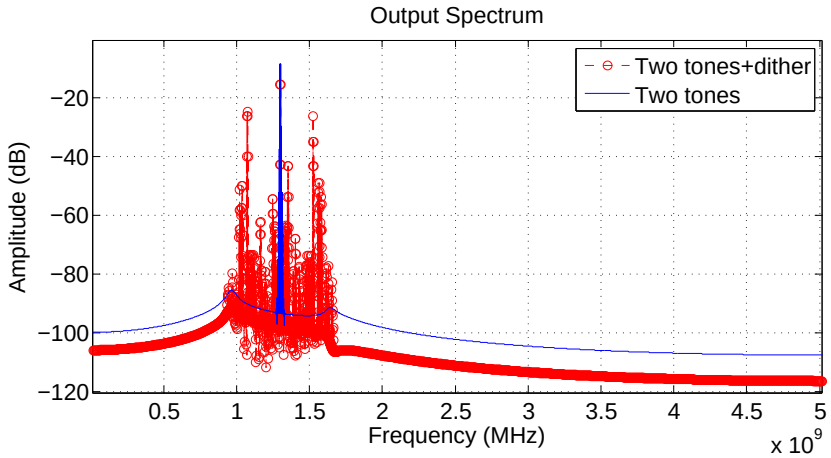


Figure 3.11: *Output spectrum of a dithered system vs system without dither for LFD. The spectrum was computed for a two tone sinusoidal, with 1V amplitude for each tone.*

frequency (358MHz) that is very close to the input signal (two tones).

In table 3.2, simulation results with the input RF power tuned to get the same output power under the two conditions are shown. As for the high-frequency dithering case, a significant decrease of the intermodulation products is clearly achieved (10 dB reduction), and the improvement of linearity is comparable for both HFD and LFD cases.

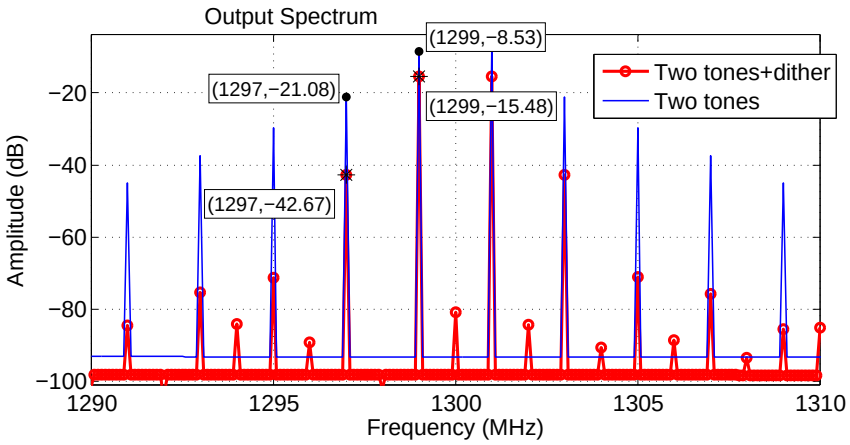


Figure 3.12: *In-band zoom of the spectrum of figure 3.11.*

Table 3.2: *IM3 analysis for LFD system.*

LFD					
Two Tones			Two Tones dithered		
Fundamental (dBV)	3rd order interm (dBV)	IM3 (dBc)	Fundamental (dBV)	3rd order interm (dBV)	IM3 (dBc)
-10.52	-32.86	-21.34	-11.53	-45.77	-34.24
-10.03	-27.43	-17.4	-10.31	-37.87	-27.56

Chapter 4

Studies on the UMS driver

Chapter 4 introduces one of the major parts of this project, the design work.

After a consistent explanation about where the thesis would fit, its main goal followed by a mathematical support, the pleasant part starts. In first place, the specifications of the given "amplifier to be modified", will be summarized. Secondly, a description of practical requirements that need to be defined regarding to the specifications of the given amplifier will be done as well as a brief review of the stability conditions of such a system.

For last, the simulations performed over the year, will be presented and conclusions will be drawn out and decisions for the prototype design will be established such as where should the dither be applied, input and output matching networks characteristics.

This chapter will give the main directions for the design of the prototype board.

4.1 UMS driver specifications

To start with the simulations, the main specifications of the device to be used need be to known. Thales NL provided a United Monolithic Semiconductors (UMS) driver that is already being used at the company for other applications. The datasheet of the power amplifier can be found in appendix B and here will be enumerated its most important characteristics.

CHZ015–QEG is a 15W input matched packaged GaN transistor. It is well suited for pulsed RADAR applications in L-Band (1–2GHz). The CHZ015–QEG is constructed around a 0.5μm gate length GaN High-Electron-Mobility Transistor (HEMT), using a Quasi Monolithic Microwave Integrated Circuit (MMIC) concept.

The input matching circuit is matched to 50Ω and is completely passive, made in Gallium Arsenide (GaAs). GaAs can also be used to produce power cells however, GaN is a very promising material that allows to operate at higher temperatures and work with higher voltages than GaAs transistors. It is seen as the next generation semiconductor technology that will help reducing the size and complexity of the overall amplifier module with efficiency improvement and high power operation, ideal for RADAR applications and high power communication transmitters.

The power bar of the version that will be used has four transistors in parallel. According to the datasheet in appendix B, the operable conditions of the amplifier for a worthy in-band performance –from 1.2 to 1.4 GHz– is:

- Bias conditions: Class AB biased: V_d=45V and I_{dq}=120mA;

- Pulsed signal mode for, at least, drain voltage, V_d, and RF signal;
- $V_{breakdown}$=200V, without RF;
- $V_{breakdown}$=60V, with RF;
- $V_g(max)$=2V,
- No output matching network.

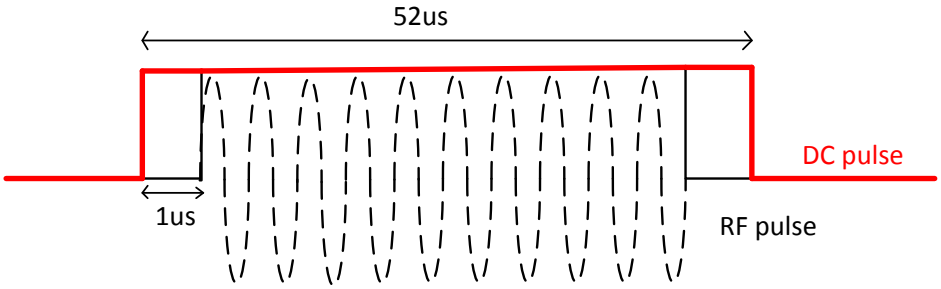


Figure 4.1: *DC and RF pulses over time.*

In accordance with RADAR specifications, the RF pulse will be of 50μs length, with a repetition time of 500μs (10%Duty Cycle) and with 1μs between RF and DC pulse as pictured in 4.1.

ADS[1], was the chosen CAD program to perform the simulations since a full non-linear model of the driver was supplied by UMS on ADS2009. Internally, the non-linear model can be divided in two: the model of the power bar which is based on polynomial equations and the model of the passive input matching that is based on electromagnetic simulation performed up to 5 GHz. Therefore, every ADS2009 simulation is valid up to 5 GHz, always having in mind the physical limits of the component, mentioned above. It is worth to note that memory effects are not taken into account and the model has been fitted to be representative of the operational conditions stated above: pulsed signals, bias voltage and current values, and limit conditions. The same circumstances will be further provided for measurements.

Externally, the power amplifier has two inputs: one for the RF input followed by an input matching circuit (hidden inside the package) and the gate bias input, and a single output where the RF output signal comes out and the drain bias voltage needs to be supplied. The backside ground pad acts as a RF/DC ground and thermal path.

4.2 Practical requirements

Regarding to the characteristics of the UMS driver that will be used, some adjustments for the global circuit need to be made. The pre-existing fixed internal input GaAs matching network and gate bias tee, both, do create frequency limitations on the two inputs that will impact the choice of which dither frequency can actually be used and where it can best be applied.

[1]ADS a trademark of Agilent Technologies, Inc.

Scattering Parameter (SP) simulations will be performed to check which is the best approach to follow. The dither input should remain as close as possible to the gate of the transistors because its amplitude will directly affect the linearization process of the driver.

Another issue is the biasing point of the given power amplifier. It is biased as class AB however, it is required to apply dither as a linearization improvements technique. As was discussed in chapter 3, to get the best improvement out of the system, it should behave as a SMPA. Therefore, another class of operation for the UMS driver should be chosen.

Fortunately, an SMPA setup can be reached by synthetizing the right output matching, which can be here freely implemented. The bias voltage values of the driver will need to be left as-is, mainly due to intrinsic temperature effects that would not be taken into account during the simulations since the model was characterized for the values above mentioned.

Sweet spots

The level of spurious of a LFD system depends on the dither and RF input signal. Whereas, for HFD, the dither would have to be at least at twice the highest frequency in the input signal, which higher in frequency means less disturbance in the desired band, for the LFD, a trade-off needs to be made to choose the right frequency for the dither.

If the dither frequency is lower than the bandwidth value of the RF signal, some of the harmonics might fall into the RF signal bandwidth, they will be of high-order/weak harmonics but still, will increase the spurious level. If the dither signal is too close to the RF signal, although the harmonics inside the band can be avoided, there will be strong harmonics close to the RF bandwidth. This phenomena can be quite troublesome since, worst case: output may be similar to a two-tone simulations when there is only one tone at the input. Because filters can not avoid it. For this sake, a careful choice needs to be done with respect to the input signal bandwidth and the dither will be pointed to be a quarter of the RF input signal.

RF signal can span from 1.2 to 1.4 GHz (BW=200 MHz), giving 50 MHz margin for each side, the system ends up with a bandwidth of 300 MHz. Before, reasons were given for the dither frequency not to be lower than the bandwidth of the desired signal thus, evaluating the harmonics of dither frequency starting from 300 MHz, a dither between [351,366] MHz will fit the best in these criteria. This rough calculation does not take into account the intermodulation products however previous studies already implemented a coded structure to calculate via a Computer-Aided Design (CAD) program, the sweet spots for their case [5]. Since this project is just a proof of concept, such a deeper calculation was not done.

On ADS2009, the frequency of the dither will only matter for the calculation of its harmonics (harmonic balance simulation defined up to 5th order) because the high order intermodulations will not be taken into account (too complex simulation).

Class of operation of the PA

For a best performance of the dithering technique, a switching mode power amplifier is required. Class A, AB, B and C are known as biasing techniques since they set the output current conduction angle with the Q-point (quiescent operating point), the given amplifier is operating under class AB conditions.

Within the high efficiency PAs there are two families: the switch-mode PAs such as class D or E and the harmonic tuned PAs, e.g., class F or F^{-1}. The last ones are based on network configurations, not bias. These classes of operation attempt to leverage some of the power

in the harmonics to obtain the maximum efficiency, presenting an open load to harmonics to tune the phase between drain voltage and current. They could be a good approach for this design since do not require the change of the bias point but do require an output matching network.

The ideal class F power amplifier mode requires a voltage square waveform and a half-rectified current waveform at its output current-generator plane [23]. There is no real power at harmonic frequencies because either has current or voltage present (never both at the same instant). The load seen by the transistor is a short circuit to even harmonics and an open circuit to odd harmonics. Thus, the drain-to-source voltage contains only odd harmonics and the drain current contains only even harmonics [24]. These waveforms can be described by the following equations [24]:

$$v_{ds}(\omega t) = V_{DC} - V_m \cos(\omega t) + \sum_{n=3,5,7,\ldots}^{\infty} V_{mn} \cos(n\omega t) \tag{4.1}$$

$$i_d(\omega t) = I_{DC} + I_m \cos(\omega t) + \sum_{n=2,4,6,\ldots}^{\infty} I_m n \cos(n\omega t) \tag{4.2}$$

where v_d and i_d represent the voltage and current at the drain, and ω, the frequency of the desired signal. Assuming a spectral content with infinite number of harmonics an efficiency of 100% could be achieved. When that number is truncated to three, the maximum efficiency reduces to 90.7% [8].

Class F^{-1} power amplifiers can be also described by the same numbers yet the shapes of the current and voltage are exchanged (reciprocal situation). The drain-to-source voltage contains only even harmonics and the drain current contains only odd harmonics. Thus, the load network represents an open circuit to even harmonics and a short circuit to odd harmonics.

These two classes may have different efficiencies for the same PA. Between them, the one that gets higher efficiency via load-pull simulations will be the chosen operation class for the desired amplifier.

4.3 Stability

Very experienced designers say that it is very easy to start designing an amplifier and end up with an oscillator in practice, and vice-versa. Stability is one of the most important criteria of an amplifier design.

In chapter 2, several characteristics of a linear system were given. One of those was bounded inputs should only generate bounded outputs. For this condition to be valid, the system must be stable. This means that the roots of the characteristic polynomial $d(s)$ (remember figure 2.1, in chapter 2: $Y(s) = n(s)/d(s)$ where n and d are polynomials in complex variable s, and the degree of n does not exceed the degree of d) must all have a negative real part. This seems simple to prove however, with real systems it is more complex to achieve. To prove that a system is stable, S-parameter simulations are used.

If the output insertion loss of the system, S_{12}, is not zero, a signal path will exist between the output and input. This feed-back can create oscillations – unstable system. Thus, the

stability factor K, (*Rollett's condition* [25]) needs to be computed.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2\,|S_{12}S_{21}|} \tag{4.3}$$

If K is greater than unity, the requirements for an unconditionally stable system are fulfilled, for any source/load matching condition of a linear two-port network.

This is quite simple when the linear system is only a two-port network (one input and one output). Applying dither at the RF input would not require further study on the topic however, if the dither is injected through the gate bias, a three port network will be simulated and built. Consequently, a three port analysis needs to be done.

The two ports stability of the driver without the dither will be simulated in section 4.4. For rigorous three ports system stability check [26]. Nevertheless, the method described in [25] will be the used one. It's a particular case of [26] and results in unconditional stability between two ports, when fixing the third one.

Using the model of figure 4.2, several simulations will be performed and the results are discussed below.

4.4 DC, SP simulations

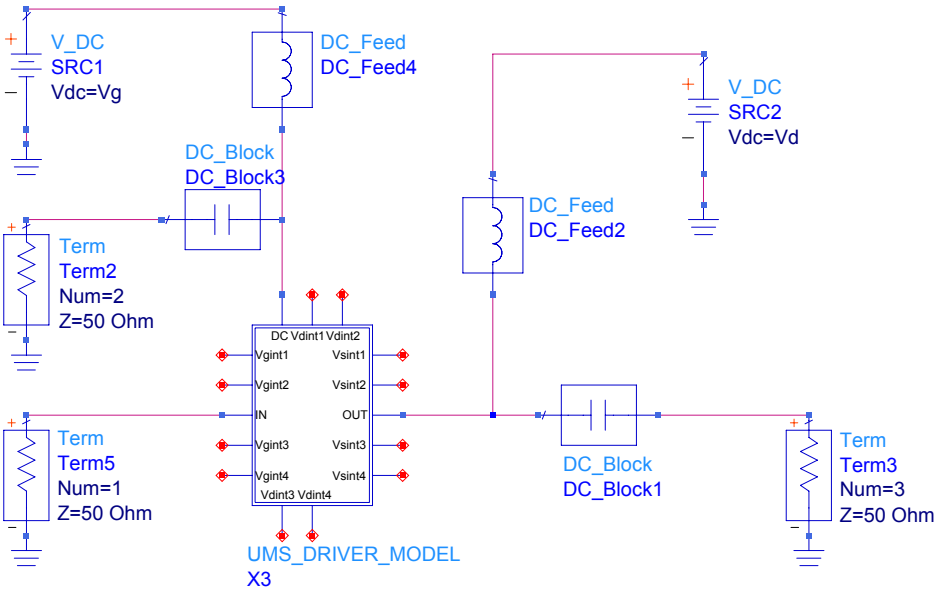
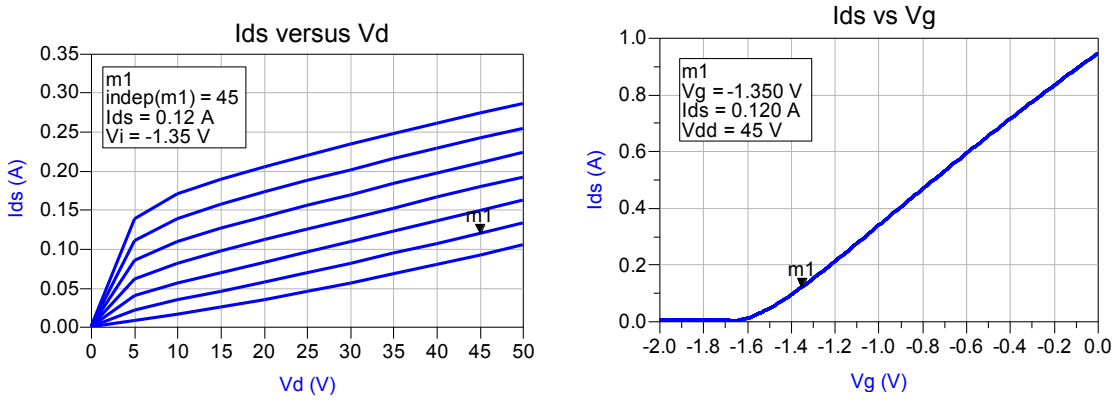


Figure 4.2: *UMS driver model for ADS2009.*

To start with the simulations of the power amplifier, biasing needs to be done. Looking to the datasheet(in appendix B), the recommended drain current for the driver, when there is no RF signal, is 120 mA. From figure 4.3(a) and 4.3(b), for a drain voltage of 45 V, the gate voltage needs to be -1.35 V to have 120 mA at the drain.

With the amplifier biased in the right class of operation, an S parameter simulation follows in the list. It provides small signal information about the driver such as gain, return losses and insertion losses.



(a) (b)

Figure 4.3: *IV curves of UMS model: (a): Drain current, in amperes, versus drain voltage, in volts; (b): Drain current, in amperes, versus gate voltage, in volts.*

The return loss presented in 4.4(a) clearly shows that the input matching network, inside the package of the driver, provides a good matching for the RF signal (low return loss) although, it presents high values of return loss for other frequencies. fixing the amplifier operating bandwidth. For example, if a signal with the dither frequency would arrive at the input of the system, barely no signal would reach the transistor because the return loss is almost 0 dB.

The return loss at port 2 is typical of a low- pass filter, used as a bias tee for injection of the gate bias voltage. Around the dither frequency, return loss is around -4 dB which means that this bias input, with some extra matching circuit, might offer a suitable input for the dither frequency. However, a good isolation between RF input and port 2, and output and the input ports needs to exist otherwise, the stability of the system could become an issue.

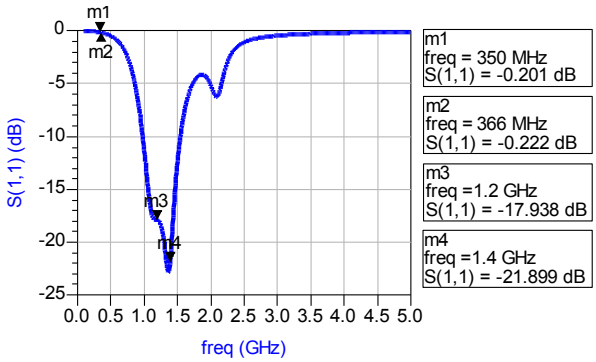
Figure 4.4(b) shows the insertion loss between input and port 2. It is always below -25 dB which is a reasonable value. Likewise the reverse isolation, from RF output(port 3) to RF input(port 1) or from RF output to gate bias input(port 2)(figure 4.5(a)) is always below -30 dB. Last but not the least S parameter remark, figure 4.4(d) shows the gain curve over frequency: this driver has 17 dB gain inside the RF band.

Two port stability factor from RF input to output and from port 2 to output are shown in 4.6. In section 4.3 was explained that a system may be considered unconditionally stable if $K > 1$. For RF input, besides, most of the time, K is over 1, in figure 4.6(a), there is a zone where $K < 1$, for lower frequencies (< 300MHz). This phenomena can bring non-idealities(spurious oscillations) to the system because, in the region where the *Rollet's condition* does not hold the system cannot be considered stable. On the other hand, on port 2, the stability factor is always above 10 thus, it is unconditionally stable.

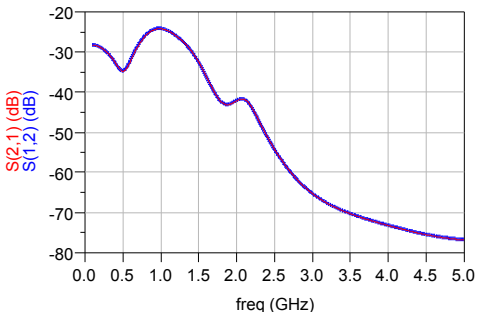
Where should the dither be injected?

According to what was defined previously in this chapter, the dither should be kept between 350 and 366 MHz.

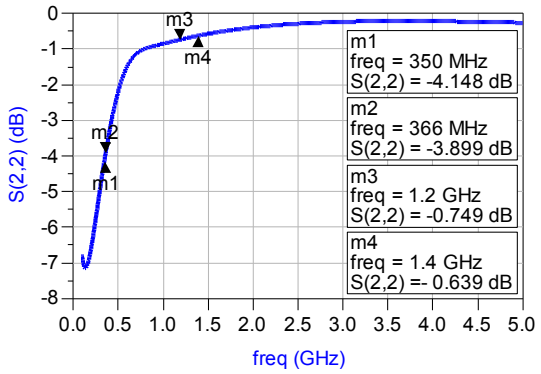
Figure 4.4 shows some of the S parameters of the driver's model, more specifically, 4.4(a) illustrates the input return loss: below -17 dB for RF signal however, for dither, as stated above,it is around 0 dB so, everything that gets in, is reflected back. This is a real problem



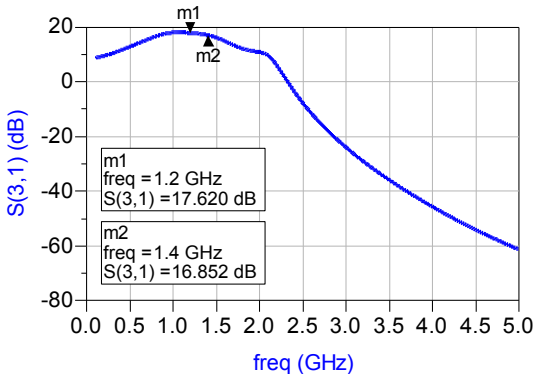
(a) Input return loss.



(b) Insertion loss from RF input(port 1) to gate bias input (port 2) and vice-versa.



(c) Return loss of port 2.



(d) Gain of the driver.

Figure 4.4: *S-parameters corresponding to the schematic in fig. 4.2.*

since the dither needs to be able to change the transfer function of the power amplifier and to do so, it needs to reach the gate with the highest amplitude possible.

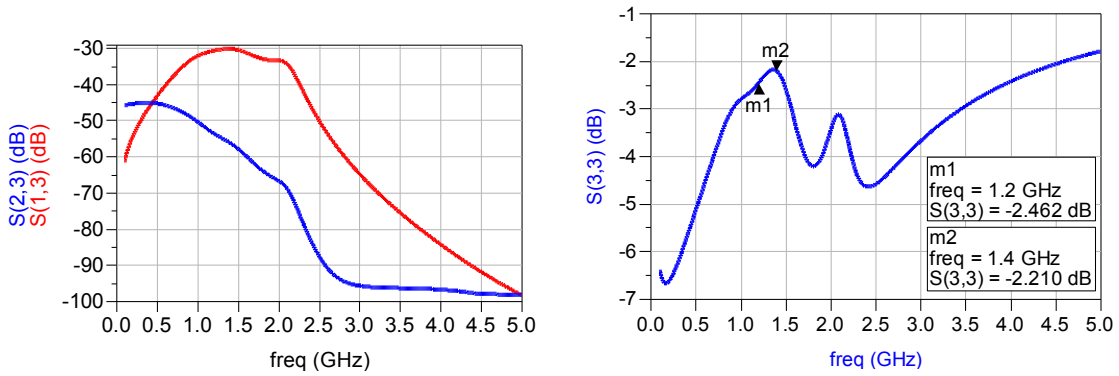
Looking to the other possible input on the gate bias access however, in figure 4.4(c) one can see that the return loss for dither frequencies it is below -3 dB so, less than half of the signal that comes in, is reflected. Using this input as an input for the dither reflects a better scenario than using the RF input. Although another AC input and a matching network will be needed to supply and improve the return loss of the dither, using port 2 in the schematic, neither the RF input or the RF signal path will be changed (it already has the input matching circuit inside package).

Thus, to provide better return loss for the dither, an extra input which will be part of the gate bias, will be added to this driver. As a consequence of applying dither at the bias path, the matching network must also include a bias tee to separate the DC from the dither source.

4.5 Input matching for dither

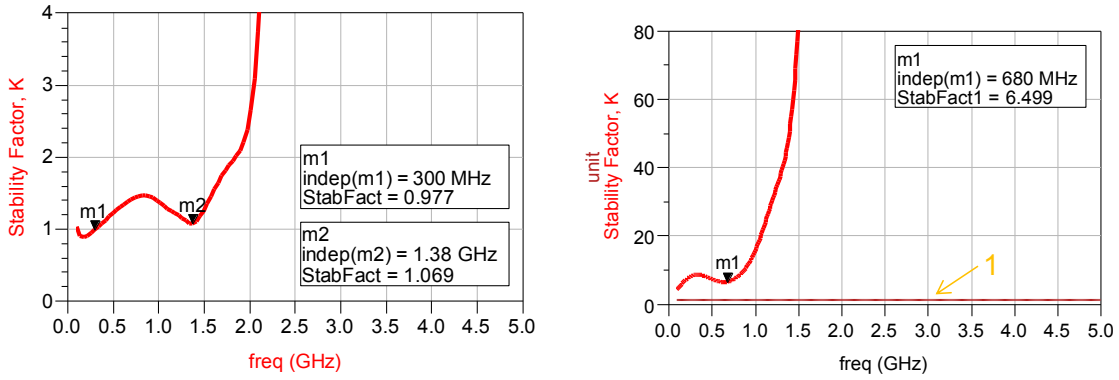
For the sake of simplicity, it was chosen to apply the dither in a 50Ω matched system which means that the dither will be a power signal.

The amplifier used in this work was chosen *a priori*, without considering the internal input impedance of the transistor's gate. Of course, this brings efficiency issues for the complete



(a) (b)

Figure 4.5: (*a*) : *Insertion loss from the output to RF input and to dither's input;* (*b*) : *Output return loss.*



(a) (b)

Figure 4.6: *Stability factor from the RF input to the output and from the gate bias input to the output, respectively.*

system that could be avoided if, at gate of the transistor, one would have a higher impedance for dither frequency than for the input signal frequency because, this way, one would achieve higher amplitude voltage for less power delivered to the transistor. However, work has been focused in the frame of this thesis on providing low-frequency dithering linearization concept, and the analysis of the impedance at gate of the transistor was left beyond the scope of this work (the complete model of the driver package has an input matching circuit included). This also allows to use standart test equipament.

In section 4.4, was said that the matching network for the dither input needed to be a combination of a bias tee, to separate the AC from DC and vice-versa, and a filter to improve the return loss for dither frequency. Figure 4.7 shows the return loss of port 2 for schematic presented in 4.2, the simplest way to match the system to 50Ω can be done through inductive components. Using the Smith Chart tool provided by ADS2009, two inductors and a capacitor were added together and, in figure 4.8, is depicted the final design of the complete matching network. The $1nF$ capacitor is used as decoupling capacitor, to get rid of the noise produced by the voltage supply.

The results are shown in fig. 4.9. Figure 4.9(a) shows the return loss after adding the

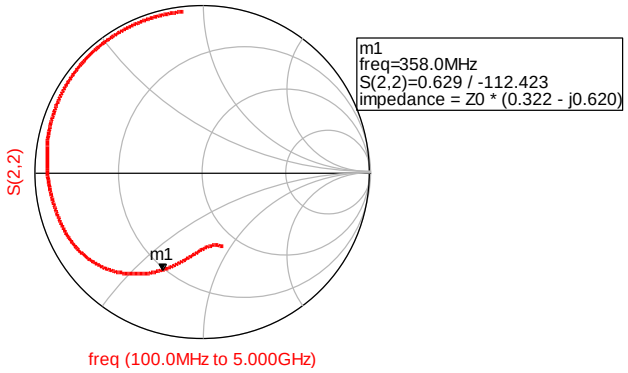


Figure 4.7: *Smith chart representation of the return loss for port 2.*

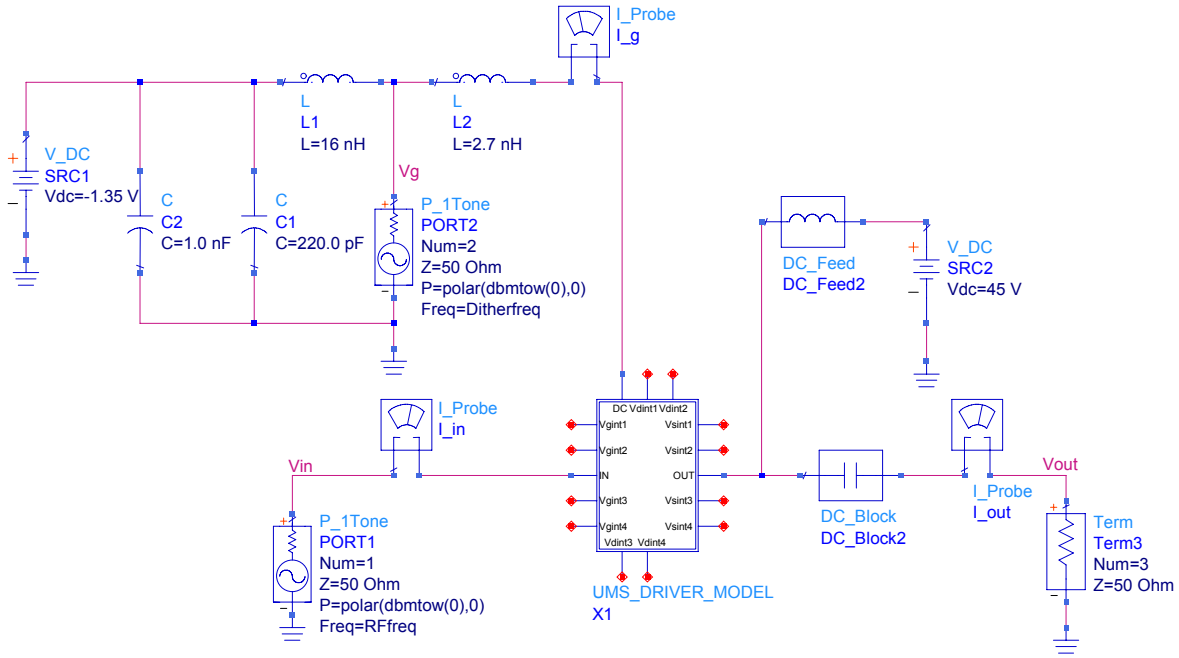
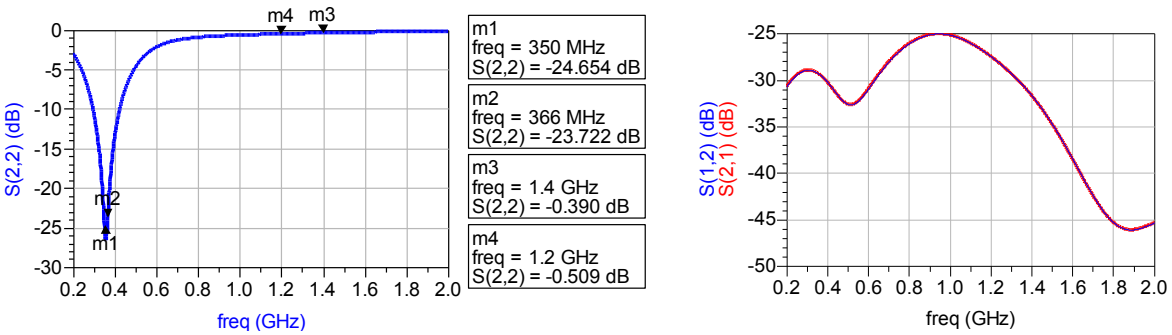


Figure 4.8: *UMS driver model with a matching network for dither input.*

matching network. As can be seen, for the required bandwidth, return loss below -22 dB were obtained while the isolation between port 1 and 2 is retained at the same level as before (figures 4.4(b) and 4.9(b)).

4.6 Load-Pull simulations

Now that one already has an idea of how to modify the given amplifier to apply the dithering technique, it is necessary to perform simulations which can give the conditions to attain a maximum PAE and output power. Such simulations are known as load-pull simulations and they do that by varying the load reflection coefficient presented to a device



(a) (b)

Figure 4.9: (*a*) : *Return loss of the dither input;* (*b*) : *Insertion loss from the RF input to the dither input and vice-versa.*

to reach operating conditions of a SMPA.

In the simulator, one can specify the circular region on the smith chart over which the reflection coefficient will be swept. This way, the simulator will present different loads to the device and for each one of them, the performance of the system will be calculated. The final result of each simulation results in one point that combined together, result in contour lines over a smith chart representing the impedances that have the same PAE and/or output power.

Load pull simulations also assign arbitrary reflection coefficients to harmonic frequencies which can be tuned by the user for his needs. It is an iterative process, because fundamental source, load impedances, and harmonic load impedances, all interact when synthetizing the output SMPA matching circuit.

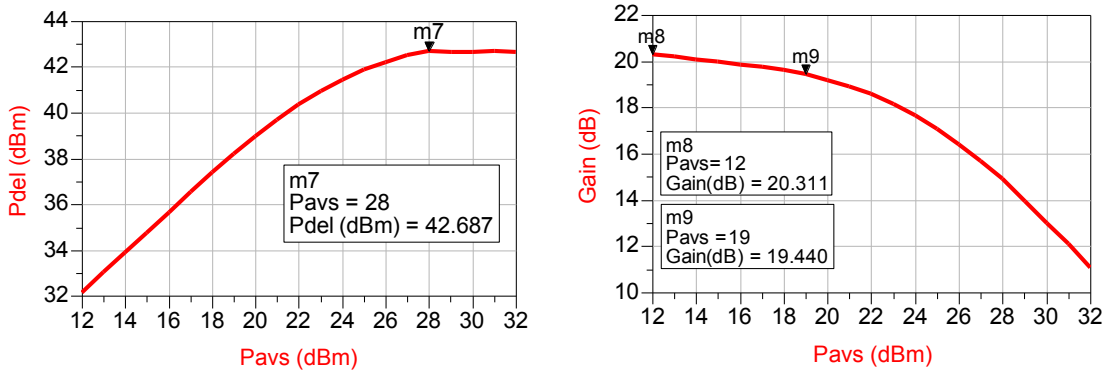
Once suitable conditions have been found for a standart SMPA under single frequency operation, extra simulations are needed to check for overall performances (power, PAE and linearity) when one tone plus the dither and two tones plus the dither are used as input. Below, several plots present the performance of the driver when subjected to different input signals. The input matching network design for the dither was used in all simulations.

During the simulations, three different driver models, provided by UMS, were tested. Among those, there was a single cell transistor model that was used in the beginning of the simulations to give a deeper understanding of the behaviour of the power cell bar inside the package that will be further used in the prototype board. With this singular model, simulations with one and two-tone were performed for a normal class AB, class F and F^{-1}. The simulations results followed the trend of the simulation outcomes that will be shown next.

The load pull template provided by ADS2009 was the starting point for the simulations. First, the given model was tried with the ADS2009 template and then on, features were added to the template, to fit the oncoming needs. In the end, a three-tone simulation with amplitude, frequency sweeps and arbitrary reflection coefficients for the harmonics of all input signals was working.

4.6.1 One tone simulation

Starting with simulations, the first load pull simulation was performed with the given driver biased in class AB for a single frequency, 1300 MHz, and its harmonic impedances matched to 50Ω. Below, is shown the power delivered to the load (fig. 4.10(a)) and the gain of the system over power input (fig. 4.10(b)):

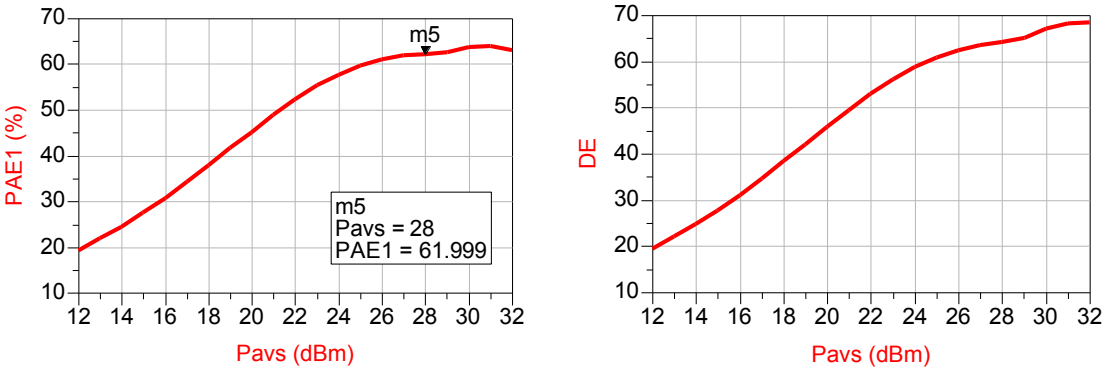


(a) (b)

Figure 4.10: *Power delivered to the load and gain for a Class AB driver, at 1300 MHz*

Analysing the provided results, a 19 dBm input compression point can be attained for a 20 dB system gain. This high gain is only possible due to the load pulling effects (matching properties). Changes in the output impedance reflect direct changes in output Voltage Standing Wave Ratio (VSWR) that may increase or decrease the power delivered to the load and efficiency of the system according to how well the output is matched. Otherwise, the gain would have been the same as for the results of the SP simulation shown in the beginning of the chapter.

Close to saturation, the UMS driver can provide a maximum of 43 dBm (20 Watts) to the load, as can be seen in figure 4.10(a).



(a) (b)

Figure 4.11: *PAE and Drain efficiency for a Class AB driver, at 1300 MHz*

Figure 4.11(a) and 4.11(b) depict the evolution of PAE and drain efficiency over power input, respectively. These curves show a maximum PAE of 62% and a maximum drain

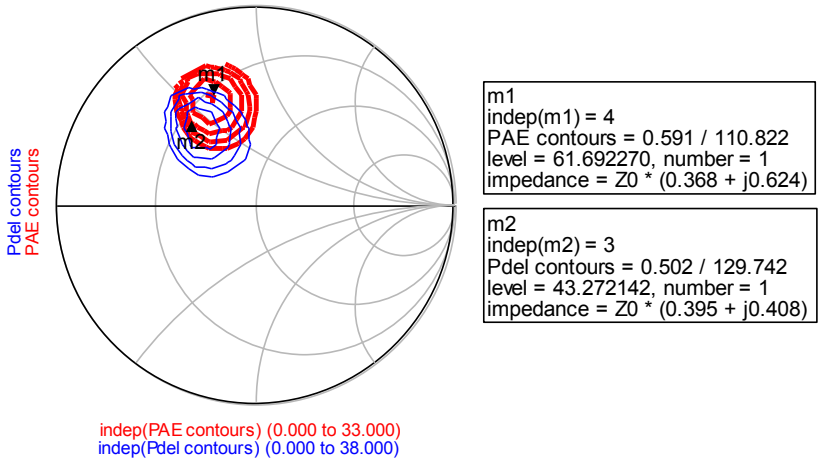
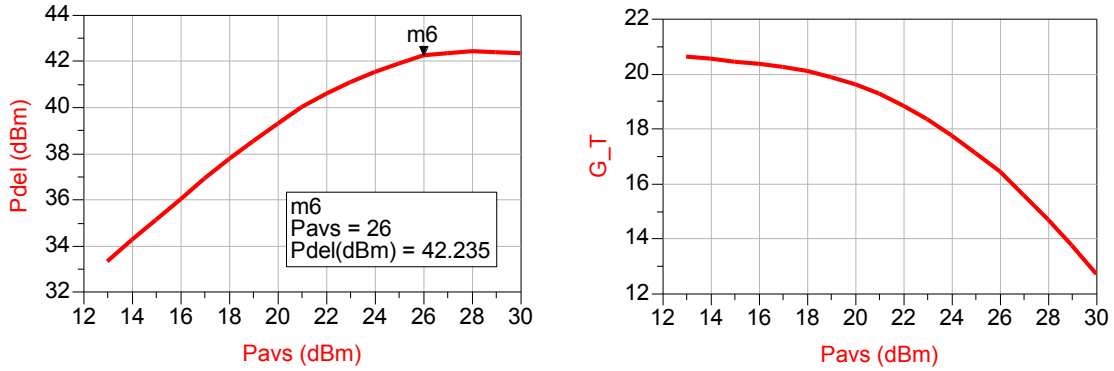


Figure 4.12: *Smith chart for a 27 dBm input signal. Step size for blue contours is 0.25 dBm and for red contours is 2%.*

efficiency around 68%. Looking to the smith chart shown in fig. 4.12, both maximum PAE and maximum output power are achieved for two distinct loads. The two markers show the values of the reflection coefficients required at the output to reach the optimum PAE and power. These power contours were attained for 27 dBm input signal, right before saturation (fig. 4.10(a)), and will be used to compare with a different class of operation for the same amplifier model. The contour lines in figure 4.12 have a step size of 0.25 dBm for the power delivered to the load contour(blue line) and 2% step size for PAE(red line). For a 27 dBm input, a maximum PAE of 61.8% or 43.3 dBm at the load can be acquired as long as a proper output matching is provided.

Still within one tone simulations, the harmonic impedance network of the simulation was changed in order to have the driver operating as class F^{-1} amplifier. Class F was also simulated however, its maximum PAE was lower than F^{-1} class of operation. Thus, class F^{-1} was chosen to apply at the output network of the prototype. Figure 4.13(a) and 4.13(b) exhibit the output power and the gain of the system over input power.

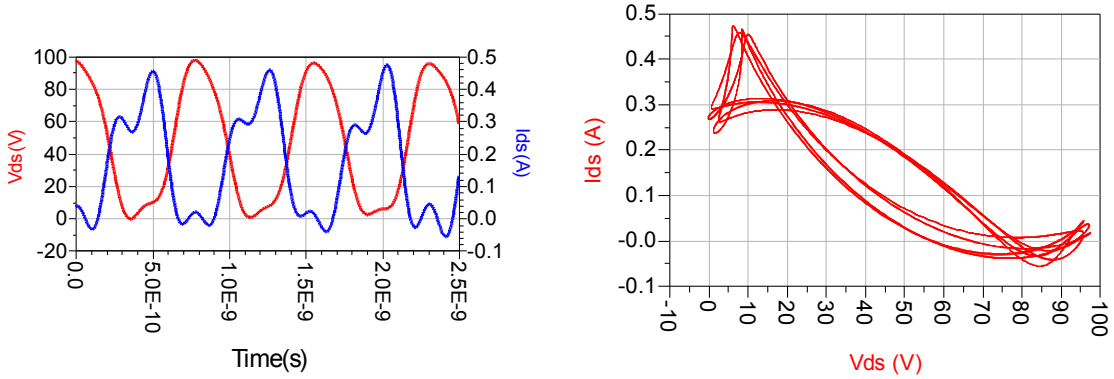


(a) (b)

Figure 4.13: *Power delivered to the load and gain for a class F^{-1} driver, at 1300 MHz.*

As can be seen from figure 4.13(a), although the saturation comes earlier than for class

AB (as it was expected), the same values for maximum output power are achieved. The input compression point is also lower than for class AB. It is important to remember that class F^{-1} is a switching mode class of operation (fig. 4.14) thus, the reduction of P1dB is in accordance. Based on SMPA principles, a higher value for PAE was expected and both smith chart 4.15(b) and figure 4.15(a) show that improvement. For a 27 dBm input power, around 72% PAE can be achieved, which is a 10% points improvement versus the 50Ω loaded harmonics case.



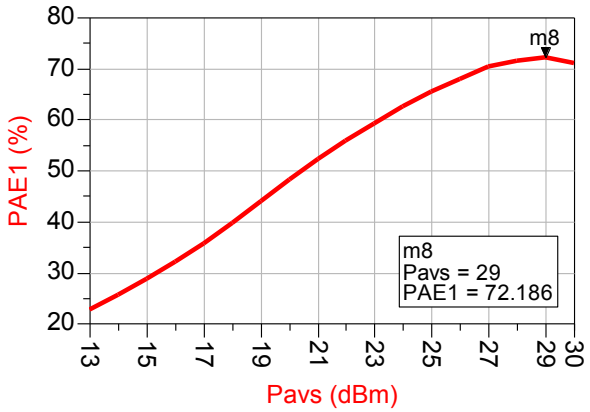
(a) (b)

Figure 4.14: (*a*) : *Drain voltage and current waveforms for a 27 dBm input signal over time;* (*b*) : *Drain I-V load cycle corresponding to (a) waveforms.*

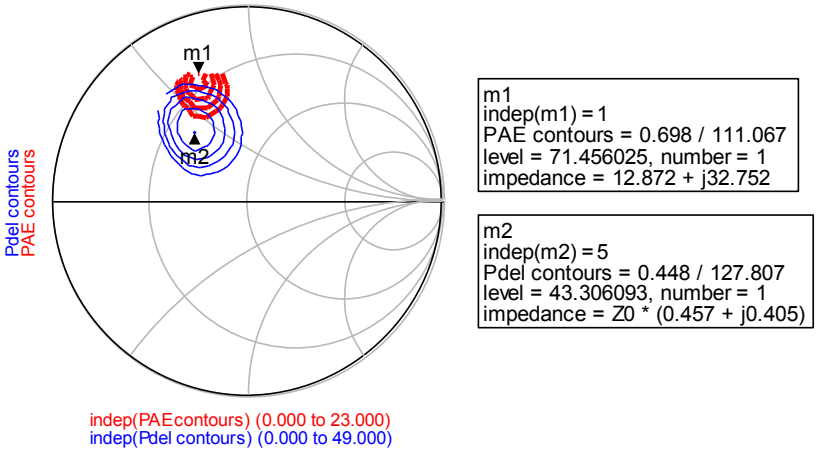
On a side note, the harmonic impedance coefficients used to have a class F^{-1} operation mode were apparently not the standard values: high impedance for even harmonics and low impedance for the odd ones. In the beginning, those values were tried but no class F^{-1} characteristics were seen at the drain. This phenomena can be easily explained by the fact that the provided model of the package, at the output, does include all package parasitic elements, and also the transistor drain-source capacitance, thereby introducing significant phase shift at the harmonic frequencies: the actual short/open circuits need to be presented at the drain current generator plane, and not at the package output where the simulation places the load-pull impedances.

In the next simulation, an extra tone is added at the input of the class F^{-1} driver. This is done via the input matching circuit described in section 4.5. The dither will be a sinusoidal waveform with 358 MHz and the RF input will be kept at 1300 MHz. Before showing the output power, gain or PAE, one must think how the dither shall be suppressed at the output. It is a strong signal and, it is not desirable to have it present at the load. Preventing the dither to arrive at the load is done by class F^{-1} matching filter however, there is still the question: should an open or a short be presented at the output of the driver for the dither frequency (or should it be at the transistor drain current generator plane)? According to ADS2009 simulations and for the same RF input conditions, the maximum PAE and power delivered output achievable, for both situations, are quite different. Whereas, for an open circuit for the dither at the output, the maximum PAE and power delivered to the load are 12.26% and 35.86 dBm, for a short circuit, 37.51% and 40.51 dBm are attained. Thus, from now on, a short circuit will be presented at the output of the driver, for the dither frequency.

Returning to the class F^{-1} amplifier simulations with dither, the output power and gain of the driver are depicted in figure 4.16, respectively. In the figure, a sweep over the amplitude



(a) PAE for class F^{-1} of operation



(b) Step size for blue contours is 0.25 dBm and for red contours is 2%.

Figure 4.15: *PAE and smith chart simulation for 27 dBm input signal.*

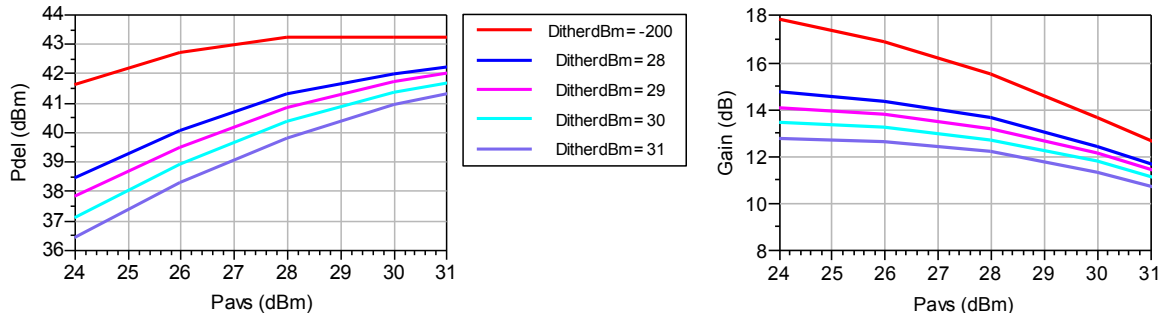
of the dither signal was done in order to track the changes. For a significant effect of the dither, its amplitude must be higher than the amplitude of the RF signal. In dark purple, for a dither power of 31 dBm, a linear variation over power input can be seen whereas, for single RF input (in red), the system is completely saturated.

For a system with no dither (dither's amplitude at -200 dBm), the original class F^{-1} is obtained. Figure 4.14 shows the voltage and current at the drain over time and respective IV curve.

Using an high amplitude sinusoidal wave to drive the system into compression and improve its linearity seems contra-intuitive. However, this is what is being done, driving the amplifier into compression at the expense of system gain. The simulated PAE is taking into account the input power of the RF and the dither signal and it is reduced over power input because the gain of the system decreases. For a 30 dBm input signal and with a 31 dBm dither signal, a maximum PAE of 41% can be achieved (figure 4.17).

Looking to fig. 4.17, for a 28dBm power input and no dither, a maximum of 70.23% and 43.41 dBm is obtained for efficiency and power delivered to the load, respectively.

Nevertheless, for the same input conditions, if the dither signal is increased up to 31 dBm,



(a) (b)

Figure 4.16: *Power delivered to the load and gain of a one tone system with dither. The legend will be the same for all plots of this kind, of this section.*

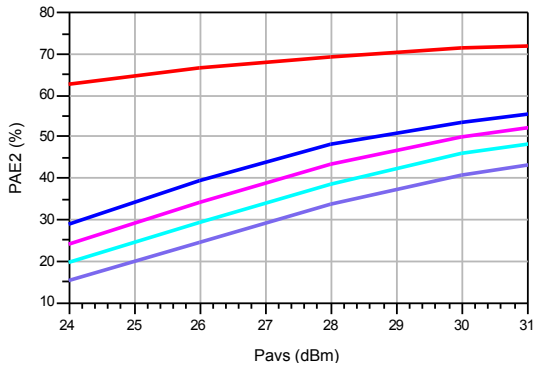


Figure 4.17: *Power added efficiency of a one tone input system with dither.*

the power added efficiency drops to 33.61% and power delivered to the load to 40 dBm (not saturated yet). However, if one look to the drain efficiency depicted in figure 4.18, for the same output power in both systems, for example, for 42 dBm at the output, similar drain efficiency values are achieved.

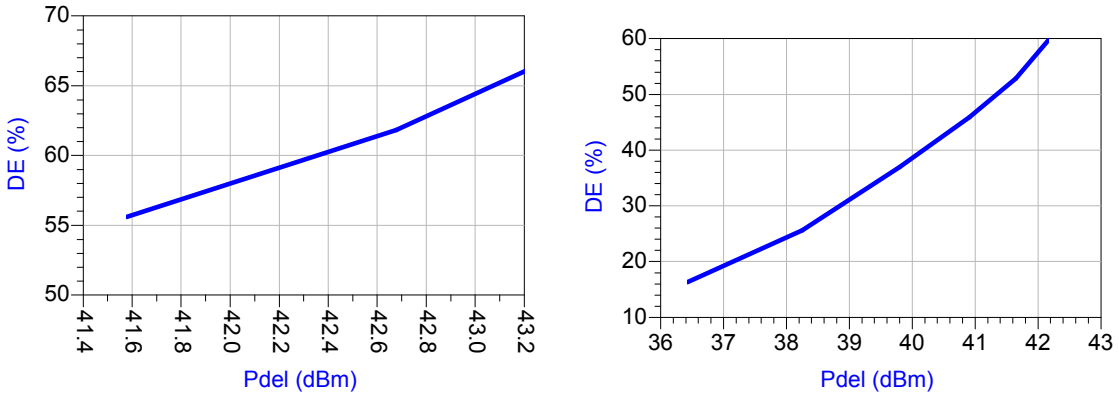
To conclude, it is interesting to look at the voltage and current drain in time as well as to IV curves and compare them with the previous simulation with no dither. The dither introduces large changes in current amplitude keeping the voltage, more or less, constant, as one can see in figure 4.19.

4.6.2 Two tone simulation

To finalize the model simulations, the results of a two tone simulation with dither will be presented. This kind of simulation was already highly complex and despite sporadic convergence problems, interesting results were still found.

First, starting with a really low amplitude for the dither, one should have the driver biased at class F^{-1}. Figure 4.20 shows the voltage and the current at the drain, for two tones, that resembles the output of a class F^{-1} amplifier, as was expected. This being checked, the amplitude of the dither can be increased for higher values.

Two RF tones with the same amplitude were presented at the RF input of the driver and, at the gate bias, a 31 dBm dither was injected. The RF tones were centred at 1300 MHz and



(a) (b)

Figure 4.18: *Drain efficiency for class F^{-1}, without, (a), and with dither, (b), over the output power of the system.*

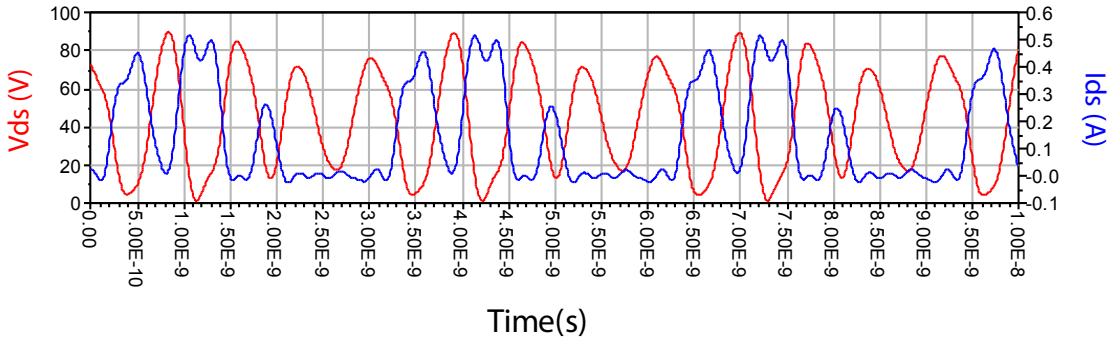


Figure 4.19: *Drain voltage and current waveforms for a 27 dBm input signal and 31 dBm dither signal, over time.*

had a 500 kHz spacing between tones while the frequency of the dither was kept at 358 MHz and its amplitude was swept over each simulation.

From now on, the input power displayed in the x-axis, it is the summed power of the two RF tones and the coloured lines of the following plots is always based on the legend of fig. 4.21.

In figure 4.21, the power delivered to the load is displayed and it can be seen that its maximum, for a system with no dither, is 41.5 dBm for 28 dBm input (25 dBm each tone). This value is slightly different than the value achieved for one tone. This is due to the fact that no optimum point was achieved for this simulations. The 1.5 dB missing can perfectly happen because of mismatches at the load. Despite no optimum points were achieved for this simulation, one can do a relative analysis, comparing the results for the same circumstances.

Moreover, for high amplitude dither, the same phenomena observed for one tone plus dither, can be seen: while red output is already into compression, the dark green signal is still "linear" till 31 dBm (when the amplitude of the dither matches the amplitude of the input signal). In the latter case, the output is still following, in a linear manner, the input.

In figure 4.22, two types of drop can be seen for both gain and PAE. A drop when compared

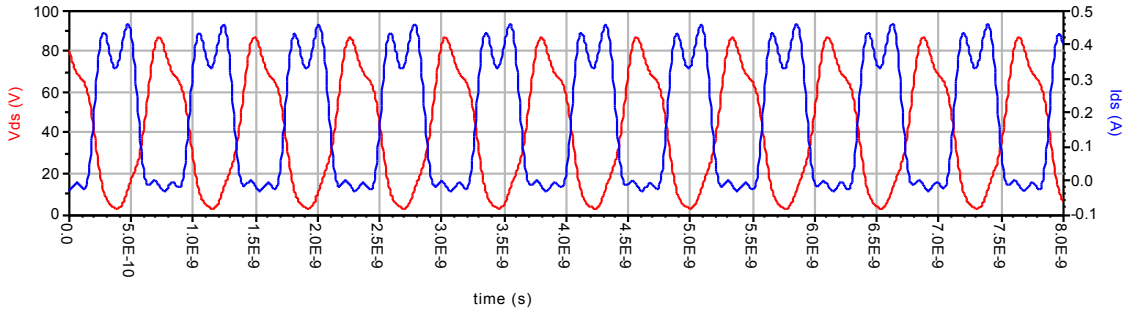


Figure 4.20: *Voltage and current at the drain of the UMS driver, for two closed tones.*

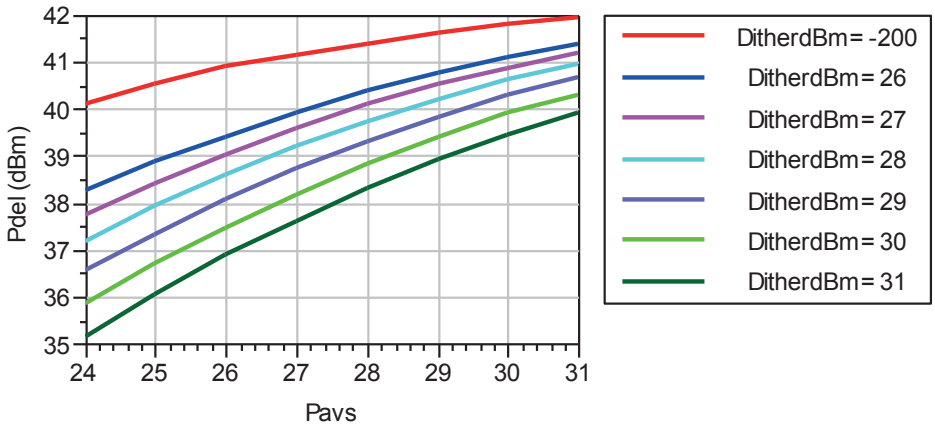
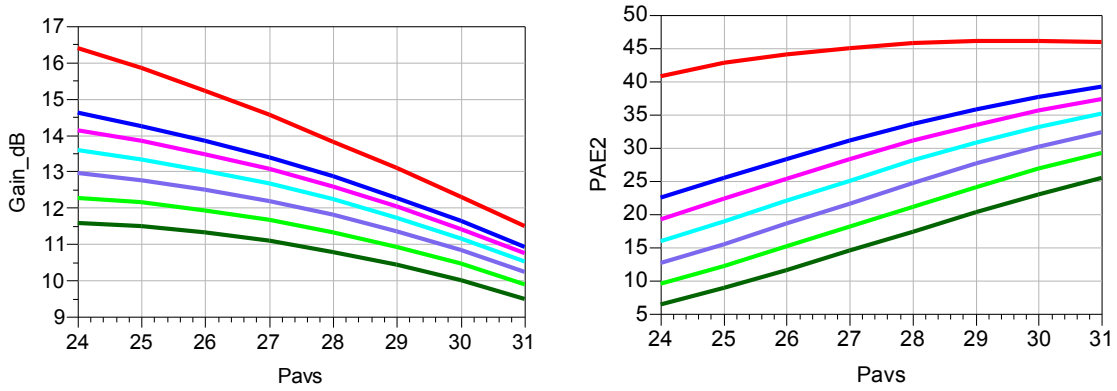


Figure 4.21: *Power delivered to the load swept over the amplitude of the dither.*

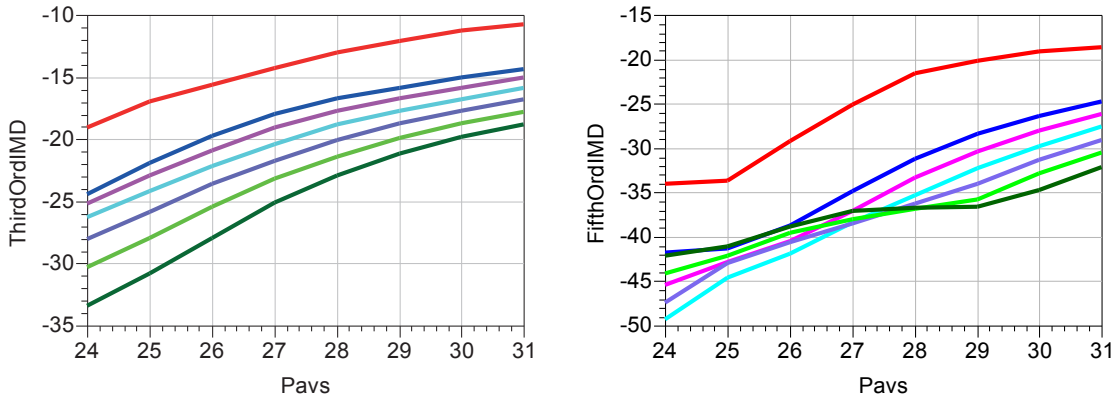


(a) Gain (b) PAE

Figure 4.22: *Gain and PAE for a two tone simulation with dither, the legend from figure 4.21 fits to these figures.*

to one tone simulations and a drop between the system with and without dither. In terms of gain, for the first case, it is, again, caused by the lack in the achievement of an optimum point in the load pull simulation. However, in the second case, for the same reflection coefficient presented at the output, one can see a larger difference, for a system with and without dither, for a 24 dBm input signal that decreases for higher input values. The gain of the non-linear

transfer function changes according to the ratio between the amplitude of the RF signal and the dither, as formulated in the dither chapter. Speaking of PAE, for the first type of drop, it can be explained as for the gain. Comparing the PAE values within the same plot, this larger difference happens because one is taking into account the power input of the dither for PAE calculations.



(a) Third-order intermodulation distortion

(b) Fifth-order intermodulation distortion

Figure 4.23: *First two intermodulation products for a two tone simulation using dither, the legend from figure 4.21 fits to these figures.*

Figure 4.23 shows the development of the third and fifth intermodulation products for the described system. Once again, it does not describe the optimal case due to simulation flaws however, the trend can be analyzed.

For the same input power, a 15 dB difference, in the IM3, is depicted for 24 dBm input power. However, closer to dither's power (this is, when the RF amplitude is close to the dither's), the difference is less, around 10 dB (between dark green and red line). A similar trend is observed for high input signals in IM5, depicted in figure 4.23(b).

Due to the complexity of the simulations (three tone simulations that go beyond the saturation point of the driver model), convergence problems arise that render more complete simulation impossible. However, a reasonable trend among the results was already clear.

It can also be noted that this 10 dB improvement obtained on IM3 in the "real case simulation" does seem to match the MATLAB theoretical results presented in section 3.2. In order to further prove the concept, the design of a complete prototype followed by actual measurements was started.

Before going into the layout design, in an attempt to prove three ports system stability, the method described in [25] was followed and the stability of the system was proven by simulation.

This analysis considered the stability between two ports with a fixed termination at the third port.

Assuming that Γ_3 is the reflection coefficient when a three port system is terminated at port 3, the three port stability condition is verified when,

$$K(\Gamma_3) = \frac{N(\Gamma_3)}{D(\Gamma_3)} > 1 \tag{4.4}$$

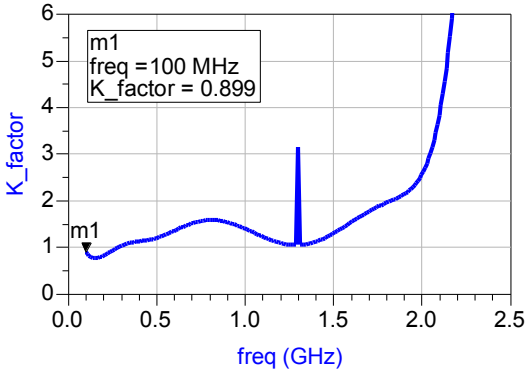
Where

$$N(\Gamma_3) = 3|1 - S_{33}\Gamma_3|^2 - 2|S_{11} - \Delta_{22}\Gamma_3|^2 - 2|S_{22} - \Delta_{11}\Gamma_3|^2 + |\Delta_{33} - \Delta_3\Gamma_3|^2 - ||1 - S_{33}\Gamma_3|^2 - |\Delta_{33} - \Delta_3\Gamma_3|^2| \quad (4.5)$$

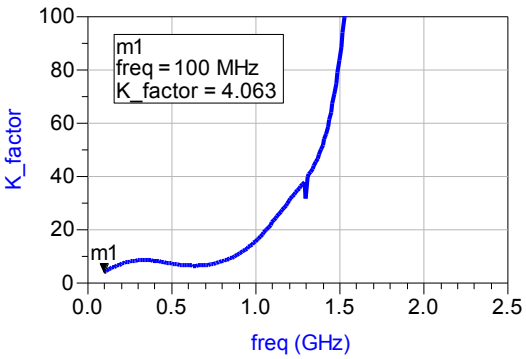
$$D(\Gamma_3) = 4|(S_{12} + \Delta_{21}\Gamma_3)(S_{21} + \Delta_{12}\Gamma_3)|, \quad (4.6)$$

and Δ_3 is the determinant of the three-port SP matrix and Δ_{ij} is the cofactor of (i,j)-th element. The stability results for the three ports system can be found below. Stability simulations have been done up to the maximum frequency of the technology however, here the results up to 2.5 GHz are shown to allow the reader to check for the frequencies of interest.

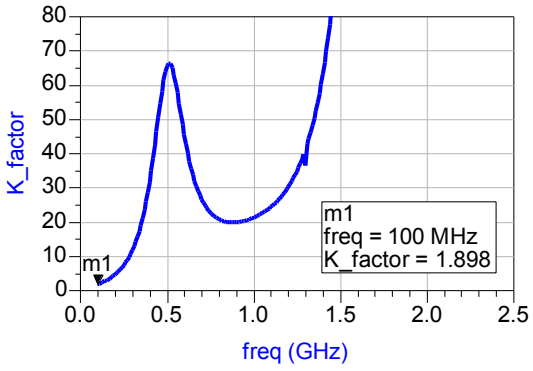
From 2.5 GHz on, the stability factor only increases.



(a) RF input to output stability.



(b) Dither input to output stability



(c) RF input to dither input stability

Figure 4.24: *Stability for a three ports system.*

For the RF input, the stability factor for the three port system (fig.4.24(a)) behaves exactly as the stability curve for two port system(fig. 4.6(a)). Thus, the same conclusions can be drawn.

Chapter 5

Prototype layout

So far, a description of the complete structure around the UMS driver was done, including the simulation analysis that support the theory of low-frequency dithering technique. In this chapter, a layout of the complete prototype will be developed.

In figure 5.1, an overall picture of the driver with the matching networks is presented. Before, the characterization of the "dither input plus gate bias tee" with lumped components was done and its performance was evaluated. However, only "ideal" components were taken into account. By "ideal", one means pure capacitors without ESR and/or inductors with infinitive Q.

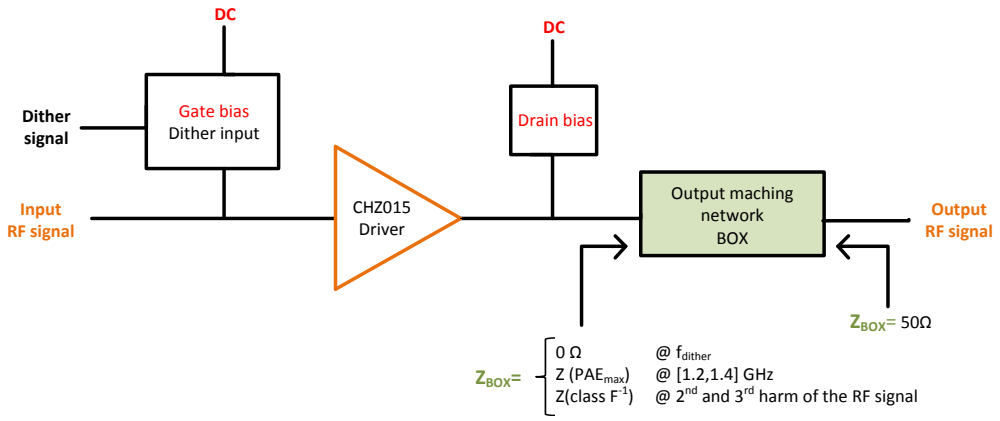


Figure 5.1: *Block diagram of the general layout.*

Unfortunately, ideal components do not exist in real life and other parameters need to be taken into account in simulation, to be able to predict, as close as possible, the real device behaviour. To do so, first simulations with S-parameter blocks, provided by the manufacturers, were used to replace the ideal lumped components, then transmission lines, with the same characteristics of the board substrate were added to the schematic, via COM1 library[1]. In second place, the complete network structure was built and simulated with MOMENTUM[2], a 2D electromagnetic simulator that computes the S-parameters for planar circuits, able of identify parasitic coupling between components.

[1] ADS library developed at Thales NL

[2] MOMENTUM a software product of Agilent Technologies, Inc.

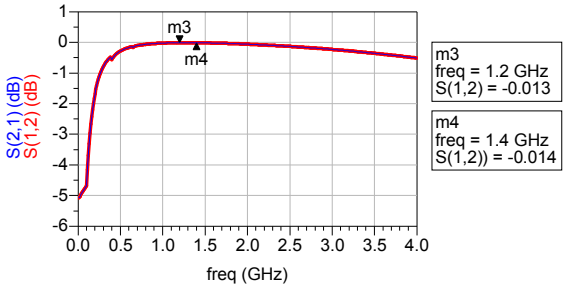
5.1 Gate and drain bias tee

Next, the final versions of the gate and drain bias tees will be presented. These structures were based on a stable structure provided by UMS and are both rather similar. Despite the gate bias tee also includes the input matching network for the dither, both of them have, as principal structure, the choke inductor, in parallel, to prevent the RF signal to flow through the DC path and a coupling capacitor in series with the gate/drain of the transistor, to separate the AC signal from the DC bias.

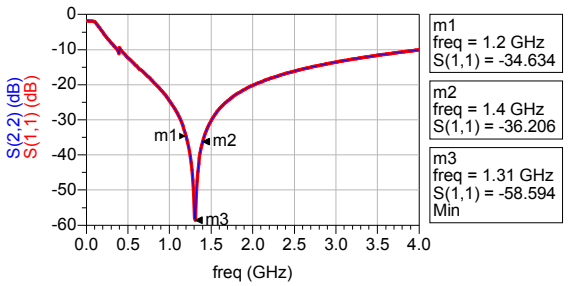
5.1.1 Drain bias tee

Beginning with the design of the simplest network: drain bias tee. It requires a complete isolation for RF and free transit of DC voltage to the drain. Certainly, this circuit, and the next, will be based on inductors and capacitors (LC filters) to reduce dissipation of energy due to resistance.

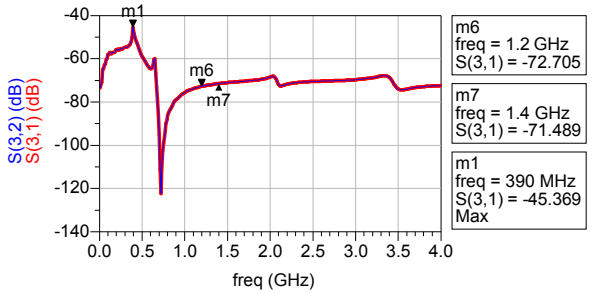
The schematic of the drain bias network is shown below(figure 5.3). The transmission lines and the ground vias were defined according to the characteristics of the board's layer substrate. For the purpose of this design, a generic type of board will be used. At Thales NL, ROGERS R4003C^{TM3} laminate is used for the RF layer covered with solder mask for component placement accuracy. The footprints and the S-parameter blocks were provided by the manufacturer and the small connectors between transmission lines are part of COM1 library.



(a) Insertion loss between RF ports.



(b) Return loss between RF ports.



(c) Insertion loss from DC to RF input (red) and to RF output port (blue).

Figure 5.2: *S-parameters of the drain bias network.*

[3]ROGERS R4003C^{TM} a trademark material of ROGERS Corporation.

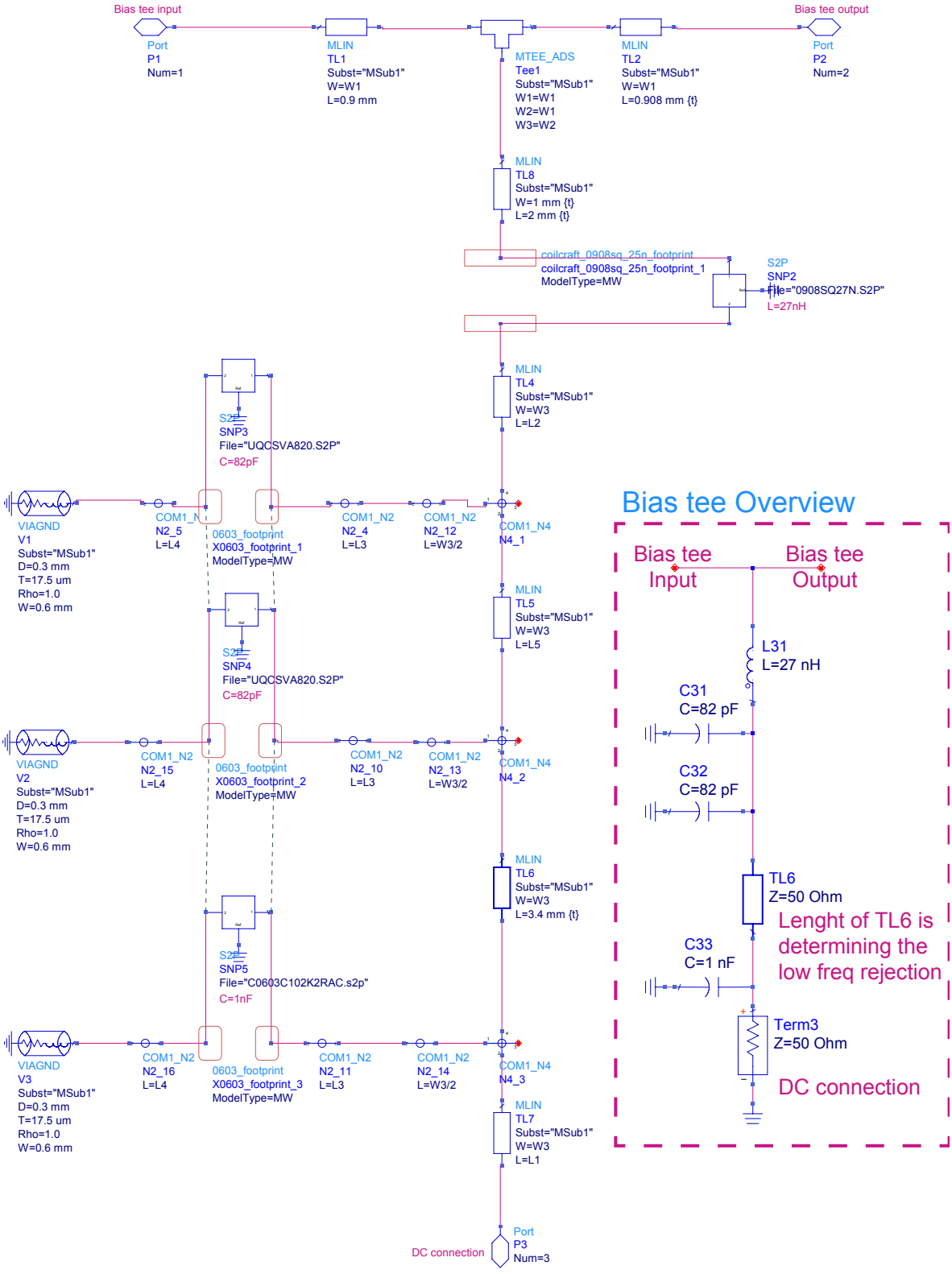


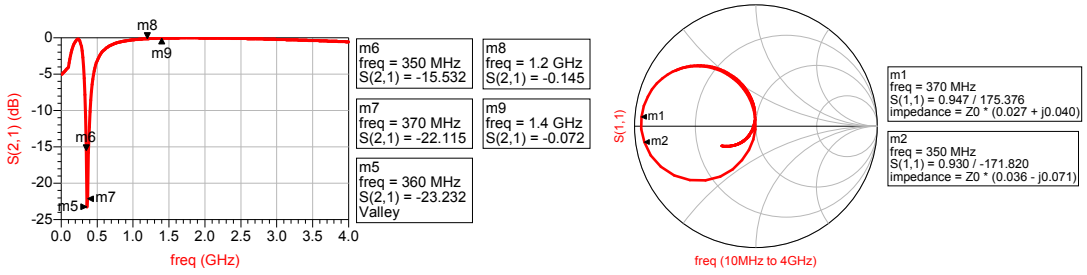
Figure 5.3: *Drain bias tee designed with transmission lines and S-parameter blocks.*

The requirements of this network are clear and were mentioned before. Figure 5.2 shows the S-parameters of figure 5.3 where port 1 represents RF input port, port 2 the RF output port, and port 3 the DC port. This schematic does not have the coupling capacitor between port 1 and 2 due to the matching network that will be after port 2 and will provide isolation between DC and RF output (fig. 5.1). In this case, all ports were carefully terminated with a 50Ω load. Note that, together with large circuit, there is a smaller and simpler version of the large network design made in ideal components. This network was included only for a better understanding of the larger circuit.

Between DC and RF output port, there are three parallel capacitors and a series inductor. In series, there is the choke inductor and, in parallel, the two $82pF$ capacitors provide low impedance for RF signal, suppressing any signal that may pass through the choke inductor and, $1nF$ capacitor is used to eliminate high frequency noise that may arise from the power supply.

From figure 5.2(a) and 5.2(b), one can see that insertion loss between RF ports is less than 0.02 dB for the RF bandwidth of the input signal, with a return loss below -30 dB on both ports. The rejection loss from DC to the RF input/output is always below -40 dB, so that no AC signal arrives at the power supply but DC is presented at the transistor drain, with no problem (fig. 5.2(c)). The insertion loss is not defined for DC due to limitations of the S-parameter blocks however, one can predict that its value would be close to 0 dB. At 390 MHz, an unusual disturbance sets the maximum of rejection loss. It was seen that the length of transmission line TL6 had a major impact on it thus, its size was thoroughly tuned for the best overall rejection of the network.

The filter used to suppress the dither at the output of the driver was considered part of the drain bias. Before was said that it should present a short-circuit to the transistor at dither frequencies. For the simplicity of the circuit, a second-order band-pass filter with 358 MHz resonance frequency was chosen. In appendix C, figure C.1 describes the schematic of the filter together with the drain bias tee (represented as BIAS1 block). Figure 5.4(a) shows the insertion loss changes in relation to 5.2(a), around the dither frequency, a good insertion loss is attained, values below -15 dB are achieved despite that, at RF, the losses have a small increase, worst case is at 1200 MHz, -0.14 dB. The smith chart confirms the short circuit for the dither bandwidth.



(a) Insertion loss of the drain bias tee combined with output dither filter.

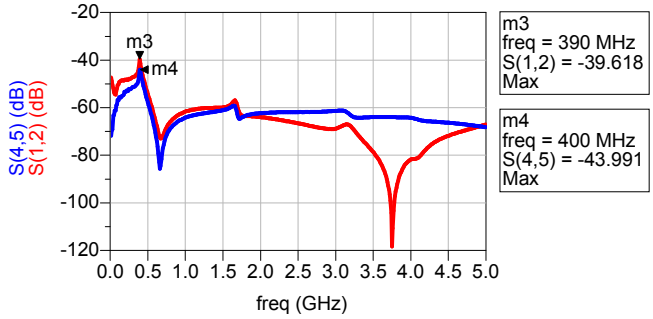
(b) Smith chart plot of the return loss of the same circuit.

Figure 5.4: *S-parameters of the drain bias tee combined with output dither filter.*

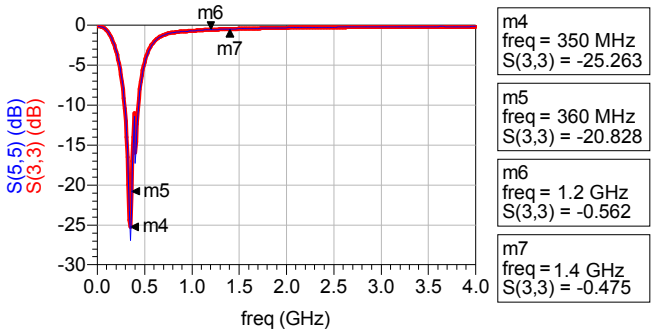
5.1.2 Gate bias tee

The gate bias will have the same structure of the drain bias tee with the input network for the dither, presented in previous chapter. In appendix C, in figure C.1, the second and the third schematics represent the complete gate bias tee (bias tee plus input network for dither). The second schematic shows two different approaches of the same circuit, one is based on transmission line simulation models and the other is based on MOMENTUM structures analysis (valid from 100 MHz up to 6 GHz). Port 1&4 represents the supply/DC input, port 2&5 connects to the gate bias input of driver and port 3&6 is the dither input, all terminated with 50Ω (the dither input is connected through a corner to the bias tee due to spacing issues). The linear behaviour of this combination was explained in the previous chapter. Here, only the non-ideal behaviour of the components is added to the equation. Simulations results can be seen in figure 5.5(a). An equivalent analysis like the one made for drain bias can be made. In this case, TL6 was tuned to a different length for the same reason.

The third schematic for this section, in appendix C.1, presents the same schematic structure with ports 2&5 connected to the gate bias input of the driver. This way, a "real" evaluation of input network for the dither can be done. A reasonable return loss, below -20 dB, can be attained (fig. 5.5(b)). The synthetized input network does provide the necessary improvement from the original -4 dB return loss.



(a) Insertion loss for both transmission line (red) and MOMENTUM structure (blue) based schematics, terminated with 50Ω at all ports (Appendix C.1-2^{nd} schematic).



(b) Return loss for both transmission line (red) and MOMENTUM structure (blue) based schematics, with the UMS driver at RF port (Appendix C.1-3^{rd} schematic).

Figure 5.5: *Gate bias tee.*

On a side note, it is interesting to analyze how close both transmission lines and MOMENTUM

structure based schematics are.

5.2 Output matching network

This part of the project was the most interesting one, where the simulation was matched with the practice.

In this chapter, the merger of the drain bias tee with a filter to suppress the dither, and with the output matching network, responsible for the maximum PAE achievable for the circuit and class F^{-1} of operation, will be done. For simplicity, let us consider each part of the complete output matching separately, the complete output network will be the combination of three parts that must be brought together: drain bias, dither filter and RF matching network.

This was a critical and challenging part of the project since it concentrated, at the output, three different networks. The drain bias tee and the filter to eliminate the dither were presented before. They are almost impartial at RF frequencies thus, another network needed be built to set the operation class of the transistors and match the circuit for its optimal conditions. Both situations were discussed in chapter 4 but only for 1300 MHz.

Starting with the optimal conditions for the circuit, figure 5.6 shows the impedance contours for which the PAE or the power delivered to the load has its maximal value. Each amplitude/phase plot (or smith chart) has three different contours, one for each RF frequency: 1200, 1300 and 1400 MHz. All simulations were done for a one tone input signal($P_{RF} = 30.5\ dBm$) with low-frequency dithering ($P_{dither} = 31\ dBm$). The input powers were chosen according to the limits of the driver and, having in mind, that the amplitude of the dither needs to be higher that the input signal. In the next chapter, one will see that these values are not easy to achieve during test due to power range limitation of the pre-amplifiers, especially the dither's one.

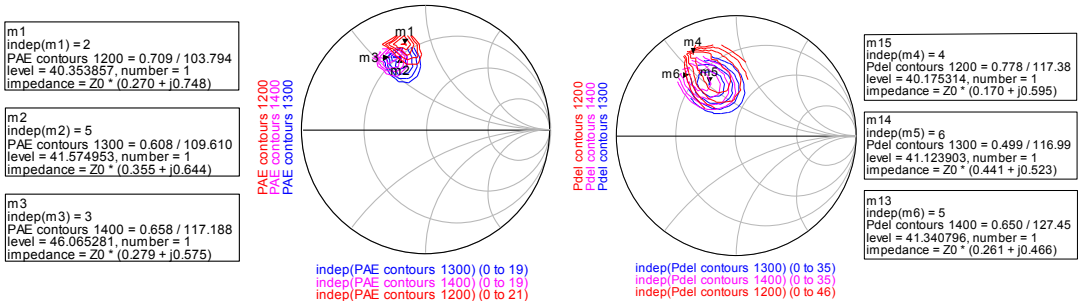
In the figure, each marker represents the maximum PAE or power delivered to the load for each frequency. After achieving the optimal points, one must choose between the two different impedance values established for each frequency or a trade-off between these two optimums, because the matching network can only represent one impedance for each frequency. The impedance value that achieves the maximum PAE value was chosen because dither will be a power signal and this situation may bring efficiency issues. Therefore, the impedances wanted to be seen at the output of the UMS driver are:

- Z_L(1200 MHz)=13+j37Ω;
- Z_L(1300 MHz)=17+j33Ω;
- Z_L(1400 MHz)=13.8+j29Ω;

Of course, the more points are taken into account, spread over the bandwidth, the better output response the system would have, nevertheless the complexity of the network would increase exponentially.

On an additional note, at 1200 MHz, the maximum power delivered to the load is 40.19 dBm and the maximum PAE is 40.45% while for 1300 MHz, the maxima are 41.13 dBm and 41.67% and, for 1400 MHz, are 41.35 dBm and 46.17%, respectively.

Before, it was decided to change the operation class of the transistors to a SMPA and the best efficiency configuration found, using this driver, was class F^{-1}. In chapter 4, it was



(a) PAE contours (step size=1%).

(b) Power delivered to the load contours (step size=0.25 dBm).

Figure 5.6: *Impedance contours for optimal PAE and power delivered to the load, for three different frequencies.*

also explained that, although a normal load impedance configuration for this operation class should be an open to even harmonics and a short to odd harmonics, the package introduces parasitics that shift the external optimum harmonic impedances away from the expected class F^{-1}. However, after tuning of the third harmonic, characteristic F^{-1} drain waveforms can be obtained at the internal drain generator test point available in the UMS driver model. This happened for high impedance of the second and third harmonic, the fourth and fifth harmonic do not have a large impact on the overall efficiency.

Thus, matching the output of the driver to those specific impedance values for three specific inside band frequencies and also for the first two harmonics, is the goal.

Based on transmission lines, in fig. 5.7 or fig. C.5, the RF matching network was built with discrete/lumped components instead of, for example, microstrip lines. The reason behind this decision has to do with the restrictions in boards' size when using microstrip lines (λ(1GHz) =0.3m), as well as the periodic behaviour they introduce. Lumped components also have small size comparative to their work-frequencies: the complete output matching depicted, in the appendix, in figure C.6 is based on MOMENTUM structures, occupies less than 1.5 cm, and their behaviour is reasonable well predicted by the manufacturer (S-parameter characterization blocks). This picture can predict a closer performance of the "real" matching then figure 5.7 which is represented by ideal components.

As shown previously, in figure 5.7, the RF network is a fourth order filter, plus the dither filter and the drain bias.Regarding to the fourth order filter, at a first sight, it seems a too complex filter to deal with however, simulations started with lower orders but reasonable results could not be achieved. Too little tuning parameters were available for the complex goals that were set while tuning the components for low order filters. Increasing the order of the filter allowed more degrees of freedom to tune every component. The fourth order filter was a trade-off between insertion losses and "tuning freedom". In 5.8, it can be seen how close the MOMENTUM structure depicted in C.6 is to fig. C.5 structure (both in the appendix) and how far are both from the impedance values which provide maximum PAE, for each frequency (three small colourful dots).

Here, the dither frequencies are not represented due to S-parameter block limitations, however the circuit behaves as depicted in figure 5.4 for dither bandwidth.

Looking to picture 5.8, marker 1 (1200 MHz), 2 (1300 MHz), 3 (1400 MHz) and 5 (2^{nd} harmonic) are really close to the expected "theoretical" places. However, marker 7 (3^{rd}

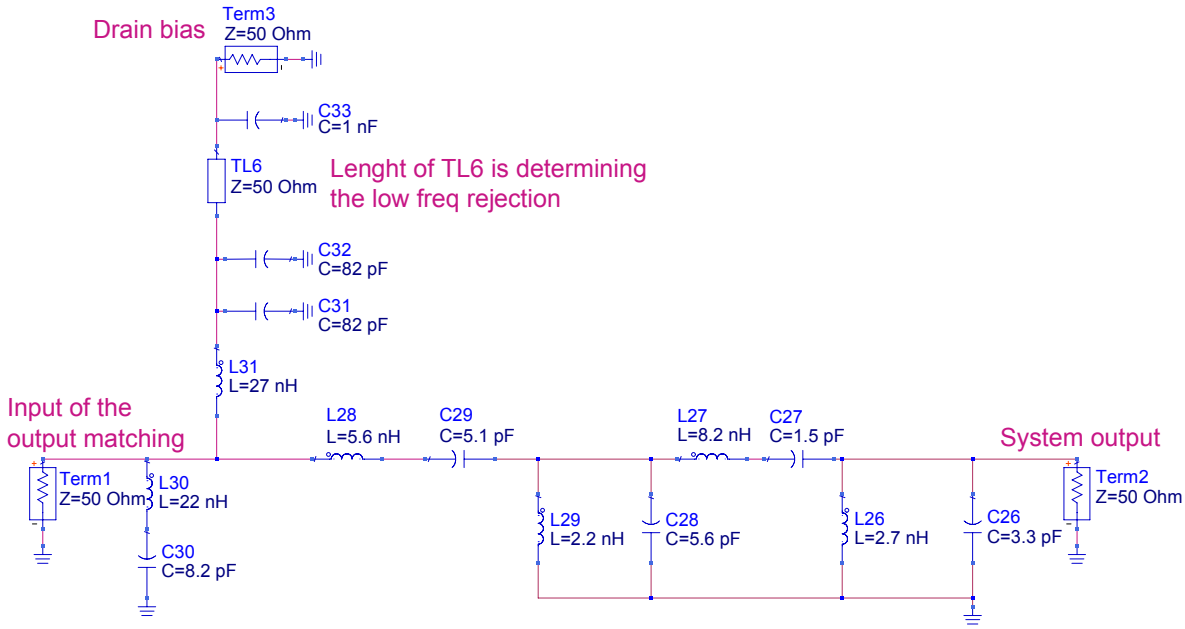


Figure 5.7: *Complete matching circuit with all ports terminated with a 50Ω load. Port 1 is connected to the output of the driver and port 3, at the power supply of the drain. Between these ports, one can see the dither filter and after the drain bias, the RF matching is drawn. Port 2 connects to the load.*

harmonic) is slightly off place. It should be closer to marker 5 (open circuit) but the output network has cannot provide that. To be able to place the third harmonic on top of the second one, a higher order filter needed to be included at the output which would mean more spread, more components,higher insertion losses, less reliability,... As increasing complexity also brings drawbacks, the fourth order output filter was kept and checked by a load pull simulation on the third harmonic to know how critical the mismatch would be for PAE performance. It is known that the PAE contours for harmonics are not so steep as for RF frequencies (fig. 5.9).

Marker 1 shows that the PAE is actually only decreased by 0.5%, relative to the originally determined optimum third harmonic impedance.

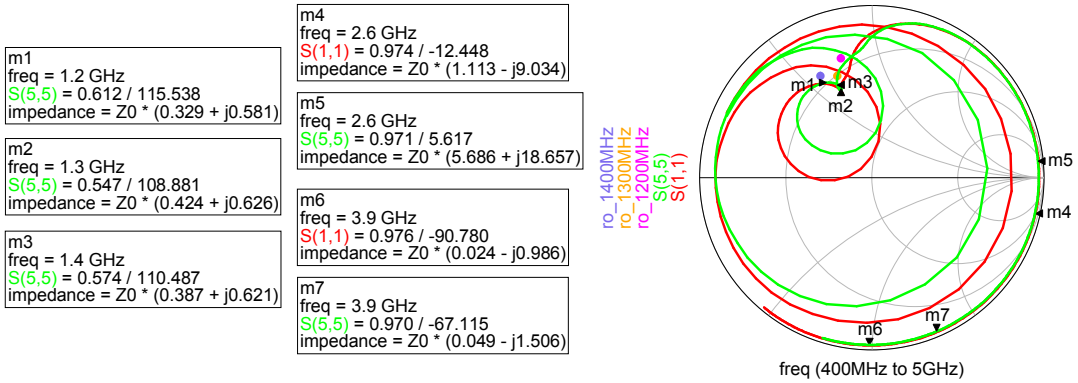


Figure 5.8: *Amplitude and phase representation of the return loss of the complete output matching network. Only available for frequencies higher than 400 MHz[A]. The three dots represent the impedances with which the maximum PAE is achieved.*

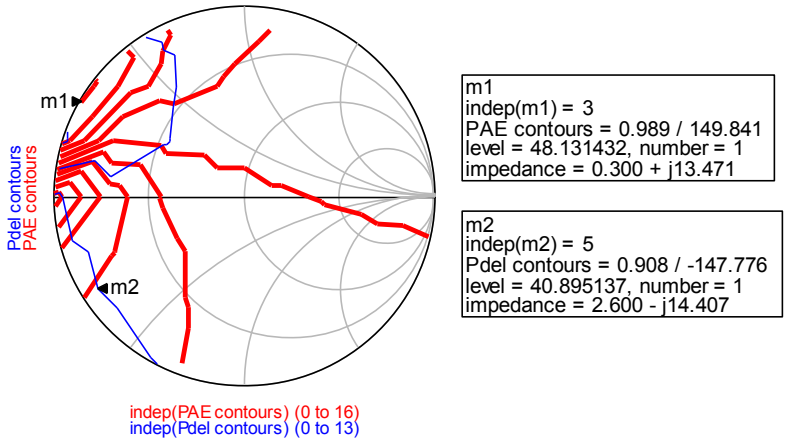


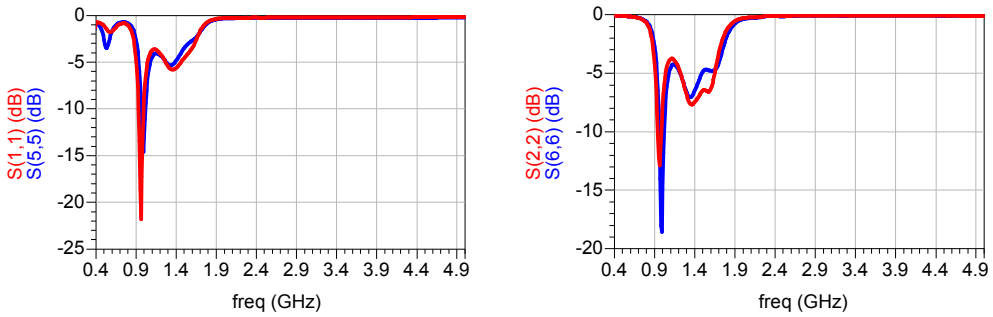
Figure 5.9: *Load-pull of the third harmonic. PAE step size is 0.5% and power delivered to the load is 0.25dBm.*

Synthesis of the RF matching network with ideal/lumped components, addition of the drain and dither filter, re-tuning of the complete matching, updating the lumped components models to S-parameter blocks and inclusion of the required transmission lines between them, finally checking the complete structure in MOMENTUM and compare all results, completes the design procedure to come to a manufacturable solution. In figure 5.10 the S-parameters, for 50Ω terminations, are plotted. In 5.10(c), the gain of the complete structure can be seen. It is expected that, when the driver is placed at the input of the network, the insertion loss will be smaller (simulation here is done using 50Ω ports while the driver non-linear equivalent output impedance is of course not 50Ω) however, the filter can be checked for some critical aspects: high output return loss for both lower frequencies, as dither's, and higher frequencies, as harmonic products.

For one tone simulation with LFD and with the complete output matching at the output, simulations for 1200, 1300 and 1400 MHz, predicted a PAE and a correspondent power delivered to the load of 20.5% and 38.94 dBm, 30.7% and 39.92 dBm, and 32.22% and 39.83 dBm. This deviates somehow from the values given in the beginning of the chapter, however it was shown that the optimal points for each impedance are close but not on the right place. The higher order filter introduces insertion losses and fundamental load-pull contours are rather steep so, small impedance variations can give large PAE variations.

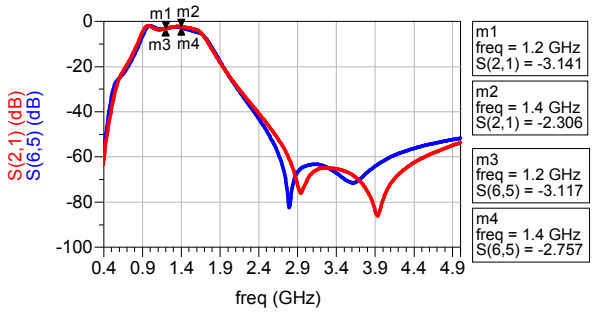
Despite this result, a prototype will be assembled to prove the concept. If one had more time, a deep analysis on these results would have been done because a different approach for the output network or corrections on the previous used could lead to better efficiency values.

[4]Some of the S-parameter blocks are only available from 400 MHz on so, even if the dither filter is there, the non-predicted behaviour of the S-parameter blocks results in unreliable simulations (hides the right behaviour). For lower frequencies, one should look into figure 5.4



(a) Input return loss.

(b) Output return loss.



(c) Transfer function of the filter.

Figure 5.10: *S-parameters of the output matching network for both transmission line (red) and MOMENTUM structure (blue), terminated with* 50Ω *at all ports circuit. Note that the output impedance of the driver is not* 50Ω.

Chapter 6

Measurements

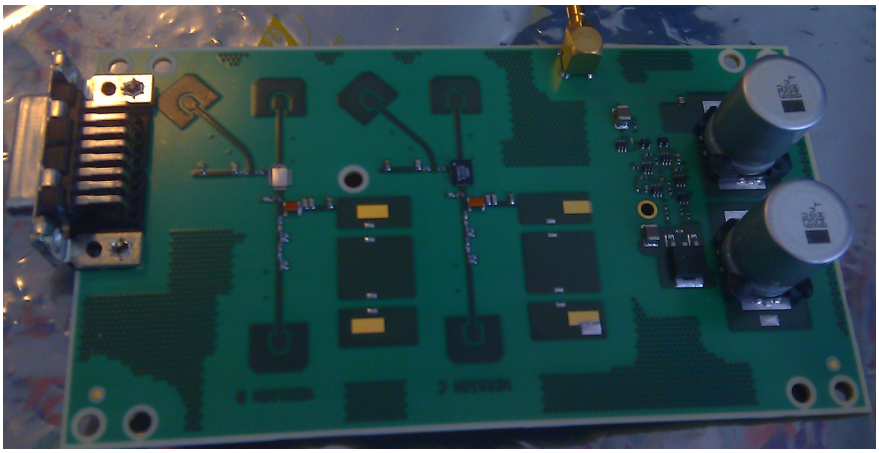


Figure 6.1: *Designed board – AMPi.*

Chapter 6 intends to show a comparison between measurements and the simulation results previously shown. In the layout panel sent to production, besides the board with with all the developed structures, also simpler and only passive boards were built: gate bias tee with dither input network and another one with the complete output network (drain bias+dither filter +matching network). These boards were used to draw the first conclusions about simulation versus measurement results. This way, a reduction in the complexity of the complete circuit analysis can be achieved, and separate deviations of the different structures can be checked.

In the panel sent to production, two similar versions of the circuit presented in the previous chapter, together with two alternative versions of the complete circuit (networks of the same type but with different component values), two passive network circuits, for further S-parameter comparison with the simulations, and a board without the output matching network (only a decoupling capacitor and the dither filter) were included. The layout of the panel sent to production can be found in the appendix, in figure D.2. For simplicity of measurements, drain paths were added to the circuits to easily measure the current. Also, some screw holes were drawn to further attach a small heatsink (piece of copper with air slots) on the backside of the Printed Circuit Board (PCB) for efficient heat dissipation.

Due to time limitations, the alternative versions of the circuit were not fully characterized; only the S-parameters of the passive networks board and comparisons between versions with

the complete output network were analyzed. To characterize the performance of these boards, small signal, large signal and two-tone measurements were performed. In chapter 4, the required settings for pulsed RADAR signals and the biasing point of the transistors were listed. The following measurements will use those settings which are re-listed below:

- V_d=45 V, pulsed signal described in chapter 4;
- I_{dq}=120 mA (V_g ≈-1.9 V CW).
- L-Band RF signal with an envelope modulation of a 2 KHz square wave with 10%Duty Cycle (50μs on);

One tone large signal measurements were done using an automatic test bench controlled by LabView[1] software that collected the data over time with power peak sensors.

These data needed to be processed offline because the output recordings were a square pulse that is on 10% of the total period and the rest of the time, off. Since the square wave shape of the envelope signal is not the interest but the value of the current and voltage drain amplitude, an average of the amplitude within those 10% of the period, when the pulse is on, is required. The output signal is a typical RADAR square pulse (explained in chapter 1).

These data needed to be processed offline and, because the output recordings were square pulses with 10% duty-cycle, an average of the respective values within the pulse was done. In D.3 is depicted the settings of the MATLAB script used to treat the data. According to the script, with a 50μs pulse-on, the amplitude of the pulse is only taken into account 5μ after the pulse starts and 5μ before it stops. This happens to avoid the overshoot effects, after the rising edge, and the average is calculated up to 5μs before it goes off, to get rid of the falling edge effects. In the same figure, it can be seen that the amplitude is not constant over the pulse, it decreases because the junction temperature of the channel increases dynamically with short time constants, leading to drain current decrease but also, at the same time, the supply voltage provided by the power supply energy storage capacitors decreases as current id being drawn.

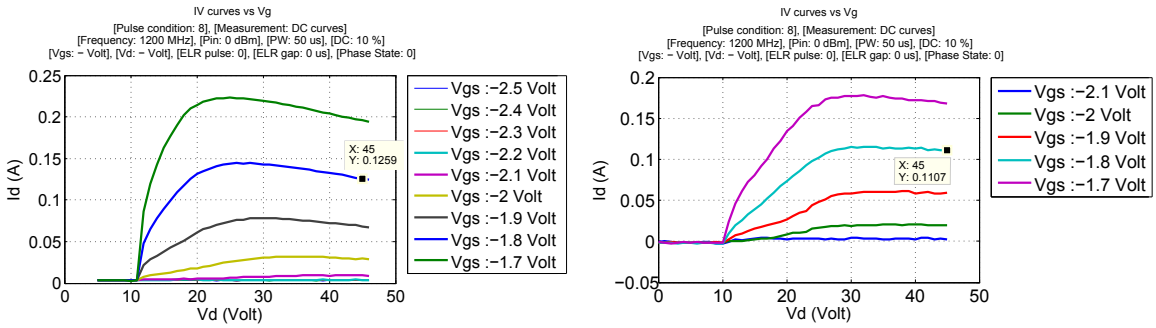
Before starting to show the results, it is important to check for differences between the boards that will be measured so that an easier and better understanding of the following results can be gained. Therefore, the results of four different boards will be depicted, two only with passive components (gate+dither input network and output network) and other two with an active device (board 1& 2, different versions with the same matching). The cooling of the driver was done with the heatsink mentioned before and a fan.

All information previously described holds for the complete chapter.

6.1 IV curves

In this section, the correct biasing point will be measured in order to correctly bias the transistor power bar. To find the proper gate voltage value corresponding to the recommended 120 mA at the drain, a sweep in the gate voltage was performed and the values of the current at the drain were listed (one is assuming V_d=45 V and no RF signal for "quiescent" bias point). Figure 6.2 and 6.3 display the IV curves for board 1 and 2. Although it is usual

[1]LabView a software product of National Instruments.



(a) Board 1 (b) Board 2

Figure 6.2: *IV curve versus gate voltage.*

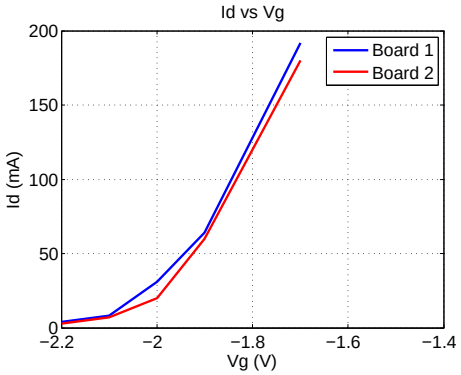


Figure 6.3: *I_d as function of V_g for a fixed V_d=45 V, for two different versions of the prototype board.*

to see some spread between samples, in 6.3 is represented the variation of the I_d over gate voltage and, both curves are rather similar.

As UMS recommends to operate the device with an I_{dq} of 120 mA, the gate voltage should be -1.8 V for both boards.

6.2 Small signal measurements

This section will be divided in two parts, passive and active measurements. For the first case, only a Vector Network Analyzer (VNA) was used to characterize the Device Under Test (DUT). By DUT, one means the gate bias tee with the dither input network or the passive output network circuits. For small signal measurements containing the board with the active device, a vector network analyzer and an attenuator at the output of the boards were used (figure 6.4).

To study the gate network, after careful calibration the complete test environment, port 1 of the VNA was connected to the gate input, port 2 to the DC input and port 3, to dither input of the network. Simulation and measurement results are depicted in 6.5. The behaviours of the curves are rather similar however, there exists an offset. The critical point for both curves is at 390 MHz because is where less isolation is achieved. The biggest offset between measurements and simulations is attained for lower frequencies, close to the dither bandwidth

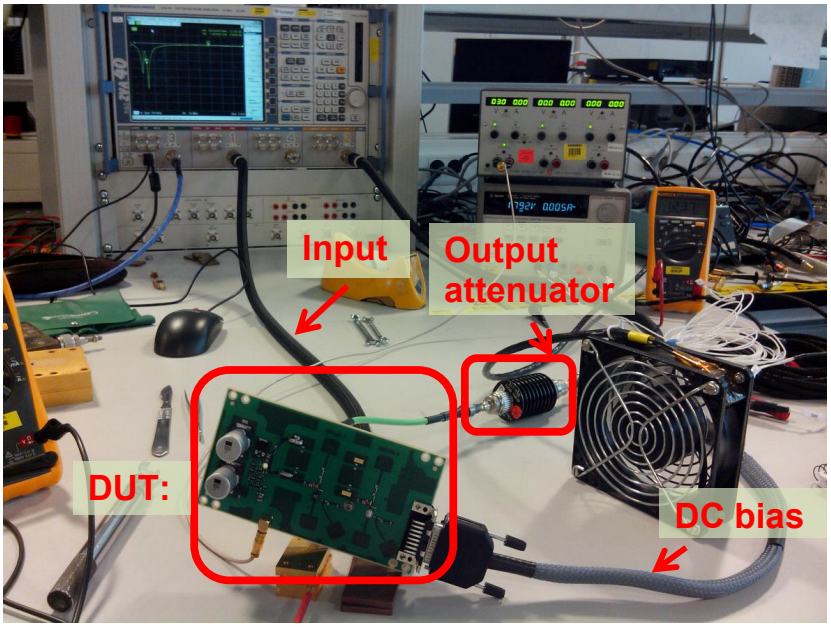


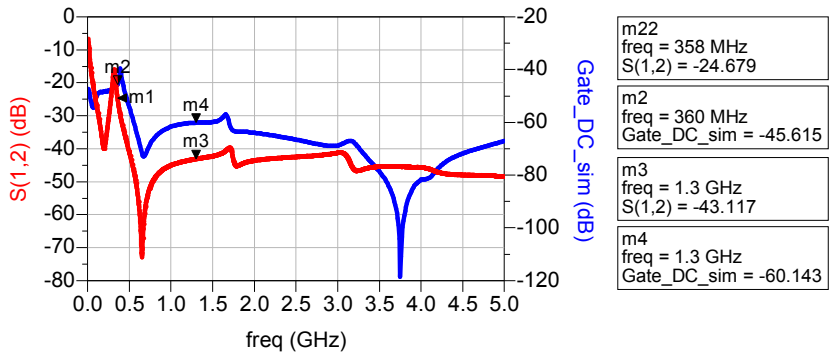
Figure 6.4: *Small signal measurements setup.*

mainly because of the impact of dither input filter. It has a good performance for frequencies above 500 MHz (insertion losses below -40 dB). On the other hand, the results for the output network with a fourth order filter are shown in figure 6.6. The weak spot of such a network is the number of components. More components carry more spread in the final design, they increase the sensitivity of the network. Therefore, some variation compared to what was shown in the previous chapter, was being expected. Figure 6.6(a) shows the return loss at the RF input of the passive board. It presents a really low impedance at dither frequency and high impedance for the second and third harmonics however, at RF, it suffered a rotation/delay that moved away the sweet spots. This deviation from the simulated target will have serious effects on the efficiency of the total circuit thus, some ideas to try to understand the reason were tried out. The first explanation that came up was the spread that could be introduced by each component thus, a comparison of the measurements with the results of a yield analysis was done(figure 6.7, analysis based on a Monte-Carlo approximation).

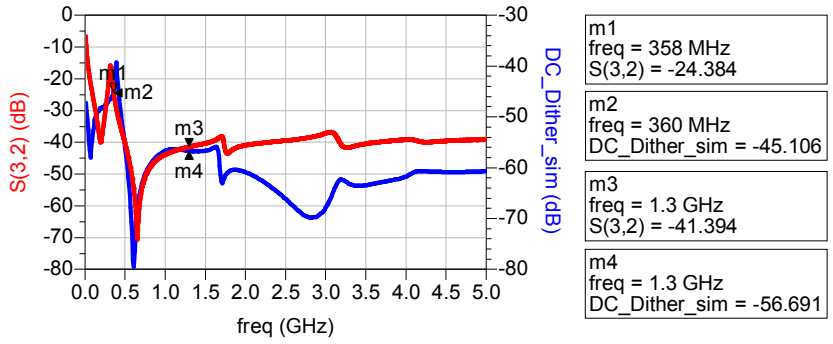
The behaviour at RF seemed not be compatible with the yield analysis results. Other ideas, such as the mismatches between the S-parameter blocks (provided by the manufacturer) used on simulation and the S-parameters of the components available for the board, the impact of the solder mask at the output or calibration issues were analyzed. In-house measurements of discrete SMD components and with different ε_r for the substrate were done and none seemed to give such different result.

There was a world of possibilities that could be causing that delay and time was short and the complete boards could not even suffer from that problem, thus measurements with board 1 and 2 began. Board 1 and 2 are two versions of the final prototype.

For V_d=45 V, I_{dq}=120 mA, V_g=-1.8 V and a small CW signal at the input, the results displayed in figure 6.8 and 6.9 were obtained. In these pictures, another comparison with the simulations previously done, is presented. The simulations are, once again, based on momentum structures and using S-parameter blocks, the closest simulation to reality. Figure 6.8 and



(a)

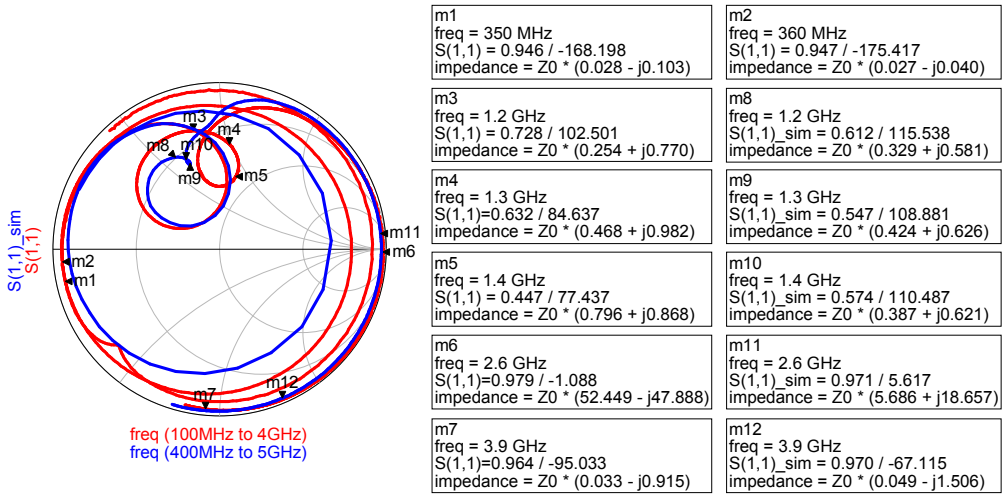


(b)

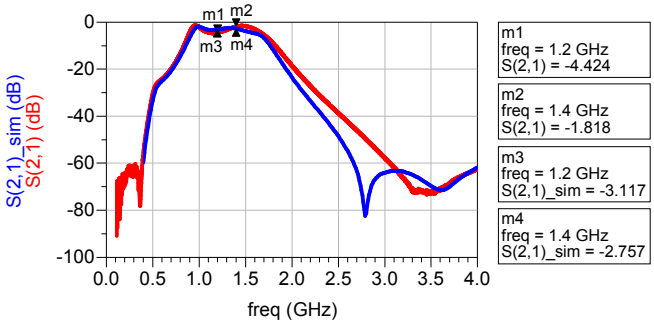
Figure 6.5: (*a*) : *Gate(port1) to DC input(port2) and,* (*b*) : *DC to dither input (port3) insertion loss. 50Ω termination for all ports.*

6.9 show the results for board 1 and 2, respectively.

The gain of both boards is rather different. Despite in the datasheet is written that the gain of the driver may vary, more or less, 2 dB, and the typical small signal gain is 18 dB in-band, board 1 only presents around 13 dB of gain, at 1400 MHz. This can be explained by the worse deviation seen in the output return loss of this board (fig. 6.8(c)), when compared to the simulations. The matching network looks de-tuned (similar to 6.6), causing the reduction of the gain for L-Band. Board 2 shows a gain above 17 dB for all RF bandwidth, 18 dB at 1200 MHz, which is much closer to the expected results. The output return loss (6.9(d))of this board is also within the simulation results however, its input return loss (6.9(c)) seemed to display a slight shift in frequency, degrading the input performance of the board. This input matching problem can not be studied further since it comes from the internal input matching circuit of the UMS driver.



(a) Return loss



(b) S_{21}

Figure 6.6: *S-parameter of the output network. Comparison between simulations (blue) and measurements (red) results.*

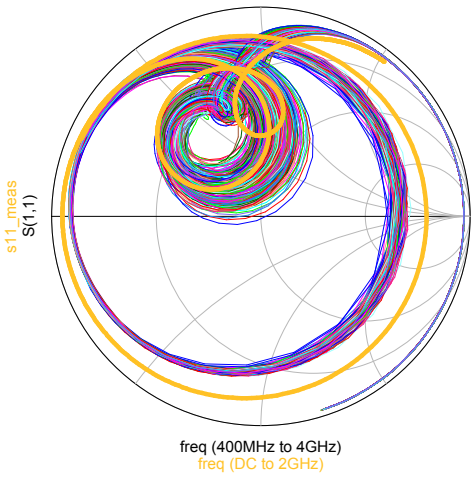
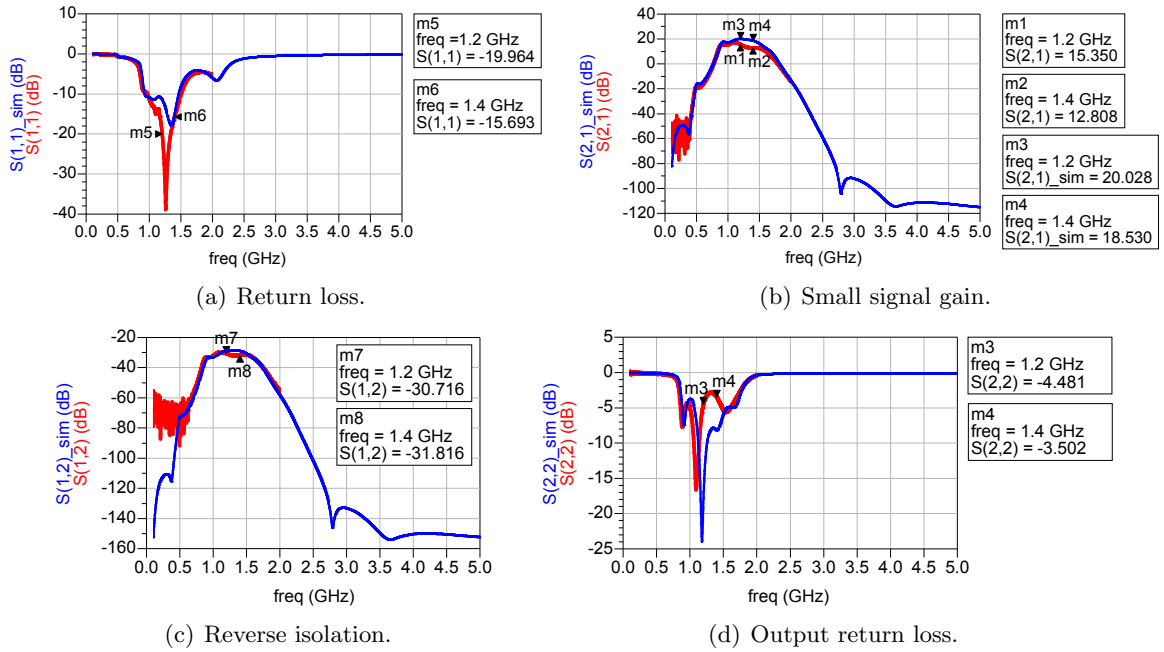


Figure 6.7: *Yield analysis performed on the momentum structure schematic.*



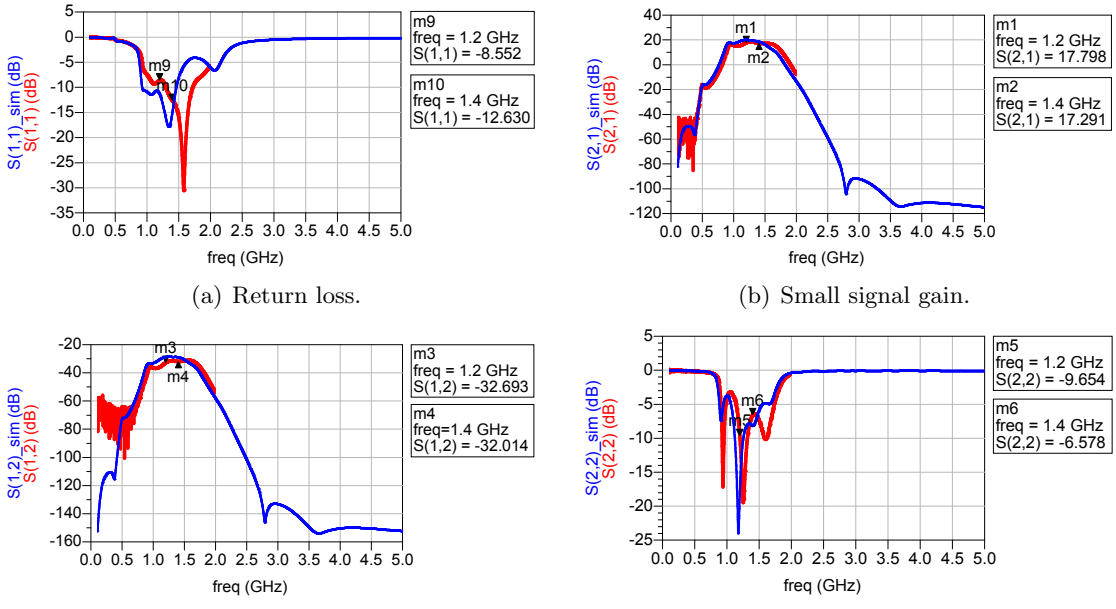
(a) Return loss.

(b) Small signal gain.

(c) Reverse isolation.

(d) Output return loss.

Figure 6.8: *Small CW signal measurements for board 1. In blue are represented the simulation and, in red, the respective measurement results. It is important to note that the ADS model, as mentioned previously, was modelled using an RF pulsed signal (typical RF pulse).*



(a) Return loss.

(b) Small signal gain.

(c) Reverse isolation.

(d) Output return loss.

Figure 6.9: *Small CW signal measurements for board 2. In blue are represented the simulation and, in red, the respective measurement results. It is important to note that the ADS model, as mention previously, was established using an RF pulsed signal (typical RF pulse).*

Board 2 was chosen to perform large signal analysis since it has higher gain and a similar output return loss. These characteristics denote an output network closer to the ideal (simulated), hence a better performance of the class F^{-1} and the dithering technique is expected.

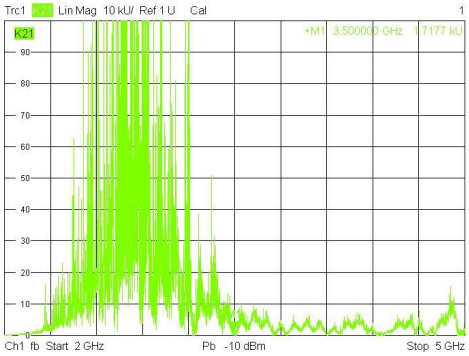
Before large signal analysis, the (small-signal) stability of the board was measured. Using the VNA, K-factor calculations were performed. In chapter 4, one discussed about the requirements for a unconditional stability of a system: K>1, for all frequencies. Figures C.4 and C.4 prove the stability of the complete board.

The input that was not being uses, was loaded to 50Ω.

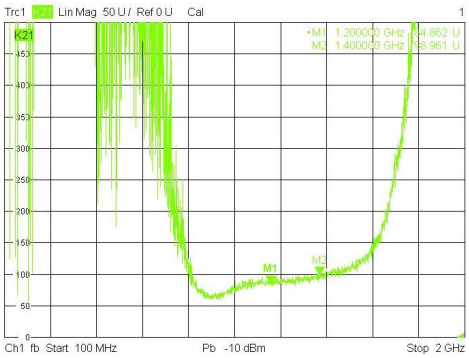
A closer look into the stability plot 6.10(b) shows that K is always above 12 and for 6.10(d), above 20. Below 100 MHz, the results given by the equipment are not trustworthy due to calibration limitations.

These measurements were divided in two plots because two different calibrations had to be used, one from 100 MHz up to 2 GHz and the other, from 2 till 5 GHz.

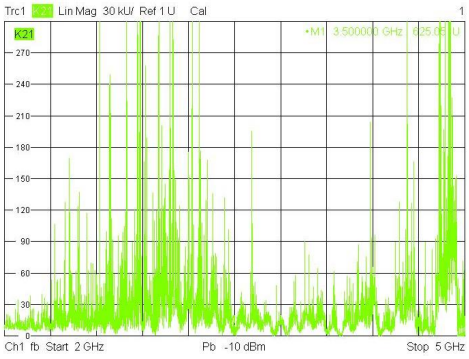
(a) K-factor from RF input to output.



(b) K-factor from RF input to output, at high frequency.



(c) K-factor from dither input to output.



(d) K-factor from dither input to output, at high frequency.

Figure 6.10: *Stability analysis of AMPi.*

6.3 Large signal measurements

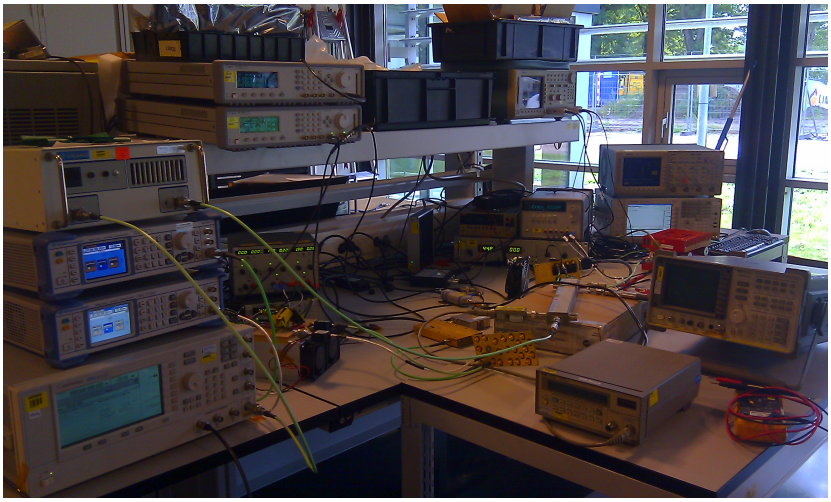


Figure 6.11: *Low-frequency dithering test bench for one and two tone measurements.*

Figure 6.11 is a photo of the complete test bench for one input tone, implemented at the lab. The block diagram of the photo is represented in 6.12 and, the setup allows an extraction of the system gain in a very simple form. To analyze the output spectrum, the power sensor would need to be replaced by a spectrum analyzer.

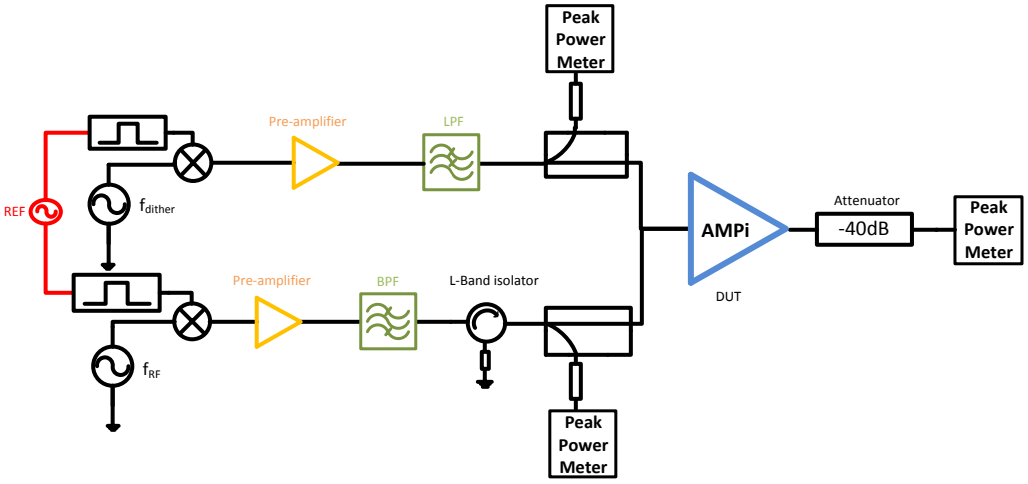
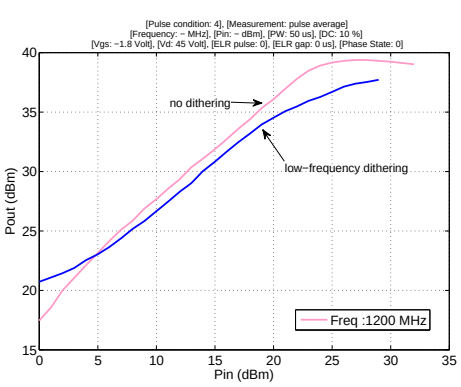


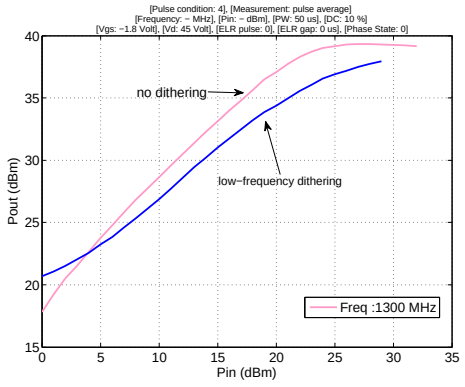
Figure 6.12: *One tone, low-frequency dithering block diagram.*

Taking advantage of the power sensors and LabView software, P_{in} versus P_{out} curves will be drawn. The effect of the low-frequency dithering for one tone input signal is pictured in 6.13. Measurements performed with the spectrum analyzer, at 1300 MHz, showed an improvement of 6 dB for IM3: IM3(normal system)=-55.03 dBm and IM3(dithered system)=60.74 dBm, for a 29 dBm input signal and a 29.6 dBm dither signal.

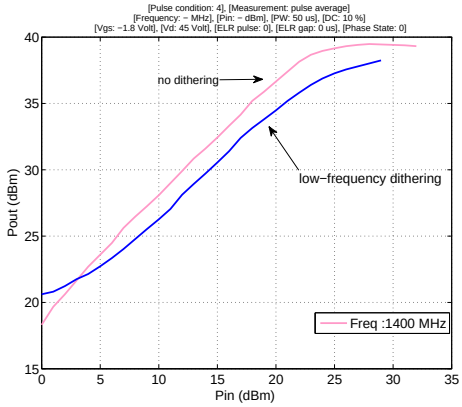
While characterizing the available pre-amplifier to provide the dither signal, it was noticed that it could not deliver an output power as high as one would wished for (simulations were



(a) 1200 MHz input signal.



(b) 1300 MHz input signal.



(c) 1400 MHz input signal.

Figure 6.13: *Power curves for one tone system, with and without LFD.*

done at 31 dBm dither power). The maximum power delivered in the dither bandwidth was around 29.5 dBm thus, adjustments in the input power range of the RF signal needed done accordingly. This will introduce differences between predictions and measurements, however the smoother effect can still be seen, for all frequencies. For low power, the LFD system artificially displays higher power gain due to the presence of the power of the dither harmonics close to the band that is integrated by the power sensor together with the actual useful RF signal power, dither leaking through the filter is, in this region, a relatively strong signal while the RF has low power in this situation.

It is important to take into account that the last points in each figure of 6.13 have the same amplitude for the RF input signal and dither, thus the linearity boundary condition is not satisfied and compression of the system starts to be seen. For better improvements, a stronger dither would have been needed.

Linearity of a system cannot only be measured by how pin/pout curves look like. Despite they seem to display a linear trend, another approach to prove the linearization of the system, needs to be taken. Much more relevant performance parameters are found in the frequency domain, the most easy to measure being the harmonics and the mixing products. Depending on the actual application, one also would characterize linearity with other figures of merits

that depend strongly of the type of modulation relevant (ACPR for example). In the lab, the simpler and more universal two-tone third-order modulation products has been measured. Figure 6.14 represents the block diagram for a two tone measurement that will be followed.

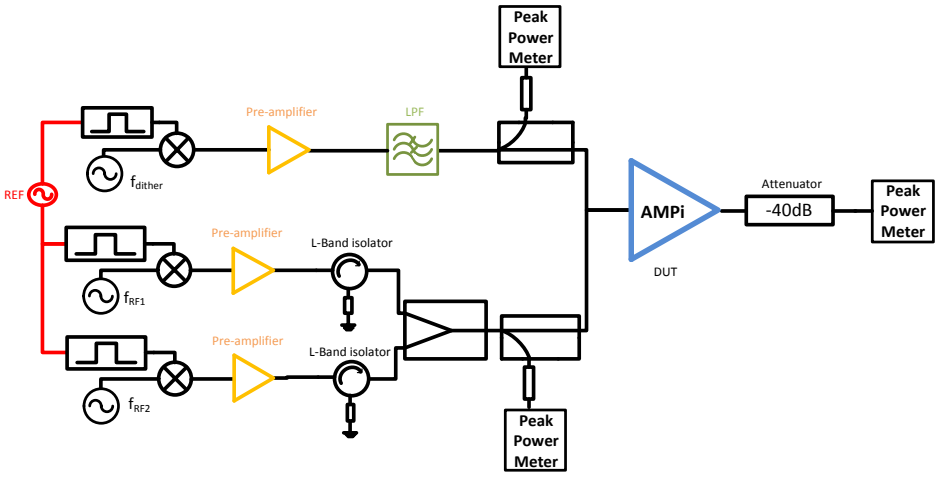
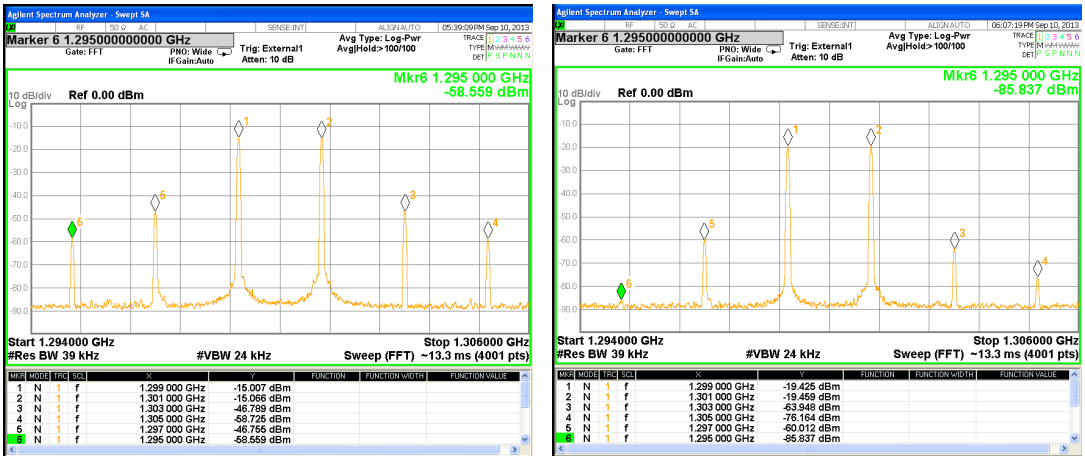


Figure 6.14: *Two tone, low-frequency dithering block diagram.*

For this setup, no automatic software was available to remotely control the devices and collect the data. Therefore, before measurements, a manual calibration between the two RF paths was performed to compensate for the power gain deltas between the two used pre-amplifiers and two-tone with equal amplitude were needed at the input of our amplifier. Their spectrum (harmonics and spurious) was carefully analyzed without the DUT as well as the dither signal, because it is essential that a clean signal is provided to the dithering amplifier to characterize its intrinsic performance. When the pre-amplifier of the dither had sufficient (its maximum) power to provide 29.5 dBm at the input of the dither on the board, the signal was already saturated thus, strong harmonic signals were seen, close to band (third and fourth harmonics).

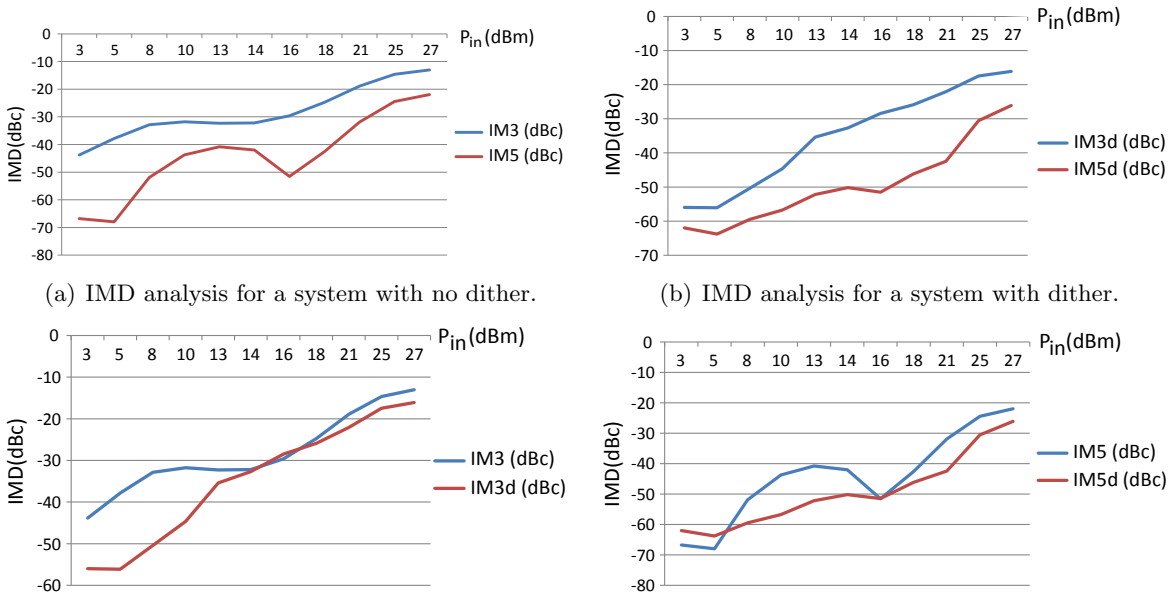
Figure 6.15 shows the output spectrum of a two tone measurement. In the first case, (a), the dither is not applied thus, the usual output of the system is depicted. In the second case, a 29.6 dBm dither is injected for the same input power signal. The output spectrum can be seen at 6.15(b). The difference in the IM3 and IM5 is easily seen. LFD does make a difference, in the frequency domain.

Analyzing tables 6.2 and 6.1, and plot reffig:imdm, one can see the influence of the dither at low power: lower amplitudes for intermodulation products are attained for a LFD system than for a system without dither. Looking at this table in another way, for a given IM3 value, the output power of the dithering system can be higher, for example: in a system with no dither, for 27.15 dBm output power, IM3 is -32.85 dBc and, for LFD, IM3 is -35.4 dBc. The PAE remains slightly lower, because the dither drives the amplifier into saturation and high current flowing through the drain is obtained, while an improvement in linearization is achieved. This high current, that directly influence the calculus of PAE, is attained because the bias point (class AB) is pushed by the dither towards class A. This behaviour cannot be avoided since for low power the amplifier will remain a class AB, only for higher power it starts to behave like class F^{-1}. This would not be the case for a SMPA.



(a) System with no dither. (b) System applying LFD.

Figure 6.15: *Output spectrum of two tone measurements without and with LFD (P_{dither} = 29.6 dBm), for a 10 dBm input signal. The amplitude values of the signals miss a correction factor, at the output.*



(a) IMD analysis for a system with no dither.

(b) IMD analysis for a system with dither.

(c) Comparison between IM3 for both systems, with (IM3d) and without dither (IM3).

(d) Comparison between IM5 for both systems, with (IM5d) and without dither (IM5).

Figure 6.16: *Intermodulation distortion for 1300 MHz.*

Table 6.1: *Two tone system performance, without dither.*

Input Power (dBm)	Output Power (dBm)	Id (mA)	IM3 (dBc)	IM5 (dBc)	PAE (%)
3	22.71	100	-43.84	-66.76	4.11
5	23.93	90	-37.83	-67.98	6.03
8	27.15	94	-32.85	-51.89	12.13
10	28.92	122	-31.77	-43.74	14.04
13	31.45	142	-32.30	-40.80	21.56
14	32.25	160	-32.20	-42.00	22.99
16	33.85	184	-29.60	-51.55	28.85
18	35.25	240	-24.75	-42.60	30.46
21	36.87	300	-18.92	-31.92	35.13
25	37.90	382	-14.65	-24.45	34.06
27	38.00	394	-13.05	-21.95	32.79

Nevertheless, the results can not be directly compared to simulations since different power values were used during testing. With dither, the system will be always working in saturation, and in chapter 3, it was shown that linearization improvements rely on the ratio between the amplitude of the RF signal and the amplitude of the given dither. Higher the ratio, higher the improvement.

In the measured case, the dither power was close/equal to the RF signal for high power signals, thus the impact is not so remarkable for high power as it is for low power signals. Increasing the power of the dither would thus improve the obtained results. Another interesting investigation path would be the use an amplifier with high impedance for the dither frequency, as mention in 3. This way, high amplitude voltages could be attained with less power delivered to the amplifier.

The last measurements performed with board 2 were pulse-to-pulse phase stability measurements that showed that the added phase noise to the RF signal from pulse-to-pulse is not affected by the dithered signal. This is a very important feature for radar systems because it shows that, despite the deterministic spurious introduced, as long as they are predicted, the dither does not interfere with the RF signal[2].

The results achieved do display some interesting trends showing the potential improvements of the linearity behaviour of the dithering techniques. The discrepancies between simulated and measured results show the level of complexity involved in the realisations of highly non-linear systems, despite the thoroughness of the non-linear modelling and simula-

[2]This is a very important fact, because in a RADAR system which uses the doppler shift to discriminate small moving targets against a stationary environment, one needs a very stable phase from transmitted pulse to transmitted pulse. That makes sure that the only phase shift that is seen between the received pulses originates from the target movement. Thus, the simple test that was done allow us to conclude that the dither signal has no influence on the phase from pulse to pulse. However, a test with a real frequency modulation (chirp) on the pulse and with pulse compression in the processing would be the real test.

Table 6.2: *Two tone system performance with dither.*

Input Power (dBm)	Output Power (dBm)	Id (mA)	IM3 (dBc)	IM5 (dBc)	PAE (%)
3	17.95	520	-56.00	-62.00	0.26
5	19.75	520	-56.10	-63.80	0.39
8	22.65	500	-50.40	-59.50	0.79
10	24.55	488	-44.64	-56.76	1.25
13	27.13	478	-35.39	-52.18	2.31
14	27.95	478	-32.70	-50.17	2.79
16	29.45	466	-28.45	-51.52	4.02
18	30.82	446	-25.92	-46.19	5.71
21	32.82	396	-22.07	-42.47	10.04
25	34.91	342	-17.46	-30.56	18.07
27	35.68	310	-16.10	-26.13	22.94

tion. Also, all real-world non-idealities and constraints have significant impact in the quality of the test results. Despite these difficulties, the manufactured prototype do show a functional dithering behaviour, with improved IMD characteristics.

Chapter 7

Conclusions

Achieving an improvement of linearity of a given power amplifier to be used in RADAR applications was the main goal of this thesis.

Throughout this report, a brief description of the conditions of such systems was presented in chapter 1 followed by a brief analysis of different linearity and efficiency improvement techniques for a solidification of the required knowledge. Moreover, in chapter 2, their principal strengths and weaknesses were listed, and a table with a summary of the state-of-the-art implementations for each one of them was presented. The simple fact that the dithering uses a SMPA which allows the RADAR system to keep using saturated input signals, and its simplicity and effectiveness, were crucial factors for this technique to be chosen. Also, the concept of low-frequency dithering is being studied at the TUe and prof. Reza Mahmoudi proposed to investigate its applicability to RADAR applications.

As a starting point, a mathematical proof of the dithering technique was developed in 3 and the practical requirements of the system were defined. This analysis also served to provide a deeper understanding of this technique. The MATLAB simulations achieved 10 dB distortion improvement of two-tone LFD IM3 for the same output power. This enhancement was earned at the expense of gain, because of the presence of the dither signal.

In chapter 4, a description of the amplifier, to be used in practice, was done. The manufacturer also provided an ADS model that allowed load-pull simulations to be made. The results also showed the same 10 dB improvement of IM3 and provided the ideal characteristics of the output matching network to be included with the driver. The design of the layout was presented in chapter 5. In chapter 6, results of small and large signal(one tone), two-tone and pulse-to-pulse phase stability measurement were shown.

Although the effect of dithering was clearly seen, the equipment limitations and manufacturing tolerances superimposed bounds in the results which introduced discrepancies between the original simulations and the measured results. Also, dithering is an open loop technique which provides a decrease of the distortion level at the expense of another signal be added to the circuit which may not be correlated to the input signal but, which do not need to add prohibitive power consumption if a suitable high-impedance scheme is used. It is rather simple, robust and stable compared with most linearization techniques. Within the frame of this project, the added value of the technique was seen, and confirms this could be a promising technique also when applied in the RADAR systems.

7.1 Recommendations

During the realization of this project, different mishaps showed up together with new ideas, to try to solve them. Due to the time boundaries of the plan, many paths were left aside as well as behaviours without explanation obtained while performing measurements. This section was reserved by the author, to list those situations.

Continuing the evaluation of the board with a high power dither, to be able to compare test results with load-pull simulations for the same conditions performed so far, would be interesting first step. Updating simulations is highly time consuming, since the model is operated in a highly non-linear domain, under multi-tone conditions for which it was not originally optimized. Convergence problems may arise as well as non-expected behaviours, one must be very careful and meticulous!

Pulse compression measurements would be a good way to draw more definite conclusions about actual results on a Radar pulse chirp and verify if the time sidelobes after pulse compression are indeed not affected by the dither signal.

After drawing more information about the first designed boards, a second board could be designed trying to fill in the lacks of the previous ones and combining a different input network for the dither, for example, trying to decrease the dither amplifier power consumption using high input impedance. Also, more time could be spent on the output matching network: smaller order filter would give less spread variations thus, better simulation predictions however, the biasing conditions would need to be changed. Work [14] done before this project, using the same linearization technique, achieved rather good results for a class D power amplifier for communication applications.

Althought information at the datasheet of the UMS driver shows a highly linear amplifier (Class AB), all our simulations, and also our first measurements do show significant linearity improvements can indeed be reached for the F^{-1} class.

Another interesting idea could be the shaping of the dither waveform. It is known that the sinusoidal waveform has a high probability density function near its extreme values. This way is hoped that the dither will have more impact in the extremes of the transfer function of the system. Knowing that for a square wave, the signal commutes between edges and its a summation of odd harmonics. If the 3rd harmonic is added to the dither, is the impact in system enhanced? In a similar way of thinking, several other shapes for the dither can be studied and final impact analyzed.

Last but not the least, is the implementation of a differential circuit as the dithered amplifier. A good match between both amplifiers could result in a symmetrical distortion of the differential signal which tends to cancel even-order harmonics of the current at the load. Hence, reducing the distortion of the output voltage.

Appendix A

MATLAB files

This code belongs to the simulations results presented in chapter 3. First, the script for high-frequency dithering is presented followed by low-frequency dithering.

```
%High-Frequency Dithering Simulation
%It was used a hiperbolic tangent function to simulate the non-linear
%transfer function and a filter firpm to filter out the input signal

%Sampling frequency and time vectors
N=100000;
fs=20e9;
n=0:(N-1);
t=n*(1/fs);

%HFD
f1=198e6;
f2=202e6;
fd=1.3e9;

%Input signals
x=0.5*sin(2*pi*f1*t);
x1=0.5*sin(2*pi*f2*t);
d=2.2*sin(2*pi*fd*t);

figure
plot(t/10^-6,x+x1+d,'r')
hold on
plot(t/10^-6,x+x1,'LineWidth',2)
set(gca,'Fontsize', 15);
title('Time domain waveforms')
legend('2tone+dither input','2tones');
xlim([0.25 0.37])
xlabel('Time (us)'); ylabel('Amplitude (V)');grid on
hold off

%Hiperbolic tangent system
g=2;
y_nl=tanh(g*(x+x1));
y_d=tanh(g*(x+x1+d));

%PLOTS with input and output signal in time domain
```

```
figure
subplot(2,2,1)
plot(t,x+x1);title('x+x1');
subplot(2,2,2)
plot(t,y_nl);title('tanh(x+x1)');
ylim([-1.3 1.3])
subplot(2,2,3)
plot(t,y_d);title('tanh(d+x+x1)');
subplot(2,2,4)
plot(t,y_d,'g',t,y_nl,'r');title('red-tanh(x+x1) vs green-tanh(d+x+x1)')
ylim([-1.3 1.3])
suptitle('Signals');

%Spectrums of the input and output
figure
x_fft=fft(x+x1);
plot(n*fs/N/10^6,20*log10(abs(x_fft)/length(x_fft)))
title('Two tones input');
xlabel('Frequency (MHz)'); ylabel('Amplitude (dB)');

figure
plot(n*fs/N/10^6,20*log10(abs(fft(x+x1+d)/length(x))))
set(gca,'Fontsize', 15);
title('Two tones+dither input');grid on
xlabel('Frequency (MHz)'); ylabel('Amplitude (dB)');

figure
plot(20*log10(abs(fft(y_nl)/length(x))))
title('Two tones output - not filtered');
xlabel('Frequency (Hz)'); ylabel('Amplitude (dB)');

figure
plot(20*log10(abs(fft(y_d)/length(x))))
title('Two tones+dither output - not filtered');
xlabel('Frequency (Hz)'); ylabel('Amplitude (dB)');

%Filter to supress the dither
fp1=f1/(fs/2);
fp2=f2/(fs/2);
B2=firpm(500, [0 fp1-fp1/3 fp1-fp1/5 fp2+fp2/5 fp2+fp2/3 1], [0 0 1 1 0 0]);

%Ouput signal after the filter
yfilt_d=filtfilt(B2,1,y_d);
yfilt_nl=filtfilt(B2,1,y_nl);

figure
plot(t,yfilt_d,'r',t,yfilt_nl)
title('Waveform in time domain');
legend('Two tones+dither','Two tones');
xlabel('Time (s)'); ylabel('Amplitude (V)');

%Output signal after filtered, in frequency domain
yfilt_d_fft=fft(yfilt_d);

figure
plot(n*fs/N/10^6,20*log10(abs(yfilt_d_fft/length(yfilt_d))),'ro--',n*fs/N/10^6,20*log10(abs(fft(
set(gca,'Fontsize',15);
```

```
title('Output Spectrum');
%xlim([170 230]);
legend('Two tones+dither','Two tones');
xlabel('Frequency (MHz)'); ylabel('Amplitude (dB)');grid on;



%Low-Frequency Dithering Simulation
%It was used a hiperbolic tangent function to simulate the non-linear
%transfer function and a filter firpm to filter out the input signal

%Sampling frequency and time vectors
N=100000;
fs=10e9;
n=0:(N-1);
t=n*(1/fs);

%%%%%LFD
f1=1299e6;
f2=1301e6;
fd=0.358e9;

%Input signals
x=0.5*sin(2*pi*f1*t);
x1=0.5*sin(2*pi*f2*t);
d=2.2*sin(2*pi*fd*t);

figure
plot(t/10^-6,x+x1+d,'r')
hold on
plot(t/10^-6,x+x1,'LineWidth',2)
set(gca,'Fontsize', 15);
title('Time domain waveforms')
legend('2tone+dither input','2tones');
%xlim([0.25 0.37])
xlabel('Time (us)'); ylabel('Amplitude (V)');grid on
hold off

figure
plot(n*fs/N/10^6,20*log10(abs(fft(x+x1+d)/length(x))))
set(gca,'Fontsize', 15);
title('Two tones+dither input');grid on
xlabel('Frequency (MHz)'); ylabel('Amplitude (dB)');

%Hiperbolic tangent system
g=2;
y=tanh(g*(x+x1));
y_d=tanh(g*(x+x1+d));

%PLOTS with input and output signal in time domain
figure
subplot(2,2,1)
plot(t,x+x1);title('x+x1');
subplot(2,2,2)
plot(t,y);title('tanh(x+x1)');
ylim([-1.3 1.3])
subplot(2,2,3)
plot(t,y_d);title('tanh(d+x+x1)');
```

```
subplot(2,2,4)
plot(t,y_d,'g',t,y,'r');title('red—tanh(x+x1) vs green—tanh(d+x+x1)')
ylim([—1.3 1.3])
suptitle('Signals');

%Spectrums of the input and output
figure
x_fft=fft(x+x1);
plot(20*log10(abs(x_fft)/length(x_fft)))
title('fft two tones input');

figure
plot(20*log10(abs(fft(x+x1+d)/length(x))))
title('fft two tones+dither input');

figure
plot(20*log10(abs(fft(y_d)/length(x))))
title('fft two tones+dither output');

figure
plot(20*log10(abs(fft(y)/length(x))))
title('fft two tones output');

%Filter to supress the dither, plot in the end (phase and magnitude)
fp1=f1/(fs/2);
fp2=f2/(fs/2);
B2=firpm(500, [0 fp1—fp1/3 fp1—fp1/5 fp2+fp2/5 fp2+fp2/3 1], [0 0 1 1 0 0]);

%Ouput signal after the filter
yfilt_d=filtfilt(B2,1,y_d);
yfilt_nl=filtfilt(B2,1,y);

figure
plot(t,yfilt_d,'r',t,yfilt_nl)
title('Waveform in time domain');
legend('Two tones+dither','Two tones');
xlabel('Time (s)'); ylabel('Amplitude (V)');

%output signal after filtered, in frequency domain
yfilt_d_fft=fft(yfilt_d);

figure
plot(n*fs/N/10^6,20*log10(abs(yfilt_d_fft/length(yfilt_d))),'ro—',n*fs/N/10^6,20*log10(abs(fft(
set(gca,'Fontsize',15);
title('Output Spectrum');
%xlim([1200 1400]);
legend('Two tones+dither','Two tones');
xlabel('Frequency (MHz)'); ylabel('Amplitude (dB)');grid on;
```

Appendix B

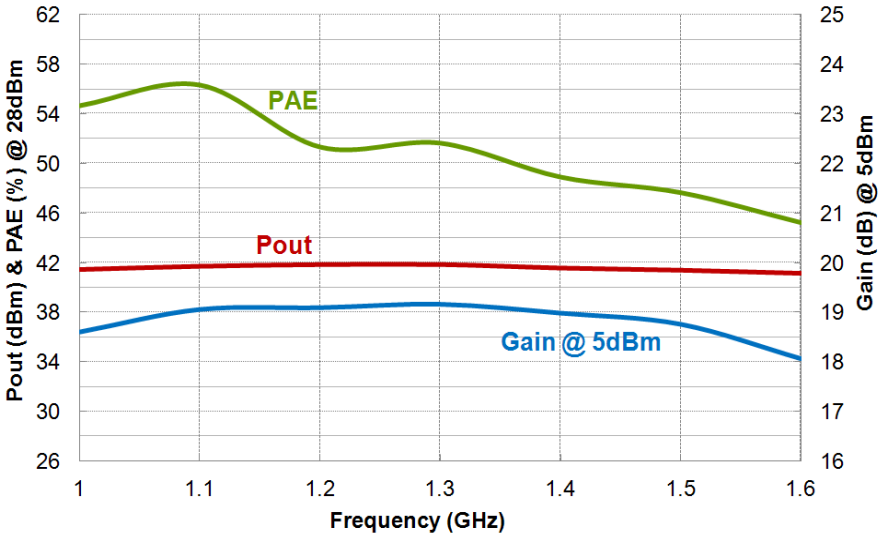
UMS Driver Datasheet

Advanced Information: AI1240

15W L-Band Driver

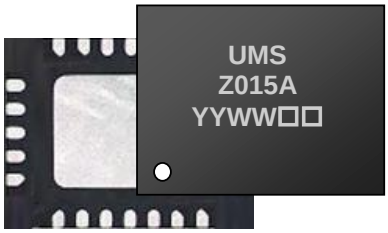
GaN HEMT on SiC

V_{DS}= 45V, I_{D_Q}= 100mA, Pin= 28dBm
Pulsed mode (25µs-10%)



Performances on the connector access planes

The CHZ015A-QEG is an input matched packaged Gallium Nitride High Electron Mobility transistor. It allows broadband solutions for a variety of RF power applications in L-band. It is well suited for pulsed radar application.
The CHZ015A-QEG is proposed on a 0.5µm gate length GaN HEMT process, based on Quasi MMIC technology.
It is available in a QFN4x5 standard surface mount 24 leads, compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006.



United Monolithic Semiconductors S.A.S.
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Recommended DC Operating Ratings

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage	20	45	50	V	
V_{GS_Q}	Gate to Source Voltage		-1.9		V	V_{DS}= 45V, I_{D_Q}= 100mA
I_{D_Q}	Quiescent Drain Current		100	350	mA	V_{DS}= 45V
I_{D_MAX}	Drain Current		650	(1)	mA	V_{DS}= 45V, Compressed mode
I_{G_MAX}	Gate Current (forward mode)		0	8	mA	Compressed mode
P_W	Pulse width			1.5	ms	
D_C	Duty cycle		10		%	
T_{j_MAX}	Junction temperature			200	°C	

(1) Limited by dissipated power

DC Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-3	-2	-1	V	V_{DS}= 45V, I_D= I_{DSS}/100
I_{D_SAT} (2)	Saturated Drain Current		2.7		A	V_{DS}= 7V, V_{GS}= 2V (1)
I_{G_leak}	Gate Leakage Current (reverse mode)	-1			mA	V_{DS}= 45V, V_{GS}= -7V (1)
V_{BDS}	Drain-Source Break-down Voltage		200		V	V_{GS}= -7V (1)
R_{TH}	Thermal Resistance		8.5		°C/W	CW Mode

(1) Parameters extrapolated from unit cell measurement
(2) For information, limited by I_{D_MAX} , see on Absolute Maximum Ratings

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RF Characteristics (1)

Tcase= +25°C, **pulsed mode** (2), V_{DS}= 45V, I_{D_Q}= 100mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1.2		1.4	GHz
G_{SS}	Small Signal Gain		19		dB
dG_{SS}	Small Signal Gain flatness		+/-0.3		dB
P_{SAT}	Saturated Output Power		42		dBm
PAE	Power Added Efficiency		50		%
I_{DSAT}	Saturated Drain Current		650		mA
Rlin	Input Return Loss		-11		dB

(1) Measured on evaluation board 61501358 on the connector access planes

(2) Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between RF and DC pulse

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Absolute Maximum Ratings

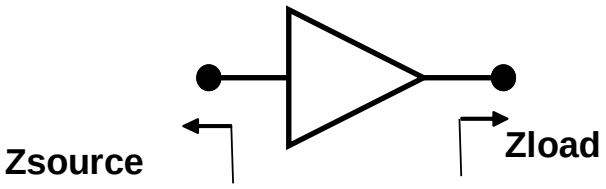
Tcase= +25°C (1), (2), (3)

Symbol	Parameter	Rating	Unit	Note
V_{DS}	Drain-Source Voltage	-0.5, +60	V	
V_{GS_Q}	Gate-Source Voltage	-10, +2	V	(4), (6)
I_{G_MAX}	Maximum Gate Current in forward mode	25	mA	
I_{G_MIN}	Maximum Gate Current in reverse mode	-4	mA	
I_{D_MAX}	Maximum Drain Current	2	A	(4)
P_{IN}	Maximum Input Power	32	dBm	(5)
P_{W_MAX}	Pulse width	3	ms	
D_{C_MAX}	Duty cycle	20	%	
T_j	Junction Temperature	220	°C	
T_{STG}	Storage Temperature	-40 to +85	°C	

(1) Operation of this device above anyone of these parameters may cause permanent damage
(2) Duration < 1s
(3) The given values have not to be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place
(4) Max junction temperature has to be considered
(5) Linked to and limited by I_{G_MAX} & I_{G_MIN} values
(6) V_{GS_Q} max limited by I_{D_MAX} and I_{G_MAX} values

Simulated Source and Load Impedance

V_{DS}= 45V, I_{D_Q}= 100mA



Frequency (GHz)	Source	Load
Typical [1.2-1.4]	50 - j0	54.0 + j29.6

These values are defined on the package interface with PCB

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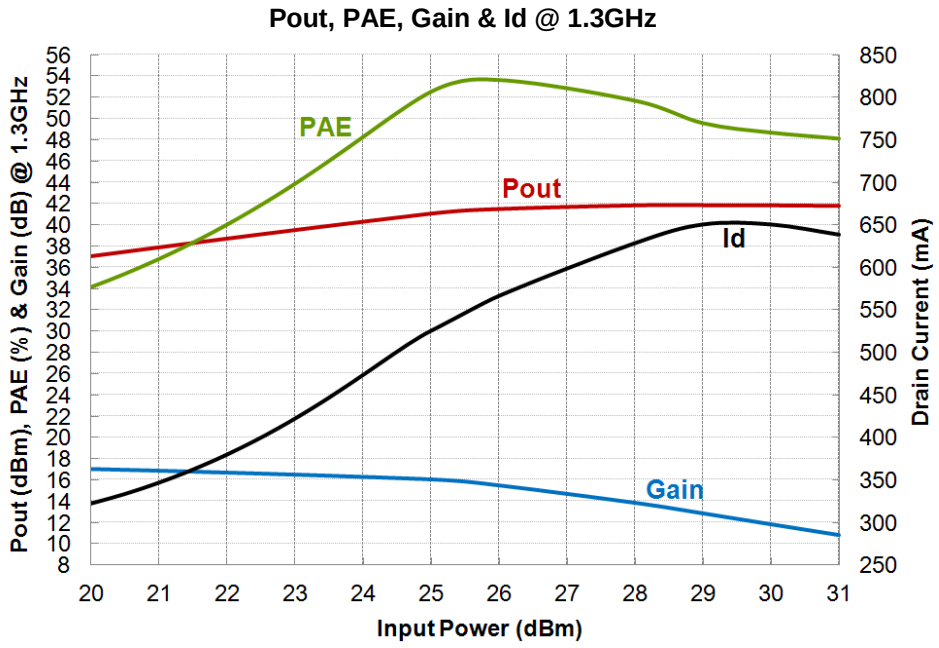
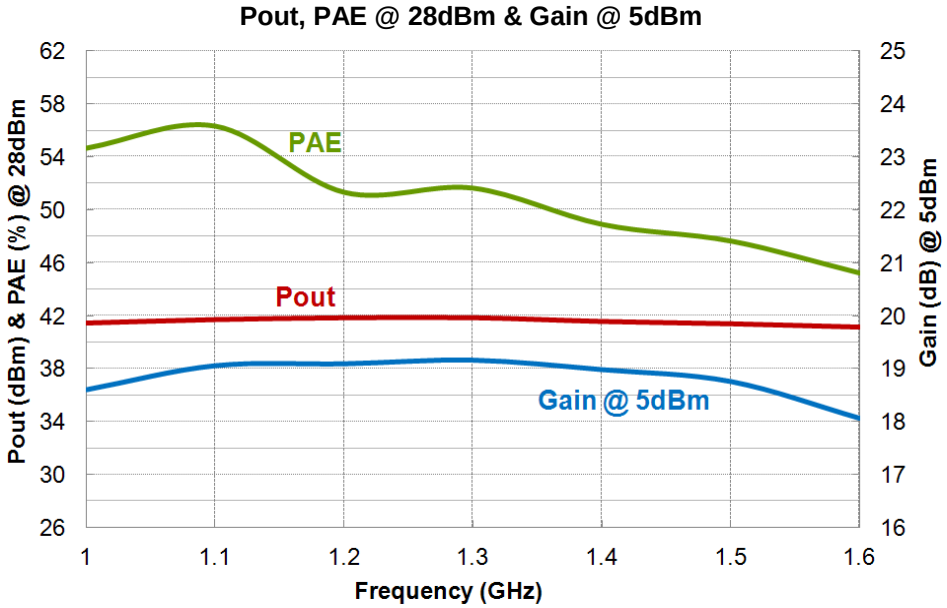
Typical Performance on demonstration board (ref 61501358)

Measured on the connector access planes.
Tcase= +25°C, **pulsed mode** (1), V_{DS}= 45V, I_{D_Q}= 100mA





(1) Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between DC and RF pulse

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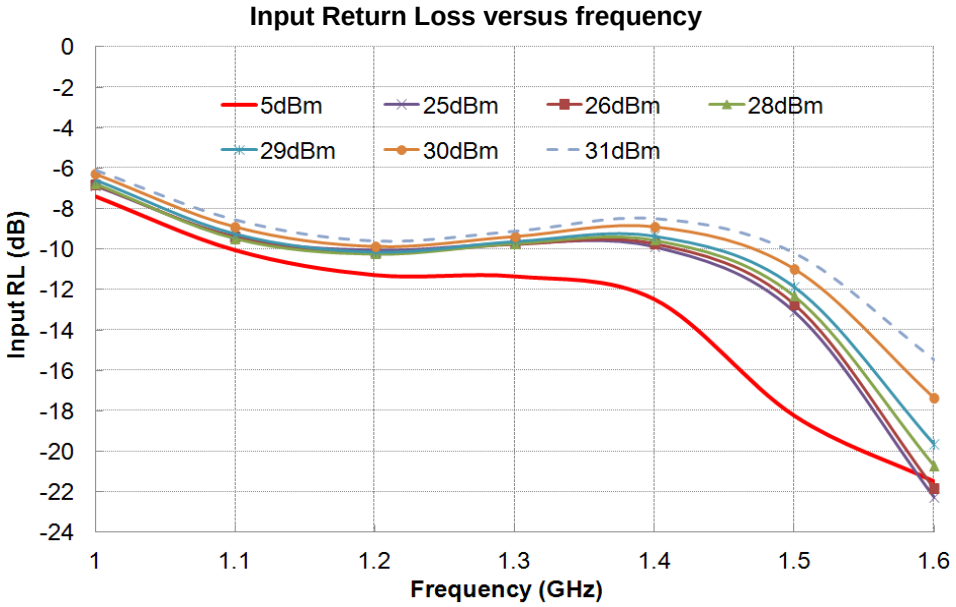
Typical Performance on demonstration board (ref 61501358)

Measured on the connector access planes.
Tcase= +25°C, **pulsed mode** (1), V_{DS}= 45V, I_{D_Q}= 100mA



(1) Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between DC and RF pulse

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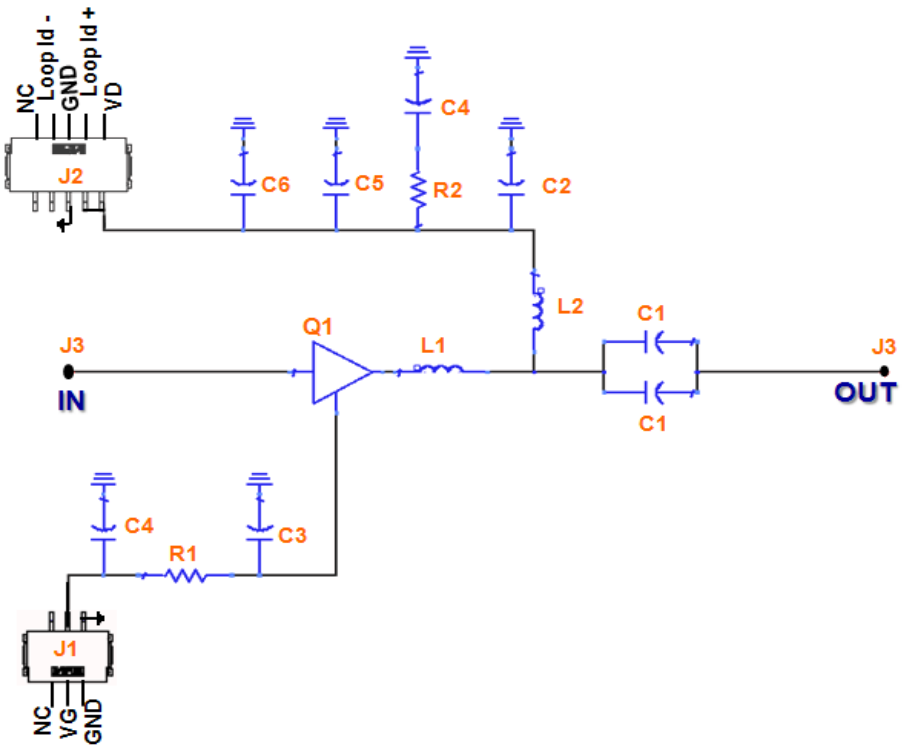
Demonstration Amplifier Low Frequency Equivalent Schematic (ref 61501358)



Demonstration Amplifier (ref 61501358) / Bill of Materials

Designator	Type	Value - Description	Qty
L1	Inductor for output pre-matching	3.6nH, +/- 5%, 0603	1
L2	Inductor	22nH, +/- 5.2%, 0908	1
C1	Capacitor	10pF, +/- 5%, 0603	2
C2	Capacitor	120pF, +/- 5%, 0805	1
C3	Capacitor	220pF, +/- 5%, 0805	1
C4	Capacitor	1nF, +/- 5%, 0805	2
C5	Capacitor	1µF, +/- 10%, 1210	1
C6	Capacitor	68µF, +/- 20%, H13	1
R1	Jumper	Jumper 0 Ω, 0603	1
R2	Resistor	3Ω, +/- 1%, 0603	1
J1	Connector	SMD 3 contacts	1
J2	Connector	SMD 5 contacts	1
J3	Connector	SMA	2
Q1	Driver	CHZ015A_QEG	1
-	PCB	RO4003, Er=3.55, h=508µm	-

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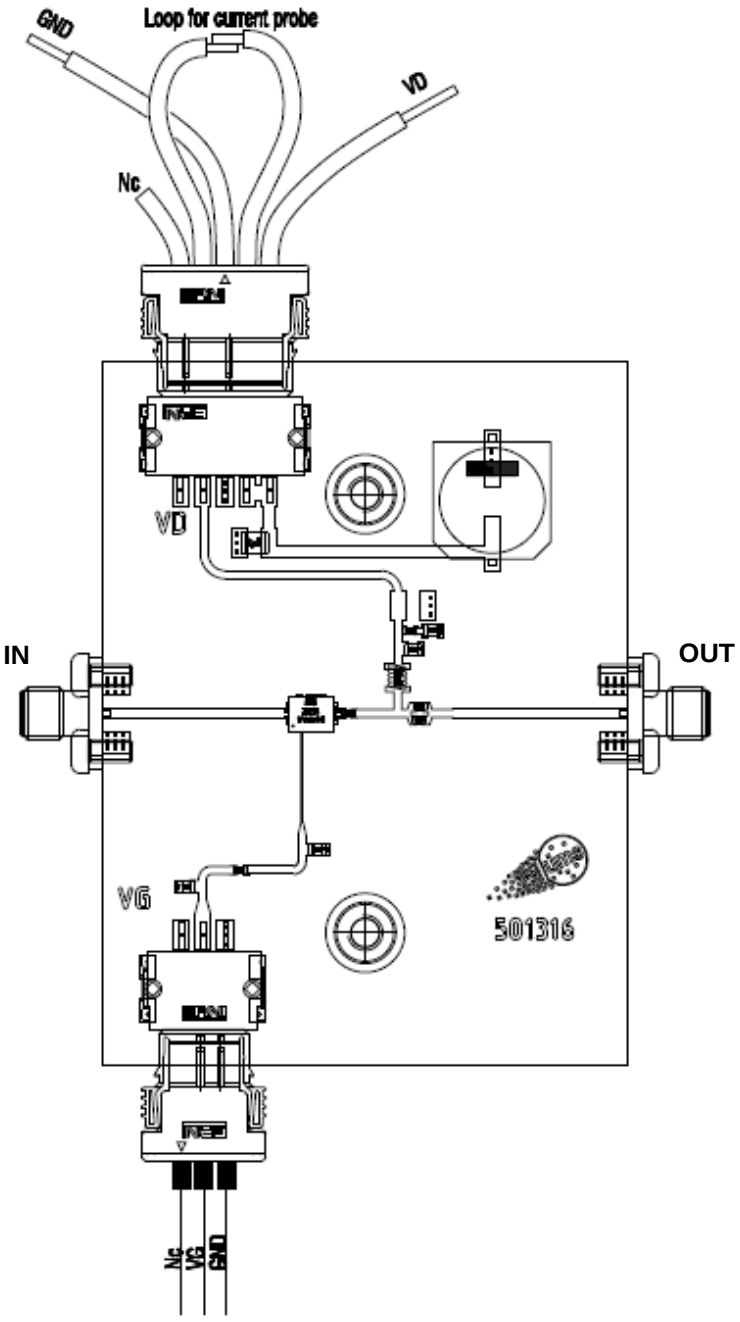
Evaluation Amplifier Board (ref 61501358)



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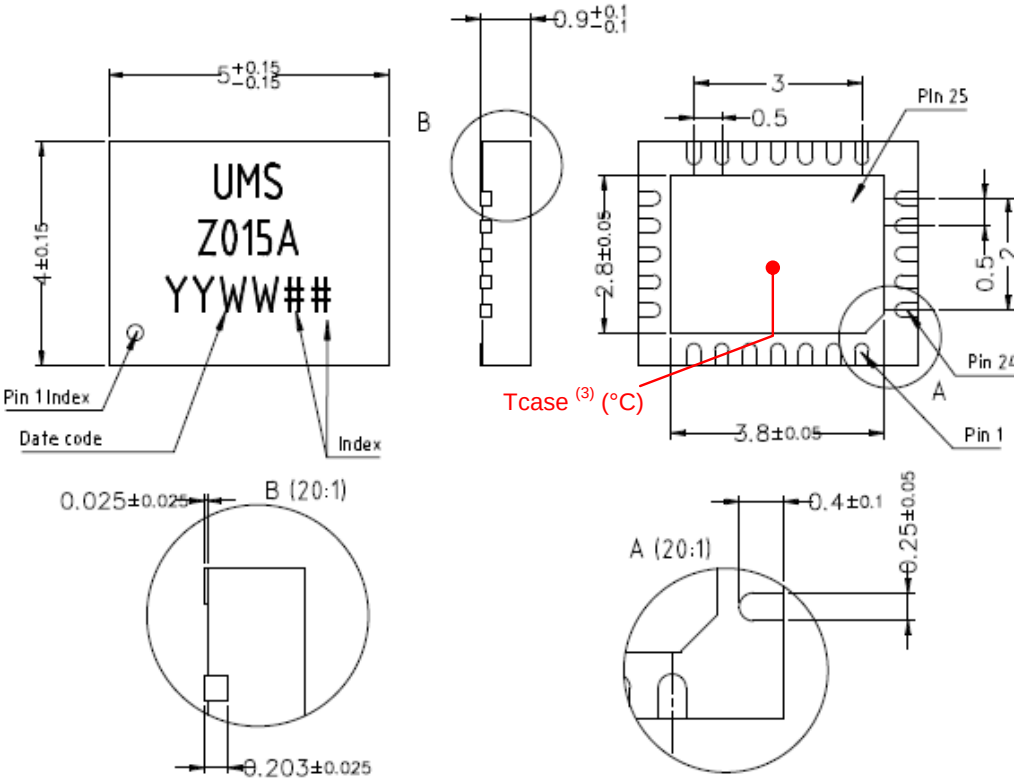
Package outline [1]



Matt tin, Lead Free (Green)	1- Nc	11- RF OUT	21- Gnd [2]
Units : mm	2- DC	12- Nc	22- RF IN
From the standard : JEDEC MO-220 (VGGD)	3- Nc	13- Nc	23- Gnd [2]
	4- Nc	14- Gnd [2]	24- Nc
25- GND	5- Gnd [2]	15- Nc	
	6- Gnd [2]	16- Nc	
	7- Nc	17- Nc	
	8- Nc	18- Gnd [2]	
	9- RF OUT	19- Nc	
	10- Nc	20- Nc	

[1] The package outline drawing included in this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

[2] It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

[3] The temperature is monitored at the package back-side interface (Tcase) as shown above.

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at http://www.ums-gaas.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Sampling request reference

Package: ES-CHZ015A-QEG

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Appendix C

ADS simulations

C.1 Gate and drain bias

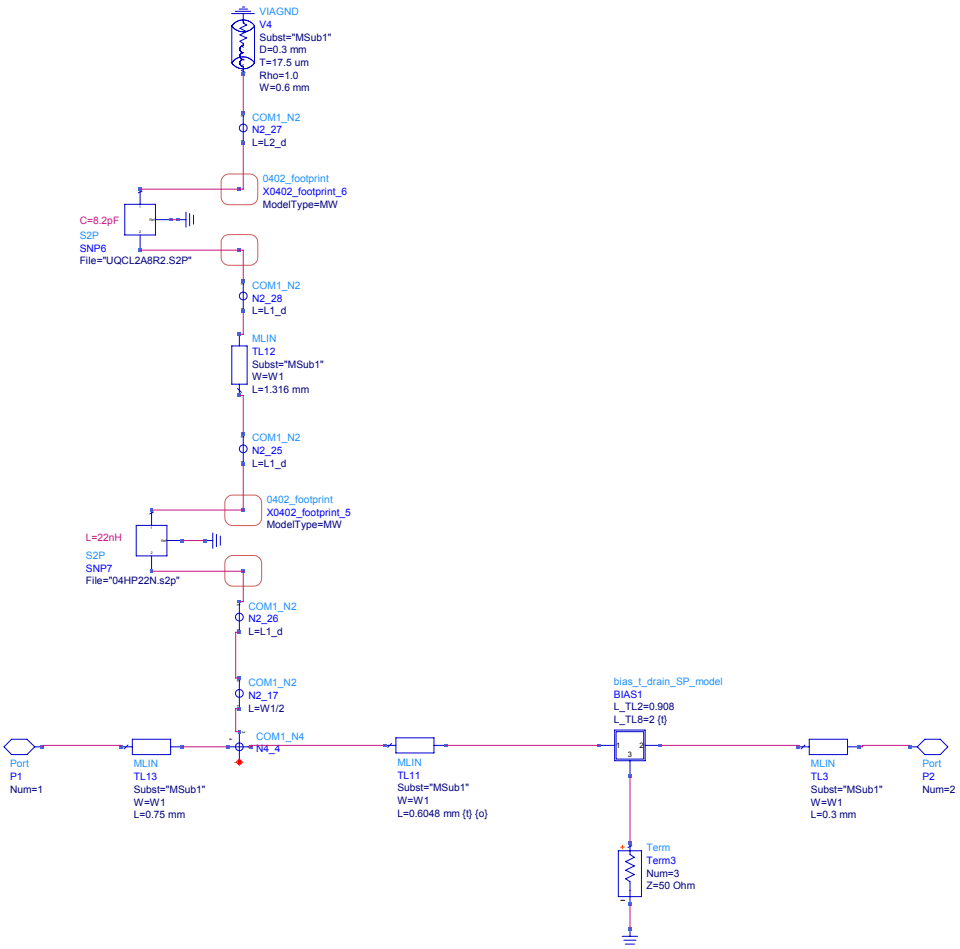

Figure C.1: *Drain bias with the dither filter, using lumped components. Port 1 represents the input of the bias, port 2 , the output and port 3, is where the drain supply is connected.*

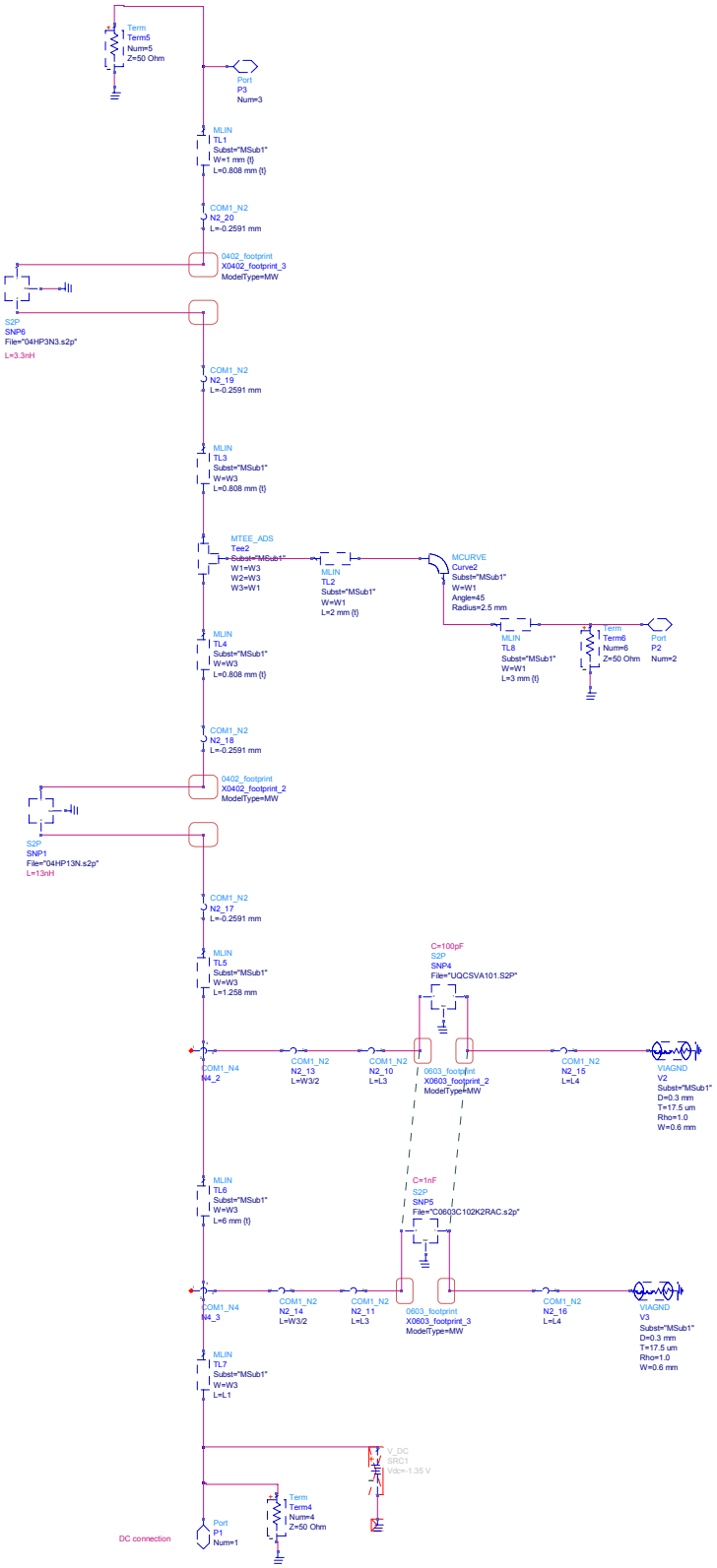

Figure C.2: *Gate bias including the dither input, based on lumped components. Figure C.3 shows the same network but based on a momentum structure rather than transmission lines. Port 1 is the input for the gate supply, port 2 is used to inject the dither and port 3 is connected to the gate input of the driver.*

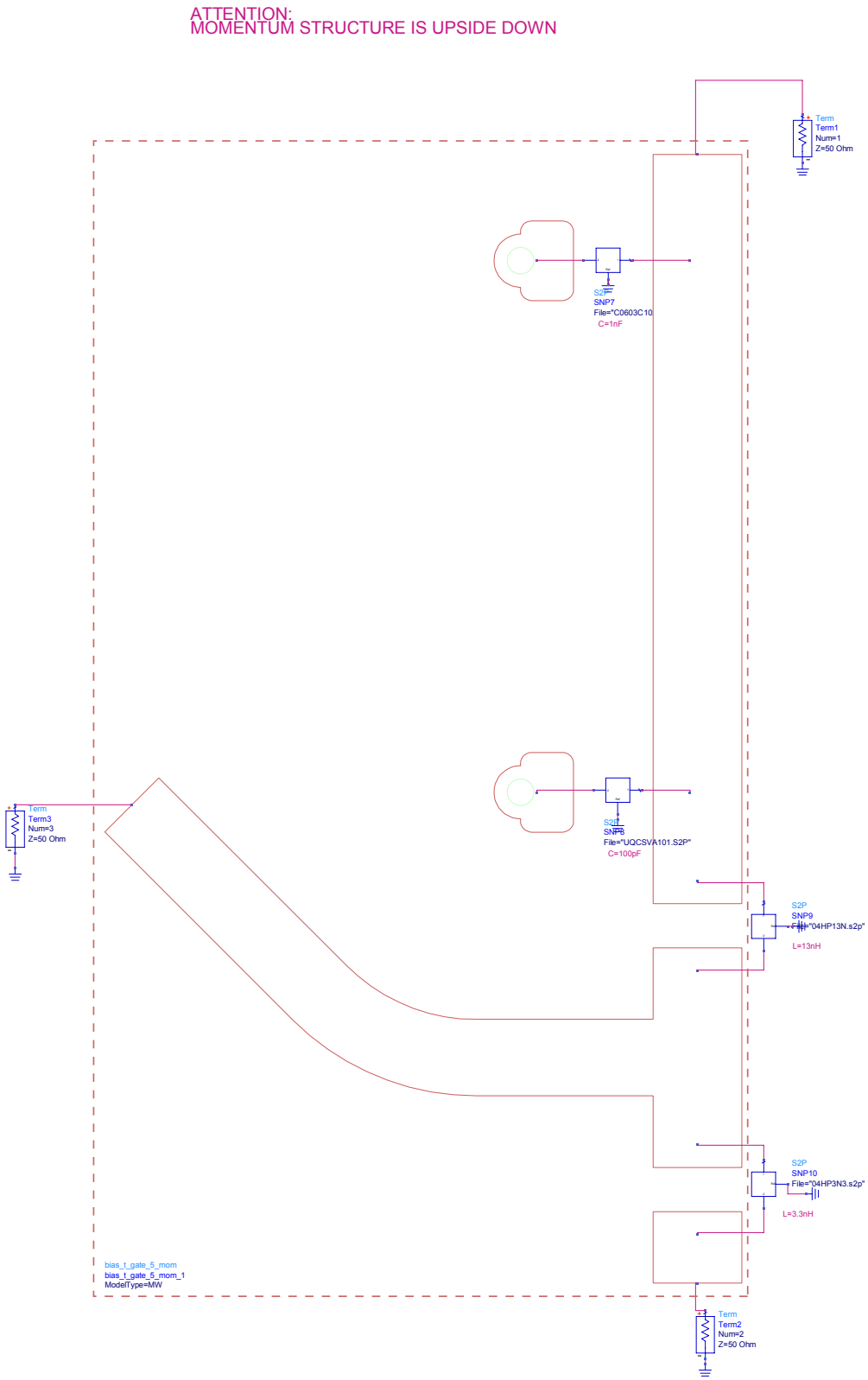

Figure C.3: *Gate bias including the dither input, based on momentum structure and lumped components. Port 1 is the input for the gate supply, port 2 is connected to the gate input of the driver, and port 3 is used to inject the dither. Port 3 uses a corner in microstrip line because of board size issues (another 50Ω input).*

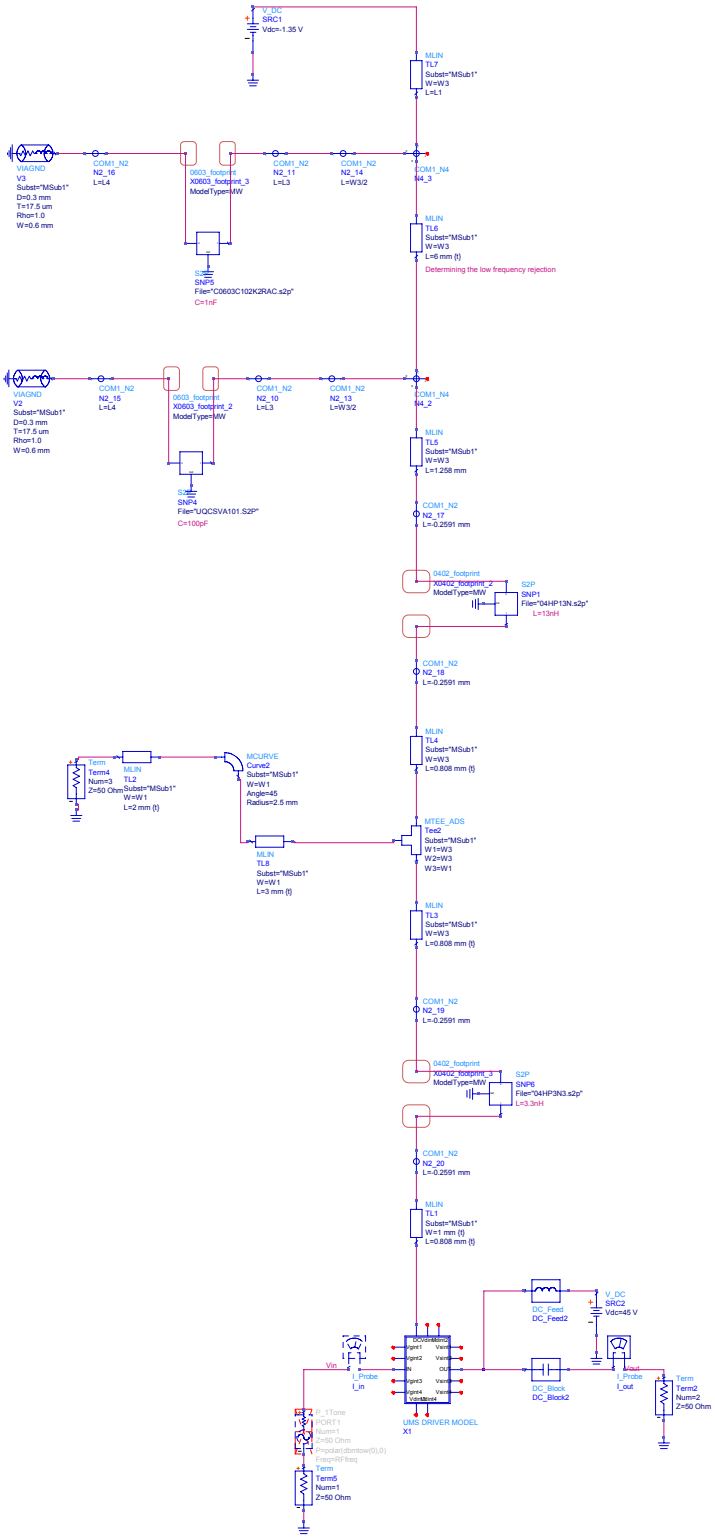

Figure C.4: *Driver with the gate bias and input matching network.*

C.2 Output matching network

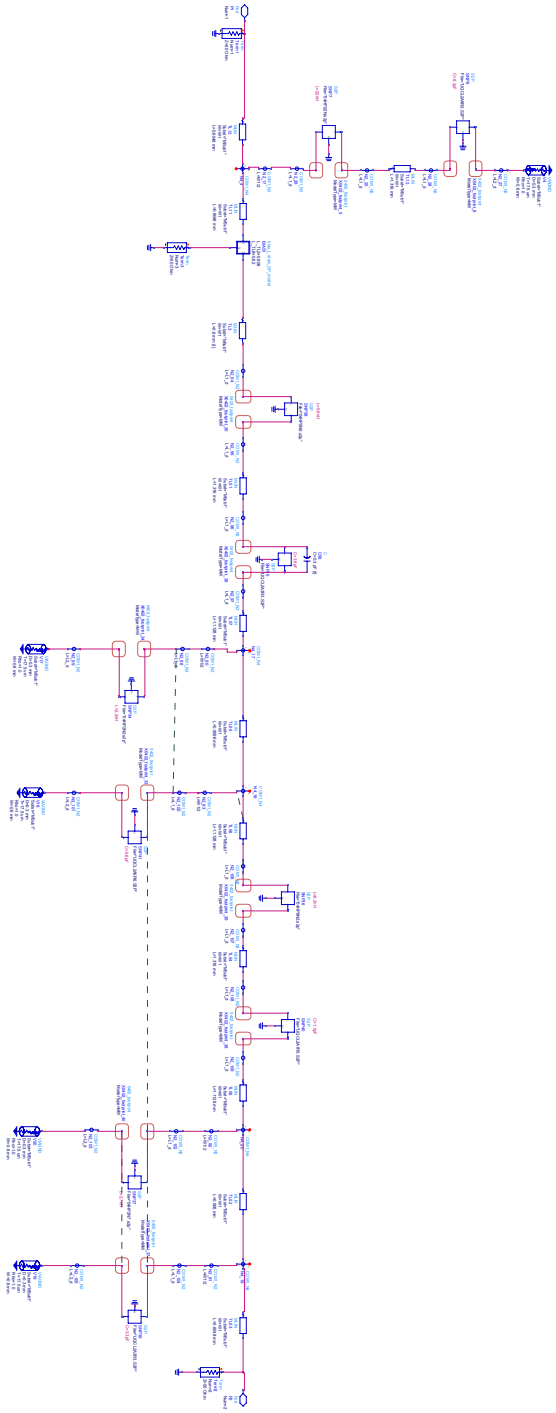

Figure C.5: *Complete output matching, based on lumped components. At the output of the driver is port 1, BIAS1 block has inside the drain bias. Between port 1 and BIAS1, the dither filter can be seen. After BIAS1, the RF output matching is depicted.*

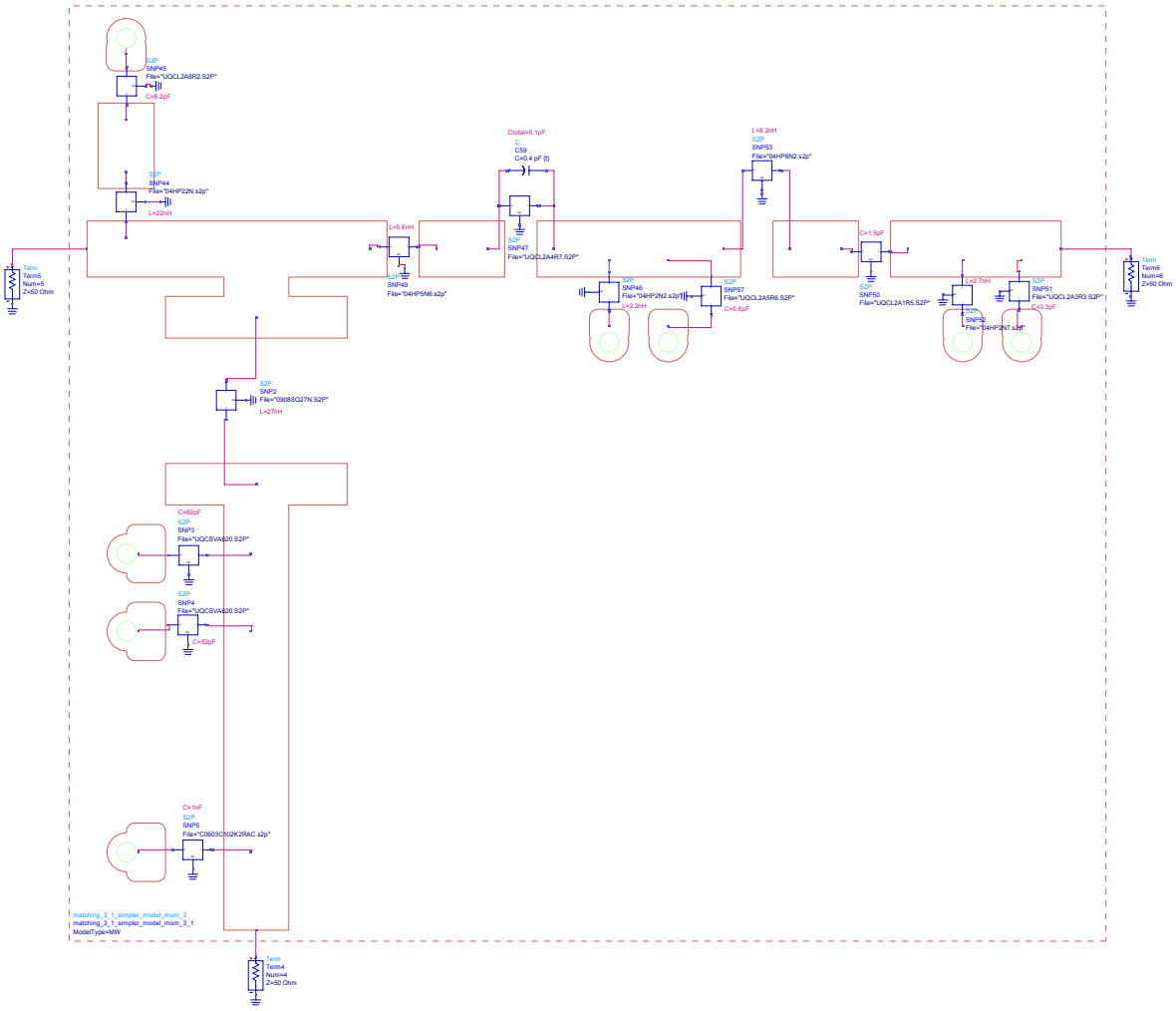

Figure C.6: *Complete matching circuit with the MOMENTUM structure and all ports terminated with a 50Ω load. Port 5 is connected to the output of the driver and port 4, at the power supply of the drain. Between these ports, one can see the dither filter and after the drain bias, the RF matching is drawn. Port 6 connects to the load.*

Appendix D

AMPi - Prototype panel

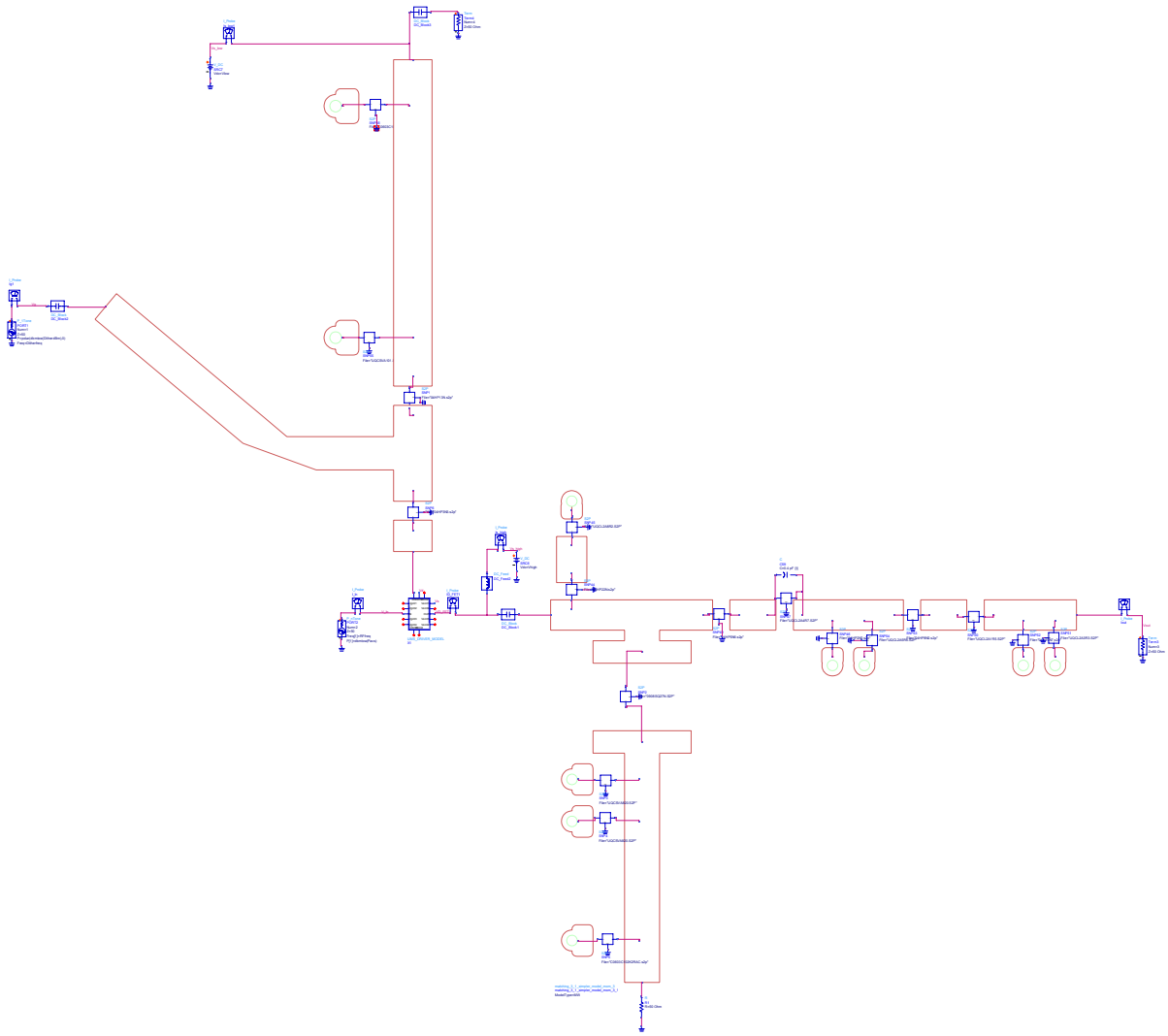

Figure D.1: *Complete design of the board, including the dither input matching network and the output matching network based on MOMENTUM structures and lumped components.*

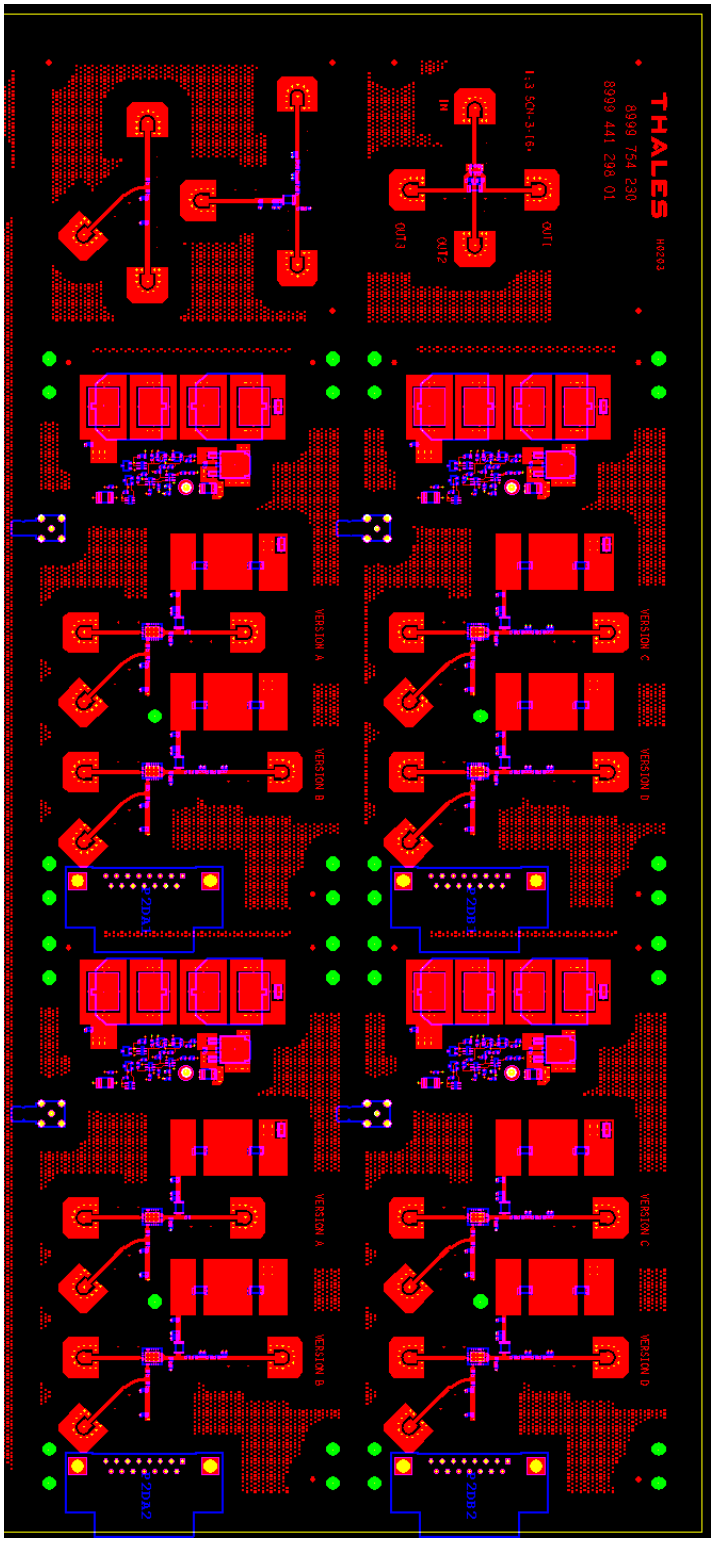

Figure D.2: *Complete designed panel which includes the different circuits: four versions of the complete layout and two passive networks.*

D.1 Script settings

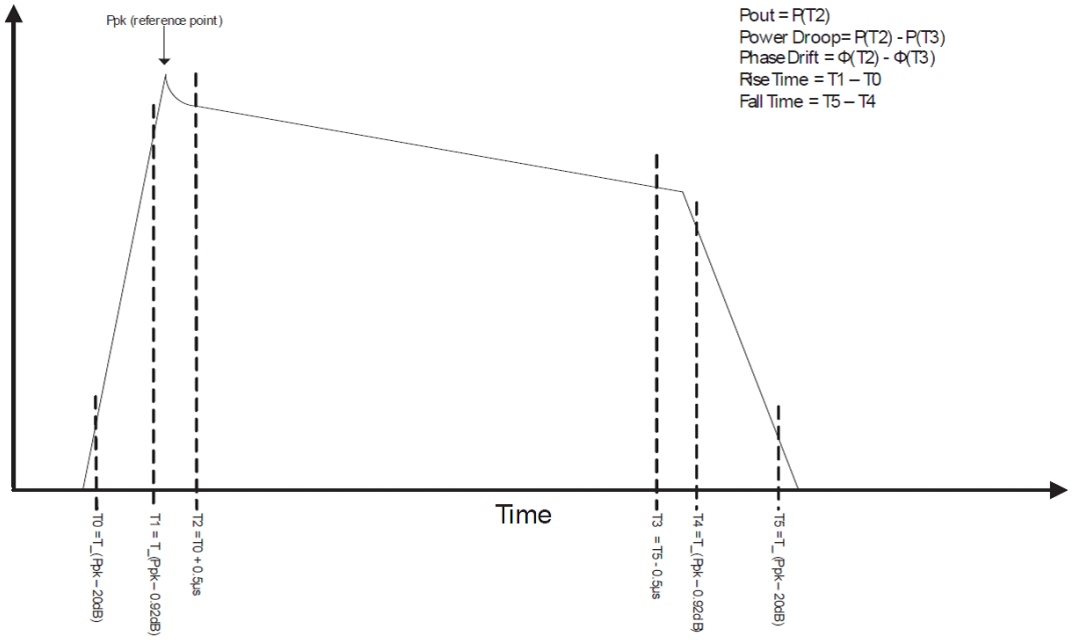

Figure D.3: *Settings for the MATLAB script, used to process data offline.*

Bibliography

[1] M. Skolnik, *RADAR Handbook, third edition.* McGraw-Hill Companies, 2008.

[2] M. Helaoui and F. Ghannouchi, "Linearization of power amplifiers using the reverse mm-linc technique," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 57, pp. 6 –10, jan. 2010.

[3] M. Vasic and, O. Garcia, J. Oliver, P. Alou, D. Diaz, J. Cobos, A. Gimeno, J. Pardo, C. Benavente, and F. Ortega, "Efficient and linear power amplifier based on envelope elimination and restoration," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 5 –9, jan. 2012.

[4] A. Katz, "Linearizing high power amplifiers," april 2013.

[5] F. A. Malekzadeh, *Analog Dithering Techniques for Wireless Transmitters.* Springer Science+Business Media New York, 2013.

[6] S. C. Cripps, *Advanced Tecniques in RF Power Amplifier Design.* Boston, London: Artech House, 2002.

[7] W. Doherty, "A new high efficiency power amplifier for modulated waves," *Proceedings of the Institute of Radio Engineers*, vol. 24, pp. 1163 – 1182, sept. 1936.

[8] S. C. Cripps, *RF Power Amplifiers for Wireless Comunications, 2nd Edition.* Boston, London: Artech House, 2006.

[9] Y. Yang, J. Cha, B. Shin, and B. Kim, "A fully matched n-way doherty amplifier with optimized linearity," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 51, pp. 986 – 993, mar 2003.

[10] M. K., "A new linearization method for cancellation of third order distortion," 2003.

[11] Y. Liao, D. Su, Y. Wang, and W. Chen, "A design of analog predistortion linearizer for rf power amplifier to reduce imd," in *Antennas, Propagation and EM Theory, 2008. ISAPE 2008. 8th International Symposium on*, pp. 1154 –1157, nov. 2008.

[12] P. Landin, J. Fritzin, W. Van Moer, M. Isaksson, and A. Alvandpour, "Modeling and digital predistortion of class-d outphasing rf power amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 60, pp. 1907 –1915, june 2012.

[13] A. Conway, Y. Zhao, P. Asbeck, M. Micovic, and J. Moon, "Dynamic gate bias technique for improved linearity of gan hfet power amplifiers," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, p. 4 pp., june 2005.

[14] F. A. Malekzadeh, "Analog dithering techniques for highly linear and efficient transmitters," March 2012.

[15] F. A. Malekzadeh, A. van Roermund, and R. Mahmoudi, "Low frequency dithering technique for linearization of current mode class d amplifiers," in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, pp. 1 –3, june 2012.

[16] K.-J. Cho, I.-H. Hwang, W.-J. Kim, J.-H. Kim, and S. Stapleton, "Linearity optimization of a high power doherty amplifier," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, p. 4 pp., june 2005.

[17] C. K., J. K., and Y. K., "Fully integrated hbt mmic series-type extended doherty amplifier for w-cdma handset applications," in *ETRI Journal*, vol. 32, p. 3 pp., february 2010.

[18] N. Delaunay, N. Deltimple, E. Kerherve and, and D. Belot, "A rf transmitter linearized using cartesian feedback in cmos 65nm for umts standard," in *Power Amplifiers for Wireless and Radio Applications (PAWR), 2011 IEEE Topical Conference on*, pp. 49 –52, jan. 2011.

[19] M. Abuelma'atti, A. Abuelmaatti, T. Yeung, and G. Parkinson, "Linearization of gan power amplifier using feedforward and predistortion techniques," in *Quality Electronic Design (ASQED), 2011 3rd Asia Symposium on*, pp. 282 –287, july 2011.

[20] S. Chung, J. Holloway, and J. Dawson, "Open-loop digital predistortion using cartesian feedback for adaptive rf power amplifier linearization," in *Microwave Symposium, 2007. IEEE/MTT-S International*, pp. 1449 –1452, june 2007.

[21] E. Cottais, Y. Wang, and S. Toutain, "Experimental results of power amplifiers linearization using adaptive baseband digital predistortion," p. 4 pp., 2005.

[22] A. Gelb and W. E. Van der Velve, *Multiple-Input Describing Functions and Nonlinear System Design*. McGraw-Hill Book Company, 1968.

[23] K. Chen and D. Peroulis, "Design of broadband high-efficiency power amplifier using in-band Class-F, 1/F mode-transferring technique," in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, pp. 1–3, 2012.

[24] M. K. Kazimierczuk, *RF Power Amplifiers*. United Kingdom: John Wiley and Sons Ltd, 2008.

[25] S. X. Tan L. and S. A. K., "Unconditional stability criteria for microwave networks," *PIERS proceedings, Beijing, China*, March 2009.

[26] B. J.F. and A. W., "Unconditional stability of a three-port network characterized with s-parameters," *IEEE transactions on MW theory and techniques*, vol. MTT-35, p. 5, June 1987.